DAC8811 16-Bit, Serial Input Multiplying Digital-to-Analog Converter

1 Features

- ±0.5 LSB DNL
- 16-Bit Monotonic
- ±1 LSB INL
- Low Noise: 12 nV/$\sqrt{Hz}$
- Low Power: I_{DD} = 2 µA
- 2.7-V to 5.5-V Analog Power Supply
- 2-mA Full-Scale Current ±20%, with V_{REF} = 10 V
- 50-MHz Serial Interface
- 0.5-µs Settling Time
- 4-Quadrant Multiplying Reference
- Reference Bandwidth: 10 MHz
- ±10-V Reference Input
- Reference Dynamics: –105 THD
- Tiny 8-Lead 3 × 3 mm VSON and 3 × 5 mm VSSOP Packages
- Industry-Standard Pin Configuration

2 Applications

- Automatic Test Equipment
- Instrumentation
- Digitally Controlled Calibration
- Industrial Control PLCs

3 Description

The DAC8811 multiplying digital-to-analog converter (DAC) is designed to operate from a single 2.7-V to 5.5-V supply.

The applied external reference input voltage V_{REF} determines the full-scale output current. An internal feedback resistor (R_{FB}) provides temperature tracking for the full-scale output when combined with an external I-to-V precision amplifier.

A serial data interface offers high-speed, three-wire microcontroller-compatible inputs using data-in (SDI), clock (CLK), and chip-select ($\overline{CS}$).

On power-up, the DAC register is filled with zeroes, and the DAC output is at zero scale.

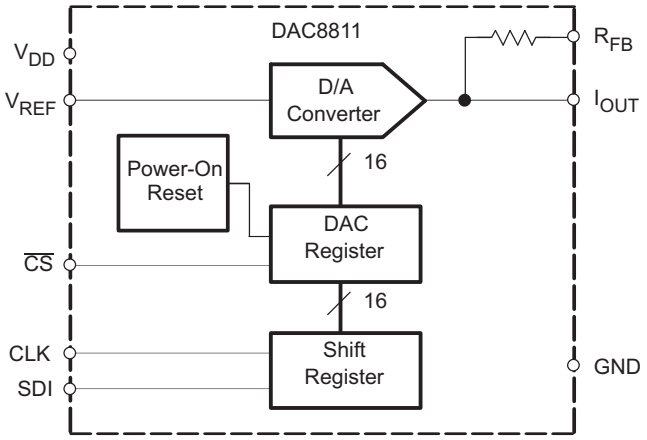
The DAC8811 is packaged in space-saving 8-lead VSON and VSSOP packages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DAC8811	VSSOP (8)	3.00 mm × 3.00 mm
	VSON (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (October 2015) to Revision D — **Page**

- Changed the *DAC8811 Timing Diagram* image to show the setup and hold time with respect to rising edge ... 7
- Changed two instances of *falling* to *rising* in the *DAC8811 Input Shift Register* section ... 15
- Changed the *$\overline{SYNC}$ Interrupt Facility* image ... 15

Changes from Revision B (February 2007) to Revision C — **Page**

- Added *ESD Ratings* table, *Recommended Operating Conditions* table, *Thermal Information* table, *Timing Requirements* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging*, and *Orderable Information* sections. ... 1
- Changed R3' From: 50 kΩ To: 50 Ω in Figure 23 ... 14

Changes from Revision A (December 2004) to Revision B — **Page**

- Added a new paragraph to the Description , "On power-up,..." ... 1
- Changed the Simplified Schematic to include the Power-On Reset ... 1
- Added V_{REF}, R_{FB} to GND to the Absolute Maximum Ratings ... 5
- Changed the ESD rating of HBM From: 1500 To: 4000 in the Absolute Maximum Ratings ... 5
- Added table note: " All ac characteristic tests are performed.." to the Electrical Characteristics ... 6
- Added test conditions to the Output voltage settling time of the *AC characteristics* section in the Timing Requirements ... 7
- Added table note: " All ac characteristic tests are performed.." to the Electrical Characteristics ... 7
- Changed Figure 9 ... 8

Changes from Original (November 2004) to Revision A **Page**

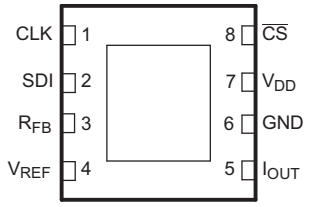
- Removed the Product Preview label 1
- Added information to the Features 1
- Added Output leakage current Data = 0000h, $T_A = T_{MAX}$ in the Electrical Characteristics 6
- Added Input high voltage for V_{DD} = 2.7 V and 2.5 V in the Electrical Characteristics 6
- Changed the values of the *Power Requirements* and the *AC characteristics* section in the Electrical Characteristics 6

5 Device Comparison Table

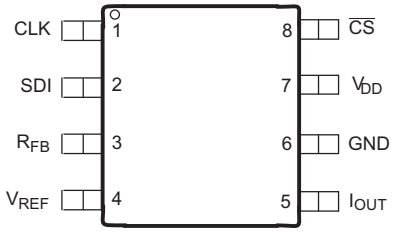
PART NUMBER	INL (LSB)	DNL (LSB)
DAC8811ICDGK	±1	±1
DAC8811IBDGK	±2	±1
DAC8811ICDRB	±1	±1
DAC8811IBDRB	±2	±1

6 Pin Configuration and Functions

DRB Package
8-Pins VSON
Top View



DGK Package
8-Pins VSSOP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
CLK	1	I	Clock input; positive edge triggered clocks data into shift register
SDI	2	I	Serial register input; data loads directly into the shift register MSB first. Extra leading bits are ignored.
R_{FB}	3	O	Internal matching feedback resistor. Connect to external op amp output.
V_{REF}	4	I	DAC reference input pin. Establishes DAC full-scale voltage. Constant input resistance versus code.
I_{OUT}	5	O	DAC current output. Connects to inverting terminal of external precision I/V op amp.
GND	6	G	Analog and digital ground.
V_{DD}	7	I	Positive power supply input. Specified operating range of 2.7 V to 5.5 V.
$\overline{CS}$	8	I	Chip-select; active low digital input. Transfers shift register data to DAC register on rising edge. See Table 1 for operation.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	V_{DD} to GND	–0.3	7	V
	V (I_{OUT}) to GND	–0.3	V_{DD} + 0.3	V
Digital input voltage	GND	–0.3	V_{DD} + 0.3	V
Reference voltage, V_{REF}	R_{FB} to GND	–25	25	V
Operating temperature		–40	105	°C
Junction temperature, T_J			125	°C
Storage temperature, T_{stg}		–65	150	

(1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage to GND	2.7		5.5	V
Operating ambient temperature, T_A	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		DAC8811		UNIT
		DGK (VSSOP)	DRB (VSON)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	169.6	46.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	64.2	61.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	90.3	22	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.7	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	88.8	22.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	3.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

V_{DD} = 2.7 V to 5.5 V; I_{OUT} = Virtual GND, GND = 0 V; V_{REF} = 10 V; T_A = full operating temperature. All specifications -40°C to 85°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
	Resolution		16			Bits
	Relative accuracy	DAC8811C			±1	LSB
	Relative accuracy	DAC8811B			±2	LSB
	Differential nonlinearity			±0.5	±1	LSB
	Output leakage current	Data = 0000h, T_A = 25°C			10	nA
	Output leakage current	Data = 0000h, $T_A = T_{MAX}$			10	nA
	Full-scale gain error	All ones loaded to DAC register		±1	±4	mV
	Full-scale tempco			±3		ppm/°C
OUTPUT CHARACTERISTICS(1)						
	Output current			2		mA
	Output capacitance	Code dependent		50		pF
REFERENCE INPUT(1)						
	V_{REF} Range		–15		15	V
	Input resistance			5		kΩ
	Input capacitance			5		pF
LOGIC INPUTS AND OUTPUT(1)						
V_{IL}	Input low voltage	V_{DD} = 2.7V			0.6	V
		V_{DD} = 5V			0.8	V
V_{IH}	Input high voltage	V_{DD} = 2.7V	2.1			V
		V_{DD} = 5V	2.4			V
I_{IL}	Input leakage current				10	µA
C_{IL}	Input capacitance				10	pF
POWER REQUIREMENTS						
V_{DD}			2.7		5.5	V
	I_{DD} (normal operation)	Logic inputs = 0 V			5	µA
	V_{DD} = 4.5 V to 5.5 V	$V_{IH} = V_{DD}$ and V_{IL} = GND		3	5	µA
	V_{DD} = 2.7 V to 3.6 V	$V_{IH} = V_{DD}$ and V_{IL} = GND		1	2.5	µA
AC CHARACTERISTICS(1) (2)						
BW –3 dB	Reference mutiplying BW	V_{REF} = 5 V_{PP}, Data = FFFFh		10		MHz
	DAC glitch impulse	V_{REF} = 0 V to 10 V, Data = 7FFFh to 8000h to 7FFFh		2		nV/s
	Feed through error V_{OUT}/V_{REF}	Data = 0000h, V_{REF} = 100 mV_{RMS}, f = 100kHz		–70		dB
	Digital feed through	$\overline{CS}$ = 1 and f_{CLK} = 1 MHz		2		nV/s
	Total harmonic distortion	V_{REF} = 5 V_{PP}, Data = FFFFh, f = 1 kHz		–105		dB
	Output spot noise voltage	f = 1 kHz, BW = 1 Hz		12		nV/√Hz

(1) Specified by design and characterization; not production tested.
(2) All ac characteristic tests are performed in a closed-loop system using the THS4011 I-to-V converter amplifier.

7.6 Timing Requirements

			MIN	NOM	MAX	UNIT
INTERFACE TIMING						
f_{CLK}	Clock input frequency				50	MHz
$t_{(CH)}$	Clock pulse width high		10			ns
$t_{(CL)}$	Clock pulse width low		10			ns
$t_{(CSS)}$	$\overline{CS}$ to Clock setup time		0			ns
$t_{(CSH)}$	Clock to $\overline{CS}$ hold time		10			ns
$t_{(DS)}$	Data setup time		5			ns
$t_{(DH)}$	Data hold time		10			ns
AC CHARACTERISTICS(1) (2)						
t_s	Output voltage settling time	To ±0.1% of full-scale, Data = 0000h to FFFFh to 0000h		0.3		µs
		To ±0.0015% of full-scale, Data = 0000h to FFFFh to 0000h		0.5		µs

(1) Specified by design and characterization; not production tested.
(2) All ac characteristic tests are performed in a closed-loop system using the THS4011 I-to-V converter amplifier.

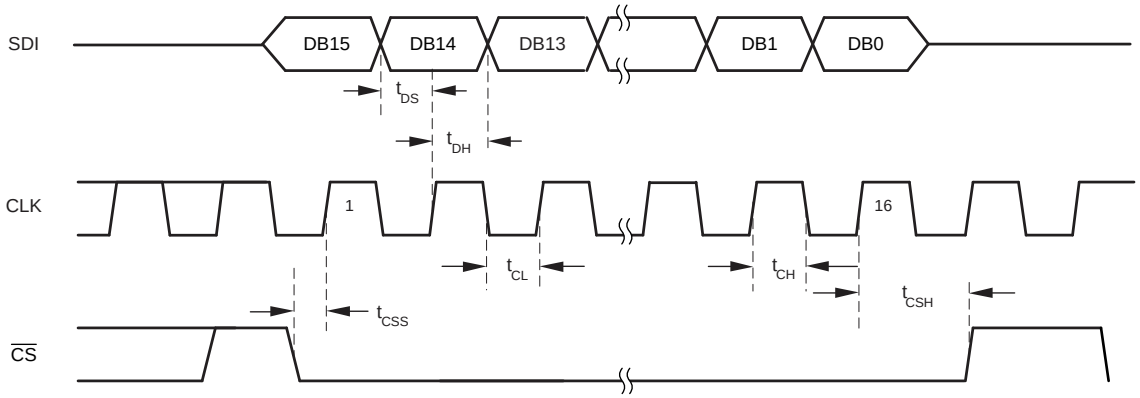
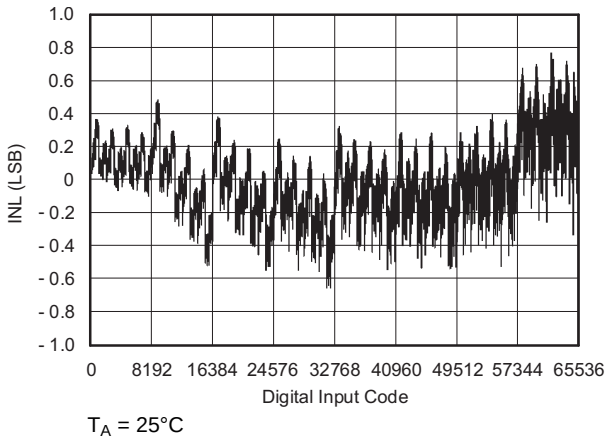


Figure 1. DAC8811 Timing Diagram

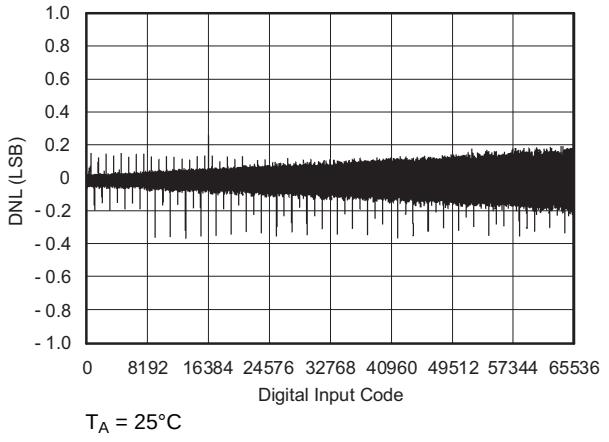
7.7 Typical Characteristics: V_{DD} = 5 V

At T_A = 25°C, $+V_{DD}$ = 5 V, unless otherwise noted.



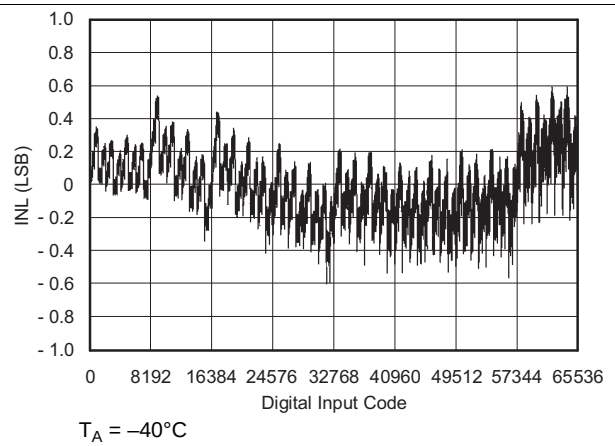
T_A = 25°C

Figure 2. Linearity Error vs Digital Input Code



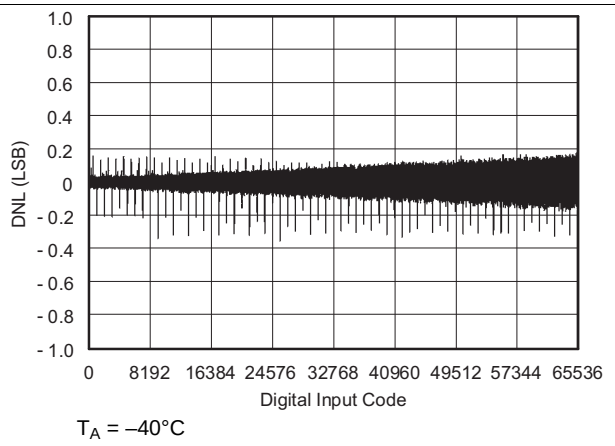
T_A = 25°C

Figure 3. Differential Linearity Error vs Digital Input Code



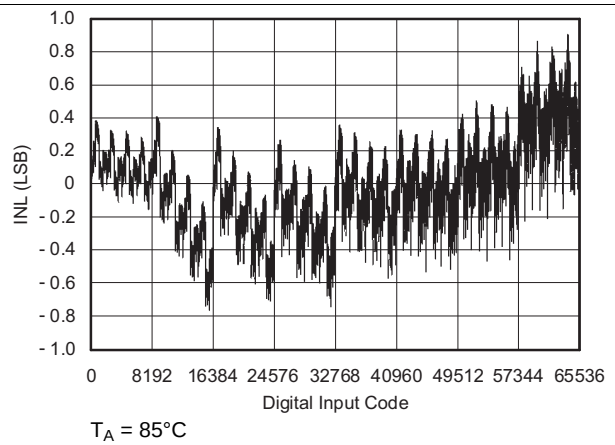
T_A = –40°C

Figure 4. Linearity Error vs Digital Input Code



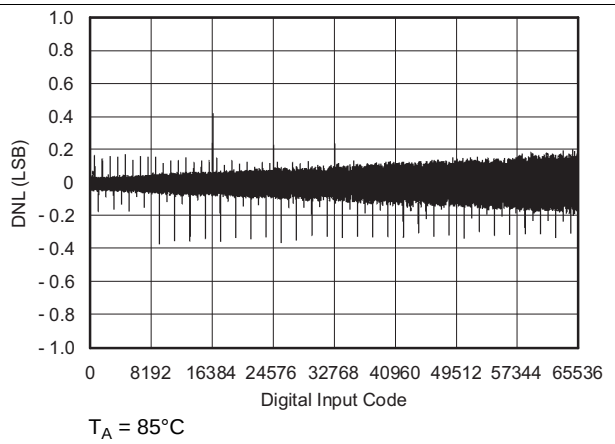
T_A = –40°C

Figure 5. Differential Linearity Error vs Digital Input Code



T_A = 85°C

Figure 6. Linearity Error vs Digital Input Code



T_A = 85°C

Figure 7. Differential Linearity Error vs Digital Input Code

Typical Characteristics: V_{DD} = 5 V (continued)

At T_A = 25°C, $+V_{DD}$ = 5 V, unless otherwise noted.

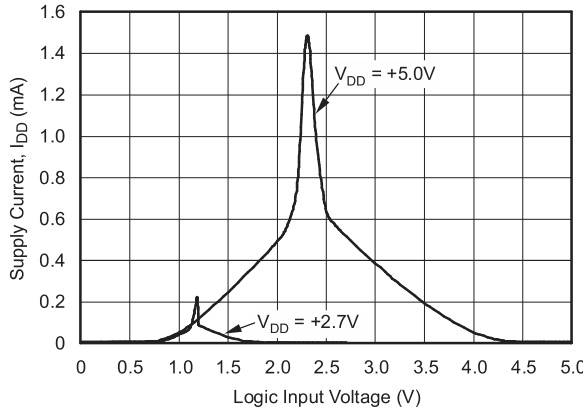


Figure 8. Supply Current vs Logic Input Voltage

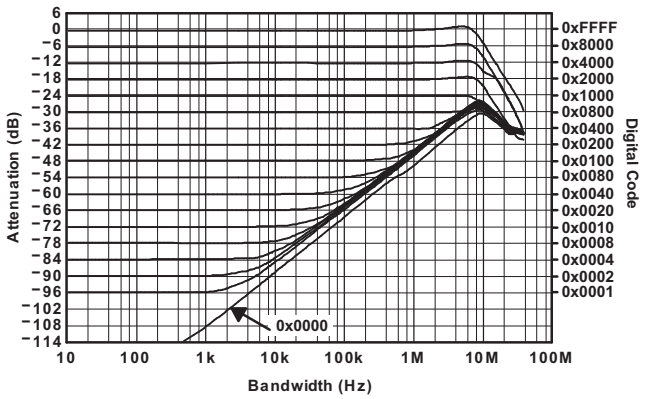


Figure 9. Reference Multiplying Bandwidth

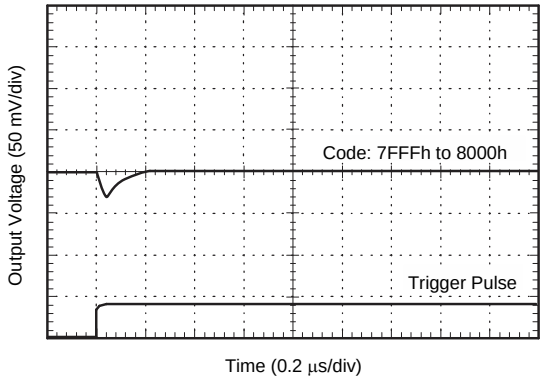


Figure 10. DAC Glitch

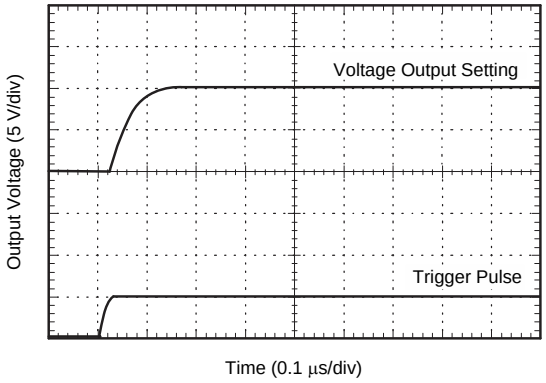
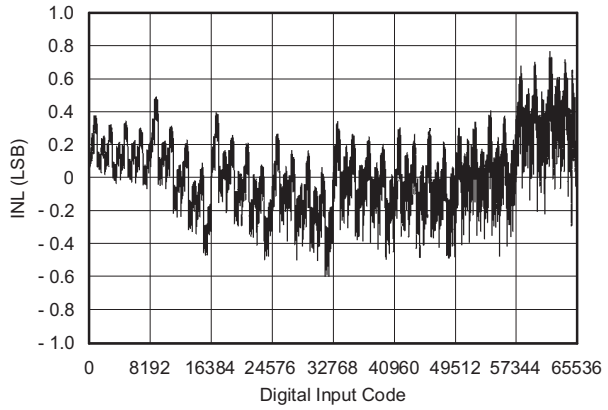


Figure 11. DAC Settling Time

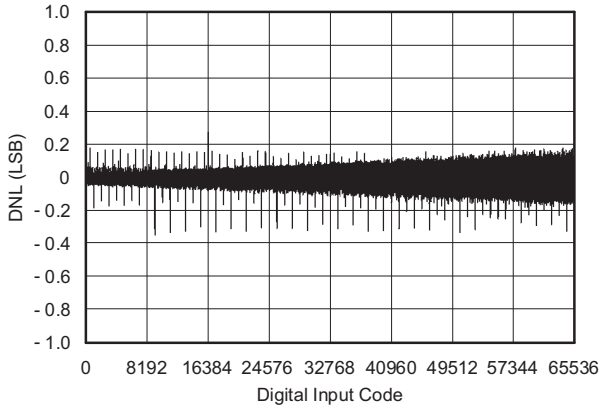
7.8 Typical Characteristics: V_{DD} = 2.7 V

At T_A = 25°C, $+V_{DD}$ = 2.7 V, unless otherwise noted.



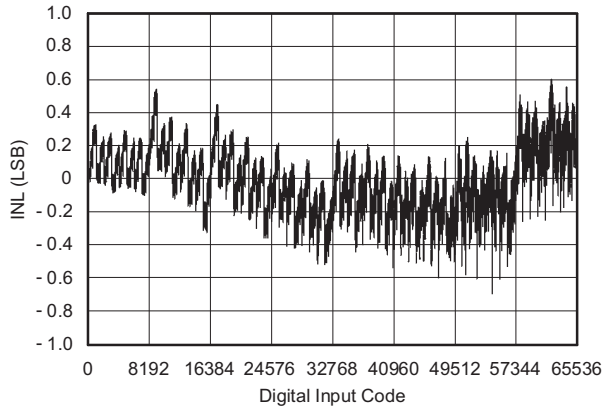
T_A = 25°C

Figure 12. Linearity Error vs Digital Input Code



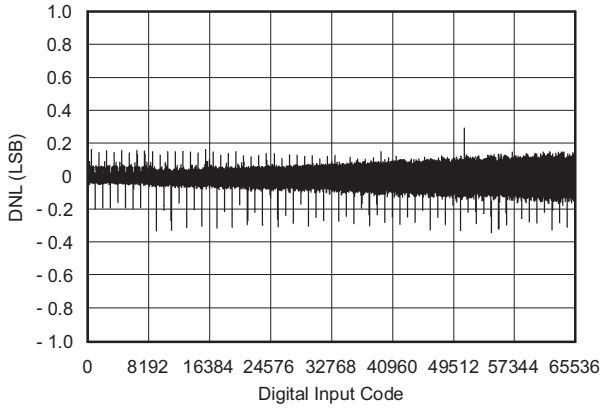
T_A = 25°C

Figure 13. Differential Linearity Error vs Digital Input Code



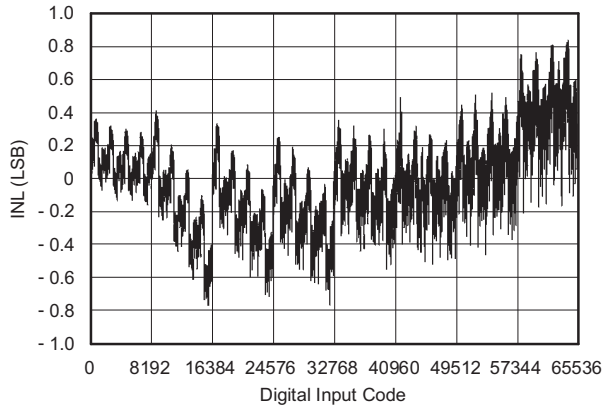
T_A = –40°C

Figure 14. Linearity Error vs Digital Input Code



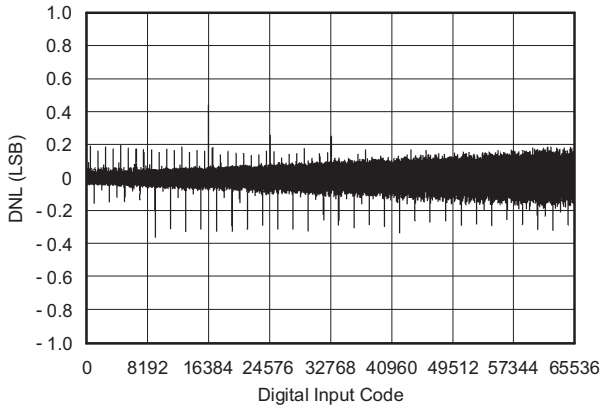
T_A = –40°C

Figure 15. Differential Linearity Error vs Digital Input Code



T_A = 85°C

Figure 16. Linearity Error vs Digital Input Code



T_A = 85°C

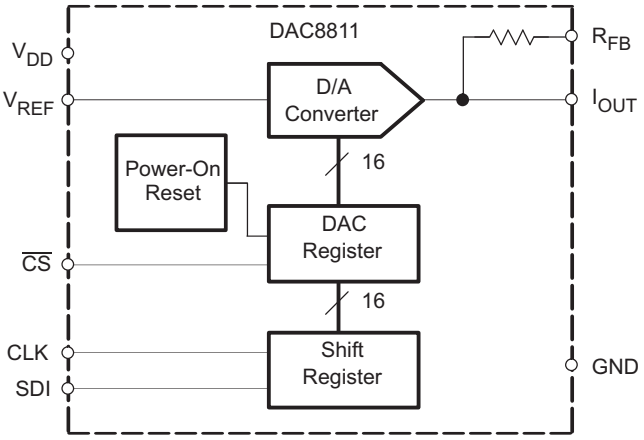
Figure 17. Differential Linearity Error vs Digital Input Code

8 Detailed Description

8.1 Overview

The DAC8811 is a single channel current output, 16-bit digital-to-analog converter (DAC). The device includes a 3-wire serial interface to communicate with most DSPs.

8.2 Functional Block Diagram



8.3 Feature Description

The DAC8811 is a single channel current output, 16-bit digital-to-analog converter (DAC). The architecture, illustrated in Figure 18, is an R-2R ladder configuration with the three MSBs segmented. Each 2R leg of the ladder is either switched to GND or the I_{OUT} terminal. The I_{OUT} terminal of the DAC is held at a virtual GND potential by the use of an external I/V converter op amp. The R-2R ladder is connected to an external reference input V_{REF} that determines the DAC full-scale current. The R-2R ladder presents a code independent load impedance to the external reference of 5 kΩ ±25%. The external reference voltage can vary in a range of -15 V to 15 V, thus providing bipolar I_{OUT} current operation. By using an external I/V converter and the DAC8811 R_{FB} resistor, output voltage ranges of $-V_{REF}$ to V_{REF} can be generated.

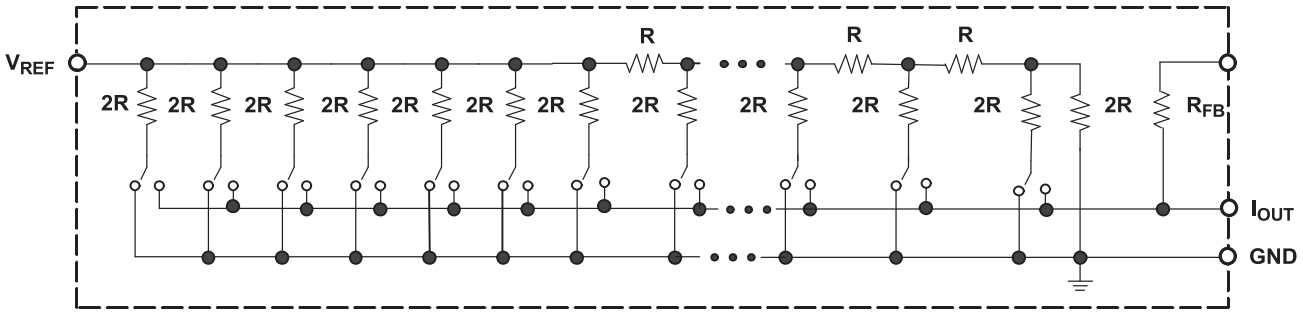


Figure 18. Equivalent R-2R DAC Circuit

When using an external I/V converter and the DAC8811 R_{FB} resistor, the DAC output voltage is given by Equation 1:

$$V_{OUT} = -V_{REF} \times \frac{CODE}{65536} \quad (1)$$

Feature Description (continued)

Each DAC code determines the 2R leg switch position to either GND or I_{OUT}. Because the DAC output impedance as seen looking into the I_{OUT} terminal changes versus code, the external I/V converter noise gain will also change. Because of this, the external I/V converter op amp must have a sufficiently low offset voltage such that the amplifier offset is not modulated by the DAC I_{OUT} terminal impedance change. External op amps with large offset voltages can produce INL errors in the transfer function of the DAC8811 due to offset modulation versus DAC code. For best linearity performance of the DAC8811, an operational amplifier (OPA277) is recommended (Figure 19). This circuit allows V_{REF} swinging from -10 V to +10 V.

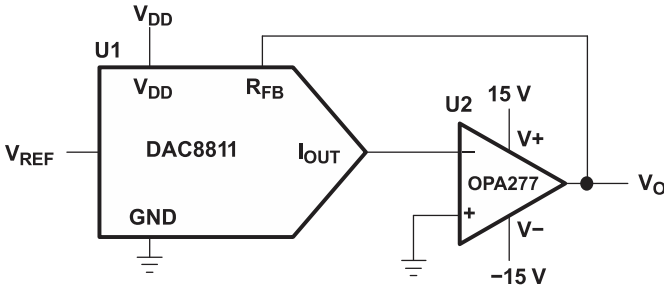


Figure 19. Voltage Output Configuration

8.3.1 Stability Circuit

For a current-to-voltage design (see Figure 20), the DAC8811 current output (I_{OUT}) and the connection with the inverting node of the op amp should be as short as possible and according to correct PCB layout design. For each code change, there is a step function. If the GBP of the op amp is limited and parasitic capacitance is excessive at the inverting node then gain peaking is possible. Therefore, for circuit stability, a compensation capacitor C1 (4 pF to 20 pF typ) can be added to the design, as shown in Figure 20.

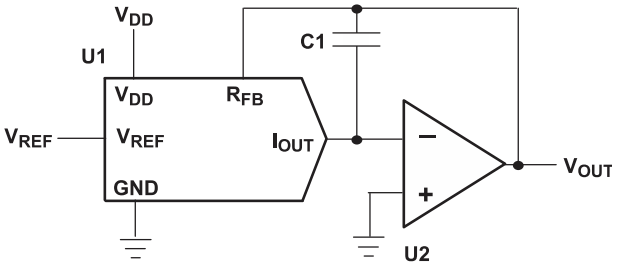


Figure 20. Gain Peaking Prevention Circuit With Compensation Capacitor

8.3.2 Positive Voltage Output Circuit

As Figure 21 illustrates, in order to generate a positive voltage output, a negative reference is input to the DAC8811. This design is suggested instead of using an inverting amp to invert the output due to tolerance errors of the resistor. For a negative reference, V_{OUT} and GND of the reference are level-shifted to a virtual ground and a –2.5 V input to the DAC8811 with an op amp.

Feature Description (continued)

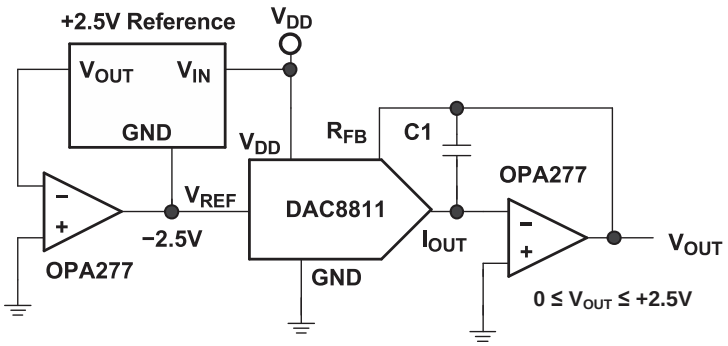


Figure 21. Positive Voltage Output Circuit

8.3.3 Bipolar Output Circuit

The DAC8811, as a 2-quadrant multiplying DAC, can be used to generate a unipolar output. The polarity of the full-scale output I_{OUT} is the inverse of the input reference voltage at V_{REF}.

Some applications require full 4-quadrant multiplying capabilities or bipolar output swing. As shown in Figure 22, external op amp U4 is added as a summing amp and has a gain of 2X that widens the output span to 5 V. A 4-quadrant multiplying circuit is implemented by using a 2.5-V offset of the reference voltage to bias U4. According to the circuit transfer equation given in Equation 2, input data (D) from code 0 to full scale produces output voltages of V_{OUT} = -2.5 V to V_{OUT} = +2.5 V.

$$V_{OUT} = \left(\frac{D}{32,768} - 1 \right) \times V_{REF} \tag{2}$$

External resistance mismatching is the significant error in Figure 22.

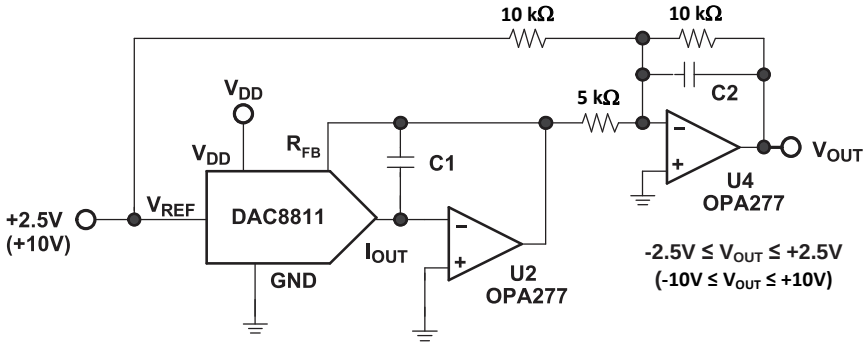


Figure 22. Bipolar Output Circuit

8.3.4 Programmable Current Source Circuit

A DAC8811 can be integrated into the circuit in Figure 23 to implement an improved Howland current pump for precise voltage to current conversions. Bidirectional current flow and high voltage compliance are two features of the circuit. With a matched resistor network, the load current of the circuit is shown by Equation 3:

$$I_L = \frac{(R2 + R3) / R1}{R3} \times V_{REF} \times D \tag{3}$$

The value of R3 in the previous equation can be reduced to increase the output current drive of U3. U3 can drive ±20 mA in both directions with voltage compliance limited up to 15 V by the U3 voltage supply. Elimination of the circuit compensation capacitor C1 in the circuit is not suggested as a result of the change in the output impedance Z_O, according to Equation 4:

Feature Description (continued)

$$Z_O = \frac{R1'R3(R1+R2)}{R1(R2'+R3') - R1'(R2=R3)} \quad (4)$$

As shown in Equation 4, with matched resistors, Z_O is infinite and the circuit is optimum for use as a current source. However, if unmatched resistors are used, Z_O is positive or negative with negative output impedance being a potential cause of oscillation. Therefore, by incorporating C1 into the circuit, possible oscillation problems are eliminated. The value of C1 can be determined for critical applications; for most applications, however, a value of several pF is suggested.

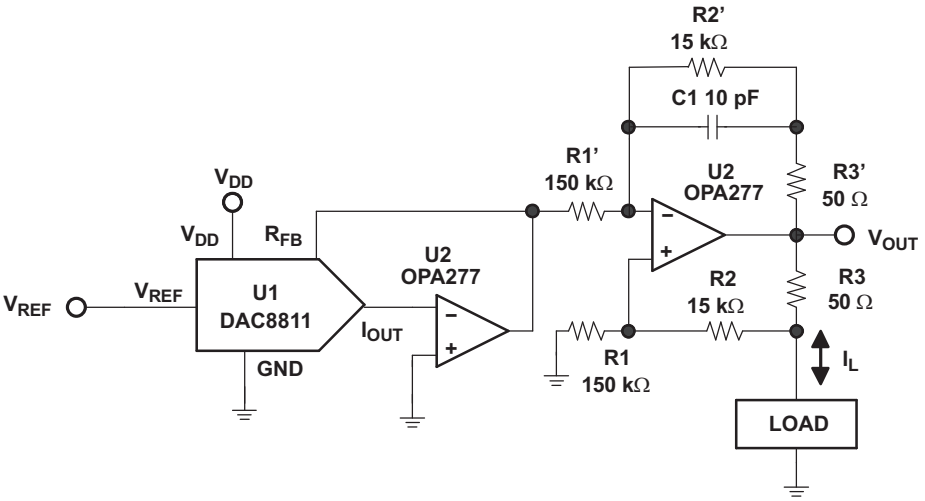


Figure 23. Programmable Bidirectional Current Source Circuit

8.4 Device Functional Mode

Table 1. Control Logic Truth Table(1)

CLK	$\overline{CS}$	SERIAL SHIFT REGISTER	DAC REGISTER
X	H	No effect	Latched
↑+	L	Shift register data advanced one bit	Latched
X	H	No effect	Latched
X	↑+	Shift register data transferred to DAC register	New data loaded from serial register

(1) ↑+ Positive logic transition; X = Don't care

8.5 Programming

8.5.1 DAC8811 Input Shift Register

The DAC8811 has a 3-wire serial interface ($\overline{CS}$, SCLK, and DIN) compatible with SPI, QSPI, and Microwire interface standards, as well as most DSPs. See Figure 1 for an example of a typical write sequence.

The input shift register is 16 bits wide, as shown in Figure 25. The write sequence begins by bringing the $\overline{CS}$ line low. Data from the DIN line are clocked into the 16-bit shift register on each rising edge of CLK. The serial clock frequency can be as high as 50 MHz, making the DAC8811 compatible with high-speed DSPs. On the 16th rising edge of the serial clock, the last data bit is clocked in and the programmed function is executed.

At this point, the $\overline{CS}$ line may be kept low or brought high. In either case, it must be brought high for a minimum of 20 ns before the next write sequence so that a falling edge of $\overline{CS}$ can initiate the next write sequence.

Figure 24. Data Input Register

DB15															DB0
D15	D15	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

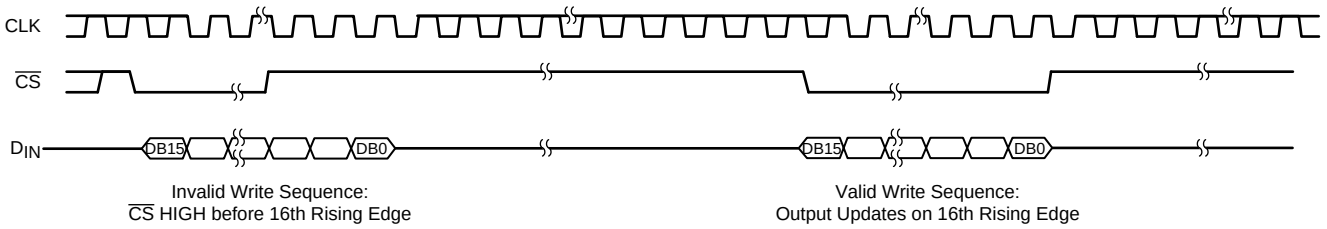


Figure 25. $\overline{CS}$ Interrupt Facility

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This design features the DAC8811 followed by a four-quadrant circuit for multiplying DACs. The circuit conditions the current output of an MDAC into a symmetrical bipolar voltage. The design uses an operational amplifier in a transimpedance configuration to convert the MDAC current into a voltage followed by an additional amplifier in a summing configuration to apply an offset voltage.

9.2 Typical Application

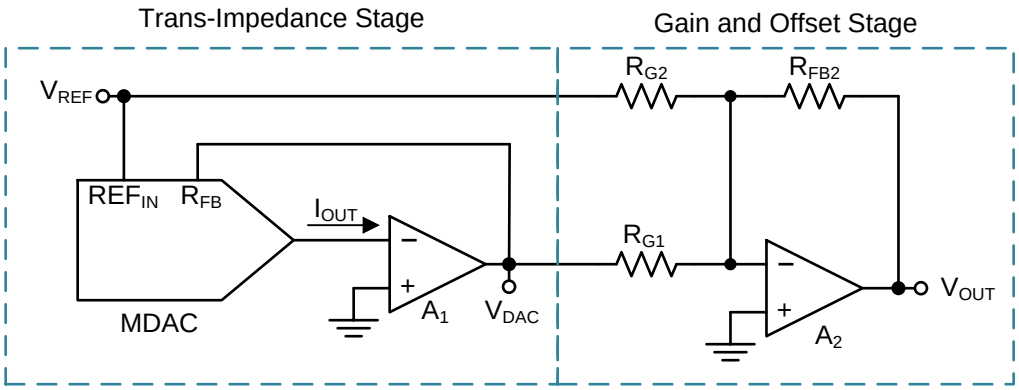


Figure 26. Typical Application

9.2.1 Design Requirements

Using a multiplying DAC requires a transimpedance stage with an amplifier with minimal input offset voltage. The tolerance of the external resistors will vary depending on the goals of the application, but for optimal performance with the DAC8811 the tolerance should be 0.1 % for all of the external resistors. The summing stage amplifier also needs low input-offset voltage and enough slew rate for the output range desired.

9.2.2 Detailed Design Procedure

The first stage of the design converts the current output of the MDAC (I_{OUT}) to a voltage (V_{OUT}) using an amplifier in a transimpedance configuration. A typical MDAC features an on-chip feedback resistor sized appropriately to match the ratio of the resistor values used in the DAC R-2R ladder. This resistor is available using the input shown in Figure 26 called RFB on the MDAC. The MDAC reference and the output of the transimpedance stage are then connected to the inverting input of the amplifier in the summing stage to produce the output that is defined by Equation 5.

$$V_{OUT}(Code) = \left(\frac{2_{FB2}}{R_{G1}} \times \frac{V_{REF} \times Code}{2^{bits}}\right) - \left(\frac{R_{FB2}}{R_{G2}} \times V_{REF}\right) \quad (5)$$

Typical Application (continued)

9.2.3 Application Curves

Figure 27 shows the output voltage vs code of this design, while Figure 28 shows the output error vs code. Keep in mind that the error gets worse as the output code increases because the contribution of the gain error increases with code.

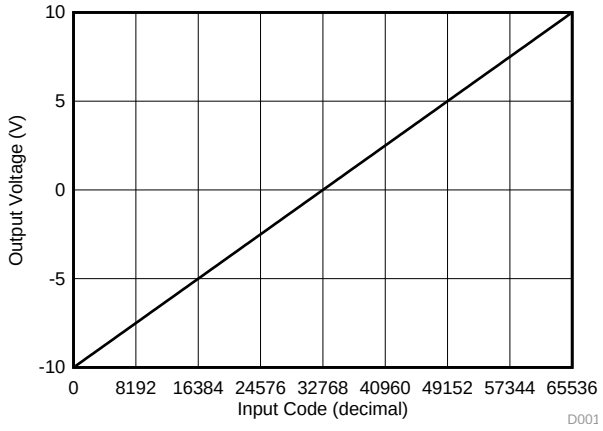


Figure 27. Output Voltage vs Input Code

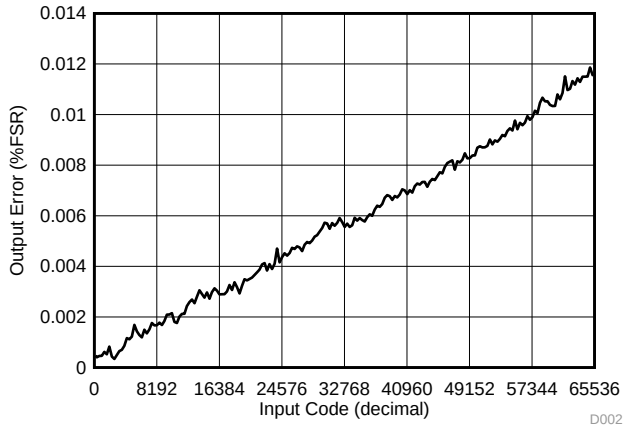


Figure 28. Output Current vs Input Code

10 Power Supply Recommendations

These devices can operate within the specified supply voltage range of 2.7 V to 5.5 V. The power applied to AVDD should be well-regulated and low-noise. In order to further minimize noise from the power supplies, a strong recommendation is to include a pair of 100 pF and 1 nF capacitors and a 0.1 µF to 1 µF bypass capacitor. The current consumption of the AVDD pin, the short-circuit current limit, and the load current for these devices are listed in the *Electrical Characteristics* table. Choose the power supplies for these devices to meet the aforementioned current requirements.

11 Layout

11.1 Layout Guidelines

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies. The DAC8811devices offer single-supply operation, and are often used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to keep digital noise from appearing at the output. As a result of the single ground pin of the DAC8811, all return currents (including digital and analog return currents for the DAC) must flow through a single point. Ideally, GND would be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they were connected at the power-entry point of the system. The power applied to AVDD should be well-regulated and low noise. Switching power supplies and dc-dc converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output. As with the GND connection, AVDD should be connected to a power-supply plane or trace that is separate from the connection for digital logic until they are connected at the power-entry point. In addition, a pair of 100-pF to 1-nF capacitors and a 0.1-µF to 1-µF bypass capacitor are strongly recommended. In some situations, additional bypassing may be required, such as a 100 µF electrolytic capacitor or even a pi filter made up of inductors and capacitors – all designed essentially to provide low-pass filtering for the supply and remove the high-frequency noise.

While all the other recommendations apply to most DACs, multiplying DACs also require that the transimpedance amplifier be placed in close proximity in order to minimize non-linearity errors introduced by any resistance between the I_{OUT} pin and V- pin of the amplifier.

11.2 Layout Example

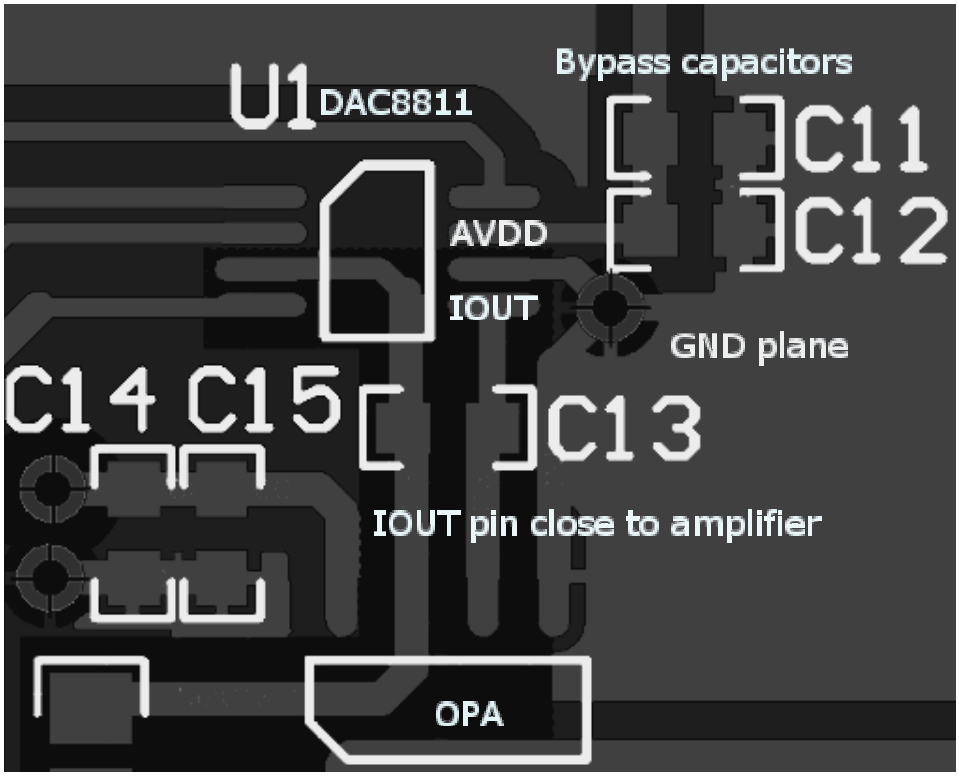


Figure 29. DAC8811 Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *DAC8801/11EVM*, SLAU151
- *Interfacing the DAC8811 to the MSP430F449*, SLAA238
- *Topology and Noise Using Multiplying DAC*, SBAA146

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC8811IBDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 105	D11	Samples
DAC8811IBDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 105	D11	Samples
DAC8811IBDGKTG4	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	D11	Samples
DAC8811IBDRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	D11	Samples
DAC8811ICDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 105	D11	Samples
DAC8811ICDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 105	D11	Samples
DAC8811ICDRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	D11	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

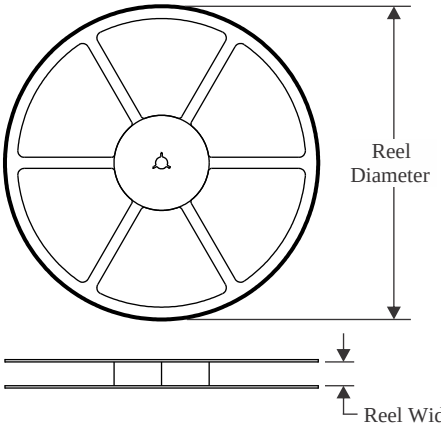
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

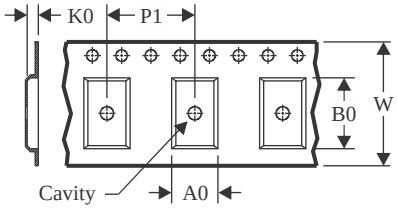
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

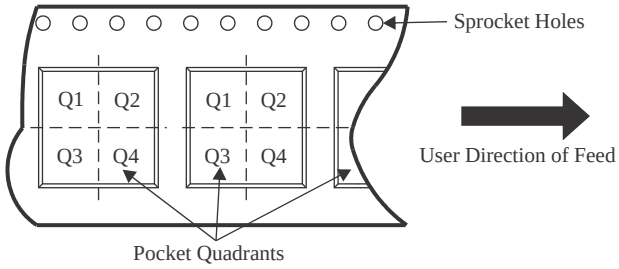


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

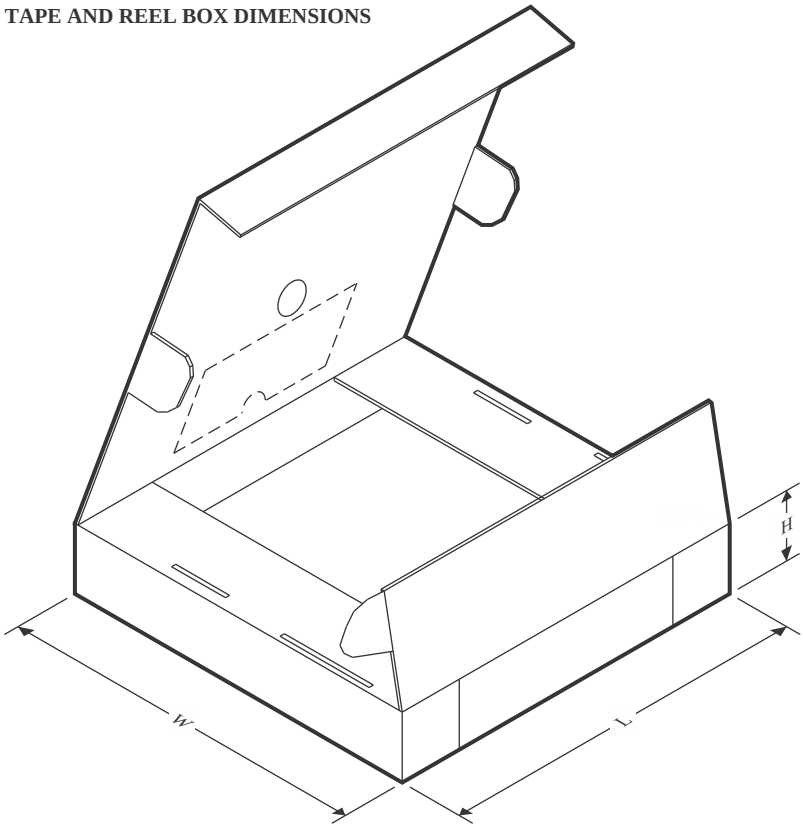
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8811IBDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
DAC8811IBDGKT	VSSOP	DGK	8	250	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
DAC8811IBDGKTG4	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC8811ICDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
DAC8811ICDGKT	VSSOP	DGK	8	250	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

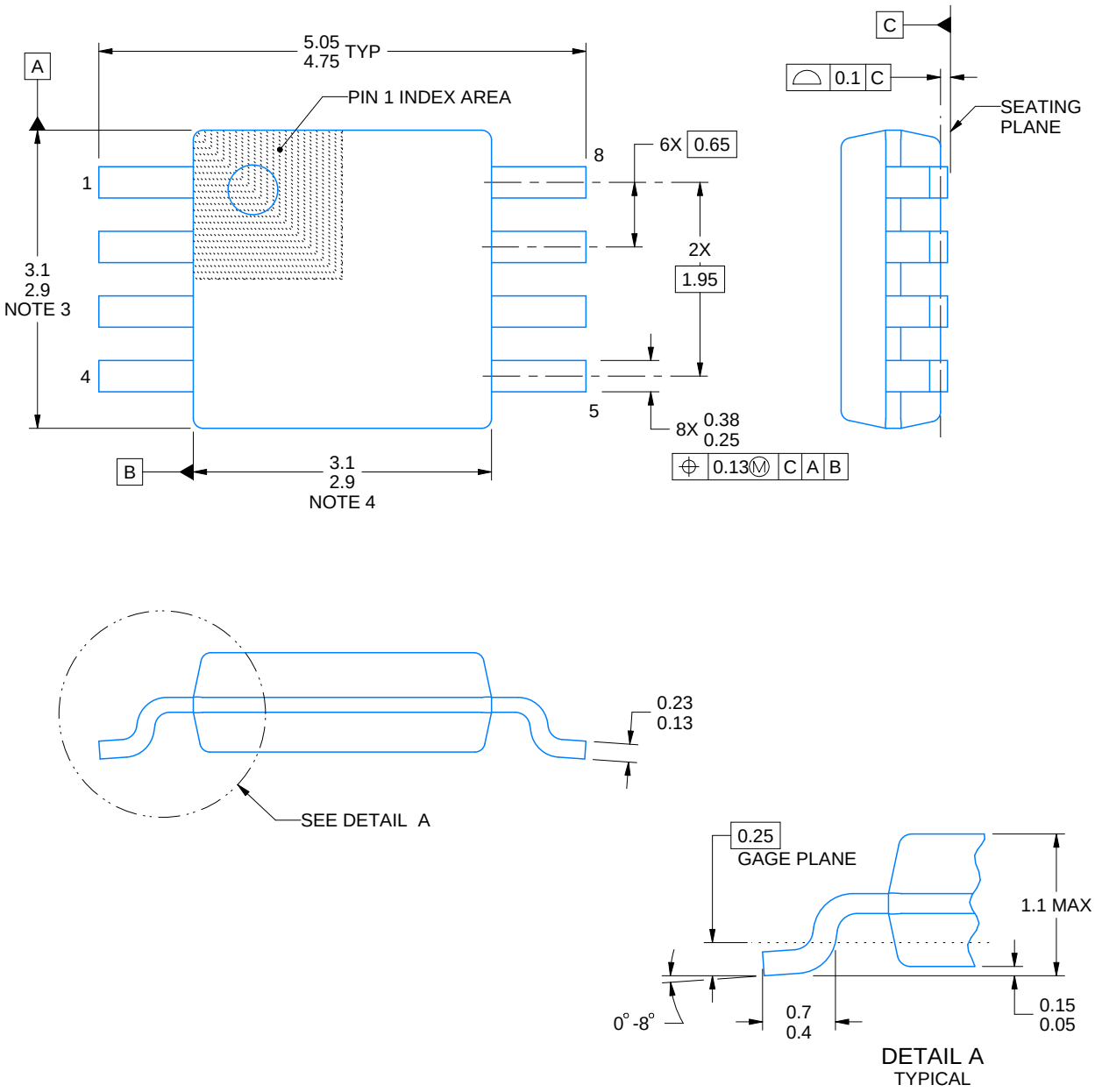
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8811IBDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
DAC8811IBDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
DAC8811IBDGKTG4	VSSOP	DGK	8	250	366.0	364.0	50.0
DAC8811ICDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
DAC8811ICDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

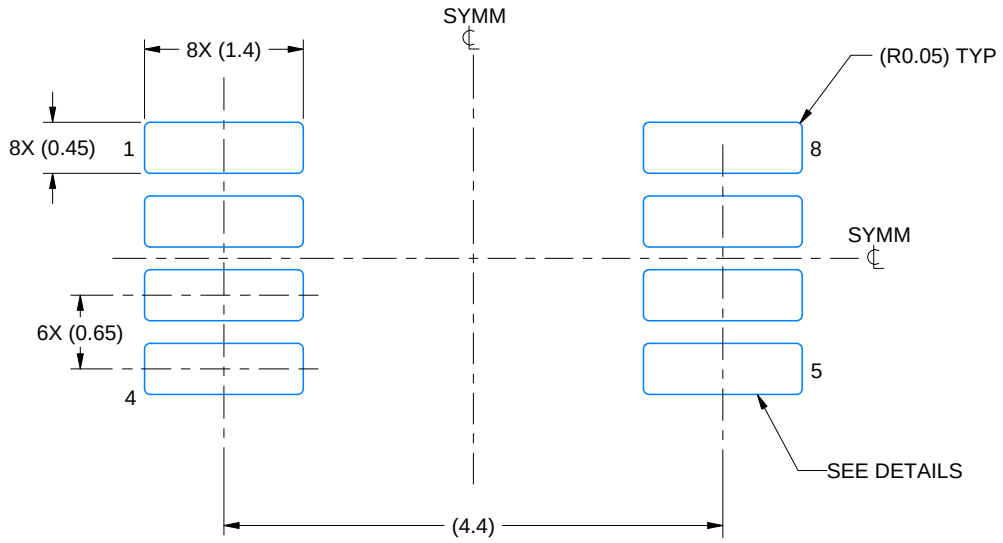
SMALL OUTLINE PACKAGE



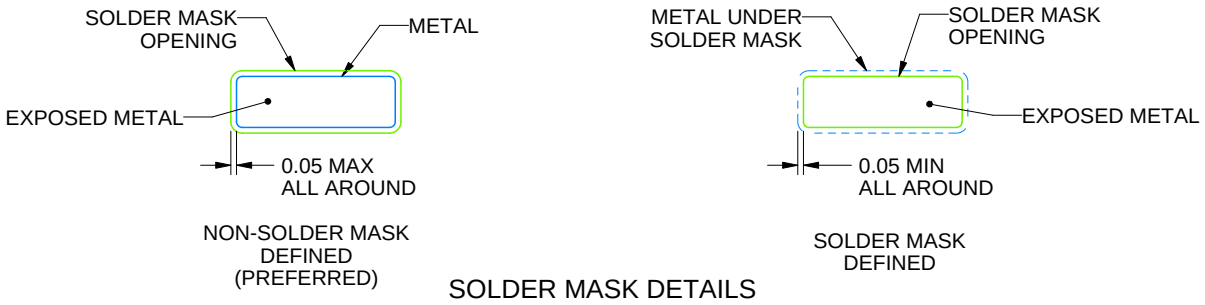
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

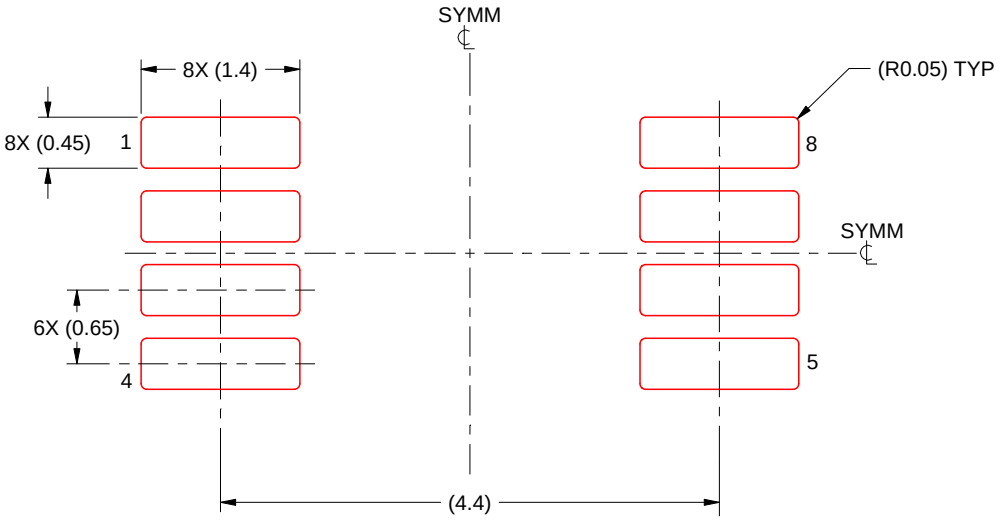


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

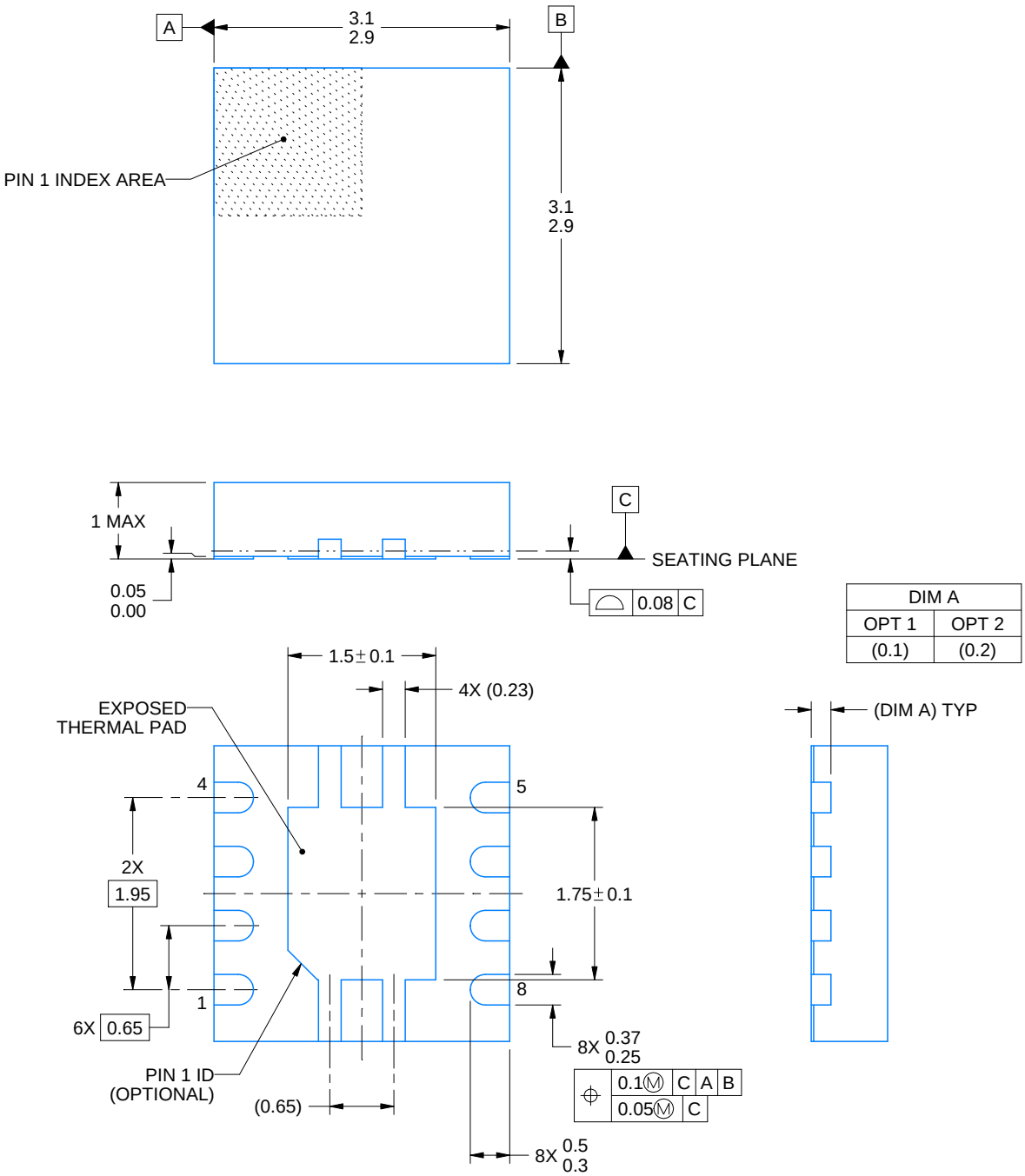
4203482/L

PACKAGE OUTLINE

DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

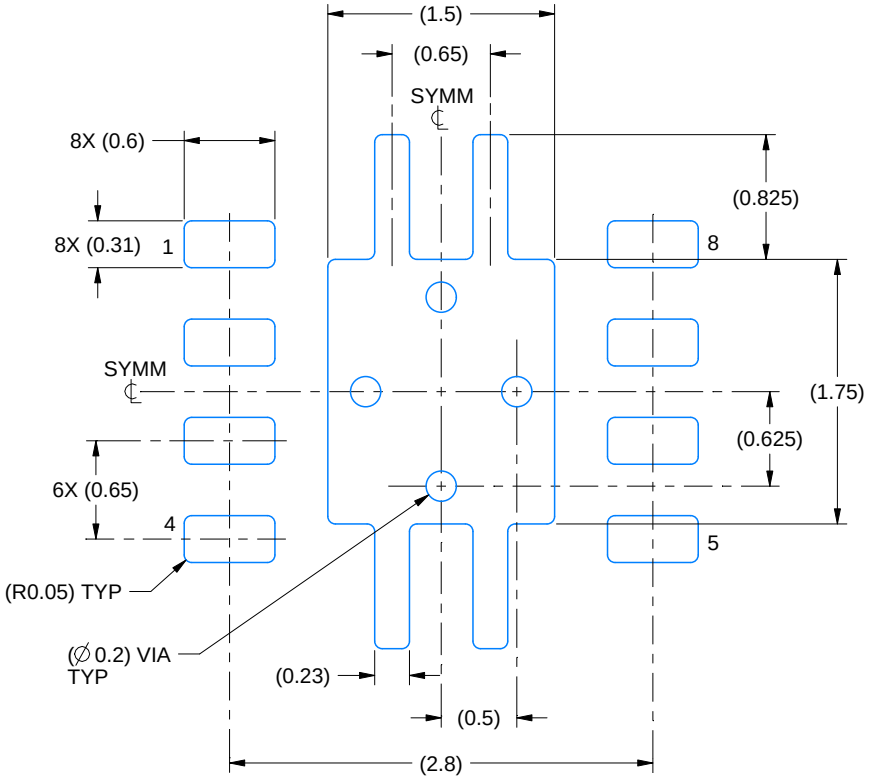
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

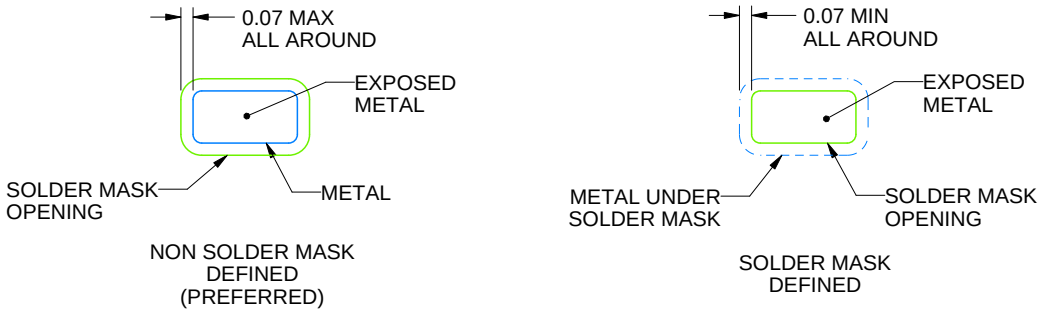
DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

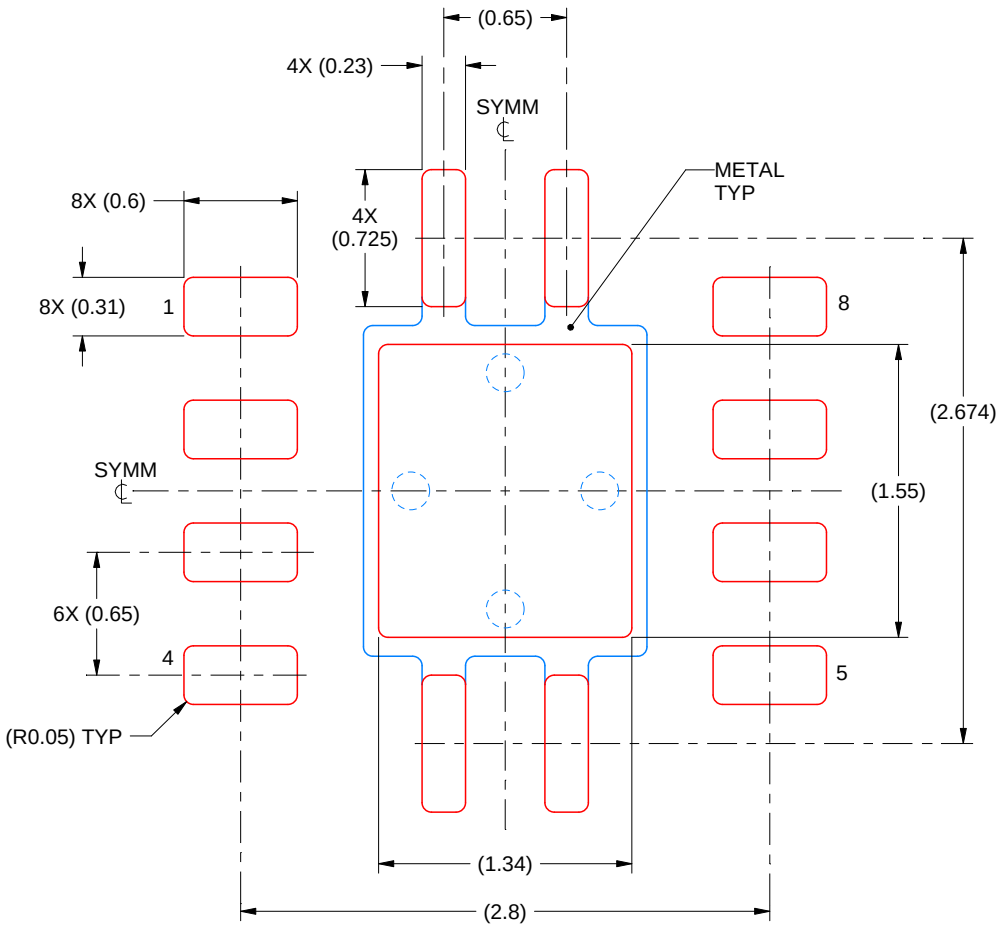


SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265