DRV8803 Quad Low-Side Driver IC

1 Features

- 4-Channel Protected Low-Side Driver
  - Four NMOS FETs With Overcurrent Protection
  - Integrated Inductive Clamp Diodes
  - Parallel Interface
- DW Package: 1.5A (Single Channel On) / 800mA (Four Channels On) Maximum Drive Current per Channel (at 25°C)
- PWP Package: 2A (Single Channel On) / 1A (Four Channels On) Maximum Drive Current per Channel (at 25°C, With Proper PCB Heatsinking)
- DYZ Package: 1.9A (Single Channel On) / 0.9A (Four Channels On) Maximum Drive Current per Channel (at 25°C, With Proper PCB Heatsinking)
- 8.2V to 60V Operating Supply Voltage Range
- Thermally Enhanced Surface Mount Package

2 Applications

- Relay Drivers
- Unipolar Stepper Motor Drivers
- Solenoid Drivers
- General Low-Side Switch Applications

3 Description

The DRV8803 provides a 4-channel low side driver with overcurrent protection. The device has built-in diodes to clamp turnoff transients generated by inductive loads and can be used to drive unipolar stepper motors, DC motors, relays, solenoids, or other loads.

In the SOIC (DW) package, the DRV8803 can supply up to 1.5A (one channel on) or 800mA (all channels on) continuous output current per channel, at 25°C. In the HTSSOP (PWP) package, the device can supply up to 2A (one channel on) or 1A (four channels on) continuous output current per channel, at 25°C . In the SOT-23-THN (DYZ) package, the DRV8803 can supply up to 1.9A (one channel on) or 900mA (all channels on) continuous output current per channel, at 25°C with proper PCB heatsinking.

The device is controlled through a simple parallel interface.

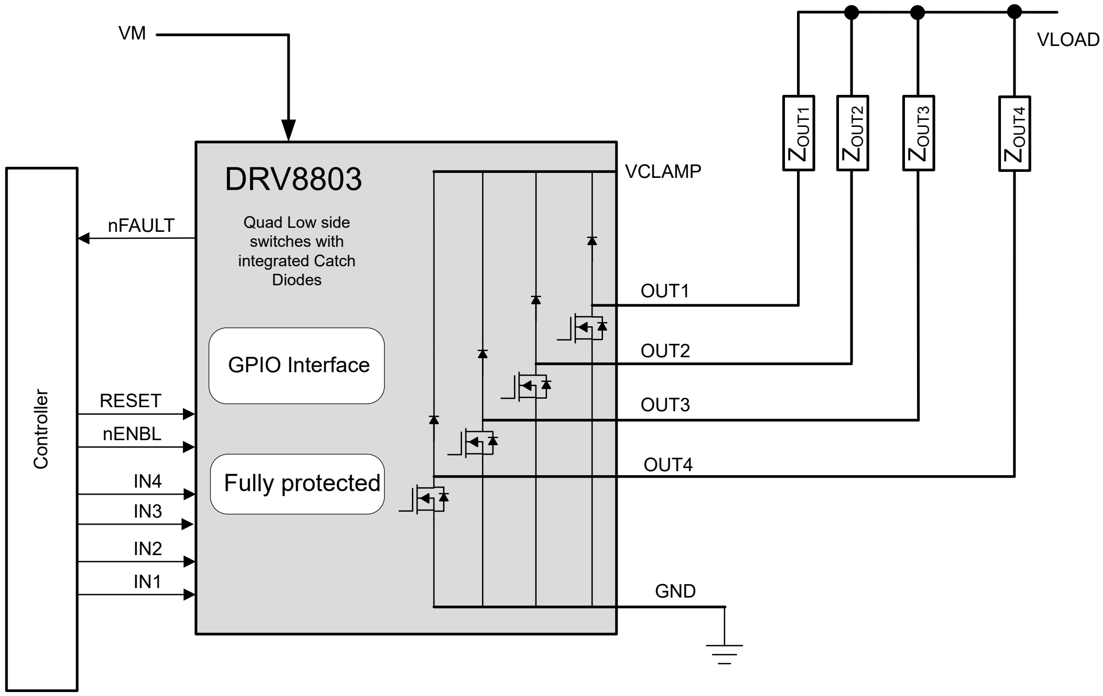
Internal shutdown functions are provided for over current protection, short circuit protection, undervoltage lockout and overtemperature and faults are indicated by a fault output pin.

The DRV8803 is available in a 20-pin thermally-enhanced SOIC package, 16-pin HTSSOP package and 16-pin SOT-23-THN package (Eco-friendly: RoHS & no Sb/Br).

Device Information (1)

PART NUMBER	PACKAGE	PACKAGE SIZE(2)	BODY SIZE (NOM)
DRV8803DW	SOIC (20)	12.80mm × 10.30mm	12.80mm × 7.50mm
DRV8803PWP	HTSSOP (16)	5.00mm × 6.40mm	5.00mm × 4.40mm
DRV8803DYZ	SOT-23-THN (16)	4.20mm × 2.00mm	4.20mm × 2.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

Table of Contents

1 Features...1
2 Applications...1
3 Description...1
4 Device Comparison...4
5 Pin Configuration and Functions...4
Pin Functions...4
6 Specification...6
6.1 Absolute Maximum Ratings...6
6.2 ESD Ratings...6
6.3 Recommended Operating Conditions...6
6.4 Thermal Information...6
6.5 Electrical Characteristics...7
6.6 Timing Requirements...9
6.7 Typical Characteristics...10
7 Detailed Description...11
7.1 Overview...11
7.2 Functional Block Diagram...11
7.3 Feature Description...11
7.4 Device Functional Modes...12
8 Application and Implementation...13
8.1 Application Information...13
8.2 Layout...18
9 Device and Documentation Support...21
9.1 Documentation Support...21
9.2 Community Resources...21
9.3 Trademarks...21
10 Revision History...21
11 Mechanical, Packaging, and Orderable Information...21

4 Device Comparison

Following is the Summary of the R_{ON} and package offerings for DRV8803

Part number	LS R_{ON}(TYP)	Package	Body Size (nominal)
DRV8803	500mΩ	SOIC (20)	12.80mm x 7.50mm
		HTSSOP (16)	5.00mm × 4.40mm
	400mΩ	SOT-23-THN (16)	4.20mm × 2mm

5 Pin Configuration and Functions

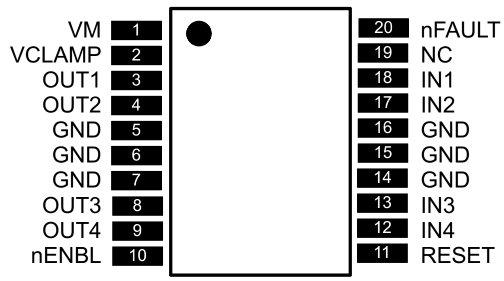


Figure 5-1. DW Package 20-Pin SOIC Top View

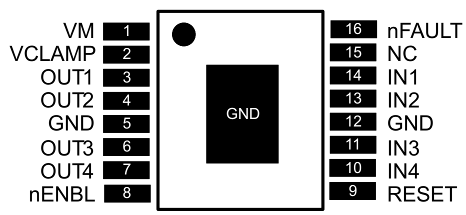


Figure 5-2. PWP Package 16-Pin HTSSOP Top View

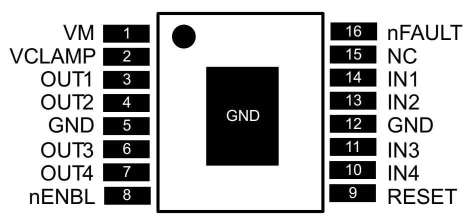


Figure 5-3. DYZ Package 16-Pin SOT-23-THN Top View

Pin Functions

PIN				I/O[1]	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	SOIC	HTSSOP	SOT-23-THN			
POWER AND GROUND						
GND	5, 6, 7, 14, 15, 16	5, 12, PPAD	5,12, PPAD	—	Device ground	All pins must be connected to GND.
VM	1	1	1	—	Device power supply	Connect to motor supply (8.2V - 60V).
CONTROL						
nENBL	10	8	8	I	Enable input	Active low enables outputs – internal pulldown

PIN				I/O[(1)]	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	SOIC	HTSSOP	SOT-23-THN			
RESET	11	9	9	I	Reset input	Active high resets internal logic and OCP – internal pulldown
IN1	18	14	14	I	Channel 1 input	IN1 = 1 drives OUT1 low – internal pulldown
IN2	17	13	13	I	Channel 2input	IN2 = 1 drives OUT2 low – internal pulldown
IN3	13	11	11	I	Channel 3 input	IN3 = 1 drives OUT3 low – internal pulldown
IN4	12	10	10	I	Channel 4 input	IN4 = 1 drives OUT4 low – internal pulldown
STATUS						
nFAULT	20	16	16	OD	Fault	Logic low when in fault condition (overtemperature, overcurrent)
OUTPUT						
OUT1	3	3	3	O	Output 1	Connect to load 1
OUT2	4	4	4	O	Output 2	Connect to load 2
OUT3	8	6	6	O	Output 3	Connect to load 3
OUT4	9	7	7	O	Output 4	Connect to load 4
VCLAMP	2	2	2	—	Output clamp voltage	Connect to VM supply, or zener diode to VM supply

(1) Directions: I = input, O = output, OD = open-drain output

6 Specification

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
VM	Power supply voltage	–0.3	65	V
VOUTx	Output voltage	–0.3	65	V
VCLAMP	Clamp voltage	–0.3	65	V
nFAULT	Output current		20	mA
	Peak clamp diode current		2	A
	DC or RMS clamp diode current		1	A
	Digital input pin voltage	–0.5	7	V
nFAULT	Digital output pin voltage	–0.5	7	V
	Peak motor drive output current, t < 1 μS	Internally limited		A
	Continuous total power dissipation	See *Thermal Information*		
T_J	Operating virtual junction temperature	–40	150	°C
T_{stg}	Storage temperature	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

				MIN	NOM	MAX	UNIT
V_M	Power supply voltage			8.2		60	V
V_{CLAMP}	Output clamp voltage(2)			0		60	V
I_{OUT}	Continuous output current	SOIC package(1), T_A = 25°C	Single channel on			1.5	A
			Four channels on			0.8	
		HTSSOP package(1), T_A = 25°C	Single channel on			2	
			Four channels on			1	
		DYZ package(1), T_A = 25°C	Single channel on			1.9	
			Four channels on			0.9	

(1) Power dissipation and thermal limits must be observed.
(2) V_{CLAMP} is used only to supply the clamp diodes. It is not a power supply input.

6.4 Thermal Information

THERMAL METRIC(1)		DRV8803			UNIT
		DW (SOIC)	PWP (HTSSOP)	DYZ (SOT -23 THN	
		20 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67.7	39.6	53.2	°C/W

THERMAL METRIC[(1)]		DRV8803			UNIT
		DW (SOIC)	PWP (HTSSOP)	DYZ (SOT -23 THN	
		20 PINS	16 PINS	16 PINS	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.9	24.6	76.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	35.4	20.3	22.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.2	0.7	8.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	34.9	20.1	22.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	2.3	9.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_A = 25°C, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VM}	VM operating supply current	V_M = 24 V		1.6	2.1	mA
V_{UVLO}	VM undervoltage lockout voltage	V_M rising			8.2	V
LOGIC-LEVEL INPUTS (SCHMITT TRIGGER INPUTS WITH HYSTERESIS)						
V_{IL}	Input low voltage			0.6	0.7	V
V_{IH}	Input high voltage		2			V
V_{HYS}	Input hysteresis			0.45		V
I_{IL}	Input low current	VIN = 0	–20		20	μA
I_{IH}	Input high current	VIN = 3.3 V			100	μA
R_{PD}	Pulldown resistance			100		kΩ
nFAULT OUTPUT (OPEN-DRAIN OUTPUT)						
V_{OL}	Output low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output high leakage current	V_O = 3.3 V			1	μA
LOW-SIDE FETS						
R_{ON}	FET on resistance, HTSSOP and SOIC package	V_M = 24 V, I_O = 700 mA, T_J = 25°C		0.5		Ω
		V_M = 24 V, I_O = 700 mA, T_J = 85°C		0.75	0.8	
	FET on resistance, SOT-23-THN package	V_M = 24 V, I_O = 700 mA, T_J = 25°C		0.4		Ω
		V_M = 24 V, I_O = 700 mA, T_J = 85°C			0.64	
I_{OFF}	Off-state leakage current		–50		50	μA
HIGH-SIDE DIODES						
V_F	Diode forward voltage	V_M = 24 V, I_O = 700 mA, T_J = 25°C		1.2		V
I_{OFF}	Off-state leakage current	V_M = 24 V, T_J = 25°C	–50		50	μA
OUTPUTS						
t_R	Rise time	V_M = 24 V, I_O = 700 mA, Resistive load	50		300	ns
t_F	Fall time	V_M = 24 V, I_O = 700 mA, Resistive load	50		300	ns
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		2.3		3.8	A
t_{OCP}	Overcurrent protection deglitch time			3.5		μs
t_{RETRY}	Overcurrent protection retry time			1.2		ms

T_A = 25°C, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{TSD}	Thermal shutdown temperature	Die temperature[1]	150	160	180	°C

(1) Not production tested.

6.6 Timing Requirements

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
1	$t_{OE(ENABLE)}$	Enable time, nENBL to output low		50	ns
2	$t_{PD(L-H)}$	Propagation delay time, INx to OUTx, low to high		800	ns
3	$t_{PD(H-L)}$	Propagation delay time, INx to OUTx, high to low		800	ns
—	t_{RESET}	RESET pulse width	20		µs

(1) Not production tested.

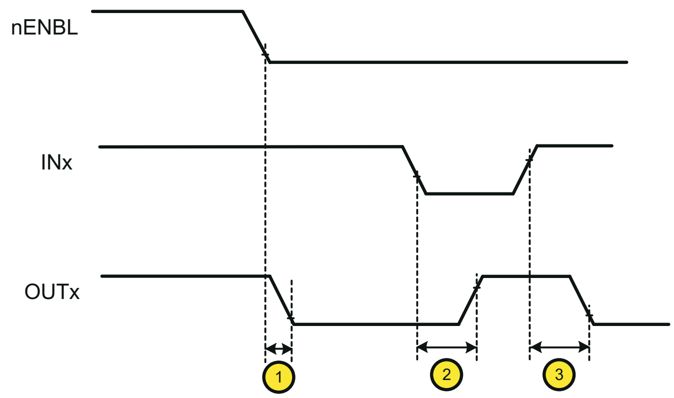


Figure 6-1. DRV8803 Timing Requirements

6.7 Typical Characteristics

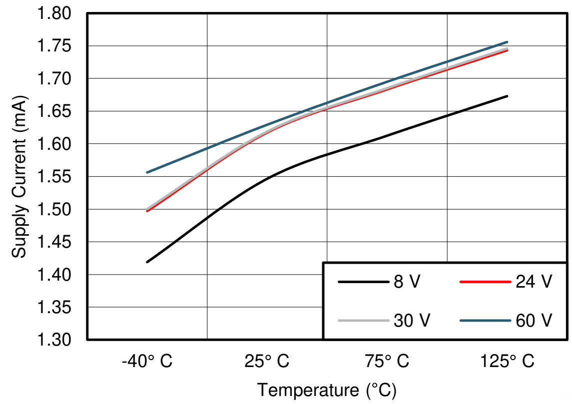


Figure 6-2. Supply Current Over Temperature

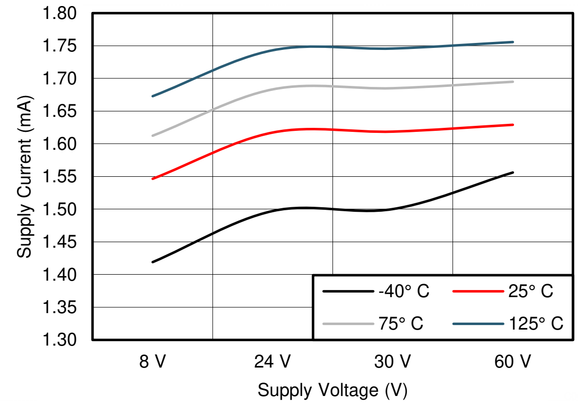


Figure 6-3. Supply Current Over V_M

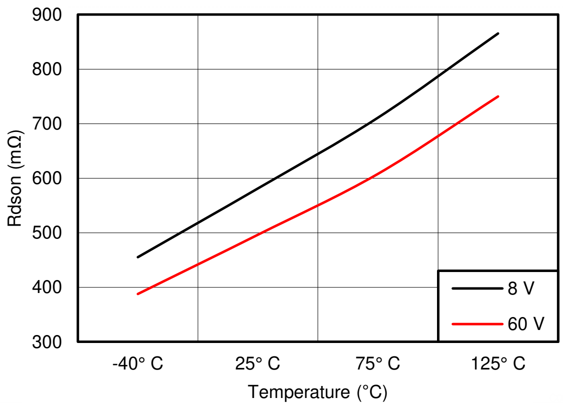


Figure 6-4. $R_{DS(on)}$ Over Temperature

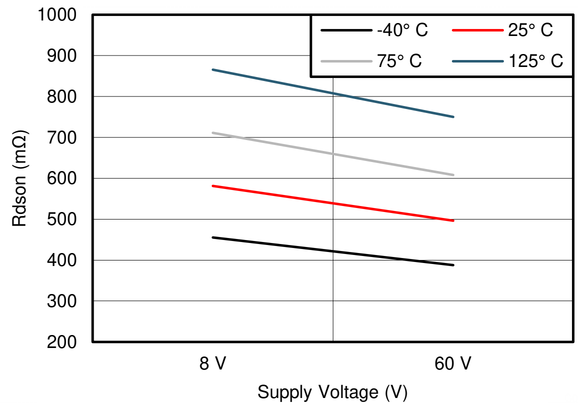


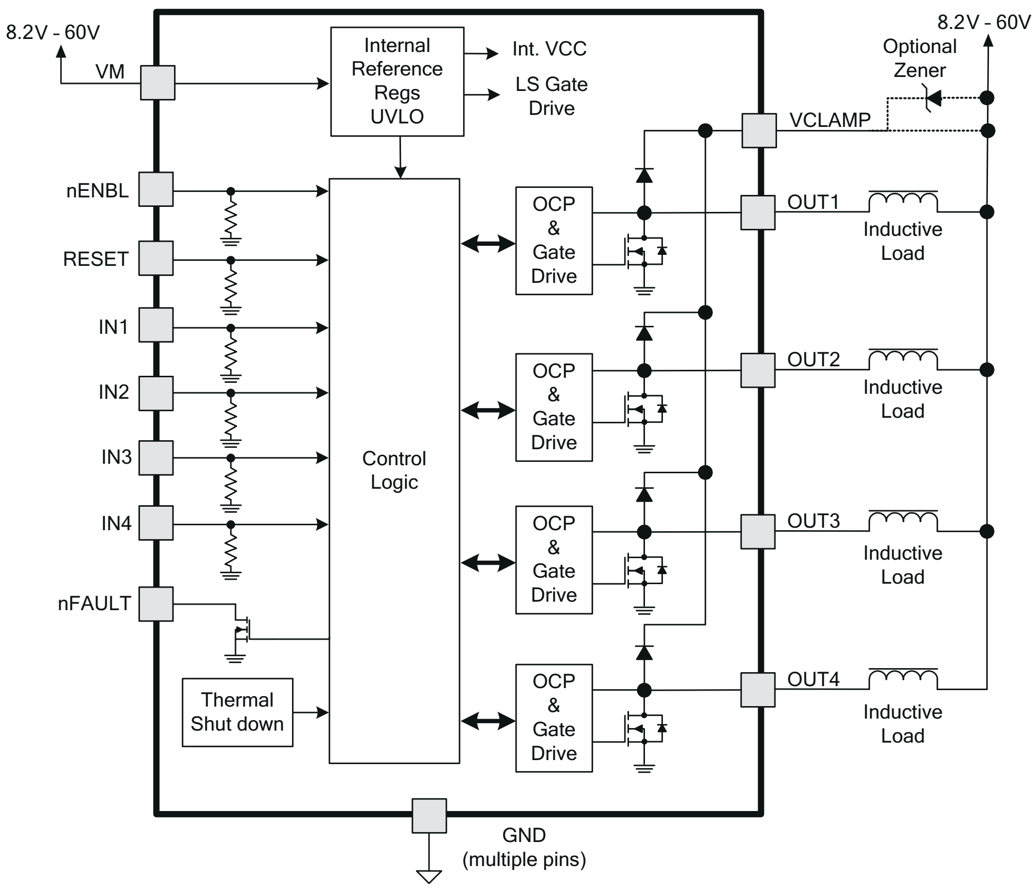
Figure 6-5. $R_{DS(on)}$ Over V_M

7 Detailed Description

7.1 Overview

The DRV8803 device is an integrated 4-channel low side driver solution for any low side switch application. The integrated overcurrent protection limits the motor current to a fixed maximum. Four logic inputs control the low-side driver outputs which consist of four N-channel MOSFETs that have a typical $R_{DS(on)}$ of 500mΩ (PWP and DW package) and 400 mΩ (DYZ Package). A single power input VM serves as the device power and is internally regulated to power the internal low side gate drive. Motor speed can be controlled with pulse-width modulation from 0kHz to 100kHz. The device outputs can be disabled by bringing nENBL pin high. The thermal shutdown protection lets the device automatically shut down if the die temperature exceeds a TTSD limit. UVLO protection will disable all circuitry in the device if V_M drops below the undervoltage lockout threshold.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Output Drivers

The DRV8803 device contains four protected low-side drivers. Each output has an integrated clamp diode connected to a common pin, VCLAMP.

VCLAMP can be connected to the main power supply voltage, VM. VCLAMP can also be connected to a Zener or TVS diode to VM, allowing the switch voltage to exceed the main supply voltage VM. This connection can be beneficial when driving loads that require very fast current decay, such as unipolar stepper motors.

In all cases, the voltage on the outputs must not be allowed to exceed the maximum output voltage specification.

7.3.2 Protection Circuits

The DRV8803 device is fully protected against undervoltage, overcurrent and overtemperature events.

7.3.2.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the t_{OCP} deglitch time (approximately 3.5μs), the driver will be disabled and the nFAULT pin will be driven low. The driver will remain disabled for the t_{RETRY} retry time (approximately 1.2ms), then the fault will be automatically cleared. The fault will be cleared immediately if either the RESET pin is activated or the VM is removed and reapplied.

7.3.2.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all output FETs will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level, operation will automatically resume.

7.3.2.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled, and internal logic will be reset. Operation will resume when VM rises above the UVLO threshold.

7.4 Device Functional Modes

7.4.1 Parallel Interface Operation

The DRV8803 device is controlled with a simple parallel interface. Logically, the interface is shown in Figure 7-1.

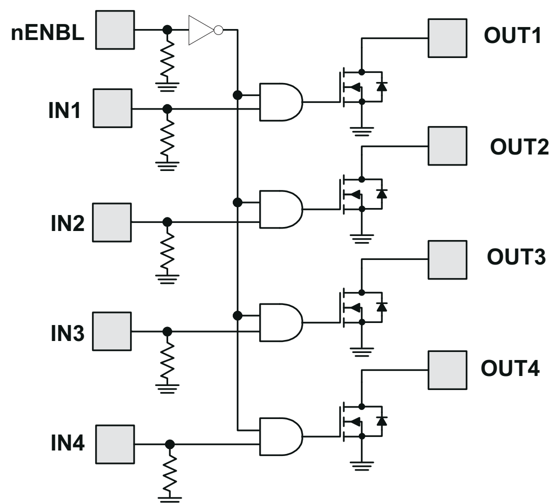


Figure 7-1. Parallel Interface Operation

7.4.2 nENBL and RESET Operation

The nENBL pin enables or disables the output drivers. nENBL must be low to enable the outputs. Note that nENBL has an internal pulldown.

The RESET pin, when driven active high, resets internal logic. All inputs are ignored while RESET is active. Note that RESET has an internal pulldown. An internal power-up reset is also provided, so it is not required to drive RESET at power up.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8803 device can be used to drive upto four independent unipolar loads such as unipolar BDCs, solenoids such as valves, relays etc. or to drive one unipolar stepper

8.1.1 Application as Load driver

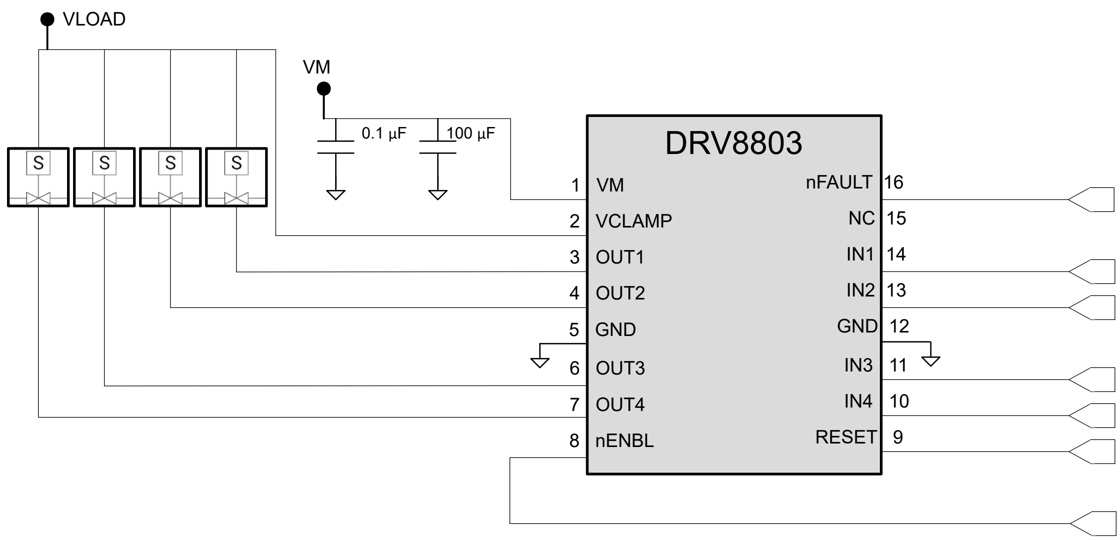


Figure 8-1. DRV8803 used to drive 4 Independent solenoid valves

8.1.1.1 Design Requirements

Table 8-1 lists the design parameters for this design example.

Table 8-1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply Voltage	V_M, V_{LOAD}	24V
Valve Peak current	I_{PEAK}	200mA
Valve Peak current time	t_{PEAK}	100ms
Valve Hold current	I_{HOLD}	100mA
PWM frequency	f_{PWM}	25kHz

8.1.1.2 Detailed Design Procedure

8.1.1.2.1 Supply Voltage

This is characteristic to the loads used. A higher voltage allows for fast opening/closing of the solenoid, enabling faster operation.

8.1.1.2.2 Load Current

The current path starts from the supply VLOAD, and moves through the inductive winding load, and low-side sinking NMOS power FET. Power dissipation losses in one sink NMOS power FET are shown in Equation 1.

$$P = I^2 \times R_{DS(on)} \tag{1}$$

The DRV8803 device has been measured to be capable of 1.5A Single Channel or 800-mA Four Channels with the DW package, 2A Single Channel or 1A Four Channels with the PWP, and 1.9A Single Channel or 0.9A Four Channels with the DYZ package at 25°C on standard FR-4 PCBs. The maximum RMS current varies based on PCB design and the ambient temperature.

With loads such as Relays and solenoid valves, the load tends to heat up and degrade if it is allowed to remain completely turned on. This can affect the long term reliability of the load and can even damage it in some cases. The DRV8803 offers an integrated Free wheeling diode and a simple-to-use parallel interface. Since such loads are inductive, the user can PWM the LSFET ON/OFF to regulate the current.

8.1.1.2.2.1 Peak Current

Load such as Solenoid/Relay needs to be energized at a temporary higher level of Load current and his higher level of current needs to be maintained for as long as Peak time (t_{PEAK}) in order for the load to reliably turn on. This Load current can be controlled by PWM control of the LSFET at required duty cycle.

8.1.1.2.2.2 Hold Current

Once the Peak time is elapsed, the Duty cycle and consequently Load current can be lowered to a Holding value of current. The Load can be kept on at this lower current for much longer durations

8.1.1.2.2.3 Frequency

The LSFET can be PWM controlled at a frequency which can be decided based on factors such as Load Inductance, Load resistance, desired/ tolerable ripply in Load current. PWM can be done outside audio band (>20kHz) for low audible noise operation

8.1.1.3 Application Curves

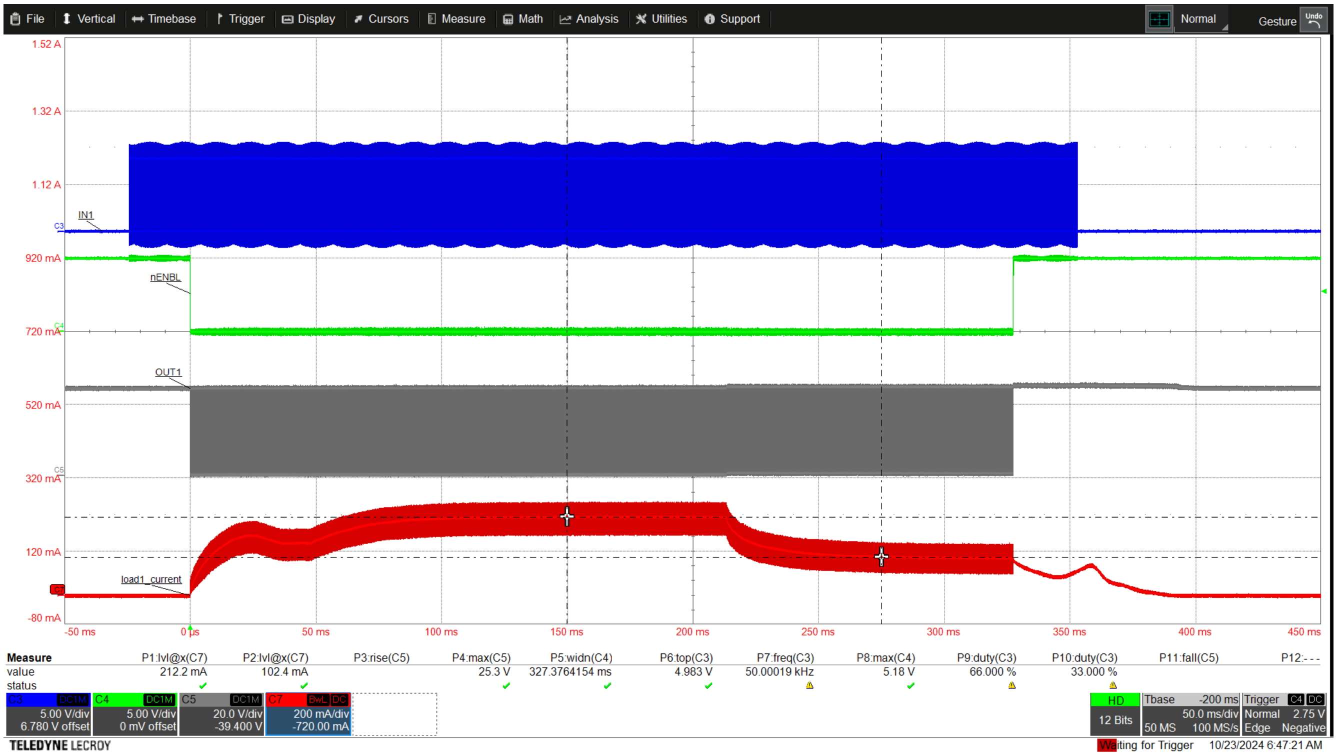


Figure 8-2. DRV8803 used to drive Solenoid Valves

8.1.2 Application as Unipolar Stepper Driver

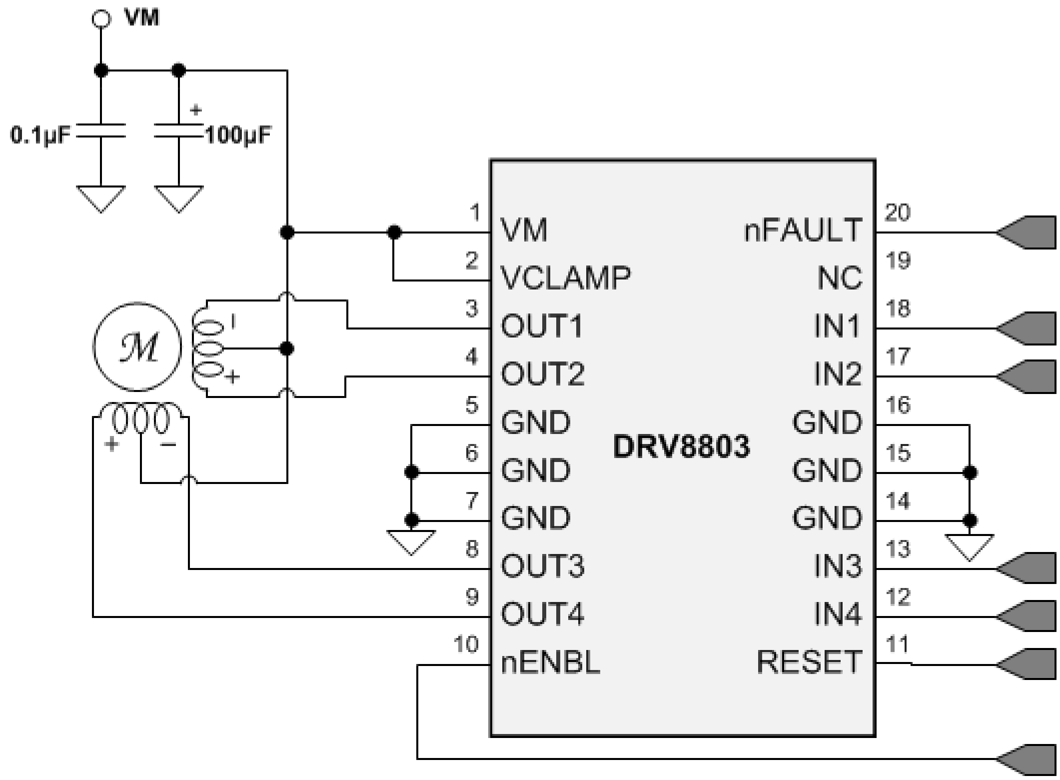


Figure 8-3. DRV8803 used to drive one 5-wire unipolar stepper

8.1.2.1 Design Requirements

Following Table lists the Design parameters for this design example

Table 8-2. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply Voltage	V_M	24V
Motor Winding Resistance	R_L	7.4Ω / phase
Motor Full step Angle	$θ_{STEP}$	1.8° /step
Motor Rated Current	I_{RATED}	0.75A
PWM frequency	f_{PWM}	31.25kHz

8.1.2.2 Detailed Design Procedure

8.1.2.2.1 Motor Voltage

The motor voltage to use will depend on the ratings of the motor selected and the desired torque. A higher voltage shortens the current rise time in the coils of the stepper motor allowing the motor to produce a greater average torque. Using a higher voltage also allows the motor to operate at a faster speed than a lower voltage.

8.1.2.2.2 Drive Current

The current path starts from the supply VM, and moves through the inductive winding load, and low-side sinking NMOS power FET. Power dissipation losses in one sink NMOS power FET are shown in Equation 1.

$$P = I^2 \times R_{DS(on)} \qquad (2)$$

The DRV8803 device has been measured to be capable of 1.5A Single Channel or 800-mA Four Channels with the DW package, 2A Single Channel or 1A Four Channels with the PWP, and 1.9A Single Channel or 0.9A Four Channels with the DYZ package at 25°C on standard FR-4 PCBs. The maximum RMS current varies based on PCB design and the ambient temperature.

8.1.2.3 Application Curves

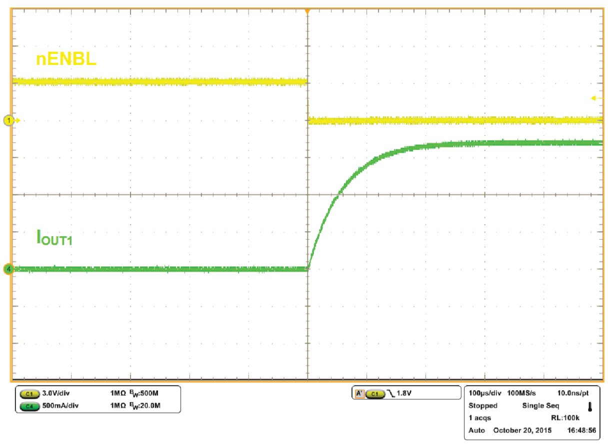


Figure 8-4. Current Ramp With a 16Ω, 1mH RL Load and V_M = 8.2V

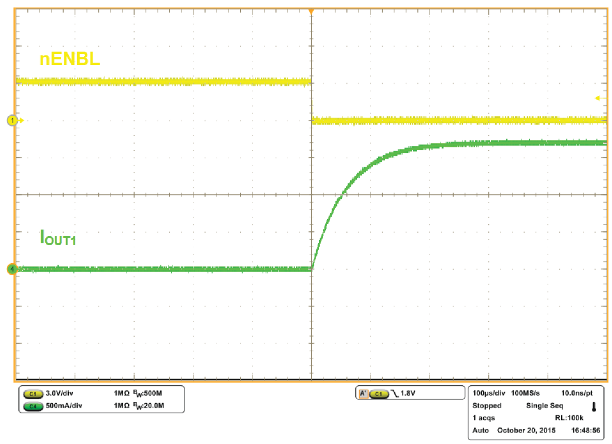


Figure 8-5. Current Ramp With a 16Ω, 1mH RL Load and V_M = 30V

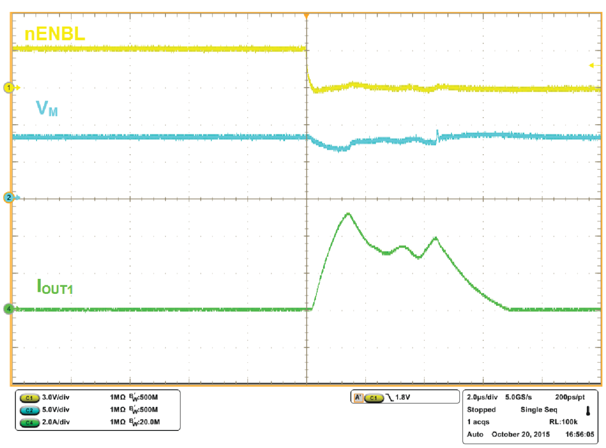


Figure 8-6. OCP With V_M = 8.2V and OUT1 Shorted to V_M

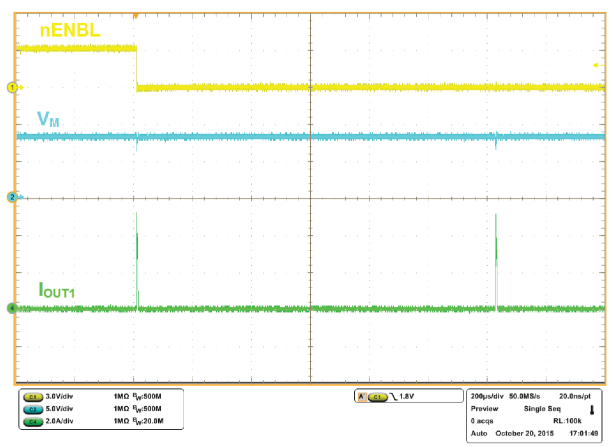


Figure 8-7. OCP Separated by t_{RETRY} With V_M = 8.2V and OUT1 Shorted to V_M

Power Supply Recommendations

8.1 Bulk Capacitance

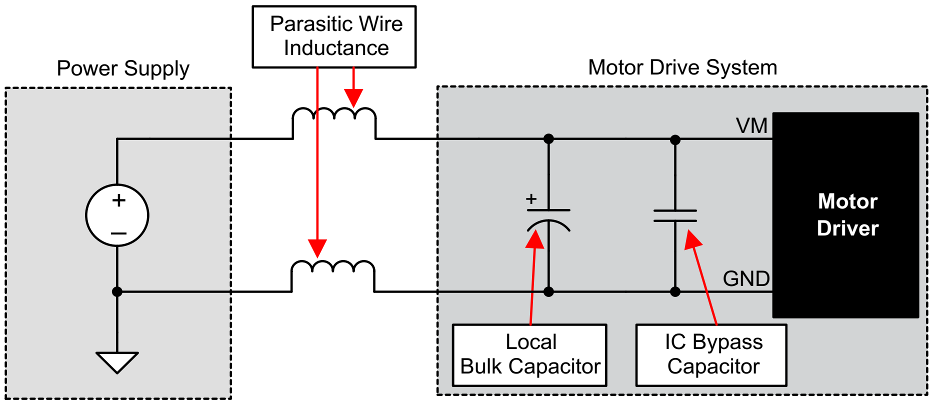
Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system.
- The power supply's capacitance and ability to source current.
- The amount of parasitic inductance between the power supply and motor system.
- The acceptable voltage ripple.
- The type of motor used (Brushed DC, Brushless DC, Stepper).

- The motor braking method.

The inductance between the power supply and the motor drive system will limit the rate of current that can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable, and a high current can be quickly supplied.



Example Setup of Motor Drive System with External Power Supply

Figure 8-8. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

8.2 Layout

8.2.1 Layout Guidelines

The bulk capacitor should be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Small-value capacitors should be ceramic, and placed closely to device pins.

The high-current device outputs should use wide metal traces.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias help dissipate the $I^2 \times R_{DS(on)}$ heat that is generated in the device.

8.2.2 Layout Example

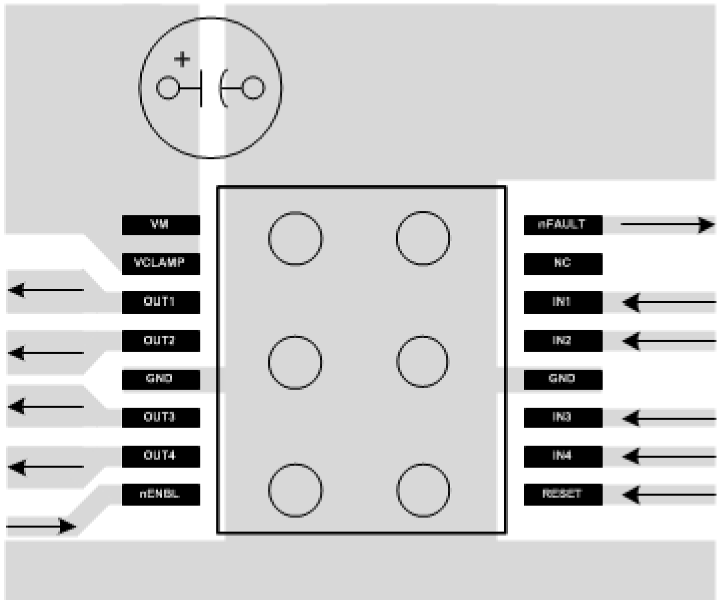


Figure 8-9. Recommended Layout

8.2.3 Thermal Consideration

8.2.3.1 Thermal Protection

The DRV8803 device has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

8.2.3.2 Power Dissipation

Power dissipation in the DRV8803 device is dominated by the power dissipated in the output FET resistance, or $R_{DS(on)}$. Average power dissipation of each FET when running a static load can be roughly estimated by Equation 3:

$$P = R_{DS(ON)} \bullet (I_{OUT})^2 \tag{3}$$

where

- P is the power dissipation of one FET
- $R_{DS(ON)}$ is the resistance of each FET
- I_{OUT} is equal to the average current drawn by the load.

At start-up and fault conditions, this current is much higher than normal running current; consider these peak currents and their duration. When driving more than one load simultaneously, the power in all active output stages must be summed.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(on)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

8.2.3.3 Heatsinking

The DRV8803DW package uses a standard SOIC outline, but has the center pins internally fused to the die pad to more efficiently remove heat from the device. The two center leads on each side of the package should be connected together to as large a copper area on the PCB as is possible to remove heat from the device. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

In general, the more copper area that can be provided, the more power can be dissipated.

The DRV8803PWP (HTSSOP package) and the DRV8803DYZ (SOT-23-THN package) uses an exposed thermal pad. The exposed pad removes heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, see the TI Application Report, *PowerPAD Thermally Enhanced Package* (SLMA002), and TI Application Brief, *PowerPAD Made Easy* (SLMA004), available at www.ti.com.

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- *PowerPAD Thermally Enhanced Package*, SLMA002.
- *PowerPAD Made Easy*, SLMA004.

9.2 Community Resources

9.3 Trademarks

All trademarks are the property of their respective owners.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (November 2015) to Revision D (July 2024) **Page**

- Added DYZ package drawing, thermal information, Updated Electrical characteristics to include DYZ Package Rdson.......... 1
- Added DYZ Package current capability.......... 6

Changes from Revision B (February 2012) to Revision C (November 2015) **Page**

- Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section.......... 1
- Changed Continuous output current, single channel on, T_A = 25°C, HTSSOP package MAX value from 1.5A to 2A.......... 7
- Changed Continuous output current, four channels on, T_A = 25°C, HTSSOP package MAX value from 0.8A to 1A.......... 7

11 Mechanical, Packaging, and Orderable Information

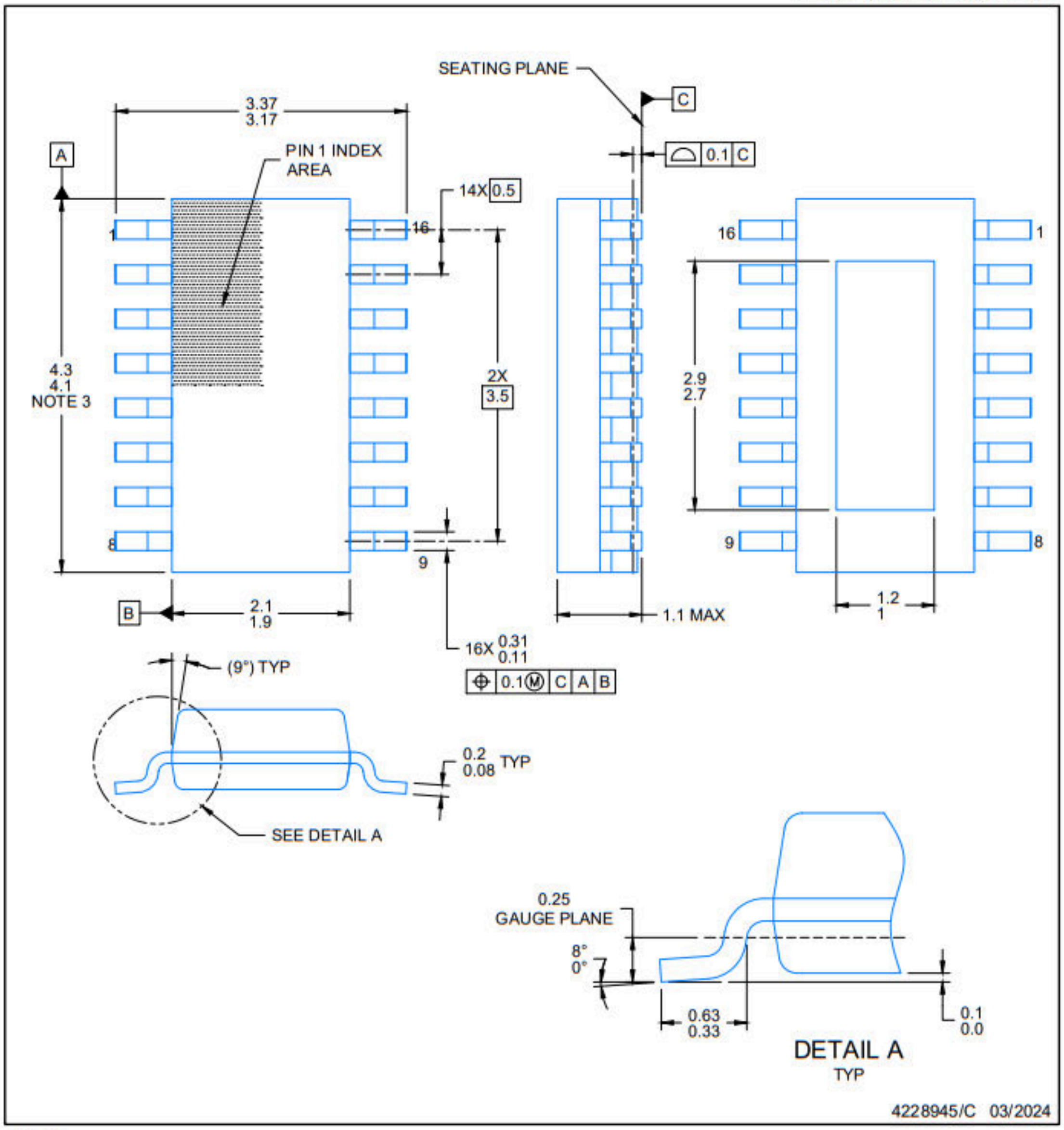
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DYZ0016A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



NOTES:

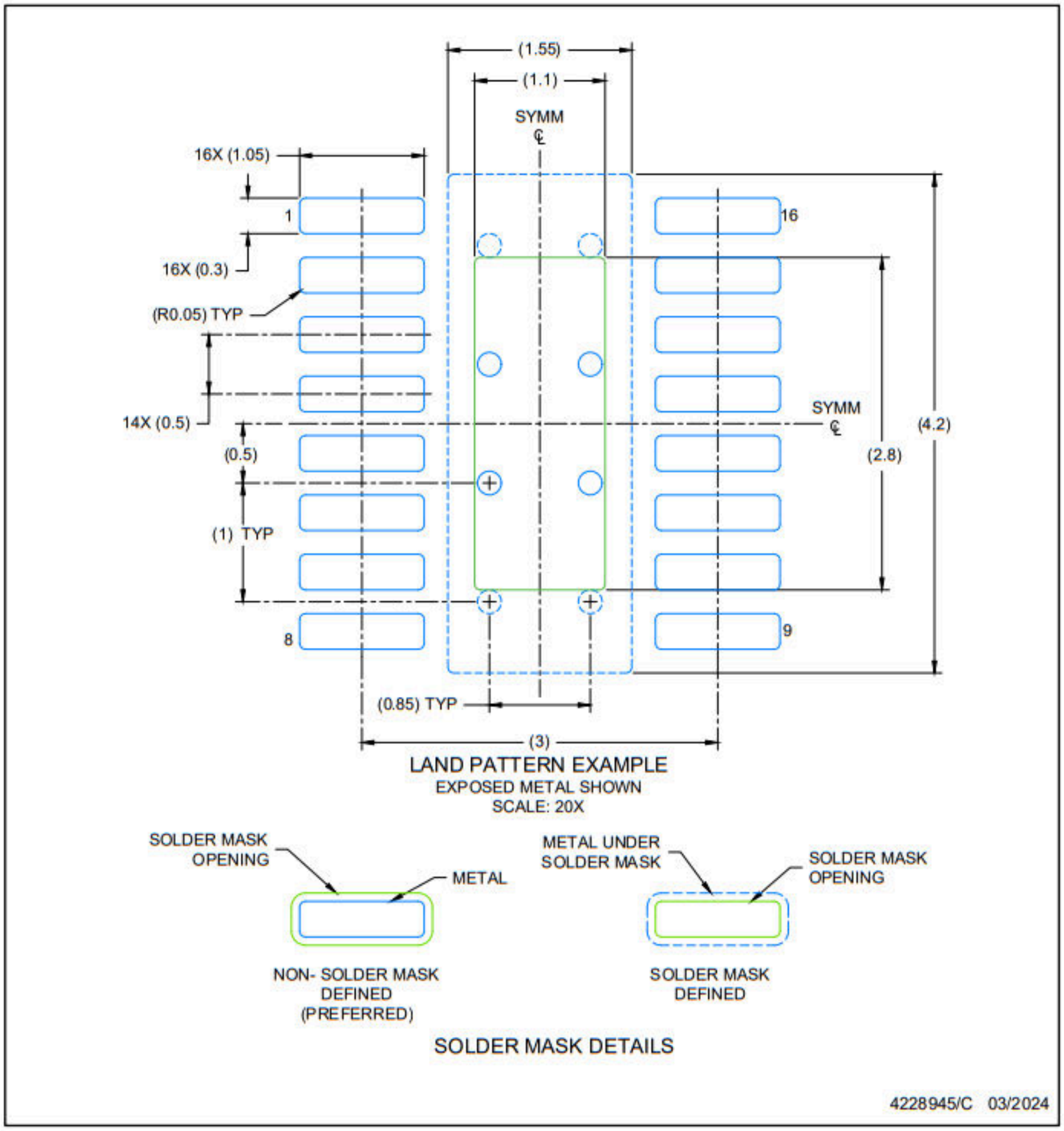
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA

www.ti.com

EXAMPLE BOARD LAYOUT

DYZ0016A **SOT-23-THIN - 1.1 mm max height**

PLASTIC SMALL OUTLINE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

TEXAS INSTRUMENTS
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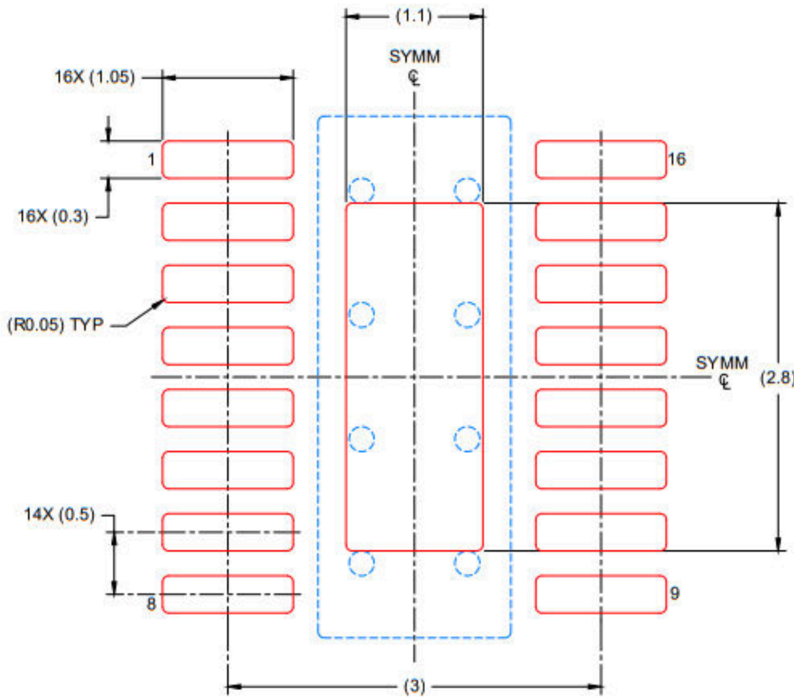
EXAMPLE STENCIL DESIGN

DYZ0016A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.23 X 3.13
0.125	1.10 X 2.80 (SHOWN)
0.15	1.00 X 2.56
0.175	0.93 X 2.37

4228945/C 03/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8803DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 125	DRV8803DW	
DRV8803DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8803DW	Samples
DRV8803DYZR	ACTIVE	SOT-23-THIN	DYZ	16	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	DRV8803	Samples
DRV8803PWP	OBSOLETE	HTSSOP	PWP	16		TBD	Call TI	Call TI	-40 to 125	DRV8803	
DRV8803PWPR	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8803	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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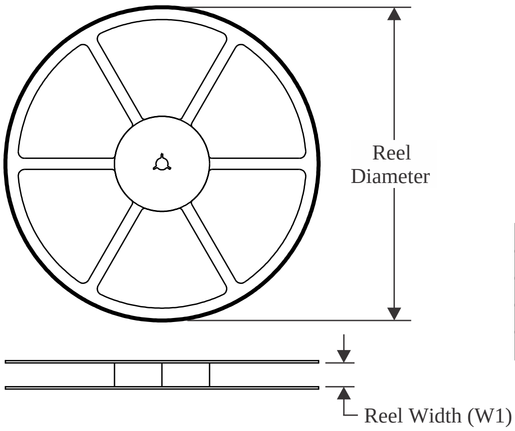
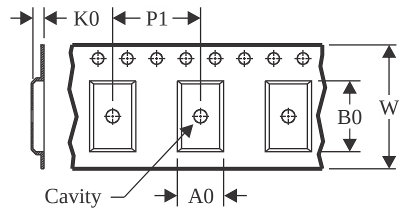
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

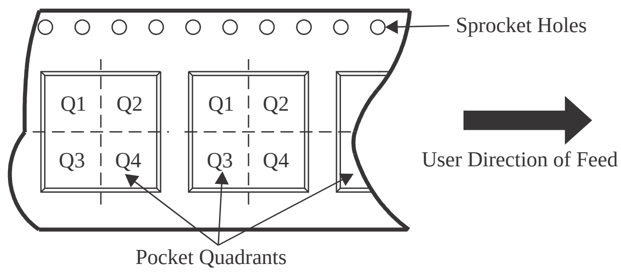
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

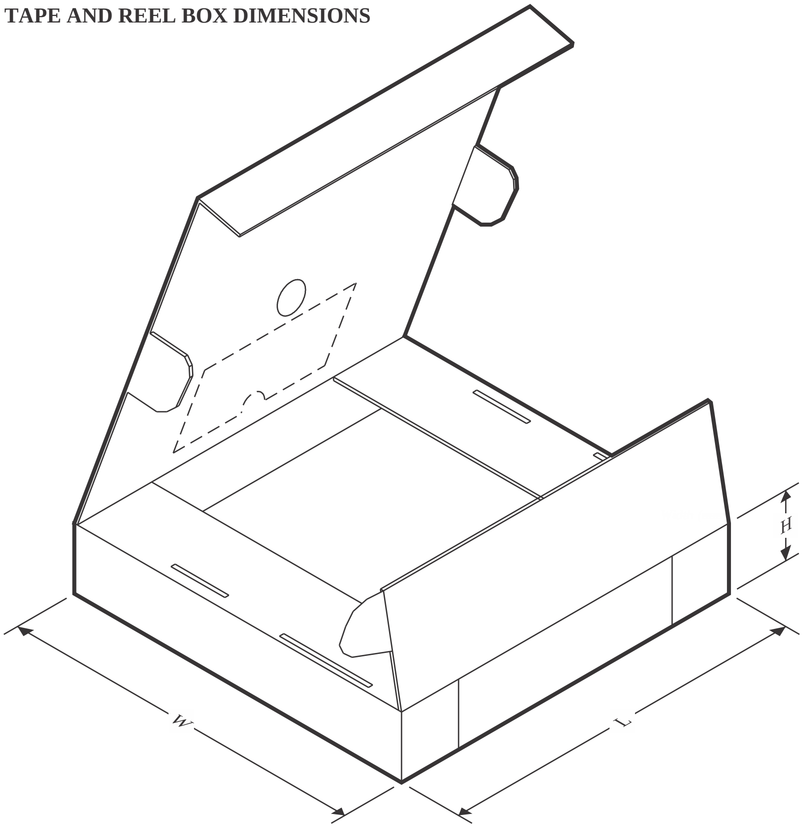
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

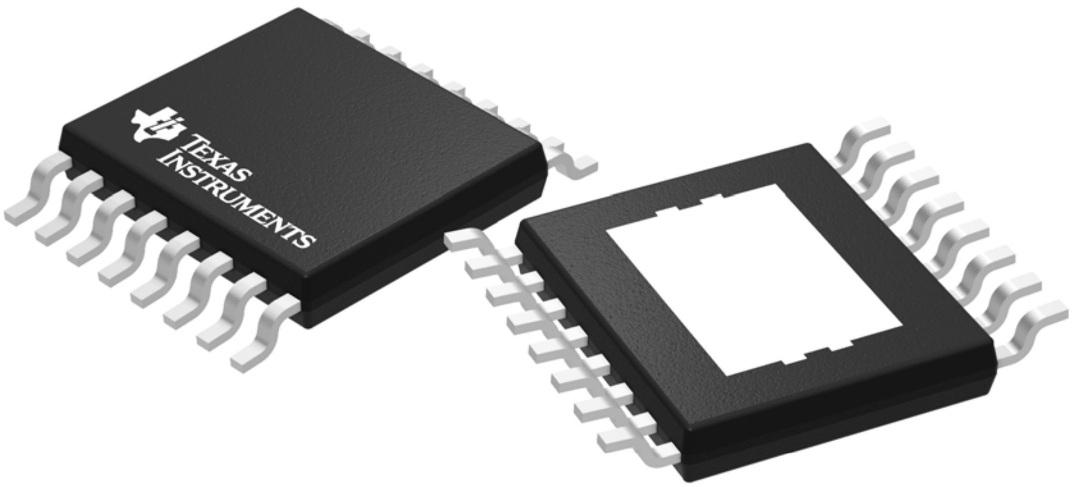
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8803DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
DRV8803PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

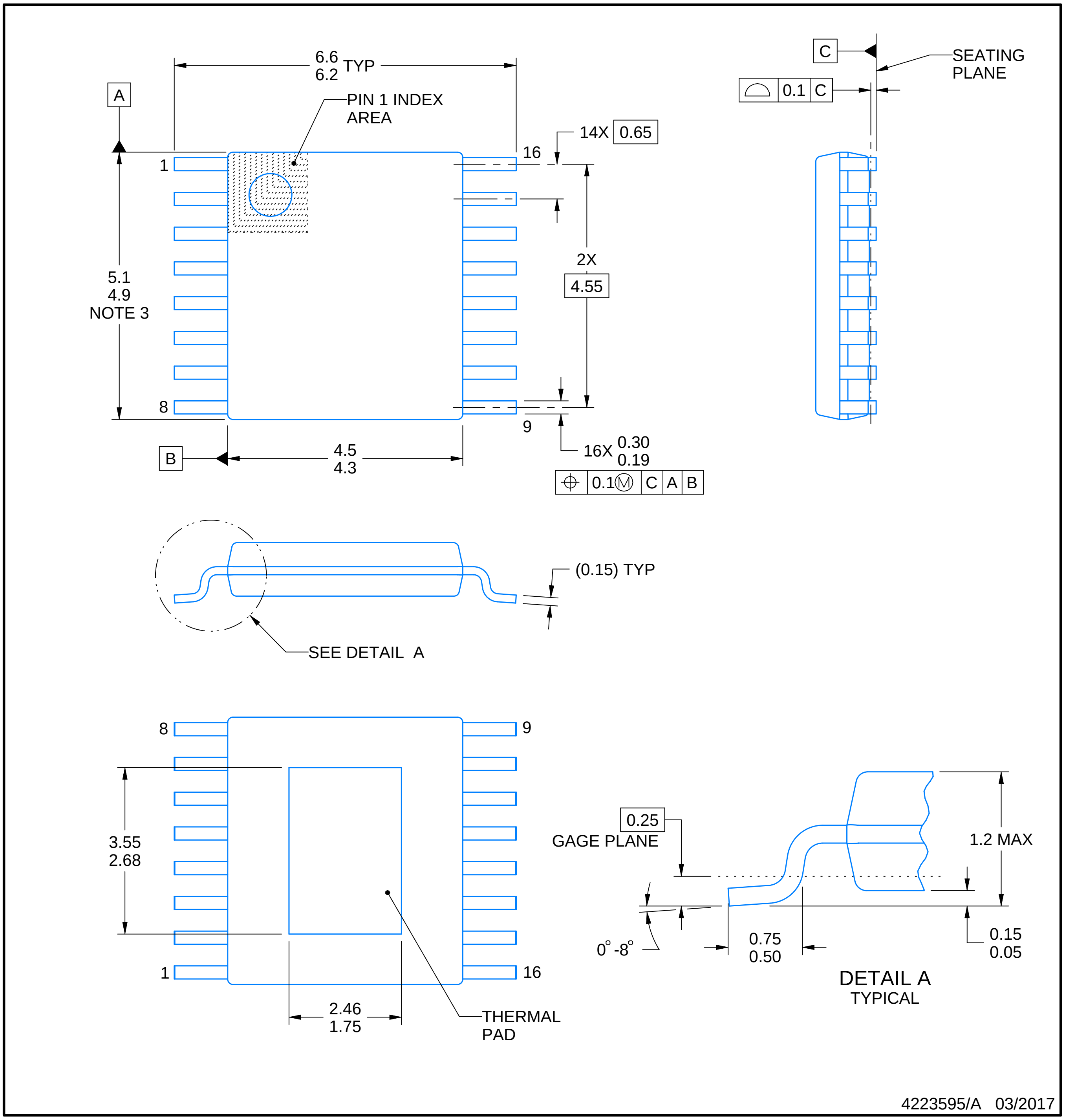


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8803DWR	SOIC	DW	20	2000	367.0	367.0	45.0
DRV8803PWPR	HTSSOP	PWP	16	2000	350.0	350.0	43.0



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



NOTES:

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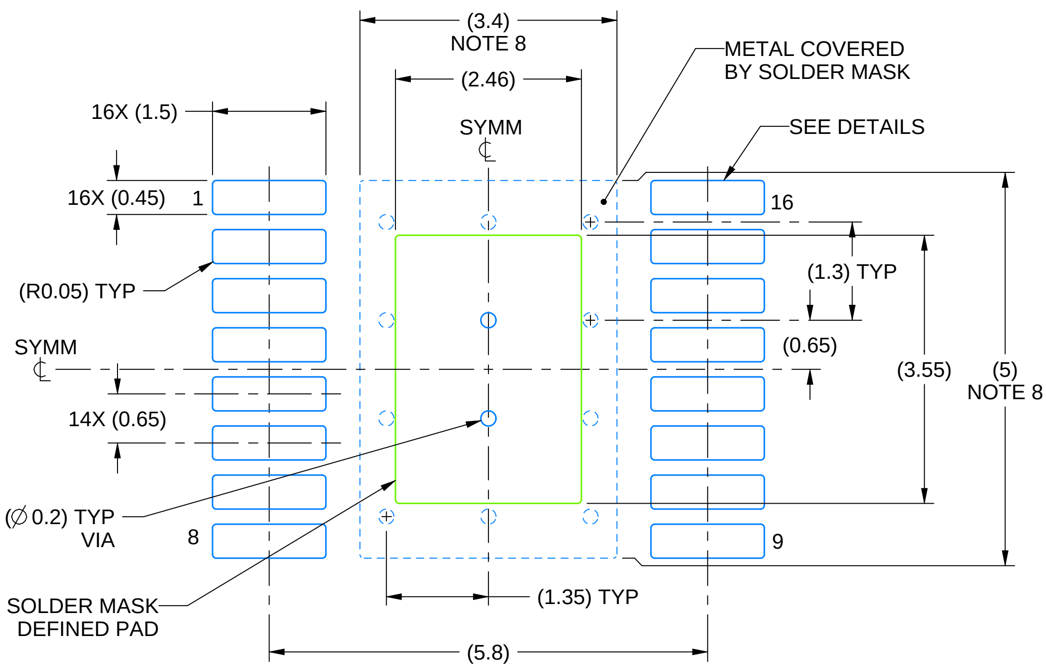
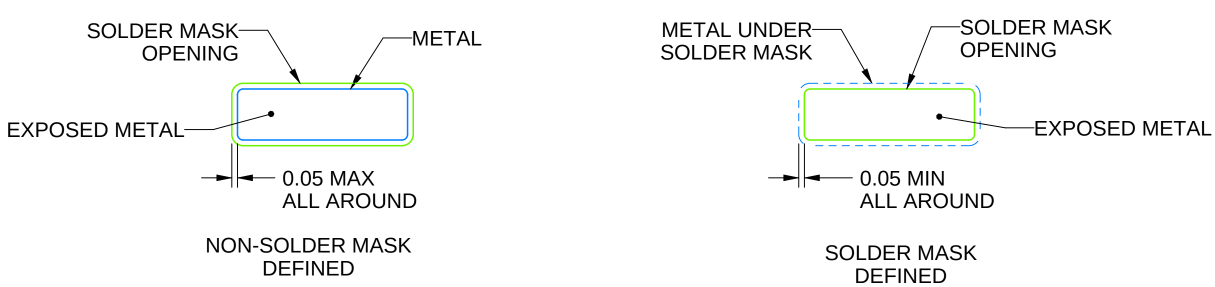
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

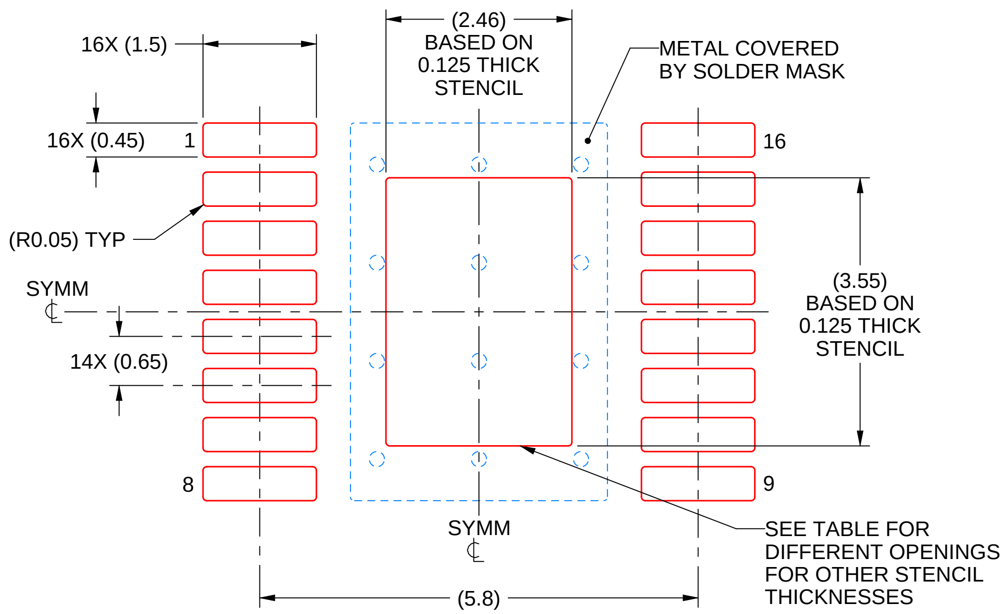


SOLDER MASK DETAILS

4223595/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
8. Size of metal pad may vary due to creepage requirement.
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



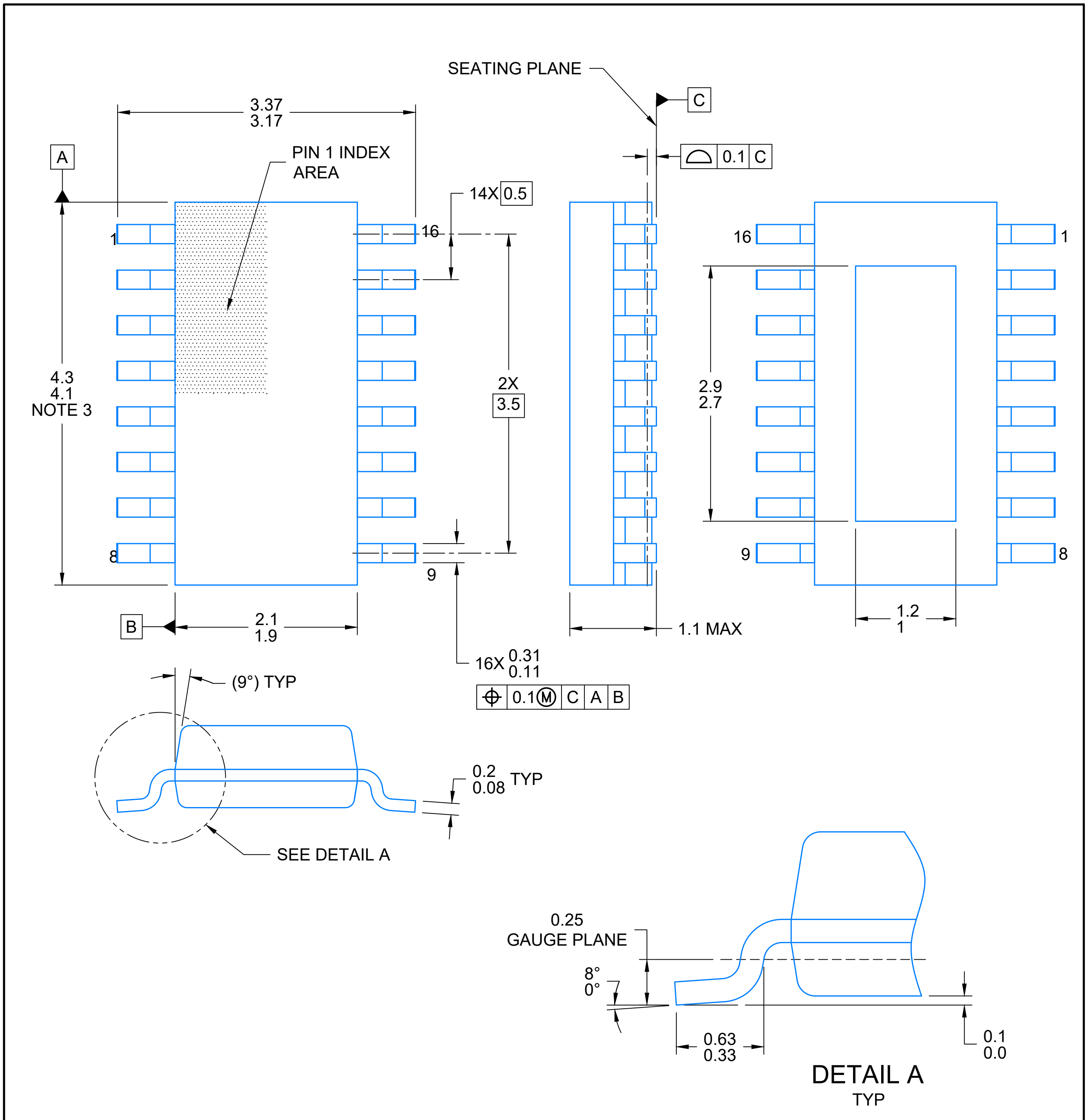
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.75 X 3.97
0.125	2.46 X 3.55 (SHOWN)
0.15	2.25 X 3.24
0.175	2.08 X 3.00

4223595/A 03/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.



4228945/C 03/2024

NOTES:

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2. This drawing is subject to change without notice.
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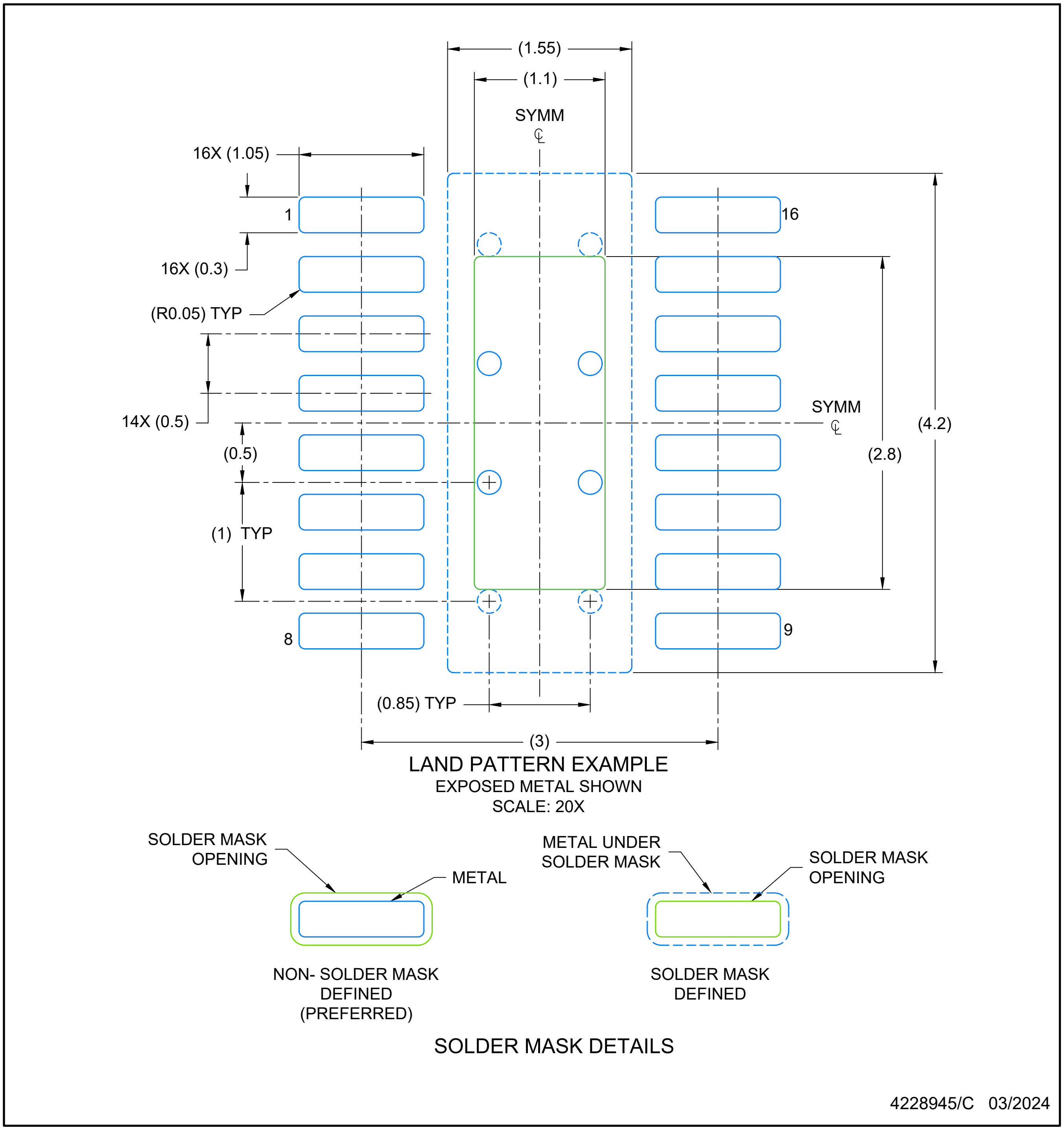
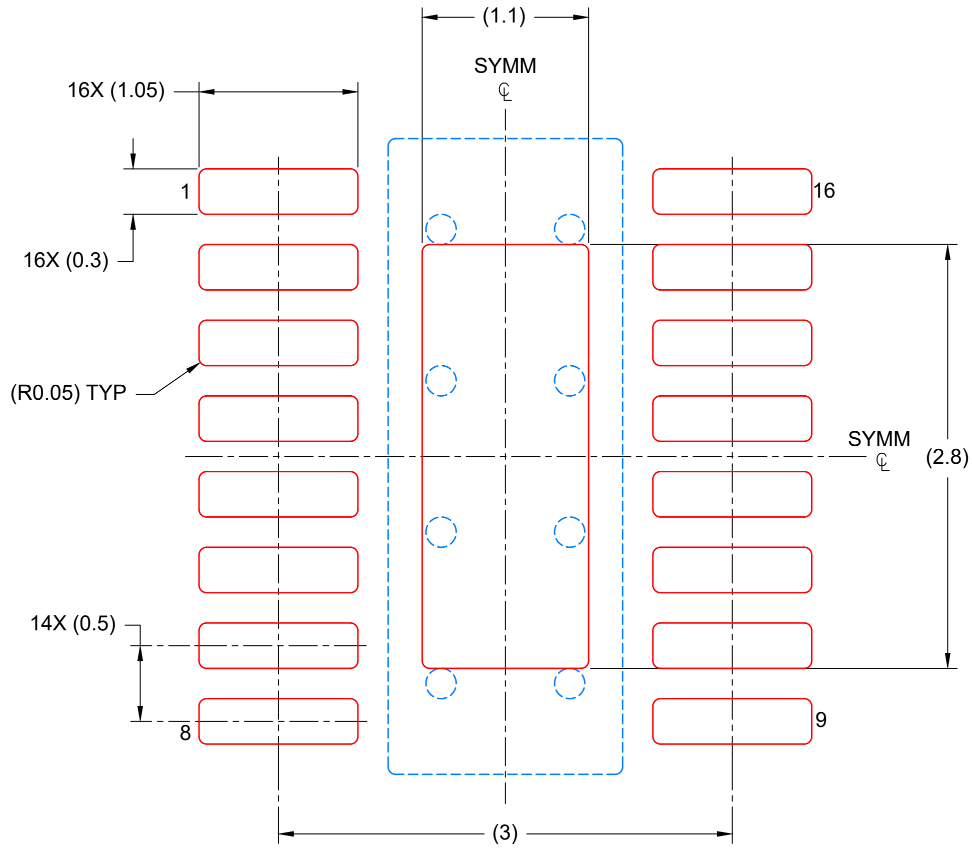
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



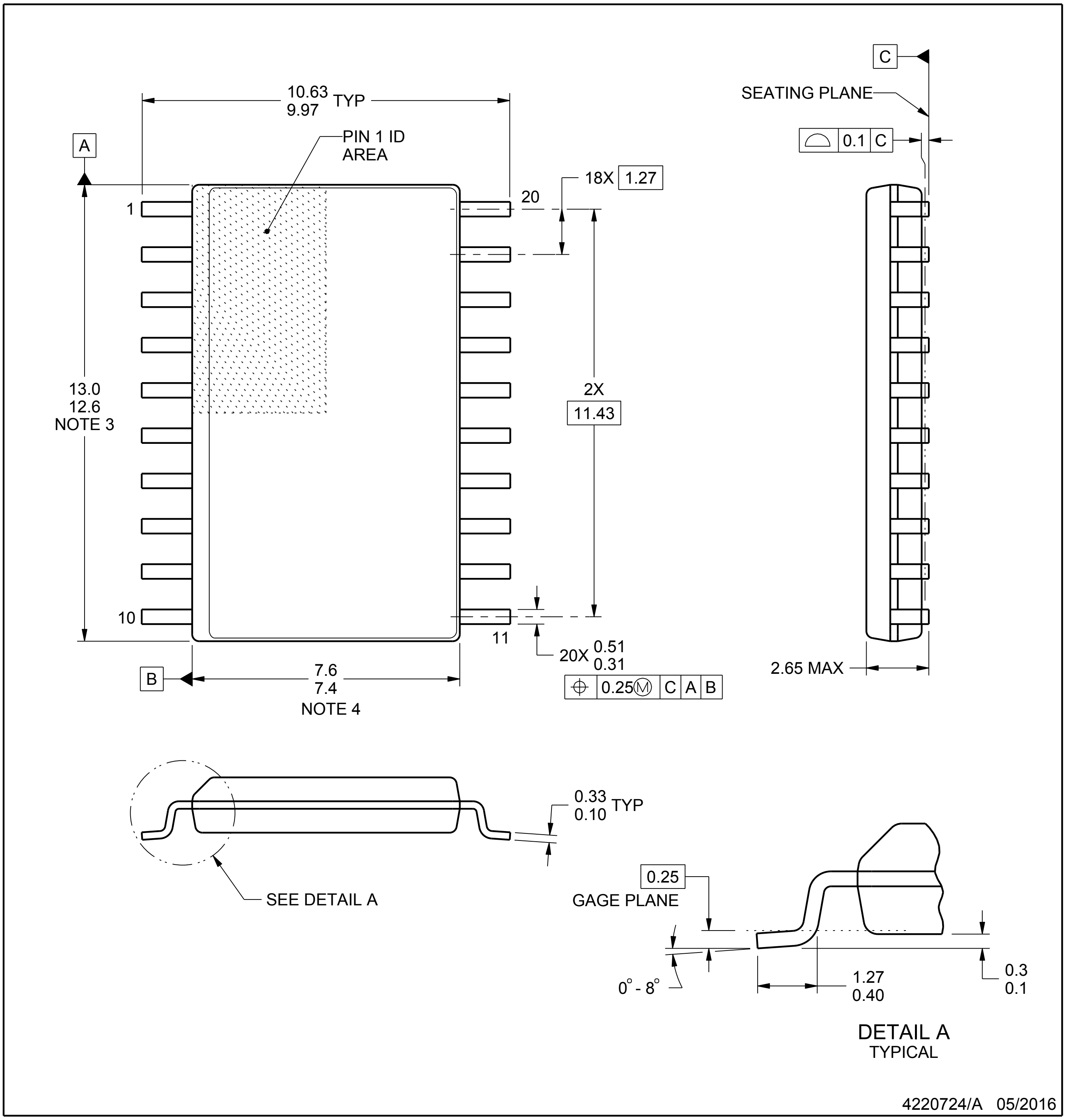
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.23 X 3.13
0.125	1.10 X 2.80 (SHOWN)
0.15	1.00 X 2.56
0.175	0.93 X 2.37

4228945/C 03/2024

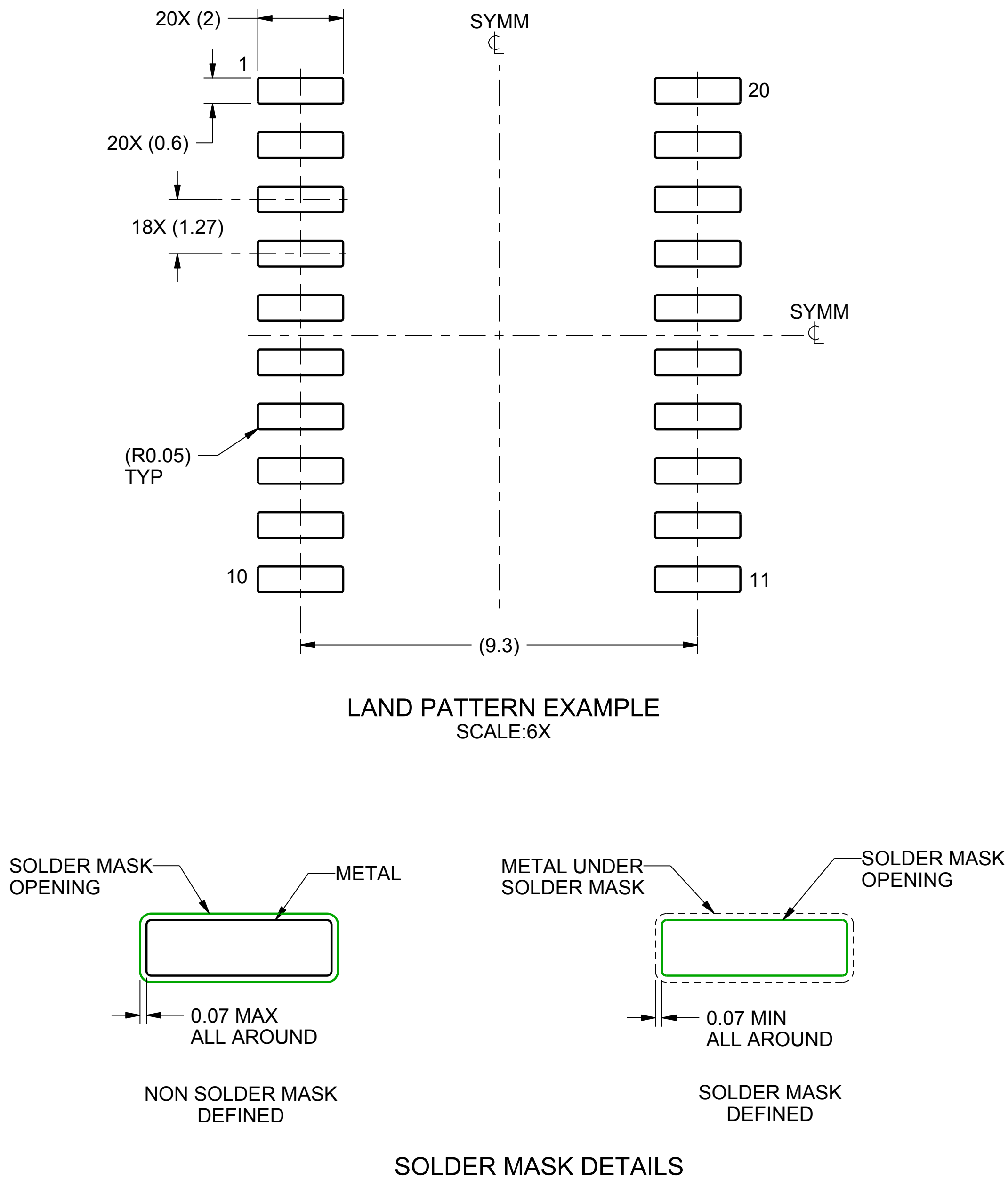
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



NOTES:

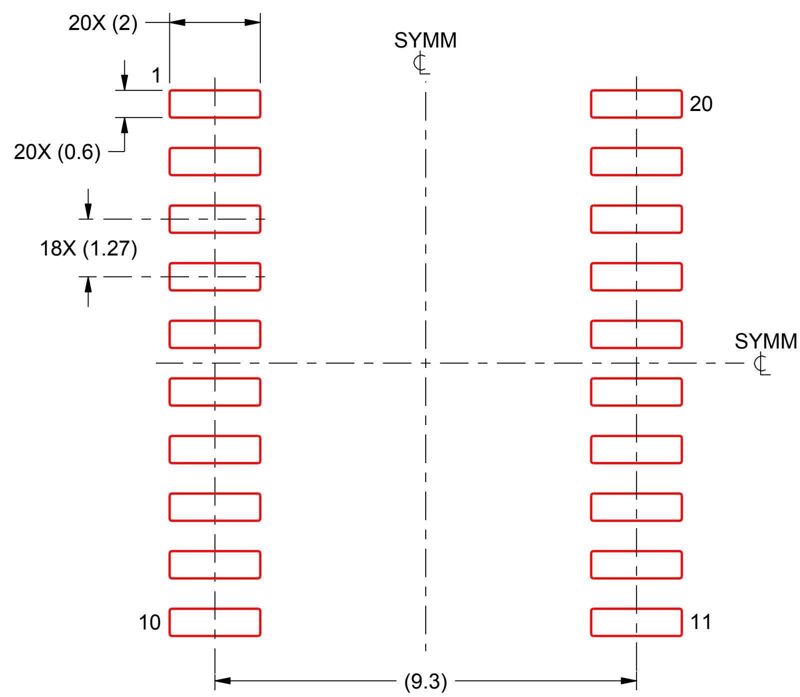
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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