dsPIC33CDV64MC106

16-Bit Digital Signal Controller with High-Speed PWM, Op Amps, Advanced Analog and MOSFET Driver

Operating Conditions

- Host dsPIC® DSC Core:
  - 3.0V to 3.6V, -40°C to +125°C, DC to 100 MIPS
- MOSFET Gate Driver module:
  - 6.25V to 29.0V, -40°C to +125°C
  - Fixed output linear regulator, 3.3V @ 70 mA

Core: 16-Bit dsPIC33C CPU

- 64 Kbytes of Program Flash with ECC and 8K RAM Memory with Built-In Self-Test (MBIST)
- Fast Six-Cycle Divide
- Code Efficient (C and Assembly) Architecture
- 40-Bit Wide Accumulators
- Single-Cycle (MAC/MPY) with Dual Data Fetch
- Single-Cycle, Mixed-Sign MUL Plus Hardware Divide
- 32-Bit Multiply Support
- Four Sets of Interrupt Context Saving Registers which Include Accumulator and STATUS for Fast Interrupt Handling
- Zero Overhead Looping

Clock Management

- 2% Internal Oscillator
- Programmable PLLs and Oscillator Clock Sources
- Reference Clock Output
- Fail-Safe Clock Monitor (FSCM)
- Fast Wake-up and Start-up
- Backup Internal Oscillator

Power Management

- Low-Power Management Modes (Sleep, Idle, Doze)
- Integrated Power-on Reset and Brown-out Reset

High-Speed PWM

- Four PWM Pairs
- Up to 2 ns PWM Resolution
- Dead Time for Rising and Falling Edges
- Dead-Time Compensation
- Clock Chopping for High-Frequency Operation
- PWM Support for:
  - BLDC, PMSM, IPM, ACIM, SRM and stepper motors
  - DC/DC, AC/DC, inverters, PFC, lighting
- Fault and Current Limit Inputs
- Flexible Trigger Configuration for ADC Triggering

Timers/Output Compare/Input Capture

- One General Purpose Timer:
  - Two 16-bit or one 32-bit timer/counter
- Peripheral Trigger Generator (PTG):
  - Up to 15 trigger sources to other peripheral modules
  - CPU independent state machine-based instruction sequencer
- Four SCCP modules which Include Timer, Capture/Compare and PWM:
  - 16 or 32-bit time base
  - 16 or 32-bit capture
  - Four-deep capture buffer
  - One PWM output
- Fully Asynchronous Operation, Available in Sleep Modes

Input/Output

- Sink/Source: 12 mA or 6 mA, Pin-Specific for Standard V_{OH}/V_{OL}, Up to 22 or 14 mA, respectively, for Non-Standard $V_{OH}1$
- 5V Tolerant Pins
- Peripheral Pin Select (PPS) to allow Digital Function Remapping
- Selectable Open-Drain Pull-ups and Pull-Downs
- Up to 5 mA Overvoltage Clamp Current
- Change Notification Interrupts on All I/O Pins
- Programmable Cyclic Redundancy Check (CRC)

Advanced Analog Features

- High-Speed ADC module:
  - 12-bit with dedicated SAR ADC core
  - Configurable resolution (up to 12-bit)
  - Up to 3.5 Msps conversion rate per channel at 12-bit resolution
  - Up to 15 input channels
  - Dedicated result buffer for each analog channel
  - Flexible and independent ADC trigger sources
  - Four digital comparators
  - Four oversampling filters for increased resolution
- One Analog Comparator with PDM DAC with Slope Compensation:
  - 15 ns analog comparator
- 12-Bit DAC:
  - Hardware slope compensation
  - Buffered DAC output
- Three Op Amps

Communication Interfaces

- Three Protocol UARTs with Automated Protocol Handling Support for:
  - LIN 2.2
  - DMX
- Two Four-Wire SPI/I^2S modules
- I^2C module with SMBus Support
- SENT module

Direct Memory Access (DMA)

- Four DMA Channels

Debugger Development Support

- In-Circuit and In-Application Programming and Debugging
- Three Complex, Five Simple Breakpoints
- IEEE 1149.2 Compatible (JTAG) Boundary Scan
- Trace Buffer and Run-Time Watch

Safety Features

- Clock Monitor System with Backup Oscillator
- DMT (Deadman Timer)
- ECC (Error Correcting Code)
- WDT (Watchdog Timer)
- CodeGuard™ Security
- CRC (Cyclic Redundancy Check)
- ICSP™ Write Inhibit
- RAM Memory Built-In Self-Test (MBIST)
- Two-Speed Start-up
- Fail-Safe Clock Monitoring (FSCM)
- Backup FRC (BFRC)
- Capless Internal Voltage Regulator
- Virtual Pins for Redundancy and Monitoring

MOSFET Gate Driver Module (Based on MCP8021 Device)

- Three Half-Bridge Drivers Configured to Drive External High-Side NMOS and Low-Side NMOS MOSFETs:
  - Peak output current: 0.5A @ 12V
  - Shoot-through protection
  - Overcurrent and short-circuit protection

Fixed Output Linear Regulator

- 3.3V @ 70 mA
- True Current Foldback

Protection Features

- Gate Drive Undervoltage Lockout: 4.5V
- Supply Voltage Undervoltage Shutdown: 4.5V
- Supply Voltage Undervoltage Lockout (UVLO): 6.25V
- Overvoltage Lockout (OVLO): 32V
- Transient (100 ms) Voltage Tolerance: 40V
- Power Module Thermal Shutdown

Functional Safety

- Class B Safety Library – IEC 60730
- For ASIL B and Beyond Applications – ISO 26262
- FMEDA Computation Spreadsheet (Evaluation of Random Hardware Failures Metric)
- Functional Safety Manual
- Functional Safety Diagnostics Suite

Qualification Support

- AEC-Q100 REV-H (Grade 1: -40°C to +125°C) Compliant

dsPIC33CDV64MC106

The dsPIC33CDV64MC106 device features are listed in Table 1.

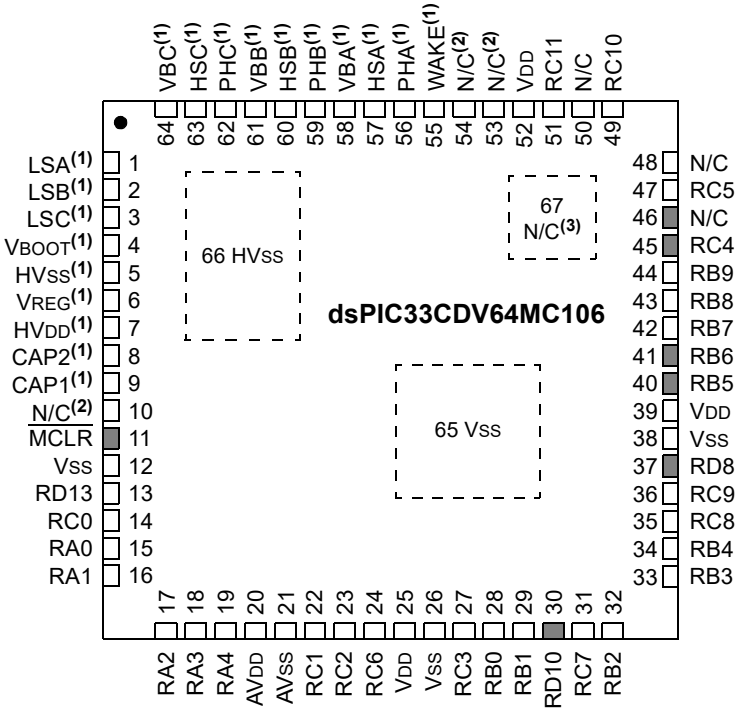
TABLE 1: dsPIC33CDV64MC106 DEVICE FEATURES

Device	Pins	Flash (Kbytes)	SRAM (Kbytes)	DMA # of Ch	GPIO/PPS	16-Bit Timer	SCCP	UART	SPI	I^2C	SENT	MC PWM	PWM Res (nS)	QEI	12-Bit ADC Module	ADC Channels	Op Amp	Analog Comp w/12-Bit DAC	PTG	CLC	REFO	CRC	WDT/DMT	Package
dsPIC33CDV64MC106	64	64	8	4	30/25	1	4	3	2	1	1	4x2	2	1	1	15	3	1	1	4	1	1	1/1	QFN

Pin Diagram

64-Pin QFN

= 5.5 VDC Tolerant



Note 1: These pins are specific to the MOSFET gate driver module.

2: Pin is connected to a device interconnect; see Table 3 for more information.

3: Pin has no electrical connection to the device, but is recommended to be connected to VSS in the PCB design to improve thermal dissipation.

TABLE 2: dsPIC33CDV64MC106 COMPLETE PIN FUNCTIONS

Pin	Function	Pin	Function
1	LSA	35	**RP56**/ASDA1/SCK2/RC8
2	LSB	36	**RP57**/ASCL1/SDI2/RC9
3	LSC	37	**RP72**/PCI19/SDO2/RD8
4	VBOOT	38	VSS
5	HVSS	49	VDD
6	VREG	40	PGD3/**RP37**/RB5
7	HVDD	41	PGC3/**RP38**/RB6
8	CAP2	42	TDO/AN2/**RP39**/RB7
9	CAP1	43	PGD1/AN10/**RP40**/SCL1/RB8
10	N/C(1)	44	PGC1/AN11/**RP41**/SDA1/RB9
11	$\overline{\text{MCLR}}$	45	**RP52**/RC4
12	VSS	46	N/C
13	ANN0/**RP77**/RD13	47	**RP53**/RC5
14	AN12/**RP48**/RC0	48	N/C
15	OA1OUT/AN0/CMP1A/IBIAS0/RA0	49	**RP58**/RC10
16	OA1IN-/RA1	50	N/C
17	OA1IN+/AN9/RA2	51	**RP59**/RC11
18	DACOUT/AN3/CMP1C/RA3	52	VDD
19	OA3OUT/AN4/IBIAS3/RA4	53	N/C(1)
20	AVDD	54	N/C(1)
21	AVSS	55	WAKE
22	OA3IN-/AN13/CMP1B/ISRC0/**RP49**/RC1	56	PHA
23	OA3IN+/AN14/ISRC1/**RP50**/RC2	57	HSA
24	IBIAS1/**RP54**/RC6	58	VBA
25	VDD	59	PHB
26	VSS	60	HSB
27	AN15/IBIAS2/**RP51**/RC3	61	VBB
28	OSCI/CLKI/AN5/**RP32**/RB0	62	PHC
29	OSCO/CLKO/AN6/**RP33**/RB1	63	HSC
30	ISRC3/**RP74**/RD10	64	VBC
31	ISRC2/**RP55**/RC7	65	VSS(2)
32	OA2OUT/AN1/AN7/CMP1D/**RP34**/INT0/RB2	66	HVSS(2)
33	PGD2/OA2IN-/AN8/**RP35**/RB3	67	N/C(3)
34	PGC2/OA2IN+/**RP36**/RB4		

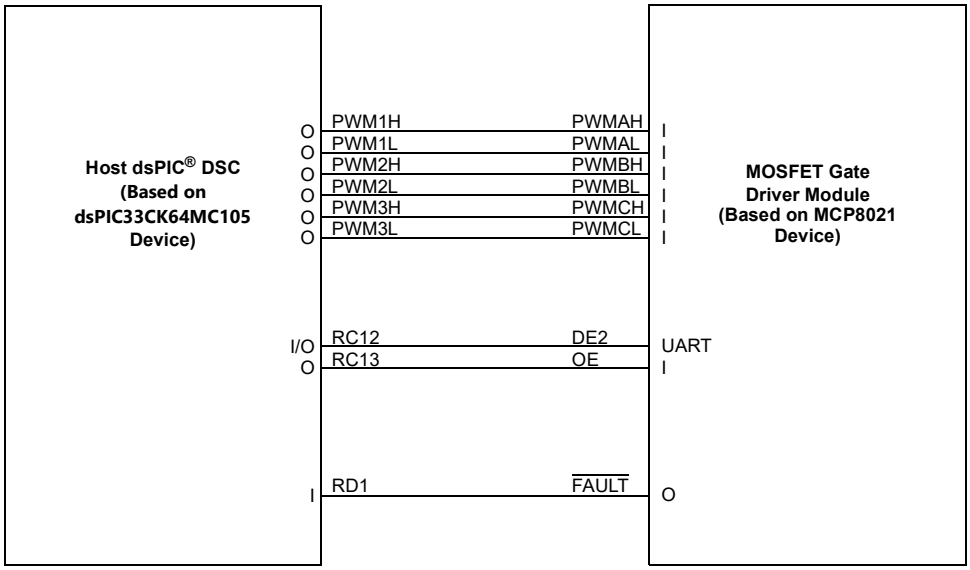
Legend: **RPn** represents remappable pins for the Peripheral Pin Select (PPS) function.

Note 1: Pin is connected to a device interconnect; see Table 3 for more information.

2: Pin is connected to a device exposed pad.

3: Pin has no electrical connection to the device, but is recommended to be connected to VSS in the PCB design to improve thermal dissipation.

FIGURE 1: dsPIC33CDV64MC106 DEVICE INTERNAL CONNECTIONS BLOCK DIAGRAM(1)



Note 1: Device Interconnections are shown in Table 3.

TABLE 3: dsPIC33CDVL64MC106 DEVICE INTERCONNECTIONS

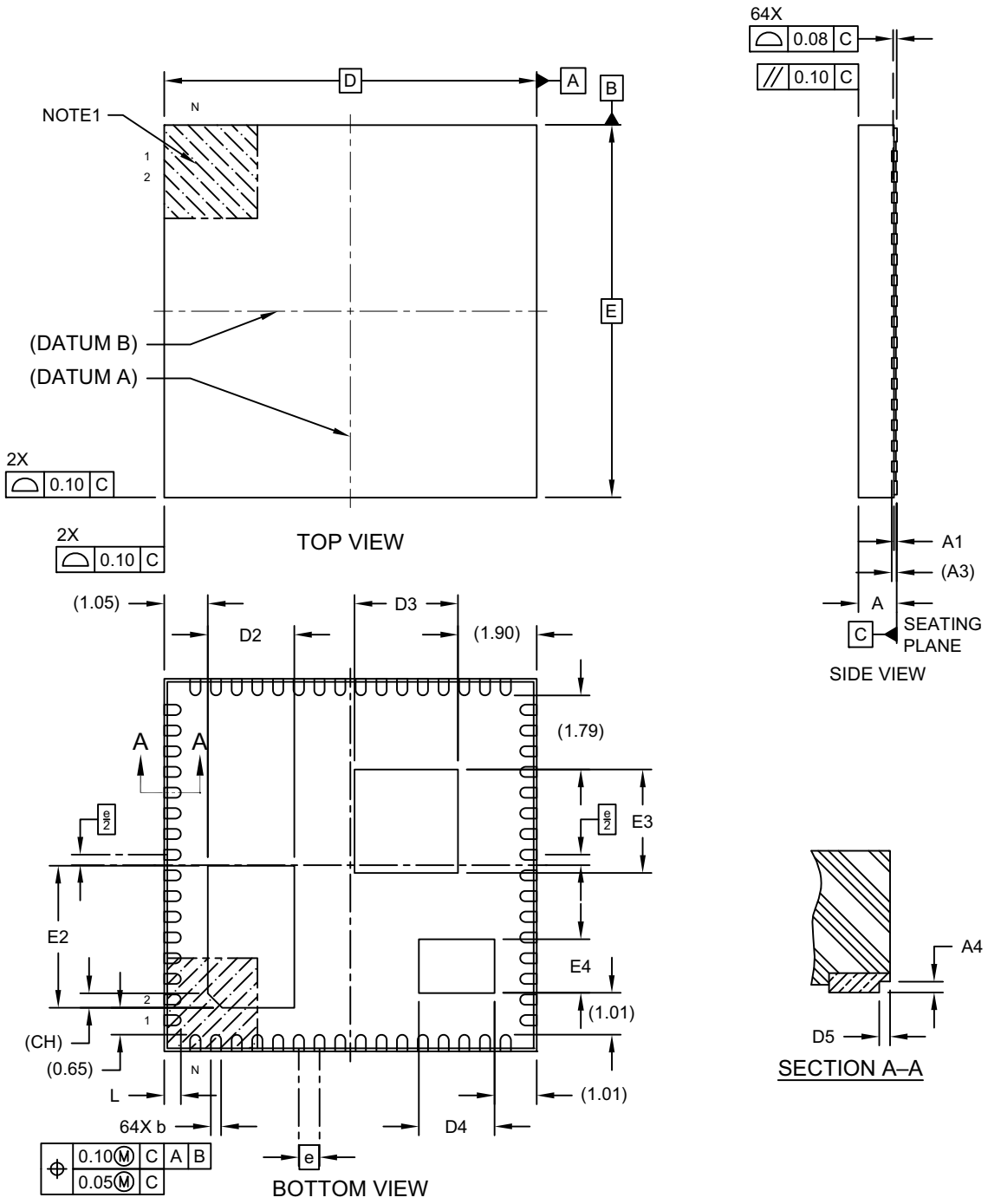
Host dsPIC® DSC to MOSFET Gate Driver	I/O	Interconnect Description
RB10/PWM3H to PWMCH(1)	O I	Digital output, configured when PWM output is enabled; Digital input, Phase C high-side control, internal 47 kΩ pull-down
RB11/PWM3L to PWMCL	O I	Digital output, configured when PWM output is enabled; Digital input, Phase C low-side control, internal 47 kΩ pull-down
RB12/PWM2H to PWMBH(1)	O I	Digital output, configured when PWM output is enabled; Digital input, Phase B high-side control, internal 47 kΩ pull-down
RB13/PWM2L to PWMBL	O I	Digital output, configured when PWM output is enabled; Digital input, Phase B low-side control, internal 47 kΩ pull-down
RD1 to FAULT	I O	Configure as digital input, use internal pull-up; Digital output, active-low Fault, open-drain
RC12/RP60 to DE2	I/O I/O	Configure as half-duplex UART, use PPS and internal pull-up; Digital communications port, open-drain
RB14/PWM1H to PWMAH(1)	O I	Digital output, configured when PWM output is enabled; Digital input, Phase A high-side control, internal 47 kΩ pull-down
RB15/PWM1L to PWMAL	O I	Digital output, configured when PWM output is enabled; Digital input, Phase A low-side control, internal 47 kΩ pull-down
RC13 to OE	O I	Configure as digital output; Digital input, output enable, Fault clearing, internal 47 kΩ pull-down

Note 1: Interconnect is also bonded to an external device pin.

Package Details

64-Lead Very Thin Grid Array Quad Flat Pack No-Lead (M8) - 9x9x0.927 mm Body [VGQFN] With Multiple Exposed Pads and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-530-M8 Rev B Sheet 1 of 2

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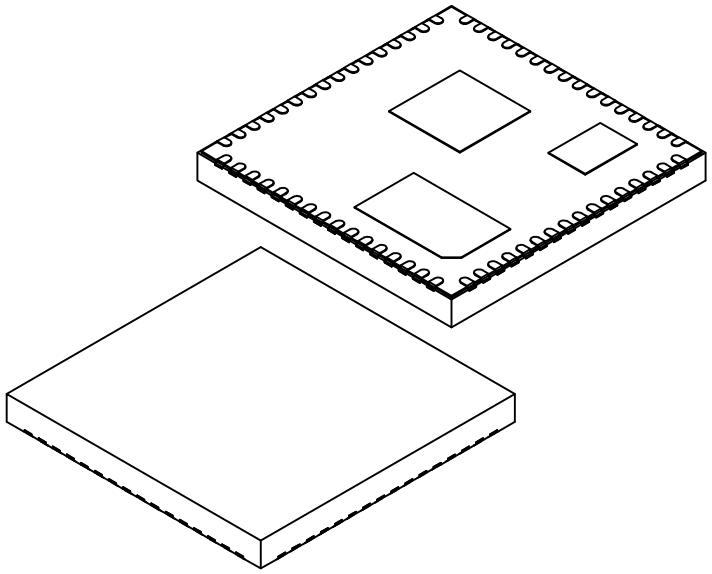

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		64	
Pitch	e		0.50 BSC	
Overall Height	A	0.827	0.877	0.927
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.127 REF	
Overall Length	D		9.00 BSC	
Exposed Pad Length	D2	1.99	2.09	2.19
Exposed Pad Length	D3	2.40	2.50	2.60
Exposed Pad Length	D4	1.73	1.83	1.93
Overall Width	E		9.00 BSC	
Exposed Pad Width	E2	3.33	3.43	3.53
Exposed Pad Width	E3	2.40	2.50	2.60
Exposed Pad Width	E4	1.20	1.30	1.40
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Exposed Pad Corner Chamfer	CH		0.35 REF	
Wettable Flank Step Cut Length	D5	0.03	0.07	0.11
Wettable Flank Step Cut Height	A4	0.05	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-530-M8 Rev B Sheet 2 of 2

64-Lead Very Thin Grid Array Quad Flat Pack No-Lead (M8) - 9x9x0.927 mm Body [VGQFN] With Multiple Exposed Pads and Stepped Wettable Flanks

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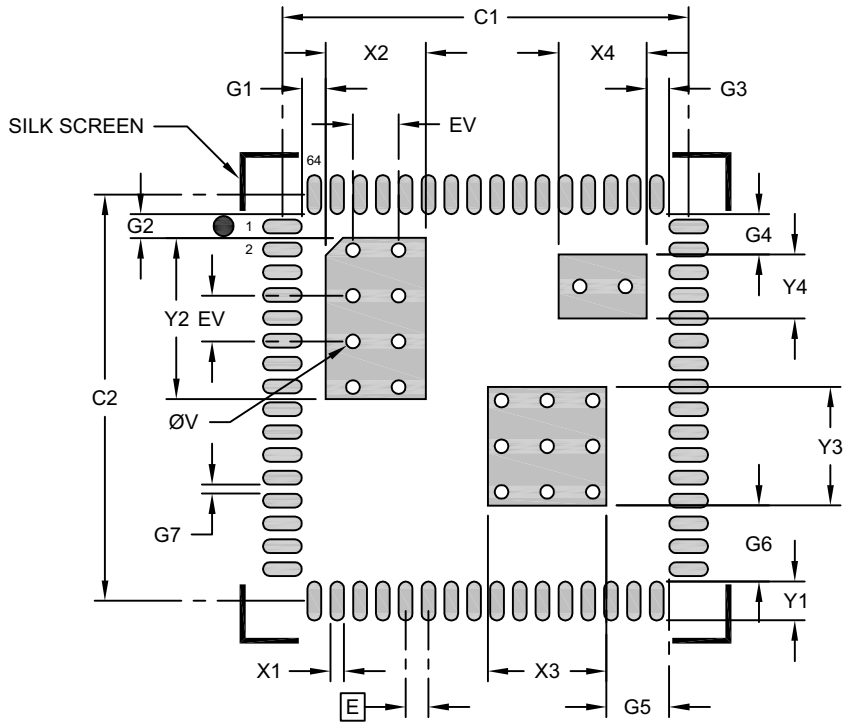

RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X2			2.19
Center Pad Length	Y2			3.53
Center Pad Width	X3			2.60
Center Pad Length	Y3			2.60
Center Pad Width	X4			1.93
Center Pad Length	Y4			1.40
Contact Pad Spacing	C1		8.90	
Contact Pad Spacing	C2		8.90	
Contact Pad Width (Xnn)	X1			0.30
Contact Pad Length (Xnn)	Y1			0.85
Contact Pad to Center Pad	G1	0.53		
Contact Pad to Center Pad	G2	0.53		
Contact Pad to Center Pad	G3	0.50		
Contact Pad to Center Pad	G4	0.86		
Contact Pad to Center Pad	G5	1.38		
Contact Pad to Center Pad	G6	1.67		
Contact Pad to Contact Pad	G7	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

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