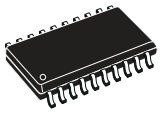
L4973

3.5 A step down switching regulator

Datasheet - production data



SO-20 (12+4+4)

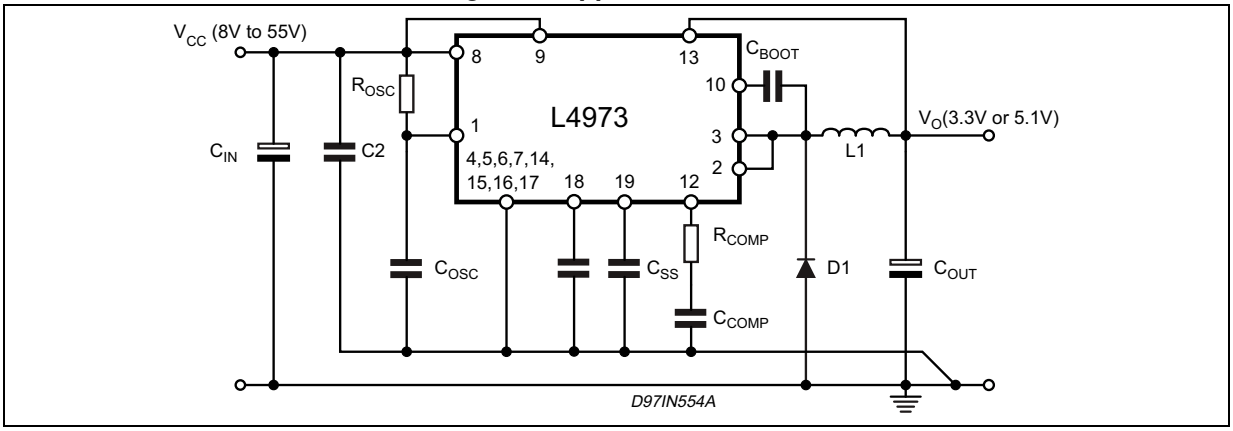
Features

- Up to 3.5 A step down converter
- Operating input voltage from 8 V to 55 V
- 3.3 V and 5.1 V (±1 %) fixed output, and adjustable outputs from:
  - 0.5 V to 50 V (3.3 type)
  - 5.1 V to 50 V (5.1 type)
- Frequency adjustable up to 300 kHz
- Voltage feed forward
- Zero load current operation (min. 1 mA)
- Internal current limiting (pulse by pulse and HICCUP mode)
- Precise 5.1 V (1.5%) reference voltage externally available
- Input/output synchronization function
- Inhibit for zero current consumption (100 mA typ. at V_{CC} = 24 V)
- Protection against feedback disconnection
- Thermal shutdown
- Output over voltage protection
- Soft-start function

Description

The L4973 is a step down monolithic power switching regulator delivering 3.5 A at fixed voltages of 3.3 V or 5.1 V and using a simple external divider output adjustable voltage up to 50 V. Realized in BCD mixed technology, the device uses an internal power D-MOS transistor (with a typical $R_{DS(on)}$ of 0.15 Ω) to obtain very high efficiency and very fast switching times. Switching frequency up to 300 kHz are achievable (the maximum power dissipation of the packages must be observed).
A wide input voltage range between 8 V to 55 V and output voltages regulated from 3.3 V to 40 V cover the majority of the today applications. Features of this new generation of DC-DC converter includes pulse by pulse current limit, hiccup mode for output short circuit protection, voltage feed forward regulation, soft-start, input/output synchronization, protection against feedback loop disconnection, inhibit for zero current consumption and thermal shutdown. Package available is SO-20 (12+4+4) for SMD assembly.

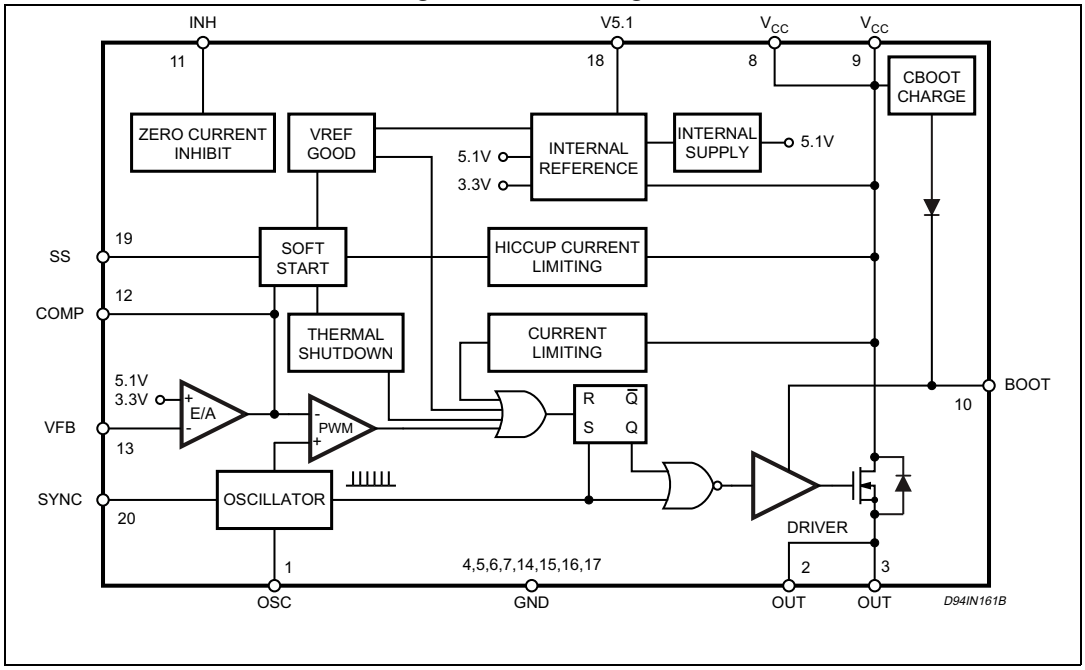
Figure 1. Application circuit



Contents

1 Block diagram

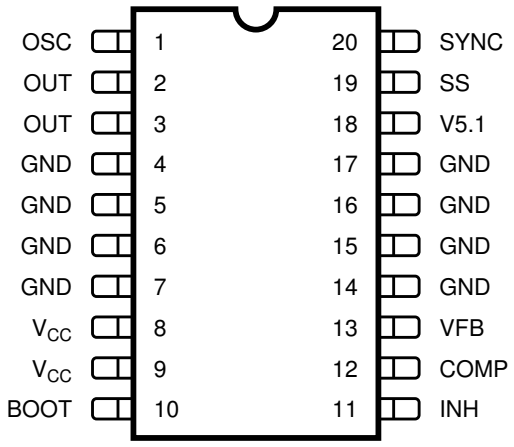
Figure 2. Block diagram



2 Pin settings

2.1 Pin connection

Figure 3. Pin connection (top view)



SO20 (12+4+4)

2.2 Pin description

Table 1. Pin description

N° Pin	Name	Description
12	COMP	E/A output to be used for frequency compensation
11	INH	A logic signal (active high) disables the device (sleep mode operation). If not used it must be connected to GND; if floating the device is disabled.
10	BOOT	A capacitor connected between this pin and the output allows to drive the internal D-MOS.
20	SYNC	Input/Output synchronization.
8,9	V_{CC}	Unregulated DC input voltage
2,3	OUT	Stepdown regulator output.
13	VFB	Stepdown feedback input. Connecting the output directly to this pin results in an output voltage of 3.3 V for the L4973V3.3 and 5.1 V for L4973V5.1. An external resistive divider is required for higher output voltages. For output voltage resistive divider is required for higher output voltages. For output voltage less than 3.3 V, see *Note:* and *Figure 30.*
18	V5.1	Reference voltage externally available.
4,5,6,7 14,15,16,17	GND	Signal ground
1	OSC	An external resistor connected between the unregulated input voltage and Pin 1 and a capacitor connected from Pin 1 to ground fixes the switching frequency. (Line feed forward is automatically obtained)

Note: The maximum power dissipation of the package must be observed.

3 Electrical data

3.1 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_9,V_8	Input voltage	58	V
V_2,V_3	Output DC voltage Output peak voltage at t = 0.1 µs f = 200 kHz	-1 - 5	V V
I_2,I_3	Maximum output current	int. limit.	
V_{10}-V_8		14	V
V_{10}	Bootstrap voltage	70	V
V_{12}	Analogs input voltage (V_{CC} = 24 V)	12	V
V_{19}	Analogs input voltage (V_{CC} = 24 V)	13	V
V_{13}	(V_{CC} = 20 V)	6 -0.3	V V
V_{20}	(V_{CC} = 20 V)	5.5 0.3	V V
V_{11}	Inhibit	V_{CC} -0.3	V V
P_{tot}	Power dissipation a T_{pins} = 90 °C	4	W
T_J,T_{STG}	Junction and storage temperature	-40 to 150	°C

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJP}	Maximum thermal resistance junction-pin	15	°C/W
R_{thJA}	Maximum thermal resistance junction-ambient	80 (1)	°C/W

1. Package mounted on board

4 Electrical characteristics

Table 4. Electrical characteristics
(Refer to the test circuit,V_{CC} = 24 V; T_J = 25 °C, C_{OSC} = 2.7 nF; R_{OSC} = 20 kΩ; unless otherwise specified)

Symbol	Parameter	Test condition		Min	Typ	Max	Unit
Dynamic characteristics							
	Input voltage range (1)	V_O = V_{REF} to 40 V; I_O = 3.5A	(2)	8		55	V
	Output voltage L4973V5.1	I_O = 1 A		5.05	5.1	5.15	V
		I_O = 0.5 A to 3.5 A V_{CC} = 8 V to 55 V		5.00	5.1	5.20	V
			(2)	4.95	5.1	5.25	V
	Output voltage L4973V3.3	I_O = 1 A		3.326	3.36	3.393	V
		I_O = 0.5 A to 3.5 A V_{CC} = 8 V to 40 V		3.292	3.36	3.427	V
			(2)	3.26	3.36	3.46	V
	$R_{DS(on)}$	V_{CC} = 10.5 V I_O = 3.5 A			0.15	0.22	Ω
			(2)			0.35	Ω
	Maximum limiting current	V_{CC} = 8 V to 55 V	(2)	3.8	4.5	5.5	A
				4	4.5	5.5	A
η	Efficiency	V_O = 5.1 V; I_O = 3.5 A			90		%
		V_O = 3.3 V; I_O = 3.5 A			85		%
	Switching frequency		(2)	90	100	110	kHz
	Supply voltage ripple rejection	V_i = V_{CC}+2 V_{RMS} V_O = V_{ref}; I_O = 1 A; f_{ripple} = 100 Hz		60			dB
Δf_{sw}	Switching frequency stability vs., supply voltage	V_{CC} = 8 V to 55 V			2	5	%
Reference section							
	Reference voltage	I_{ref} = 0 to 20 mA; V_{CC} = 8 to 55 V		5.025	5.1	5.175	V
			(2)	4.950	5.1	5.250	V
	Line regulation	I_{ref} = 0 mA; V_{CC} = 8 to 55 V			5	10	mV
	Load regulation	V_{ref} = 0 to 5 mA;			2	10	mV
		V_{CC} = 0 to 20 mA			6	25	mV
	Short circuit current			30	65	100	mA

Table 4. Electrical characteristics (continued)
(Refer to the test circuit, V_{CC} = 24 V; T_J = 25 °C, C_{OSC} = 2.7 nF; R_{OSC} = 20 kΩ; unless otherwise specified)

Symbol	Parameter	Test condition		Min	Typ	Max	Unit
Soft-start							
	Soft-start charge current			30	45	60	µA
	Soft-start discharge current			15	22	30	µA
Inhibit							
	High level voltage		(2)	3.0			V
	Low level voltage		(2)			0.8	V
	I_{source} high level	V_{INH} = 3 V	(2)	10	16	50	µA
	I_{source} low level	V_{INH} = 0.8 V	(2)	10	15	50	µA
DC characteristics							
	Total operating quiescent current	Duty cycle = 50 %			4	6	mA
	Quiescent current	Duty cycle = 0			2.7	4	mA
	Total stand-by quiescent current	V_{CC} = 24 V; V_{INH} = 5 V			100	200	µA
		V_{CC} = 55 V; V_{INH} = 5 V			150	300	µA
Error amplifier							
	High level output voltage			11.0			V
	Low level output voltage					0.65	V
	Source bias current			1	2	3	µA
	Source output current			200	300	600	µA
	Sink output current			200	300		µA
	Supply voltage ripple rejection	V_{COMP} = VFB C_{REF} = 4.7 µF 1-5 mA load current		60	80		dB
	DC open loop gain	R_L = ∞		50	60		dB
	Transconductance	I_{comp} = -0.1 to 0.1 mA; V_{comp} = 6 V			2.5		mS
Oscillator section							
	Ramp valley			0.78	0.85	0.92	V
	Ramp peak	V_{CC} = 8 V V_{CC} = 55 V		1.9 9	2.1 9.6	2.3 10.2	V V
	Maximum duty cycle			95	97		%

Table 4. Electrical characteristics (continued)
(Refer to the test circuit, V_{CC} = 24 V; T_J = 25 °C, C_{OSC} = 2.7 nF; R_{OSC} = 20 kΩ; unless otherwise specified)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
	Maximum frequency	Duty cycle = 0%; R_{OSC} =13 kΩ; C_{OSC} = 820 pF;			300	kHz
Sync function						
	High input voltage	V_{CC} = 8 V to 55 V	3.5			V
	Low input voltage	V_{CC} = 8 V to 55 V			0.9	V
	Slave sink current		0.15	0.25	0.45	mA
	Master output amplitude	I_{source} = 3 mA	4	4.5		V
	Output pulse width	No load, V_{sync} = 4.5 V	0.20	0.35		µs

1. Pulse testing with a low duty cycle
2. Specifications referred to T_J from -40 °C to 125 °C.

5 Application circuit

Figure 4. Application circuit (D5.1)

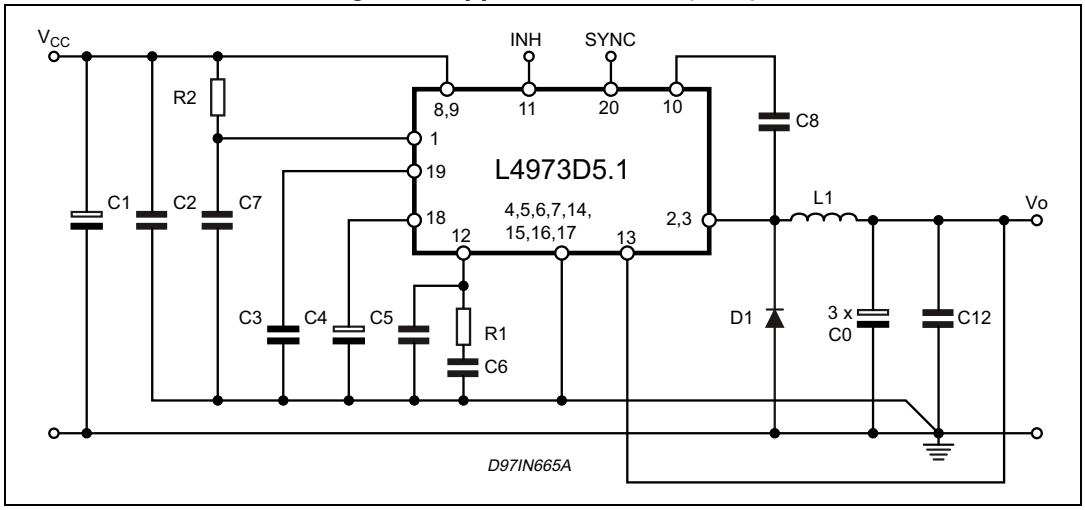
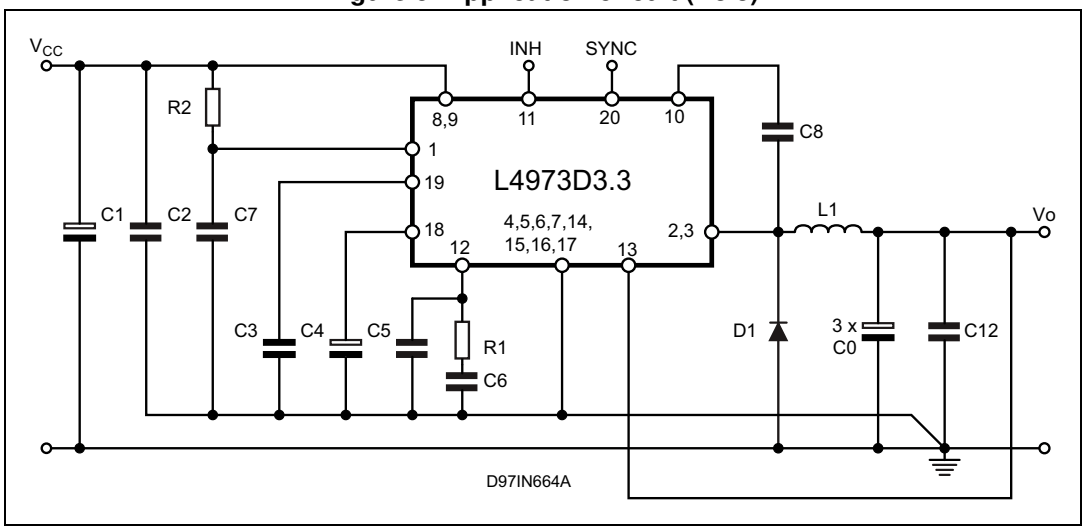


Figure 5. Application circuit (D3.3)



6 Typical characteristics

Figure 6. Quiescent drain current vs. input voltage (0% duty cycle)

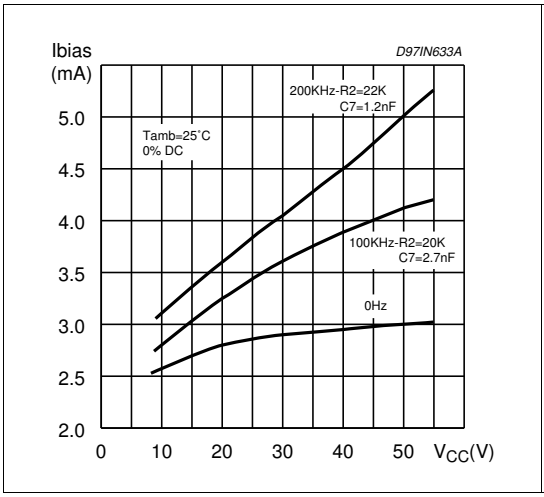


Figure 7. Quiescent drain current vs. junction temperature

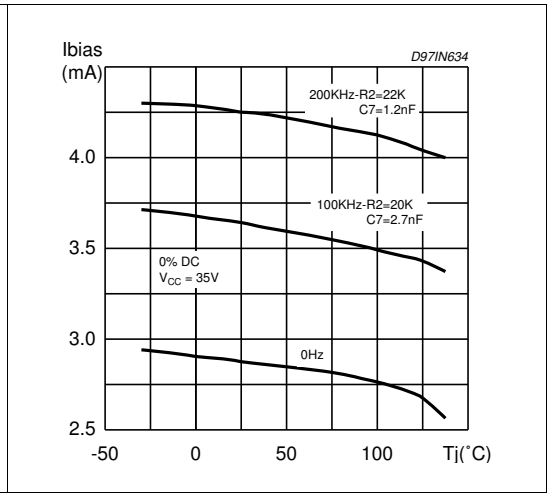


Figure 8. Stand by drain current vs. input voltage

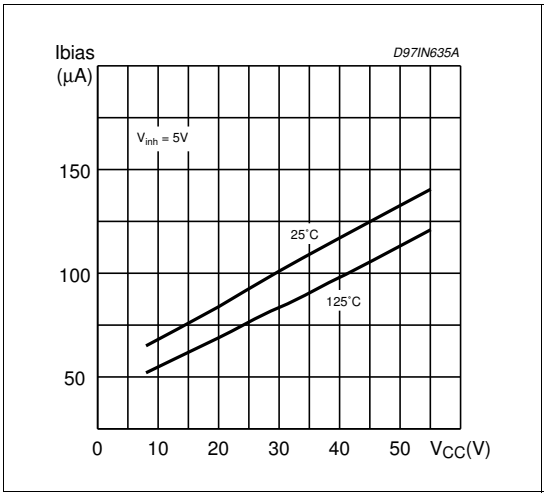


Figure 9. Reference voltage vs. junction temperature (pin 16)

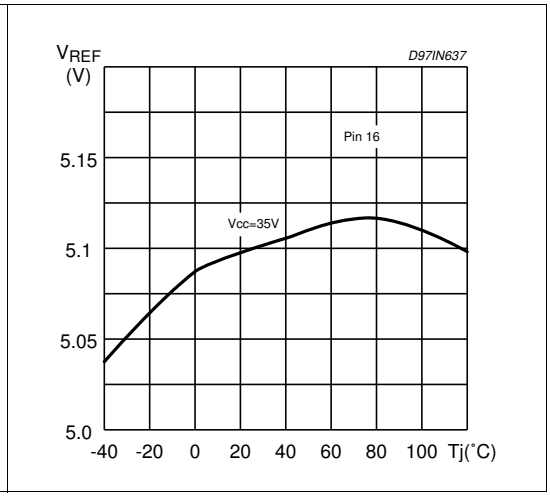


Figure 10. Reference voltage vs. input voltage (pin 16)

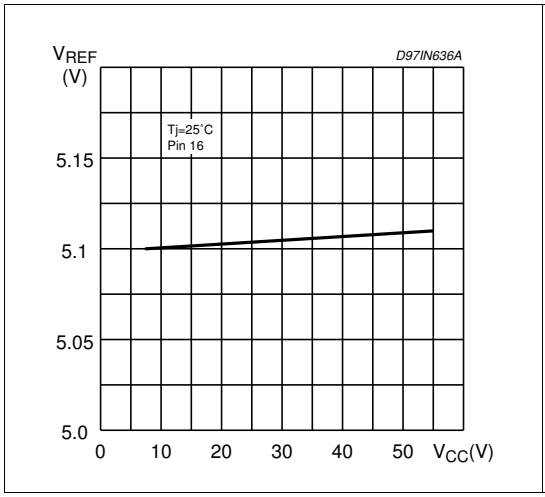


Figure 11. Reference voltage vs. reference input current

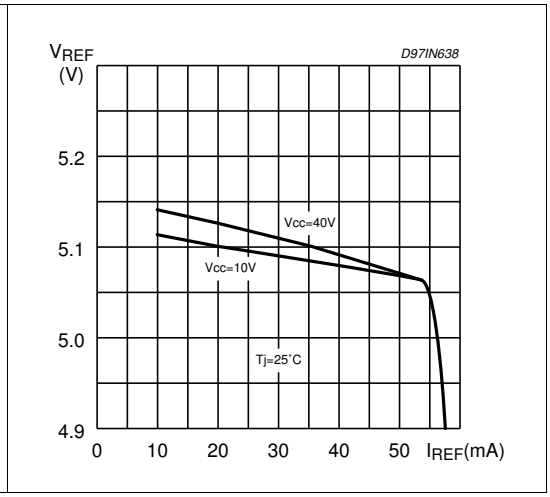


Figure 12. Inhibit current vs. inhibit voltage (pin 10)

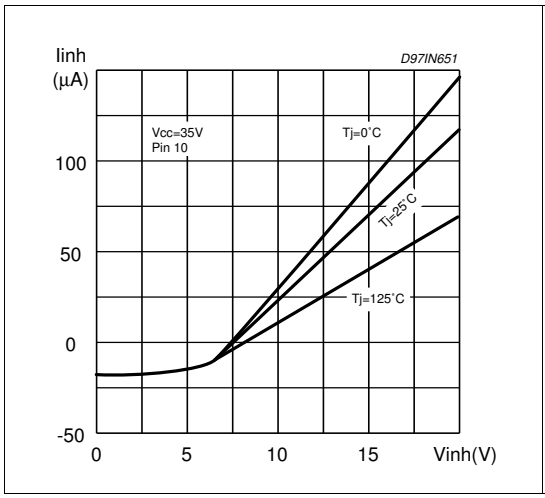


Figure 13. Line regulation (see *Figure 4*)

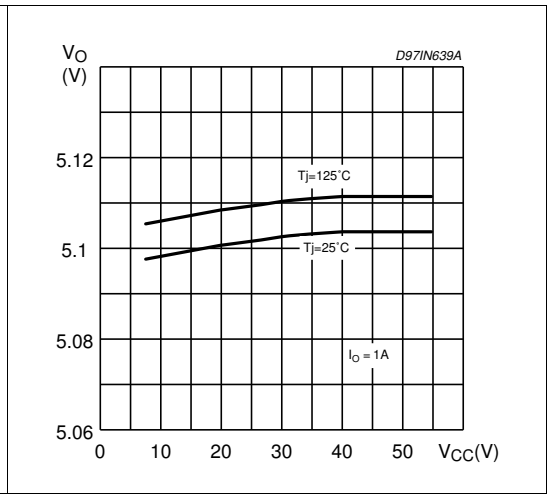


Figure 14. Load regulation (see *Figure 4*)

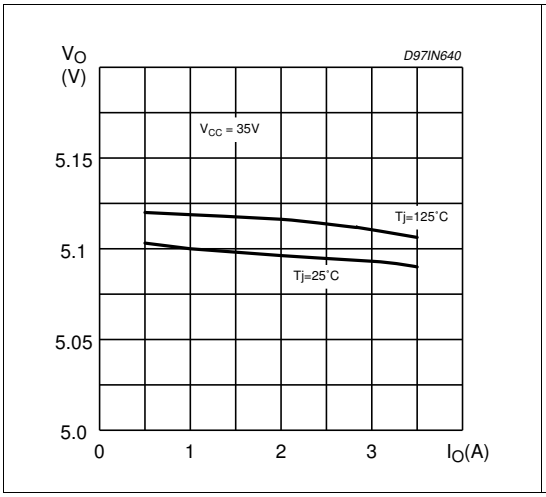


Figure 15. Line regulation (see *Figure 5*)

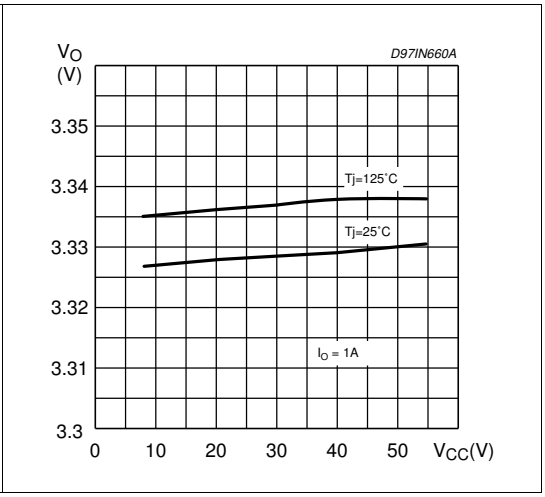


Figure 16. Load regulation

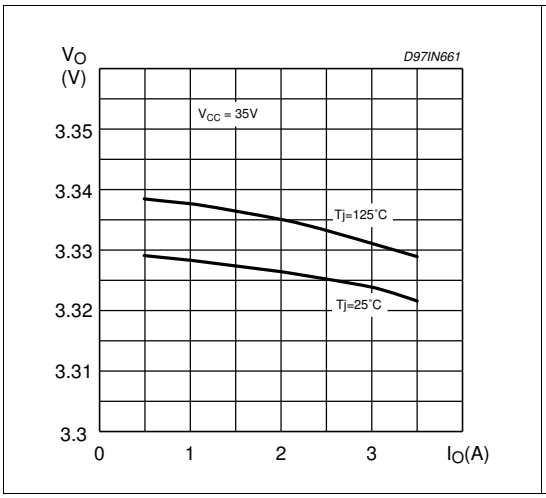


Figure 17. Switching frequency vs. R2 and C7

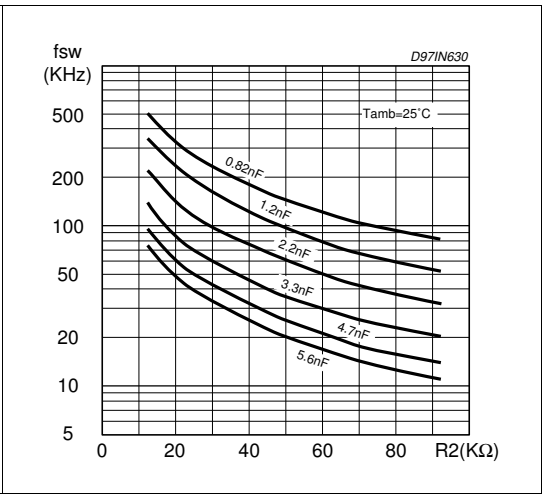


Figure 18. Switching frequency vs. input voltage

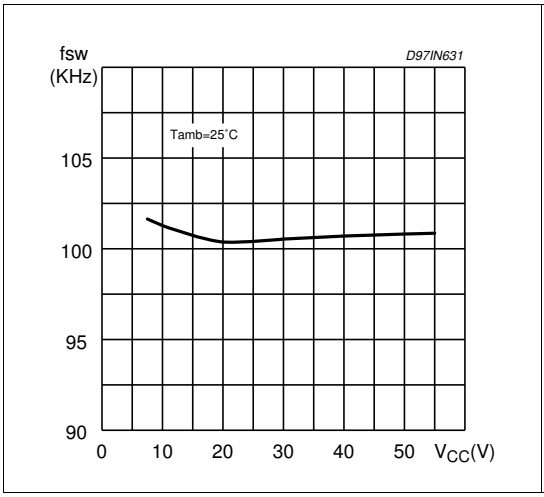


Figure 19. Switching frequency vs. junction temperature

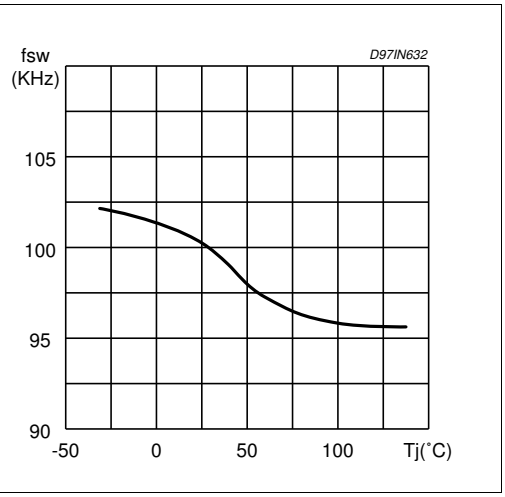


Figure 20. Dropout voltage between pin 7,8 and 2,3

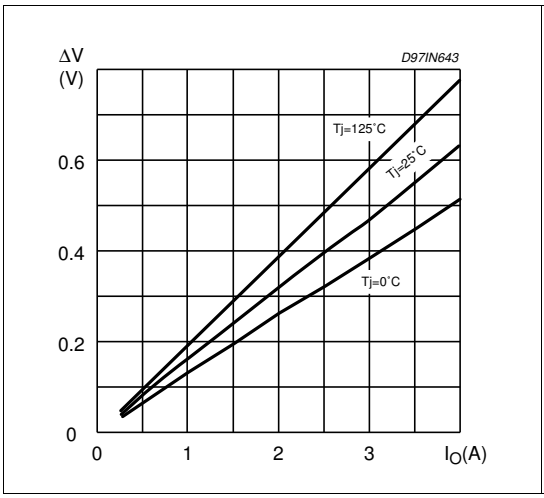


Figure 21. Efficiency vs. output voltage

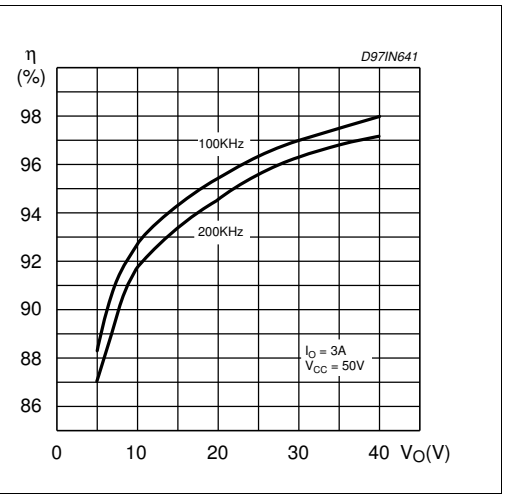


Figure 22. Dropout voltage between pin 7,8 and 2,3

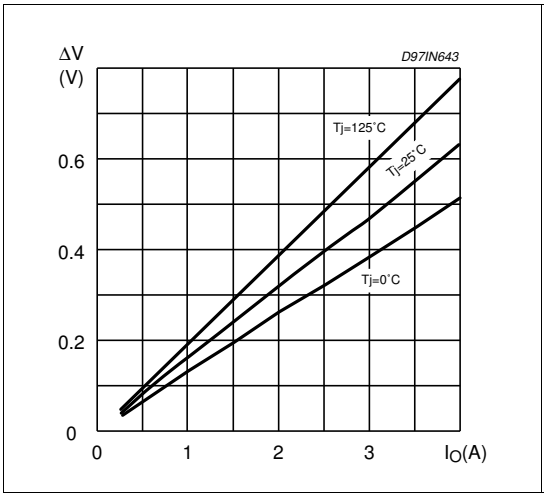


Figure 23. Efficiency vs. output voltage

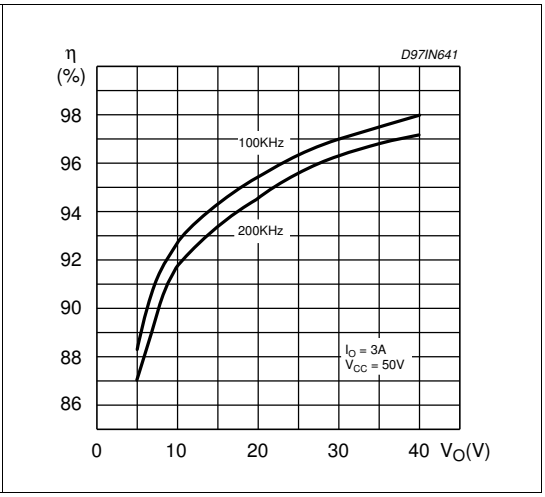


Figure 24. Efficiency vs. output voltage (Diode STPS745D)

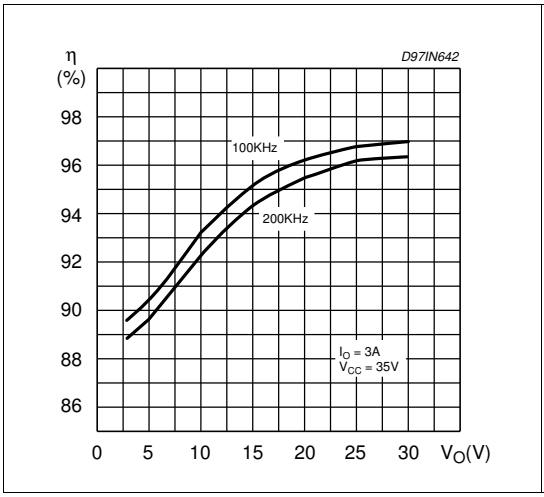


Figure 25. Efficiency vs. output current (see *Figure 4*)

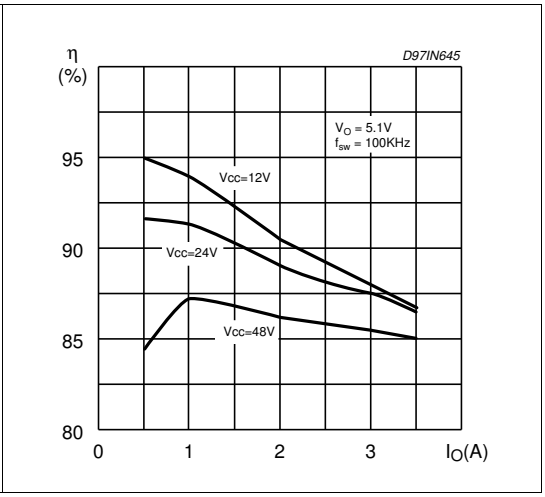


Figure 26. Efficiency vs. output current (see *Figure 4*)

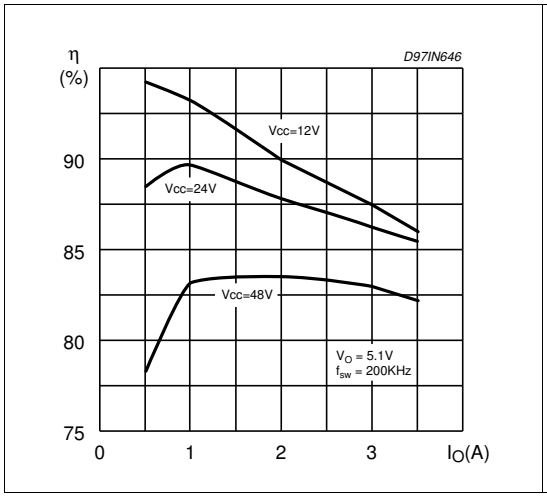


Figure 27. Efficiency vs. output current (see *Figure 5*)

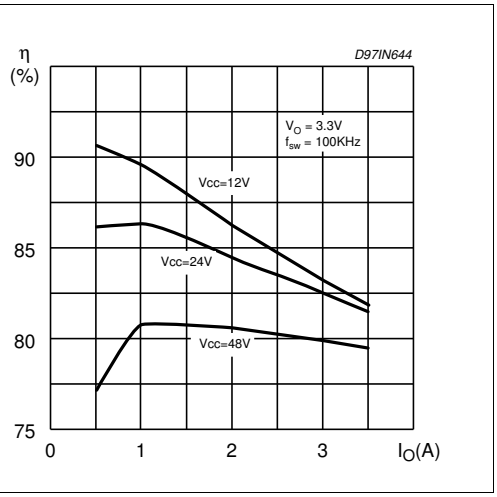


Figure 28. Efficiency vs. output current (see *Figure 5*)

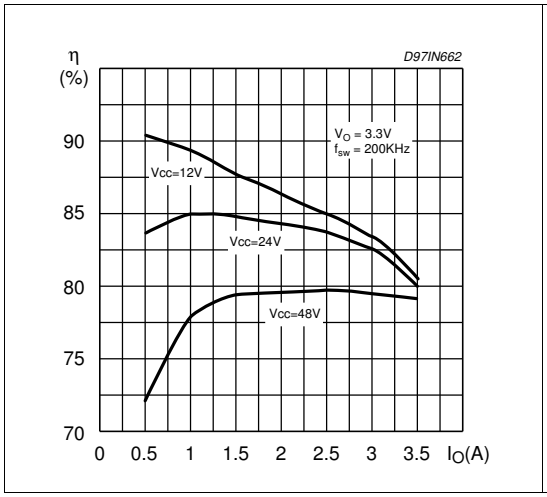


Figure 29. Power dissipation vs. input voltage (device only) (see *Figure 4*)

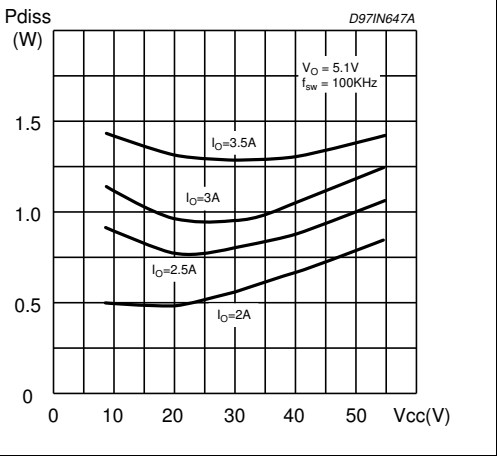


Figure 30. Power dissipation vs. output voltage (device only)

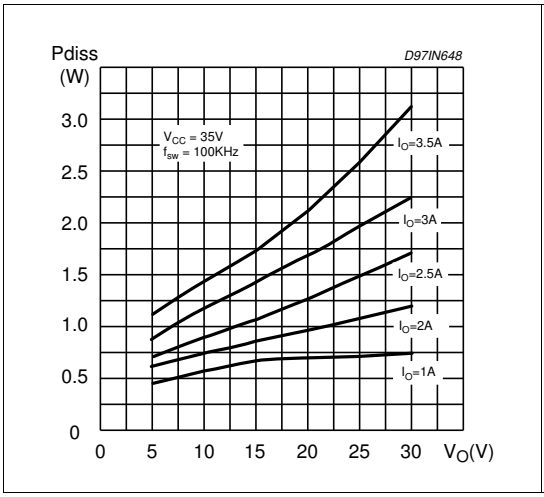


Figure 31. Pulse by pulse limiting current vs. junction temperature

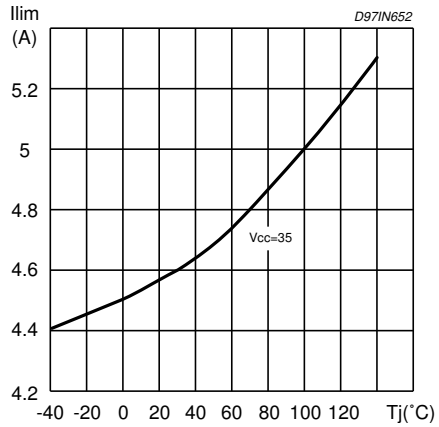


Figure 32. Load transient

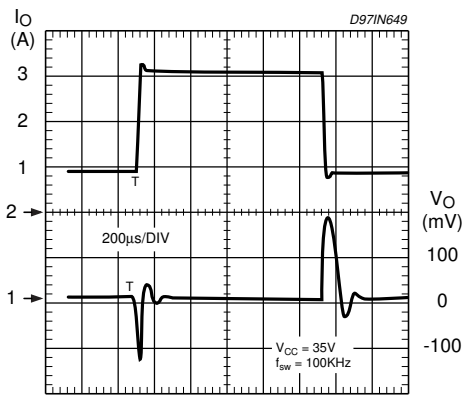


Figure 33. Line transient

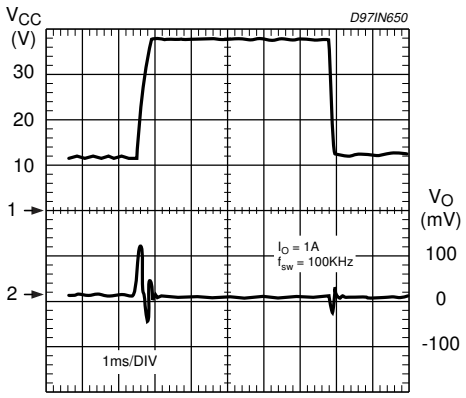


Figure 34. Source current rise and fall time, pin 2, 3

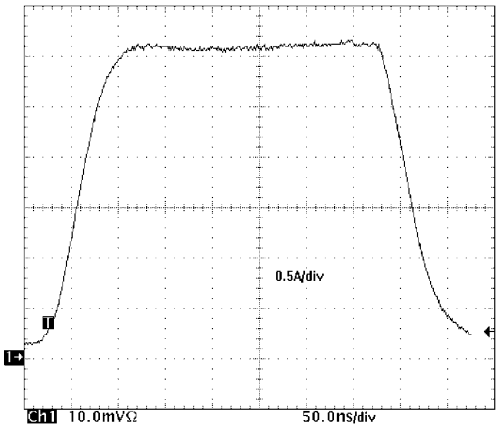


Figure 35. Soft-start capacitor selection vs. inductor and V_{CC} max (ref. AN938)

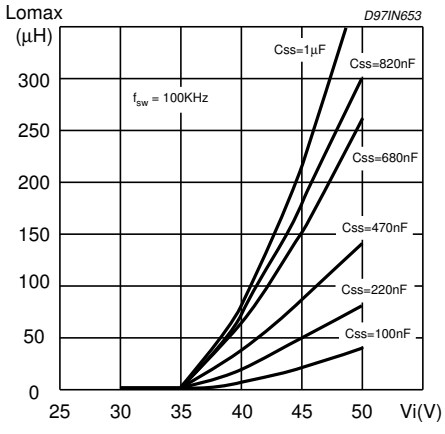


Figure 36. Soft-start capacitor selection vs. inductor and V_{CC} max (ref. AN938)

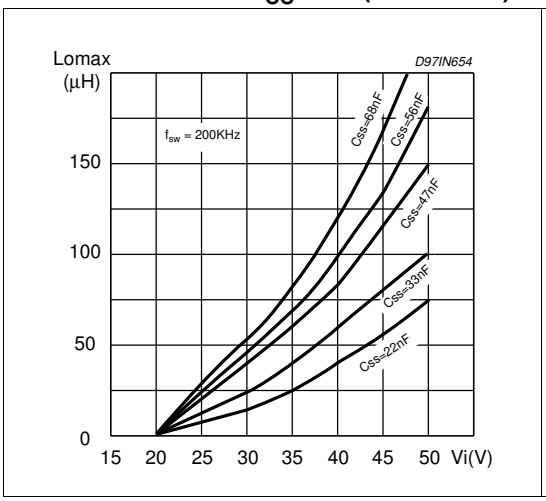
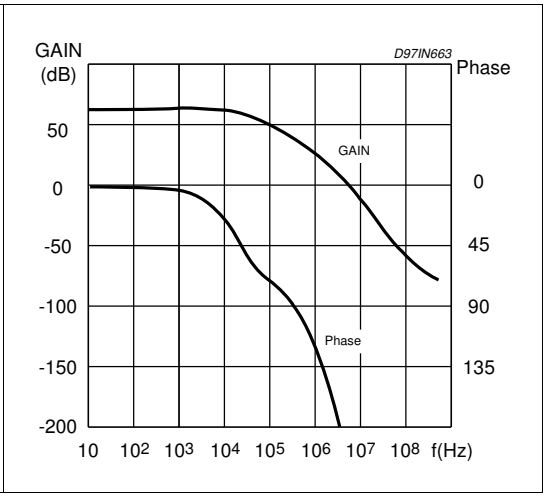


Figure 37. Open loop frequency and phase of error amplifier



7 Application ideas

Figure 38. 3.5 A at V_O < 3.3 V

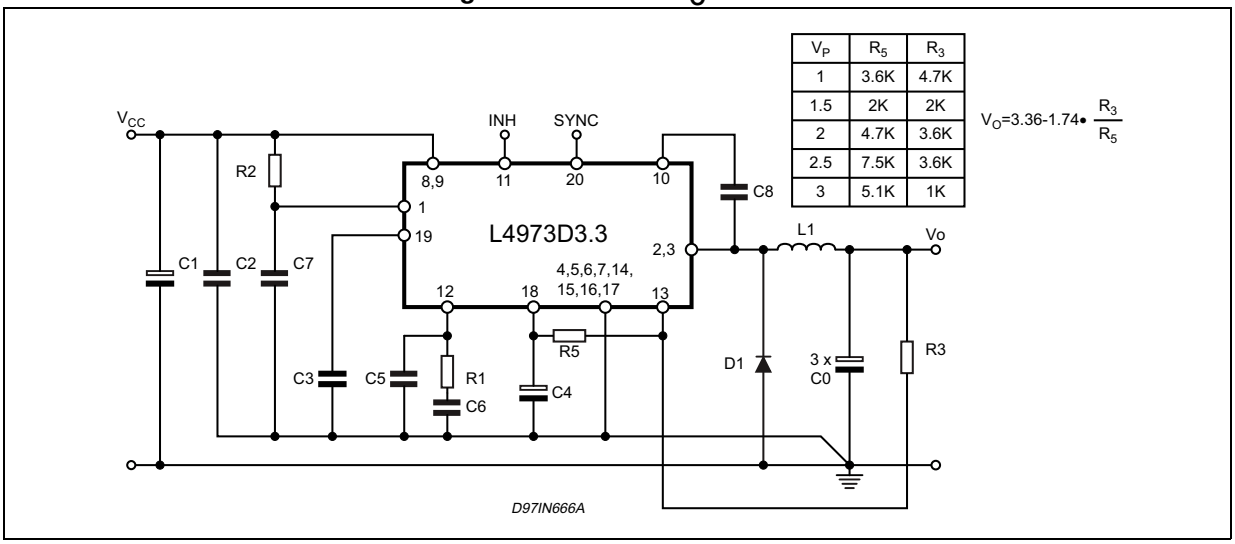


Figure 39. 12 V to 3.3 V high performance buck converter (fsw = 200 kHz)

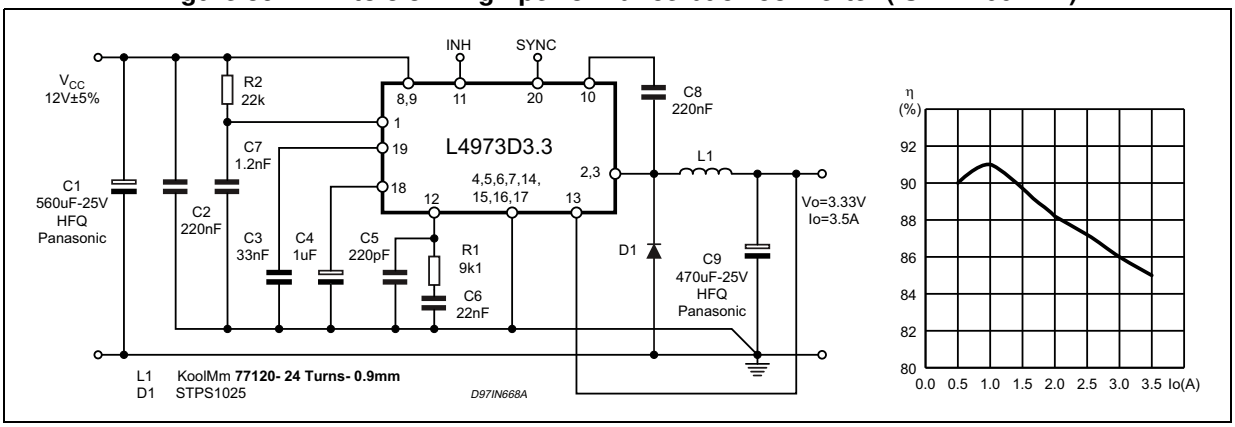


Figure 40. Synchronization example

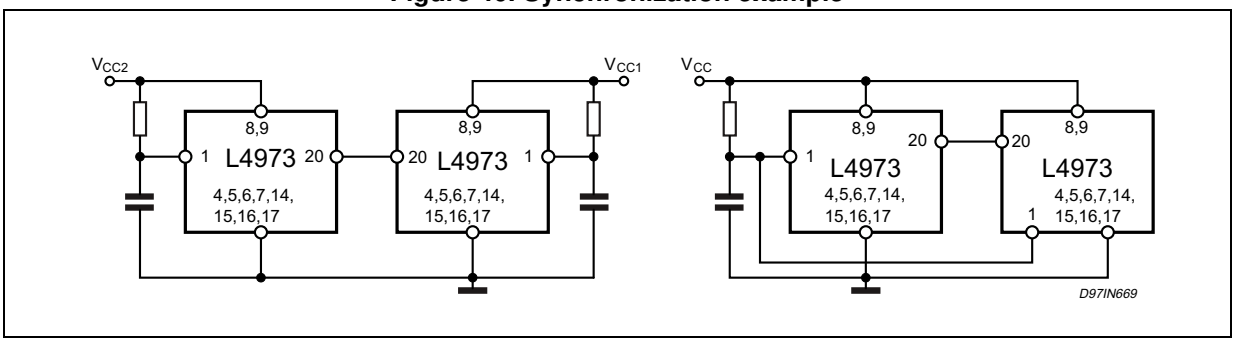
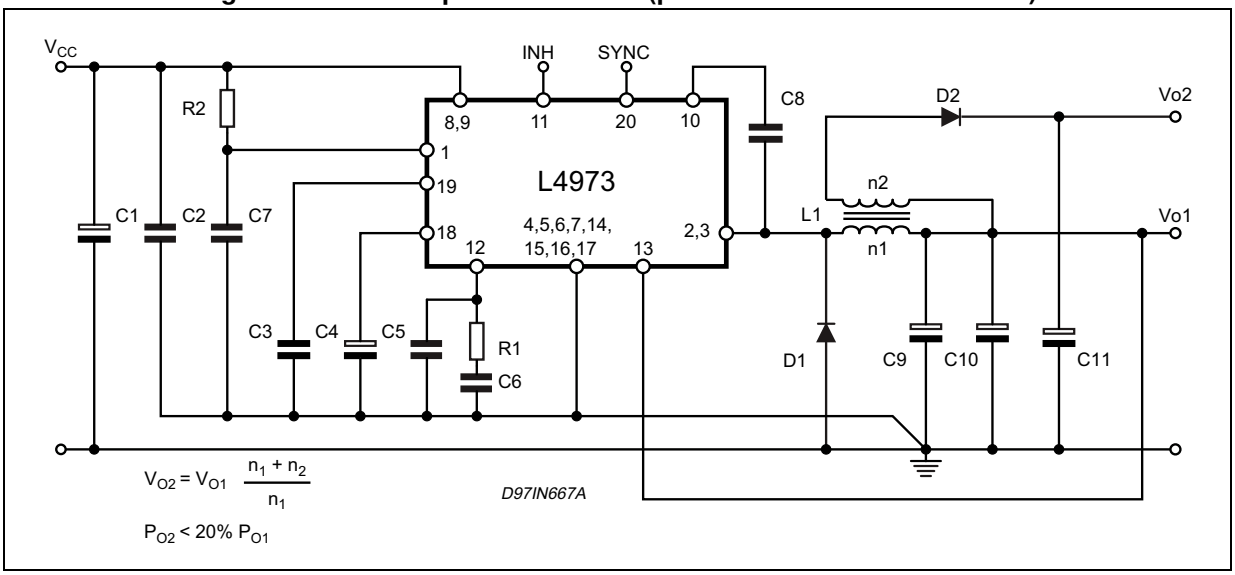


Figure 41. Multi output not isolated (pin out referred to DIP12+3+3)



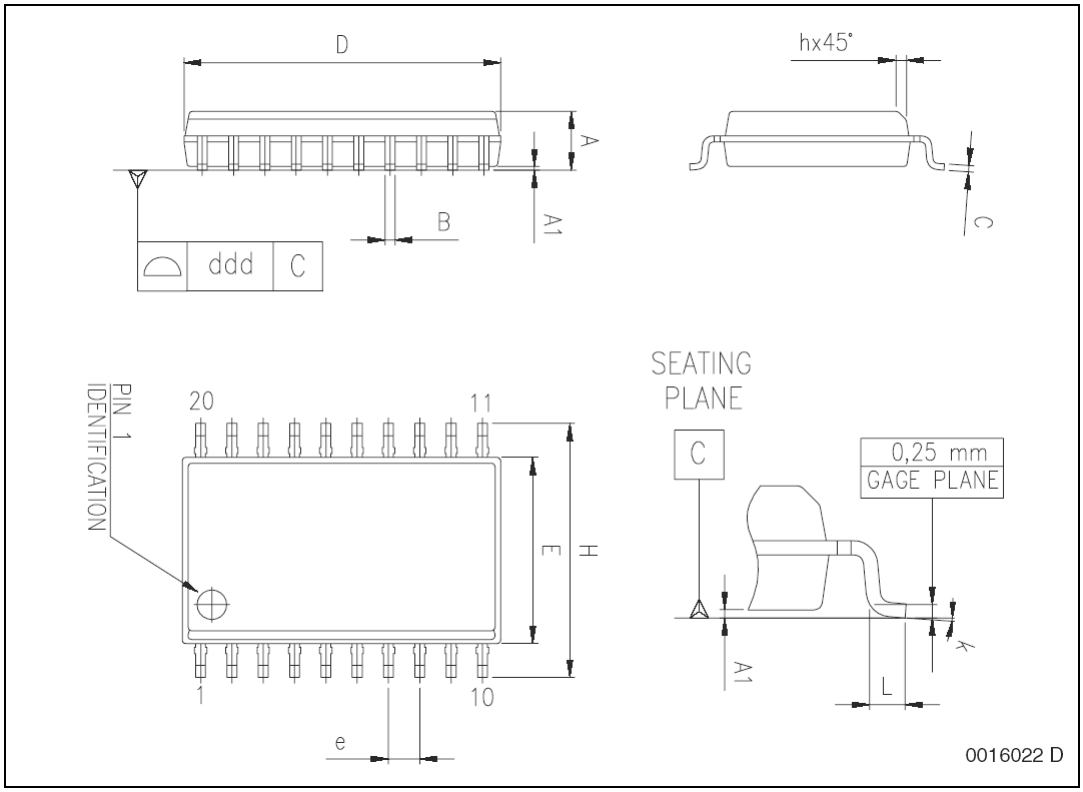
8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 5. SO-20 mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.200
C	0.23		0.32	0.009		0.013
D (1)	12.60		13.00	0.496		0.512
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

Figure 42. Package dimensions



9 Order code

Table 6. Order code

Part number	Package	Packaging
L4973D3.3-013TR, E-L4973D3.3-TR	SO-20	Tape and reel
L4973D5.1-013TR	SO-20	Tape and reel

10 Revision history

Table 7. Document revision history

Date	Revision	Changes
12-Sep-2001	13	First Issue
07-May-2005	14	Updated the Layout look & feel. Changed name of the D1 on the fig. 5.
14-Dec-2005	15	Added the ECOPACK part numbers in the Table 1. Order Codes.
06-Dec-2006	16	The document has been reformatted, and order codes updated
07-May-2007	17	New data on Table 4.
26-Feb-2009	18	Updated Section5: Evaluation board on page 10.
03-May-2024	19	Updated *Table 6*.