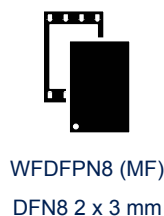
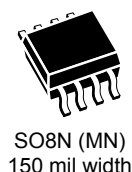



## Automotive 4-Kbit serial I<sup>2</sup>C bus EEPROM with 1 MHz clock



### Features

- AEC-Q100 qualified 
- Compatible with all I<sup>2</sup>C bus modes
  - 1 MHz
  - 400 kHz
  - 100 kHz
- Memory array
  - 4 Kbits (512 bytes) of EEPROM
  - Page size: 16 bytes
  - Additional write lockable page (identification page)
- Extended temperature and voltage ranges
  - -40 °C to 125 °C; 1.7 V to 5.5 V
- Schmitt trigger inputs for noise filtering
- Short write cycle time
  - Byte write within 4 ms
  - Page write within 4 ms
- Write cycle endurance
  - 4 million write cycles at 25 °C
  - 1.2 million write cycles at 85 °C
  - 600 k write cycles at 125 °C
- Data retention
  - 50 years at 125 °C
  - 100 years at 25 °C
- ESD protection (human body model)
  - 4000 V
- Packages
  - RoHS compliant and halogen-free (ECOPACK2®)

#### Product status link

[M24C04-A125](#)

#### Product label



## 1 Description

The M24C04-A125 is a 4-Kbit serial EEPROM automotive grade device operating up to 125 °C. The M24C04-A125 is compliant with the very high level of reliability defined by the automotive standard AEC-Q100 grade 1.

The device is accessed by a simple serial I<sup>2</sup>C compatible interface running up to 1 MHz.

The memory array is based on advanced true EEPROM technology (electrically erasable programmable memory). The M24C04-A125 is a byte-alterable memory (512 × 8 bits) organized as 32 pages of 16 bytes in which the data integrity is significantly improved with an embedded error correction code logic.

The M24C04-A125 offers an additional identification page (16 bytes) in which the ST device identification can be read. This page can also be used to store sensitive application parameters which can be later permanently locked in read-only mode.

**Figure 1. Logic diagram**

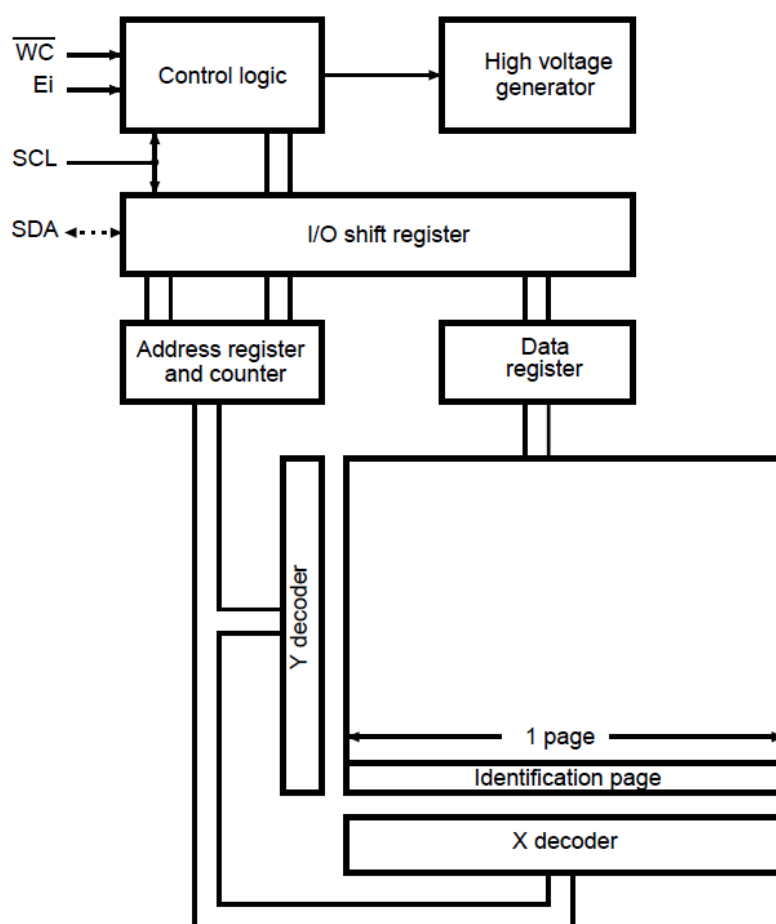
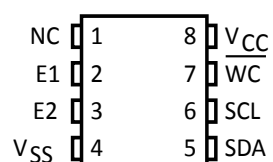


Table 1. Signal names

Signal name	Function	Direction
E2, E1	Chip enable	Input
SDA	Serial data	I/O
SCL	Serial clock	Input
$\overline{WC}$	Write control	Input
V <sub>CC</sub>	Supply voltage	-
V <sub>SS</sub>	Ground	-

Figure 2. 8-pin package connections



1. See [Section 9: Package mechanical data](#) for package dimensions, and how to identify pin 1.

## 2 Signal description

### 2.1 Serial clock (SCL)

The signal applied on this input is used to strobe the data available on SDA(in) and to output the data on SDA(out).

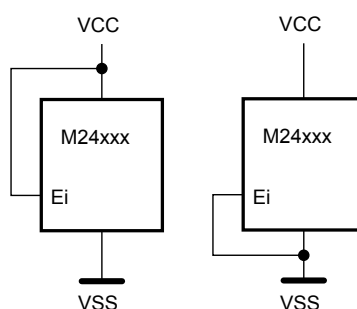
### 2.2 Serial data (SDA)

SDA is an input/output used to transfer data in or out of the device. SDA(out) is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected between SDA and  $V_{CC}$  (Figure 10 and Figure 11 indicate how to calculate the value of the pull-up resistor).

### 2.3 Chip enable (E2, E1)

This input signal is used to set the value that is to be looked for on the two bit (b3, b2) of the 7-bit device select code (see Table 2). These inputs must be tied to  $V_{CC}$  or  $V_{SS}$  to establish the device select code, as shown in Figure 3. When not connected (left floating), these inputs are read as low (0).

Figure 3. Device select code



DT12806V1

### 2.4 Write control ( $\overline{WC}$ )

This input signal is useful for protecting the entire contents of the memory from inadvertent write operations. Write operations are disabled to the entire memory array when write control ( $\overline{WC}$ ) is driven high. Write operations are enabled when write control ( $\overline{WC}$ ) is either driven low or left floating.

When write control ( $\overline{WC}$ ) is driven high, device select and address bytes are acknowledged, Data bytes are not acknowledged.

### 2.5 $V_{SS}$ (ground)

$V_{SS}$  is the reference for the  $V_{CC}$  supply voltage.

### 2.6 Supply voltage ( $V_{CC}$ )

$V_{CC}$  is the supply voltage pin.

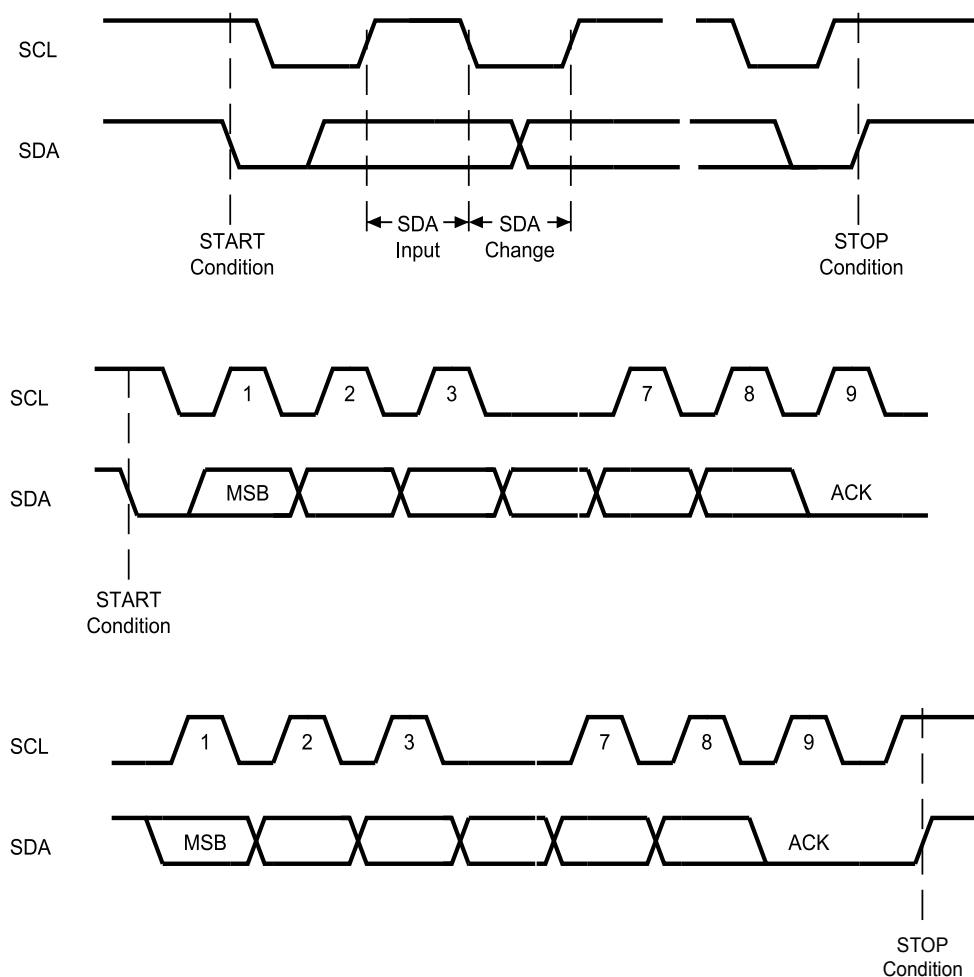
### 3 Device operation

The device supports the I<sup>2</sup>C protocol (see Figure 4).

The I<sup>2</sup>C bus is controlled by the bus controller and the device is always a target in all communications.

The device (bus controller or a target) that sends data on to the bus is defined as a transmitter; the device (bus controller or a target) is defined as a receiver when reading the data.

**Figure 4. I<sup>2</sup>C bus protocol**



DT00792BV1

#### 3.1 Start condition

Start is identified by a falling edge of serial data (SDA) while the serial clock (SCL) is stable in the high state. A start condition must precede any data transfer instruction. The device continuously monitors (except during a write cycle) serial data (SDA) and serial clock (SCL) for a start condition.

#### 3.2 Stop condition

Stop is identified by a rising edge of serial data (SDA) while the serial clock (SCL) is stable in the high state. A stop condition terminates communication between the device and the bus controller.

A stop condition at the end of a write instruction triggers the internal write cycle.

### 3.3 Data input

During data input, the device samples serial data (SDA) on the rising edge of serial clock (SCL). For correct device operation, serial data (SDA) must be stable during the rising edge of serial clock (SCL), and the serial data (SDA) signal must change only when serial clock (SCL) is driven low.

### 3.4 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus controller or target device, releases serial data (SDA) after sending eight bits of data. During the ninth clock pulse period, the receiver pull serial data (SDA) low to acknowledge the receipt of the eight data bits.

### 3.5 Device addressing

To start communication between the bus controller and the target device, the bus controller must initiate a Start condition. Following this, the bus controller sends the device select code, as shown in Table 2.

The device select code consists of a 4-bit device type identifier and a 2-bit chip enable address (E2, E1). A device select code handling any value other than 1010b (to select the memory) or 1011b (to select the identification page) is not acknowledged by the memory device.

Up to four memory devices can be connected on a single I2C bus. Each one is given a unique 2-bit code on the chip enable (E2, E1) inputs. When the device select code is received, the memory device only responds if the chip enable address is the same as the value decoded on the E2, E1 inputs.

The eighth bit is the read/write bit (RW). This bit is set to 1 for read and 0 for write operations.

**Table 2. Device select code**

	Device type identifier <sup>(1)</sup>				Chip enable address <sup>(2)</sup>			RW
	b7	b6	b5	b4	b3	b2	b1	b0
When accessing the memory	1	0	1	0	E2	E1	A8	RW
When accessing the identification page	1	0	1	1	E2	E1	X	RW

1. The most significant bit, b7, is sent first.

2. X bit is a don't care bit.

If the memory device does not match the device select code, it deselects itself from the bus, and enters the standby mode.

If the memory device matches the device select code, the corresponding memory device gives an acknowledgment on Serial Data (SDA) during the ninth SCL clock period. Once the memory device has acknowledged the device select code, the memory device waits for the controller to send the address byte. The memory device responds to the address byte with an acknowledge bit.

**Table 3. Significant address bits**

		Memory (Device type identifier = 1010b)		Identification page (Device type identifier = 1011b)			
		Random address read	Write	Read identification page	Write identification page	Lock identification page	Read lock status
Most significant bits	b1 <sup>(1)</sup>	A8	A8	X	X	X	see Section 4.2.5
Address byte	b7	A7	A7	0	0	1	
	b6	A6	A6	X	X	X	
	b5	A5	A5	X	X	X	
	b4	A4	A4	X	X	X	
	b3	A3	A3	A3	A3	X	
	b2	A2	A2	A2	A2	X	
	b1	A1	A1	A1	A1	X	
	b0	A0	A0	A0	A0	X	

1. Address bits defined inside the device select code (see Table 2)

**Note:**        *A: significant address bit.*  
                  *X: bit is don't care.*

### 3.6 Identification page

The M24C04-A125 offers an identification page (16 bytes) in addition to the 4-Kbit memory.

The identification page contains two fields:

- Device identification code: the first three bytes are programmed by STMicroelectronics with the device identification code, as shown in [Table 4](#).
- Application parameters: the bytes after the device identification code are available for application-specific data.

*Note:* If the end application does not need to read the device identification code, this field can be overwritten and used to store application-specific data. Once the application-specific data are written in the identification page, the whole identification page should be permanently locked in read-only mode.

The instructions to read, write, and lock the identification page are detailed in [Section 4](#).

**Table 4. Device identification code**

Address in identification page	Content	Value
00h	ST manufacturer code	20h
01h	I <sup>2</sup> C family code	E0h
02h	Memory density code	09h (4-Kbit)



## 4 Instructions

### 4.1 Write operations

For a write operation, the bus controller sends a start condition followed by a device select code with the R/W bit reset to 0. The device acknowledges this, as shown in [Figure 5](#), and waits for the controller to send the address byte with an acknowledge bit, and then waits for the data byte.

When the bus controller generates a stop condition immediately after a data byte ACK bit (in the “10<sup>th</sup> bit” time slot), either at the end of a byte write or a page write, the internal write cycle  $t_W$  is then triggered. A stop condition at any other time slot does not trigger the internal write cycle.

During the internal write cycle, serial data (SDA) is disabled internally, and the device does not respond to any requests.

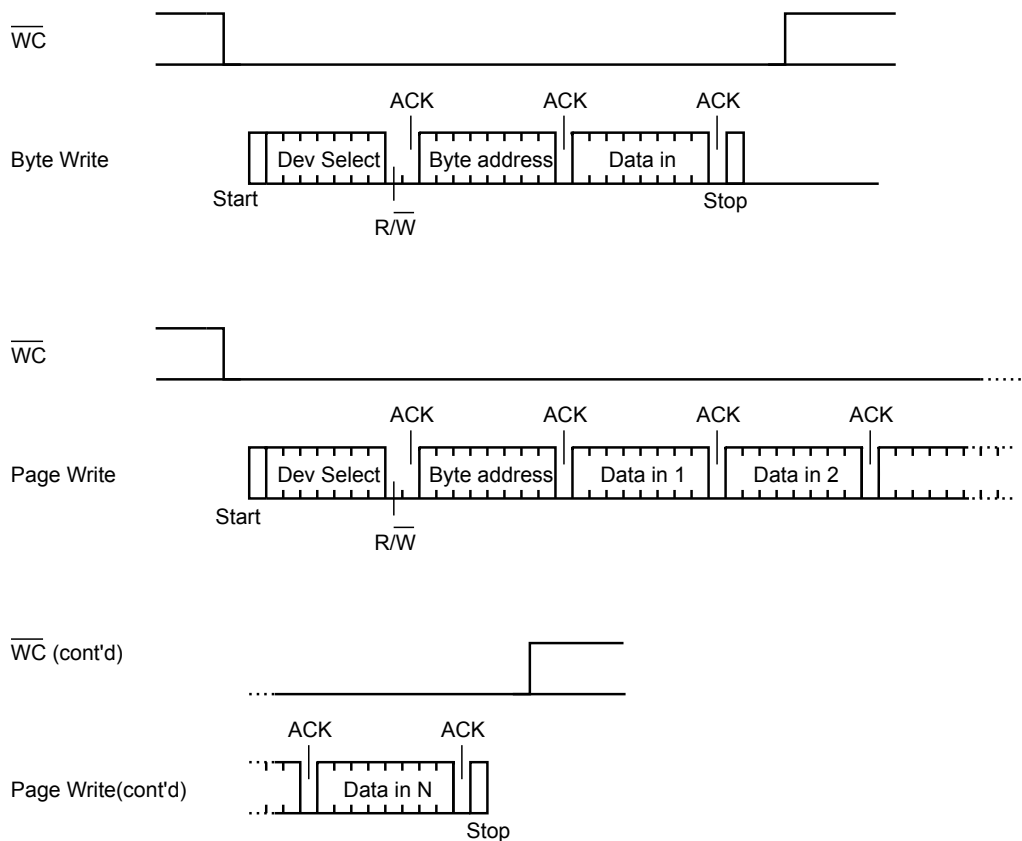
After the successful completion of an internal write cycle ( $t_W$ ), the device internal address counter is automatically incremented to point to the next byte after the last modified byte.

If the write control input ( $\overline{WC}$ ) is driven high, the write instruction is not executed and the accompanying data bytes are *not* acknowledged, as shown in [Figure 6](#).

### 4.1.1 Byte write

After the device select code and the address byte, the bus controller sends one data byte. If the addressed location is write-protected, by write control ( $\overline{WC}$ ) being driven high, the device replies with NoACK on the received data byte, and the location is not modified (see Figure 6). If, instead, the addressed location is not write-protected, the device replies with ACK. The bus controller terminates the transfer by generating a stop condition, as shown in Figure 5.

**Figure 5. Write mode sequences with  $\overline{WC} = 0$  (data write enabled)**



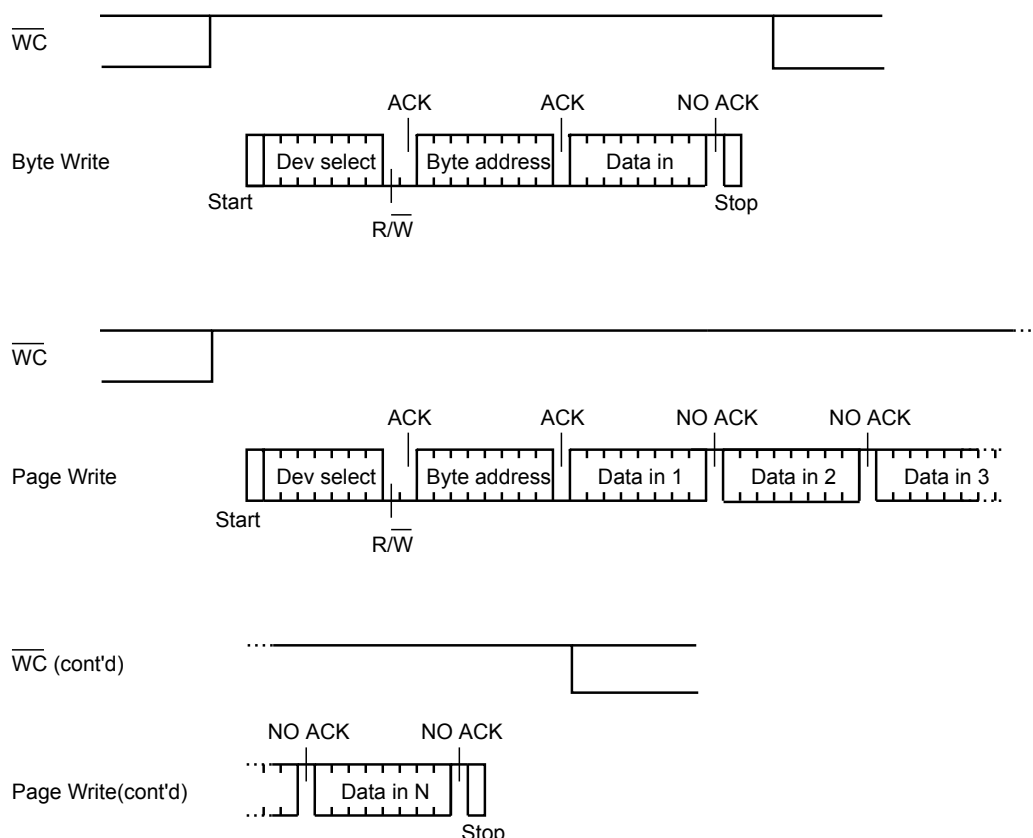
DT02804cV1

### 4.1.2 Page write

The page write mode allows up to N (N is the number of bytes in a page) bytes to be written in a single write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits, A8/A4, are the same. If more bytes are sent than will fit up to the end of the page, a condition known as "roll-over" occurs. In case of roll-over, the first bytes of the page are overwritten.

*Note:* The bus controller sends from 1 to N bytes of data, each of which is acknowledged by the device if write control ( $\overline{WC}$ ) is low. If write control ( $\overline{WC}$ ) is high, the contents of the addressed memory location are not modified, and each data byte received by the device is not acknowledged, as shown in Figure 6. After each byte is transferred, the internal byte address counter is incremented. The transfer is terminated by the bus controller generating a stop condition.

**Figure 6. Write mode sequences with  $\overline{WC} = 1$  (data write inhibited)**



DT02803dV1

### 4.1.3 Write identification page

The identification page (16 bytes) is an additional page which can be written and (later) permanently locked in read-only mode. It is written by issuing the write identification page instruction. This instruction uses the same protocol and format as page write (into memory array), except for the following differences:

- Device type identifier = 1011b
- Most significant address bits A8/A4 are don't care, except for address bit A7 which must be "0". Least significant address bits A3/A0 define the byte location inside the identification page.

If the identification page is locked, the data bytes transferred during the write identification page instruction are not acknowledged (NoACK).

### 4.1.4 Lock identification page

The lock identification page instruction (lock ID) permanently locks the identification page in read-only mode. The lock ID instruction is similar to byte write (into memory array) with the following specific conditions:

- Device type identifier = 1011b

- Address bit A7 must be '1'; all other address bits are don't care
- The data byte must be equal to the binary value xxxx xx1x, where x is don't care

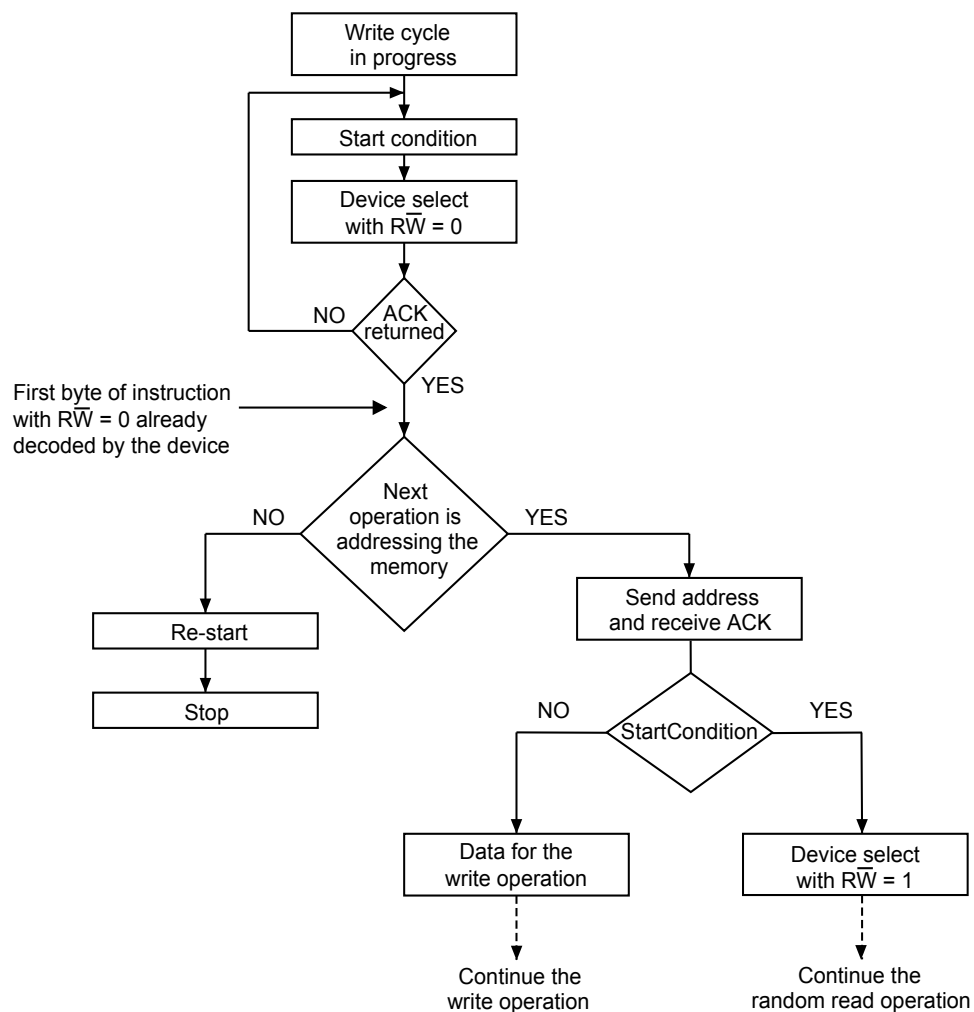
#### 4.1.5 Minimizing write delays by polling on ACK

The maximum write time ( $t_w$ ) is shown in AC characteristics tables in [Section 8: DC and AC parameters](#), but the typical time is shorter. To utilize this, a polling sequence can be used by the bus controller.

The sequence, as shown in [Figure 7](#), is:

- Initial condition: a write cycle is in progress.
- Step 1: the bus controller issues a start condition followed by a device select code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal write cycle, no ACK is returned and the bus controller goes back to step 1. If the device has terminated the internal write cycle, it responds with an ACK, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during step 1).

**Figure 7. Write cycle polling flowchart using ACK**



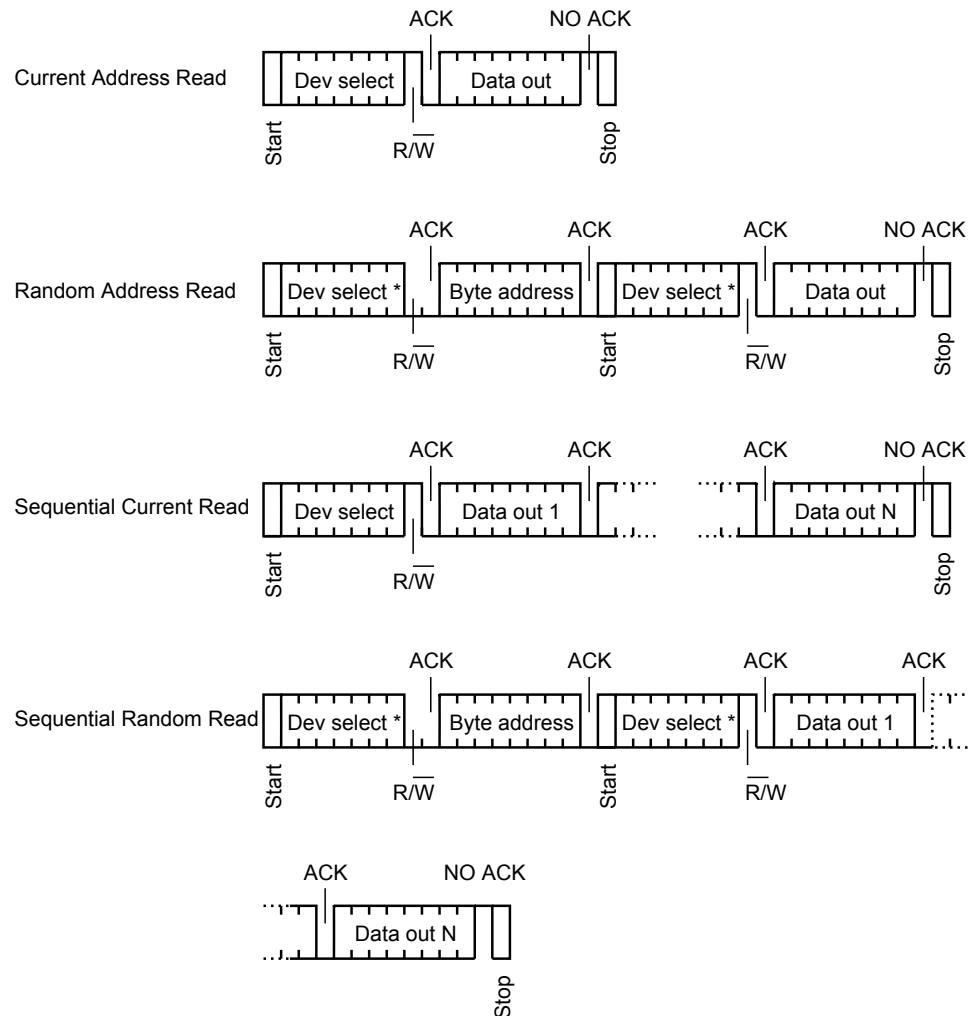
DT01847eV1

## 4.2 Read operations

Read operations are performed independently of the state of the write control ( $\overline{WC}$ ) signal.

After the successful completion of a read operation, the device internal address counter is incremented by one, to point to the next byte address.

**Figure 8. Read mode sequences**



DT01942bV1

### 4.2.1 Random address read

The random address read is a sequence composed of a truncated write sequence (to define a new address pointer value, see [Table 3](#)) followed by a current read.

The random address read sequence is therefore the sum of [start + device select code with R/W=0 + address byte] (without stop condition, as shown in [Figure 8](#)) and [start condition + device select code with R/W=1]. The memory device acknowledges the sequence and then outputs the contents of the addressed byte. To terminate the data transfer, the bus controller does not acknowledge the last data byte and then issues a stop condition.

### 4.2.2 Current address read

For the current address read operation, following a start condition, the bus controller only sends a device select code with the R/W bit set to 1. The device acknowledges this, and outputs the byte pointed by the internal address counter. The counter is then incremented. The bus controller terminates the transfer with a stop condition, as shown in [Figure 8](#), without acknowledging the byte.

Note that the address counter value is defined by instructions accessing either the memory or the identification page. When accessing the identification page, the address counter value is loaded with the identification page byte location, when accessing the memory, it is safer to always use the random address read instruction (this instruction loads the address counter with the byte location to read in the memory) instead of the current address read instruction.

#### 4.2.3 Sequential read

A sequential read can be used after a current address read or a random address read.

After a read instruction, the device can continue to output the next byte(s) in sequence if the bus controller sends additional clock pulses and if the bus controller does acknowledge each transmitted data byte. To terminate the stream of bytes, the bus controller must not acknowledge the last byte, and must generate a stop condition, as shown in [Figure 8](#).

The sequential read is controlled with the device internal address counter which is automatically incremented after each byte output. After the last memory address, the address counter rolls-over, and the device continues to output data from memory address 00h.

#### 4.2.4 Read identification page

The identification page can be read by issuing a read identification page instruction. This instruction uses the same protocol and format as the random address read (from memory array) with device type identifier defined as 1011b. The most significant address bits A8/A4 are don't care except bit A7 which must be 0, the least significant address bits A3/A0 define the byte location inside the identification page. The number of bytes to read in the ID page must not exceed the page boundary.

#### 4.2.5 Read the lock status

The locked/unlocked status of the identification page can be checked by transmitting a specific truncated command [identification page write instruction + one data byte] to the device. The device returns an acknowledge bit after the data byte if the identification page is unlocked, otherwise a NoACK bit if the identification page is locked.

Right after this, it is recommended to transmit to the device a start condition followed by a stop condition, so that:

- Start: the truncated command is not executed because the start condition resets the device internal logic,
- Stop: the device is then set back into standby mode by the stop condition.

#### 4.2.6 Acknowledge in read mode

For all read instructions, the device waits, after each byte sent out, for an acknowledgment from the bus controller during the ninth bit time slot. If the bus controller does not send the acknowledge (the controller drives SDA high during the ninth bit time), the device terminates the data transfer and enters its standby mode.

## 5 Application design recommendations

### 5.1 Supply voltage

#### 5.1.1 Operating supply voltage ( $V_{CC}$ )

Prior to selecting the memory and issuing instructions to it, a valid and stable  $V_{CC}$  voltage within the specified [ $V_{CC}(\min)$ ,  $V_{CC}(\max)$ ] range must be applied (see [Table 6](#)).

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a write instruction, until the completion of the internal write cycle ( $t_W$ ). To secure a stable DC supply voltage, it is recommended to decouple the  $V_{CC}$  line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the  $V_{CC}/V_{SS}$  package pins.

#### 5.1.2 Power-up conditions

When the power supply is turned on, the  $V_{CC}$  voltage has to rise continuously from 0 V up to the minimum  $V_{CC}$  operating voltage defined in [Table 6](#).

To prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included.

At power-up, the device does not respond to any instruction until  $V_{CC}$  reaches the internal threshold voltage (this threshold is defined in the DC characteristic [Table 10](#) as  $V_{RES}$ ).

When  $V_{CC}$  passes over the POR threshold, the device is reset and in the following state:

- In the standby power mode
- Deselected

As soon as the  $V_{CC}$  voltage has reached a stable value within the [ $V_{CC}(\min)$ ,  $V_{CC}(\max)$ ] range (defined in [Table 6](#)), the device is ready for operation.

#### 5.1.3 Power-down

During power-down (continuous decrease in the  $V_{CC}$  supply voltage below the minimum  $V_{CC}$  operating voltage defined in [Table 6](#)), the device must be in standby power mode (that is after a stop condition or after the completion of the write cycle  $t_W$  if an internal write cycle is in progress).

### 5.2 Error correction code (ECC x 1)

The error correction code (ECC x 1) is an internal logic function which is transparent for the I<sup>2</sup>C communication protocol.

The ECC x 1 logic is implemented on each byte of the memory array. If a single bit out of the byte happens to be erroneous during a read operation, the ECC x 1 detects this bit and replaces it with the correct value. The read reliability is therefore much improved.



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## 6 Delivery state

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The device is delivered as follows:

- The memory array is set to all 1s (each byte = FFh).
- Identification page: the first three bytes define the device identification code (value defined in [Table 4](#)). The content of the following bytes is don't care.

## 7 Maximum rating

Stressing the device outside the ratings listed in Table 5 may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 5. Absolute maximum ratings**

Symbol	Parameter	Min.	Max.	Unit
-	Ambient operating temperature	-40	130	°C
T <sub>STG</sub>	Storage temperature	-65	150	°C
T <sub>LEAD</sub>	Lead temperature during soldering	See note <sup>(1)</sup>		°C
V <sub>IO</sub>	Input or output range	-0.50	6.5	V
I <sub>OL</sub>	DC output current (SDA = 0)	-	5	mA
V <sub>CC</sub>	Supply voltage	-0.50	6.5	V
V <sub>ESD</sub>	Electrostatic pulse (human body model) <sup>(2)</sup>	-	4000	V

1. Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb-free assembly), the ST ECOPACK 7191395 specification, and the European directive on restrictions on hazardous substances (RoHS directive 2011/65/EU of July 2011).
2. Positive and negative pulses applied on pin pairs, according to AEC-Q100-002 (compliant with ANSI/ESDA/JEDEC JS-001-2012, C1=100 pF, R1=1500 Ω, R2=500 Ω).

## 8 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device.

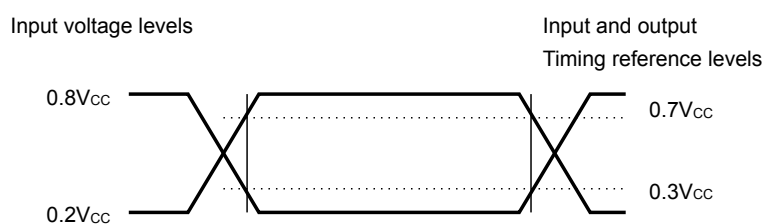
**Table 6. Operating conditions (voltage range)**

Symbol	Parameter	Min.	Max.	Unit
$V_{CC}$	Supply voltage	1.7	5.5	V
$T_A$	Ambient operating temperature	-40	125	°C

**Table 7. AC measurement conditions**

Symbol	Parameter	Min.	Max.	Unit
$C_{bus}$	Load capacitance	-	100	pF
-	SCL input rise/fall time, SDA input fall time	-	50	ns
-	Input levels	$0.2 V_{CC}$ to $0.8 V_{CC}$		V
-	Input and output timing reference levels	$0.3 V_{CC}$ to $0.7 V_{CC}$		V

**Figure 9. AC measurement I/O waveform**



DT19774V1

**Table 8. Input parameters**

Symbol	Parameter <sup>(1)</sup>	Test condition	Min.	Max.	Unit
C <sub>IN</sub>	Input capacitance (SDA)	-	-	8	pF
C <sub>IN</sub>	Input capacitance (other pins)	-	-	6	pF
Z <sub>L</sub>	Input impedance ( $\overline{WC}$ )	V <sub>IN</sub> < 0.3 V <sub>CC</sub>	30	-	kΩ
Z <sub>H</sub>		V <sub>IN</sub> > 0.7 V <sub>CC</sub>	500	-	kΩ

1. Evaluated by characterization - Not tested in production.

**Table 9. Cycling performance**

Symbol	Parameter	Test condition	Min.	Max.	Unit
Ncycle	Write cycle endurance	TA ≤ 25 °C, 1.7 V < V <sub>CC</sub> < 5.5 V	-	4,000,000	Write cycle <sup>(1)</sup>
		TA = 85 °C, 1.7 V < V <sub>CC</sub> < 5.5 V	-	1,200,000	
		TA = 125 °C, 1.7 V < V <sub>CC</sub> < 5.5 V	-	600,000	

1. A Write cycle is executed when either a Page Write, a Byte Write, a Write Identification Page or a Lock Identification Page instruction is decoded.

**Table 10. DC characteristics**

Symbol	Parameter	Test conditions (in addition to those in Table 6 and Table 7)	Min.	Max.	Unit
$I_{LI}$	Input leakage current (SCL, SDA, Ei)	$V_{IN} = V_{SS}$ or $V_{CC}$ , device in standby mode	-	$\pm 2$	$\mu A$
$I_{LO}$	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: $V_{SS}$ or $V_{CC}$	-	$\pm 2$	$\mu A$
$I_{CC}$	Supply current (Read)	$f_C = 400 \text{ kHz}$ , $V_{CC} = 5.5 \text{ V}$	-	2	mA
		$f_C = 400 \text{ kHz}$ , $V_{CC} = 2.5 \text{ V}$	-	2	mA
		$f_C = 400 \text{ kHz}$ , $V_{CC} = 1.7 \text{ V}$	-	1	mA
		$f_C = 1 \text{ MHz}$ , $V_{CC} = 5.5 \text{ V}$	-	2	mA
		$f_C = 1 \text{ MHz}$ , $V_{CC} = 2.5 \text{ V}$	-	2	mA
		$f_C = 1 \text{ MHz}$ , $V_{CC} = 1.7 \text{ V}$	-	2	mA
$I_{CC0}$	Supply current (Write)	During $t_W$	-	2	mA
$I_{CC1}$	Standby supply current	Device not selected <sup>(1)</sup> , $t^\circ = 85^\circ C$ , $V_{IN} = V_{SS}$ or $V_{CC}$ , $V_{CC} = 1.7 \text{ V}$	-	1	$\mu A$
		Device not selected <sup>(1)</sup> , $t^\circ = 85^\circ C$ , $V_{IN} = V_{SS}$ or $V_{CC}$ , $V_{CC} = 2.5 \text{ V}$	-	2	$\mu A$
		Device not selected <sup>(1)</sup> , $t^\circ = 85^\circ C$ , $V_{IN} = V_{SS}$ or $V_{CC}$ , $V_{CC} = 5.5 \text{ V}$	-	3	$\mu A$
		Device not selected <sup>(1)</sup> , $t^\circ = 125^\circ C$ , $V_{IN} = V_{SS}$ or $V_{CC}$ , $V_{CC} = 1.7 \text{ V}$	-	15	$\mu A$
		Device not selected <sup>(1)</sup> , $t^\circ = 125^\circ C$ , $V_{IN} = V_{SS}$ or $V_{CC}$ , $V_{CC} = 2.5 \text{ V}$	-	15	$\mu A$
		Device not selected <sup>(1)</sup> , $t^\circ = 125^\circ C$ , $V_{IN} = V_{SS}$ or $V_{CC}$ , $V_{CC} = 5.5 \text{ V}$	-	20	$\mu A$
$V_{IL}$	Input low voltage (SCL, SDA, $\overline{WC}$ , Ei) <sup>(2)</sup>	-	-0.45	$0.3 V_{CC}$	V
$V_{IH}$	Input high voltage (SCL, SDA)	-	$0.7 V_{CC}$	6.5	V
	Input high voltage ( $\overline{WC}$ , Ei) <sup>(3)</sup>	-	$0.7 V_{CC}$	$V_{CC} + 0.6$	V
$V_{OL}$	Output low voltage	$I_{OL} = 2.1 \text{ mA}$ , $V_{CC} = 2.5 \text{ V}$ or $I_{OL} = 3 \text{ mA}$ , $V_{CC} = 5.5 \text{ V}$	-	0.4	V
		$I_{OL} = 1 \text{ mA}$ , $V_{CC} = 1.7 \text{ V}$	-	0.3	V
$V_{RES}$ <sup>(4)</sup>	Internal reset threshold voltage	-	0.5	1.5	V

1. The device is not selected after power-up, after a read instruction (after the stop condition), or after the completion of the internal write cycle  $t_W$  ( $t_W$  is triggered by the correct decoding of a write instruction).
2. Ei inputs should be tied to  $V_{SS}$  (see Section 2.3).
3. Ei inputs should be tied to  $V_{CC}$  (see Section 2.3).
4. Evaluated by characterization - Not tested in production.

**Table 11. 400 kHz AC characteristics**

Symbol	Alt.	Parameter	Min.	Max.	Unit
$f_C$	$f_{SCL}$	Clock frequency	-	400	kHz
$t_{CHCL}$	$t_{HIGH}$	Clock pulse width high	600	-	ns
$t_{CLCH}$	$t_{LOW}$	Clock pulse width low	1300	-	ns
$t_{QL1QL2}^{(1)}$	$t_F$	SDA (out) fall time <sup>(2)</sup>	20	120	ns
$t_{XH1XH2}$	$t_R$	Input signal rise time	(3)	(3)	ns
$t_{XL1XL2}$	$t_F$	Input signal fall time	(3)	(3)	ns
$t_{DXCH}$	$t_{SU:DAT}$	Data in set up time	100	-	ns
$t_{CLDX}$	$t_{HD:DAT}$	Data in hold time	0	-	ns
$t_{CLQX}^{(4)}$	$t_{DH}$	Data out hold time	100	-	ns
$t_{CLQV}^{(5)}$	$t_{AA}$	Clock low to next data valid (access time)	-	900	ns
$t_{CHDL}$	$t_{SU:STA}$	Start condition setup time	600	-	ns
$t_{DLCL}$	$t_{HD:STA}$	Start condition hold time	600	-	ns
$t_{CHDH}$	$t_{SU:STO}$	Stop condition set up time	600	-	ns
$t_{DHDL}$	$t_{BUF}$	Time between Stop condition and next Start condition	1300	-	ns
$t_{WLDL}^{(1)(6)}$	$t_{SU:WC}$	$\overline{WC}$ set up time (before the start condition)	0	-	$\mu s$
$t_{DHWH}^{(1)(7)}$	$t_{HD:WC}$	$\overline{WC}$ hold time (before the stop condition)	1	-	$\mu s$
$t_W$	$t_{WR}$	Write time	-	4	ms
$t_{NS}^{(1)}$	-	Pulse width ignored (input filter on SCL and SDA) - single glitch	-	80	ns

1. Evaluated by characterization - Not tested in production.

2. With  $C_L = 10$  pF.

3. There is no minimum or maximum values for the input signal rise and fall times. It is however recommended by the I<sup>2</sup>C specification that the input signal rise and fall times be more than 20 ns and less than 300 ns when  $f_C < 400$  kHz.

4. To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.

5.  $t_{CLQV}$  is the time (from the falling edge of SCL) required by the SDA bus line to reach either 0.3V<sub>CC</sub> or 0.7V<sub>CC</sub>, assuming that  $R_{bus} \times C_{bus}$  time constant is within the values specified in Figure 10.

6.  $\overline{WC}=0$  set up time condition to enable the execution of a write command.

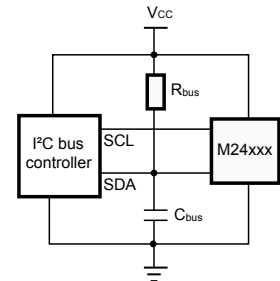
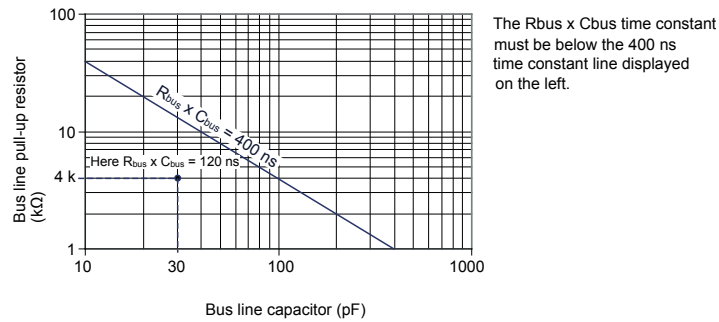
7.  $\overline{WC}=0$  hold time condition to enable the execution of a write command.

**Table 12. 1 MHz AC characteristics**

Symbol	Alt.	Parameter	Min.	Max.	Unit
$f_C$	$f_{SCL}$	Clock frequency	0	1	MHz
$t_{CHCL}$	$t_{HIGH}$	Clock pulse width high	260	-	ns
$t_{CLCH}$	$t_{LOW}$	Clock pulse width low	500	-	ns
$t_{XH1XH2}$	$t_R$	Input signal rise time	(1)	(1)	ns
$t_{XL1XL2}$	$t_F$	Input signal fall time	(1)	(1)	ns
$t_{QL1QL2}^{(2)}$	$t_F$	SDA (out) fall time	20	120	ns
$t_{DXCH}$	$t_{SU:DAT}$	Data in setup time	50	-	ns
$t_{CLDX}$	$t_{HD:DAT}$	Data in hold time	0	-	ns
$t_{CLQX}^{(3)}$	$t_{DH}$	Data out hold time	100	-	ns
$t_{CLQV}^{(4)}$	$t_{AA}$	Clock low to next data valid (access time)	-	450	ns
$t_{CHDL}$	$t_{SU:STA}$	Start condition setup time	250	-	ns
$t_{DLCL}$	$t_{HD:STA}$	Start condition hold time	250	-	ns
$t_{CHDH}$	$t_{SU:STO}$	Stop condition setup time	250	-	ns
$t_{DHDL}$	$t_{BUF}$	Time between Stop condition and next Start condition	500	-	ns
$t_{WLDL}^{(2)(5)}$	$t_{SU:WC}$	$\overline{WC}$ set up time (before the Start condition)	0	-	$\mu s$
$t_{DHWL}^{(2)(6)}$	$t_{HD:WC}$	$\overline{WC}$ hold time (after the Stop condition)	1	-	$\mu s$
$t_W$	$t_{WR}$	Write time	-	4	ms
$t_{NS}^{(2)}$	-	Pulse width ignored (input filter on SCL and SDA)	-	80	ns

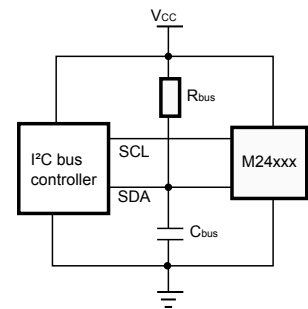
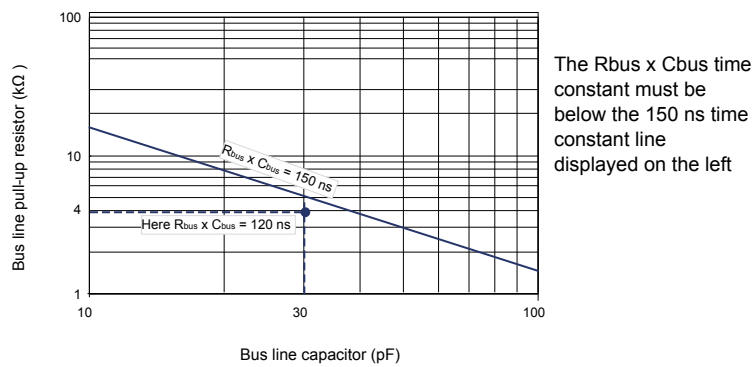
1. There is no minimum or maximum values for the input signal rise and fall times. However, it is recommended by the I<sup>2</sup>C specification that the input signal rise and fall times be more than 20 ns and less than 120 ns when  $f_C < 1$  MHz.
2. Evaluated by characterization - Not tested in production.
3. To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
4.  $t_{CLQV}$  is the time (from the falling edge of SCL) required by the SDA bus line to reach either 0.3  $V_{CC}$  or 0.7  $V_{CC}$ , assuming that the  $R_{bus} \times C_{bus}$  time constant is within the values specified in Figure 11.
5.  $\overline{WC}=0$  set up time condition to enable the execution of a WRITE command.
6.  $\overline{WC}=0$  hold time condition to enable the execution of a WRITE command.

**Figure 10. Maximum  $R_{bus}$  value versus bus parasitic capacitance ( $C_{bus}$ ) for an I<sup>2</sup>C bus at maximum frequency  $f_C = 400$  kHz**



DT14796

**Figure 11. Maximum  $R_{bus}$  value versus bus parasitic capacitance ( $C_{bus}$ ) for an I<sup>2</sup>C bus at maximum frequency  $f_C = 1$  MHz**



DT19745



### Figure 12. AC waveforms



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## **9 Package mechanical data**

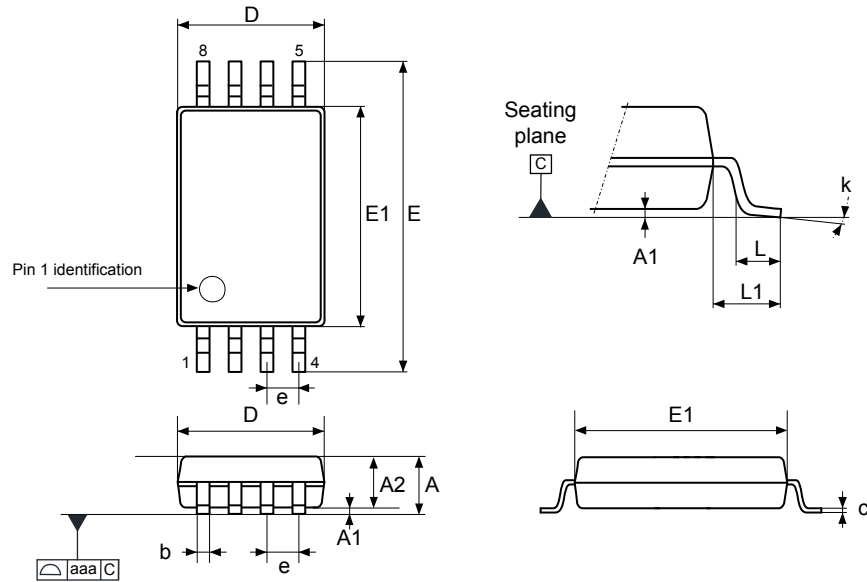
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In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

## 9.1 TSSOP8 package information

This TSSOP is an 8-lead, 3 x 6.4 mm, 0.65 mm pitch, thin shrink small outline package.

**Figure 13. TSSOP8 – Outline**



DT\_6P\_A\_TSSOP8\_ME\_V4

1. Drawing is not to scale.

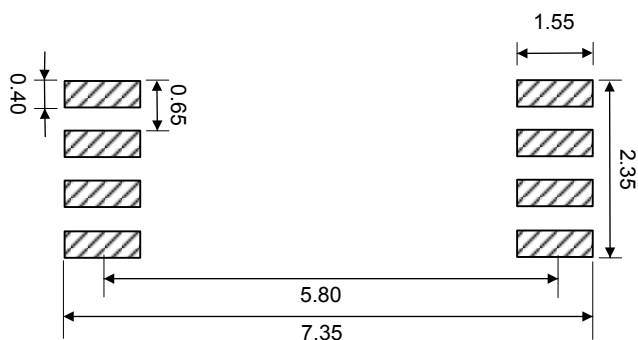
**Table 13. TSSOP8 - Mechanical data**

Symbol	millimeters			inches <sup>(1)</sup>		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
D <sup>(2)</sup>	2.900	3.000	3.100	0.1142	0.1181	0.1220
e	-	0.650	-	-	0.0256	-
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1 <sup>(3)</sup>	4.300	4.400	4.500	0.1693	0.1732	0.1772
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimension D does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
3. Dimension E1 does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.

**Note:** The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of the mold flash, tie bar burrs, gate burrs, and interleads flash, but including any mismatch between the top and bottom of the plastic body. The measurement side for the mold flash, protrusions, or gate burrs is the bottom side.

**Figure 14. TSSOP8 – Footprint example**



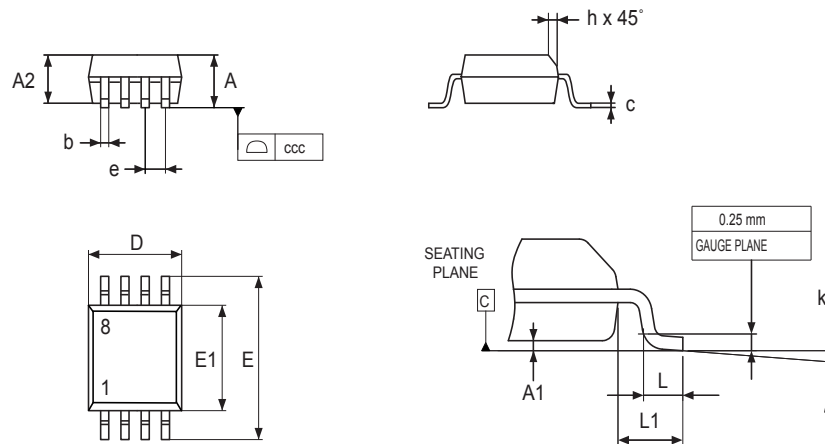
DT\_6P\_TSSOP8\_FP\_V2

1. Dimensions are expressed in millimeters.

## 9.2 SO8N package information

This SO8N is an 8-lead, 4.9 x 6 mm, plastic small outline, 150 mils body width, package.

**Figure 15. SO8N - Outline**



07\_SO8\_ME\_V2

1. Drawing is not to scale.

**Table 14. SO8N - Mechanical data**

Symbol	millimeters			inches <sup>(1)</sup>		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.750	-	-	0.0689
A1	0.100	-	0.250	0.0039	-	0.0098
A2	1.250	-	-	0.0492	-	-
b	0.280	-	0.480	0.0110	-	0.0189
c	0.170	-	0.230	0.0067	-	0.0091
D <sup>(2)</sup>	4.800	4.900	5.000	0.1890	0.1929	0.1969
E	5.800	6.000	6.200	0.2283	0.2362	0.2441
E1 <sup>(3)</sup>	3.800	3.900	4.000	0.1496	0.1535	0.1575
e	-	1.270	-	-	0.0500	-
h	0.250	-	0.500	0.0098	-	0.0197
k	0°	-	8°	0°	-	8°
L	0.400	-	1.270	0.0157	-	0.0500
L1	-	1.040	-	-	0.0409	-
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal digits.

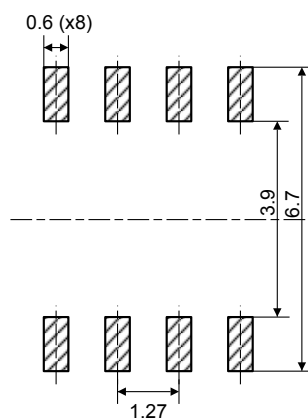
2. Dimension D does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side

3. Dimension E1 does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.

**Note:**

The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interleads flash, but including any mismatch between the top and bottom of the plastic body. The measurement side for mold flash, protrusions, or gate burrs is the bottom side.

**Figure 16. SO8N - Footprint example**



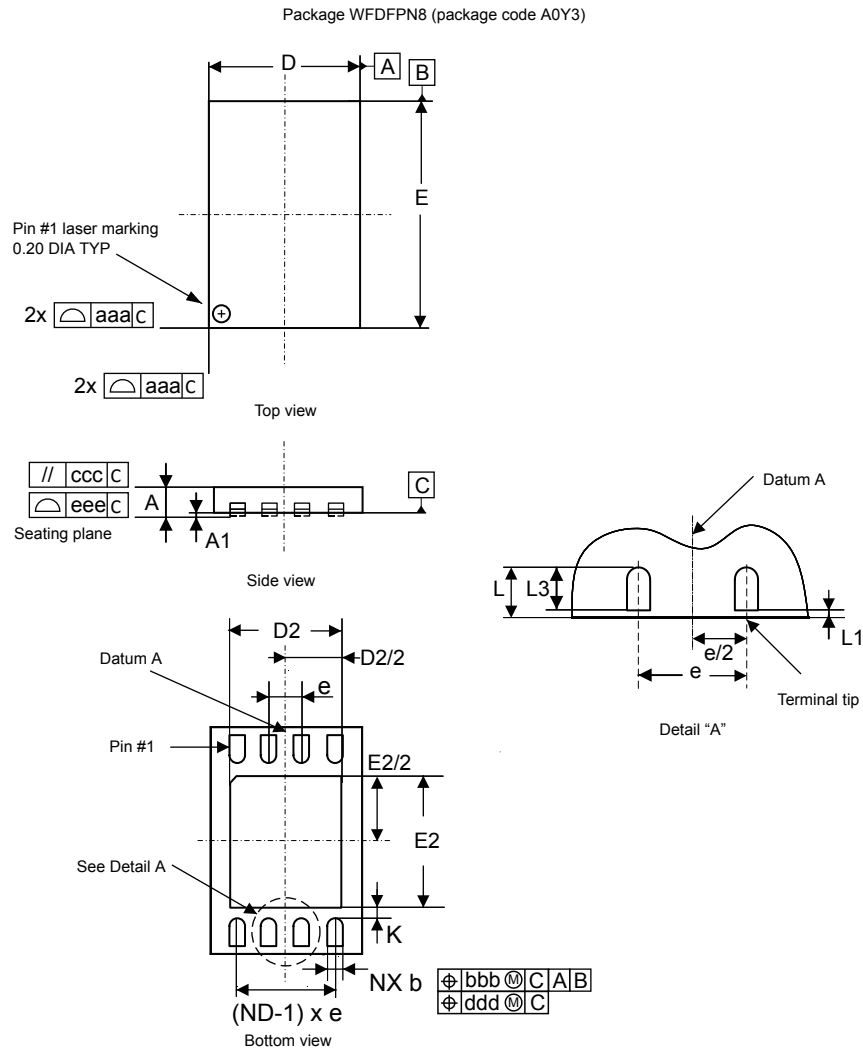
07\_SO8N\_FP\_V2

1. Dimensions are expressed in millimeters.

### 9.3 WFDFPN8 (DFN8) package information

This WFDFPN is a 8-lead, 2 x 3 mm, 0.5 mm pitch very very thin fine pitch dual flat package.

**Figure 17. WFDFPN8 (DFN8) – Outline**

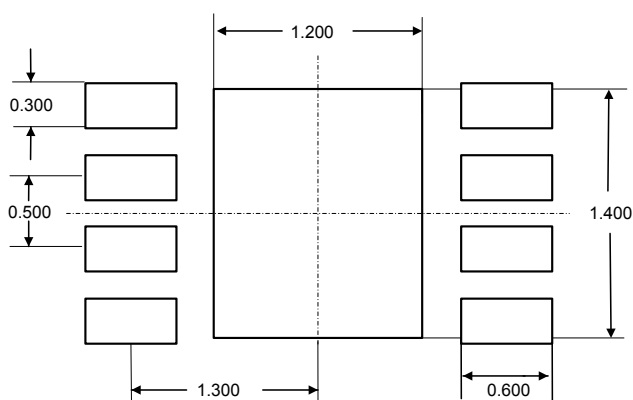


1. Drawing is not to scale.
2. Exposed copper is not systematic and can appear partially or totally according to the cross section.

**Table 15. WFDFPN8 (DFN8) – Mechanical data**

Symbol	millimeters			inches <sup>(1)</sup>		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.700	0.750	0.800	0.0276	0.0295	0.0315
A1	0.025	0.045	0.065	0.0010	0.0018	0.0026
b <sup>(2)</sup>	0.200	0.250	0.300	0.0079	0.0098	0.0118
D	1.900	2.000	2.100	0.0748	0.0787	0.0827
E	2.900	3.000	3.100	0.1142	0.1181	0.1220
e	-	0.500	-	-	0.0197	-
L1	-	-	0.150	-	-	0.0059
L3	0.300	-	-	0.0118	-	-
D2	1.400	-	1.600	0.0551	-	0.0630
E2	1.200	-	1.400	0.0472	-	0.0551
K	0.400	-	-	0.0157	-	-
L	0.300	-	0.500	0.0118	-	0.0197
NX <sup>(3)</sup>	8					
ND <sup>(3)</sup>	4					
aaa	-	-	0.150	-	-	0.0059
bbb <sup>(4)</sup>	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee <sup>(5)</sup>	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimension b applies to plated terminal and is measured between 0.15 and 0.30 mm from the terminal tip.
3. N is the number of terminals, ND is the number of terminals on "D" sides.
4. Max package warpage is 0.05 mm.
5. Applied for exposed die paddle and terminals. Exclude embedding part of exposed die paddle from measuring.

**Figure 18. WFDFPN8 (DFN8) – Footprint example**


**Note:** The central pad (the area E2 by D2 in the [Figure 17](#)) must be either connected to  $V_{SS}$  or left floating (not connected) in the end application.



## 10 Ordering information

**Table 16. Ordering information scheme**

Example:	M24	C04-D	R	MN	3	T	P	/K
<b>Device type</b>								
M24 = I2C serial access EEPROM								
<b>Device function</b>								
C04-D = 4 Kbits (512 x 8 bits) plus identification page								
<b>Operating voltage</b>								
R = $V_{CC} = 1.7\text{ V to }5.5\text{ V}$								
<b>Package<sup>(1)</sup></b>								
MN = SO8 (150 mil width)								
DW = TSSOP8 (169 mil width)								
MF = WDFPN8 (DFN8)								
<b>Device grade</b>								
3 = -40 to 125 °C. Automotive grade.								
<b>Option</b>								
T = Tape and reel packing								
blank = tube packing								
<b>Planting technology</b>								
P or G = ECOPACK2®								
<b>Process</b>								
/K = Manufacturing technology code								

1. All packages are ECOPACK2® (RoHS compliant and free of brominated, chlorinated and antimonyoxide flame retardants).

**Note:** For a list of available options (speed, package, etc.) or for further information on any aspect of the devices, please contact your nearest ST sales office.

### Engineering samples

Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

## Revision history

**Table 17. Document revision history**

Date	Revision	Changes
22-May-2014	1	Initial release.
18-Aug-2014	2	Changed product maturity from target spec to preliminary data.
17-Sep-2014	3	Changed product maturity from Preliminary to Production data. Updated Package information on Cover page. Updated Table 15. and Table 16
07-Jan-2015	4	Updated: <ul style="list-style-type: none"> <li>Note 2 on Table 5</li> <li>Figure 17</li> <li>Table 10 and Table 15</li> </ul> Added sentence about Engineering sample on Section 10.
15-Mar-2016	5	Updated: <ul style="list-style-type: none"> <li>Features</li> <li>Table 9. Cycling performance, Table 10, Table 16</li> </ul>
24-Jan-2019	6	Updated: <ul style="list-style-type: none"> <li>WLCSP8 package definition from MLP8 to DFN8</li> <li>Table 15. WFDFPN8 (DFN8) – Mechanical data</li> </ul>
31-Oct-2024	7	Updated: <ul style="list-style-type: none"> <li>Section Features</li> <li>Section 9.3: WFDFPN8 (DFN8) package information</li> <li>Section 10: Ordering information</li> </ul>

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