Li-Ion Switching Charger, High Efficiency, 1.55 A, with Integrated Power Path, USB-OTG, in a Small Solution Size

FAN54063

WLCSP25
CASE 567SQ

MARKING DIAGRAM

__ = Lot Code
X = Year Code
Y = 2 Weeks Code
Z = Plant/Site Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Description

The FAN54063 is a 1.55 A USB−compliant switch−mode charger featuring integrated power path operation, USB OTG boost support, JEITA temperature control, and production test mode support, in a small 25 bump, 0.4 mm pitch WLCSP package.

To facilitate fast system startup, the IC includes an integrated power path circuit, which disconnects the battery from the system rail, ensuring that the system can power up quickly following a VBUS connection. The power path circuit ensures that the system rail stays up when the charger is plugged in, even if the battery is dead.

The charging parameters and operating modes are programmable through an I^2C Interface that operates up to 3.4 Mbps. The charger and boost regulator circuits switch at 3 MHz to minimize the size of external passive components.

The FAN54063 provides battery charging in three phases: conditioning, constant current and constant voltage. The IC automatically restarts the charge cycle when the battery falls below a voltage threshold. If the input source is removed, the IC enters a high−impedance mode blocking battery current from leaking to the input. Charger status is reported back to the host through the I^2C port.

Dynamic input voltage control prevents a weak adapter's voltage from collapsing, ensuring charging capability from such adapters.

The FAN54063 is available in a space saving 2.4 mm x 2.0 mm WLCSP package.

Features

- Fully Integrated, High−Efficiency Switch−Mode Charger for Single−Cell Li−Ion and Li−Polymer Batteries
- Integrated Power Path Circuit Ensures Fast System Startup with a Dead Battery when VBUS is Connected
- 1.55 A Maximum Charge Current
- Programmable High Accuracy Float Voltage:
  - ♦ ±0.5% at 25°C
  - ♦ ±1% from 0 to 125°C
- ±5% Input and Charge Current Regulation Accuracy
- Temperature−Sense Input for JEITA Compliance
- Thermal Regulation and Shutdown
- 4.2 V at 2.3 A Production Test Support
- 5 V, 500 mA Boost Mode for USB OTG

Features (continued)

- 28 V Absolute Maximum Input Voltage
- 6 V Maximum Input Operating Voltage
- Programmable through High−Speed I^2C Interface (3.4 Mb/s) with Fast Mode Plus Compatibility
  - ♦ Input Current
  - ♦ Fast−Charge / Termination Current
  - ♦ Float Voltage
  - ♦ Termination Enable
- 3 MHz Synchronous Buck PWM Controller with Wide Duty Cycle Range
- Small Footprint 1 μH External Inductor
- Safety Timer with Reset Control
- Dynamic Input Voltage Control
- Very Low Battery Current when Charger Inactive

Applications

- Cell Phones, Smart Phones, PDAs
- Tablet, Portable Media Players
- Gaming Device, Digital Cameras

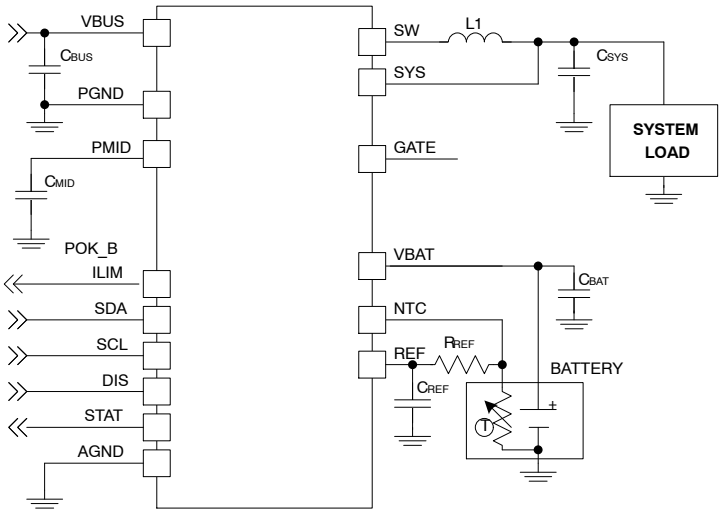


Figure 1. Typical Application

ORDERING INFORMATION

Part Number	Temperature Range	Package	PN Bits: IC_INFO[5:3]	Packing Method
FAN54063UCX	−40 to 85°C	25−Bump, Wafer−Level Chip−Scale Package (WLCSP), 0.4 mm Pitch	010	Tape and Reel

Table 1. FEATURE SUMMARY

Part Number	Slave Address	Automatic Charge	Battery Absent Behavior	E1 Pin	Watchdog Timer Default
FAN54063	1101011	No	On	POK_B	Disabled

Block Diagram

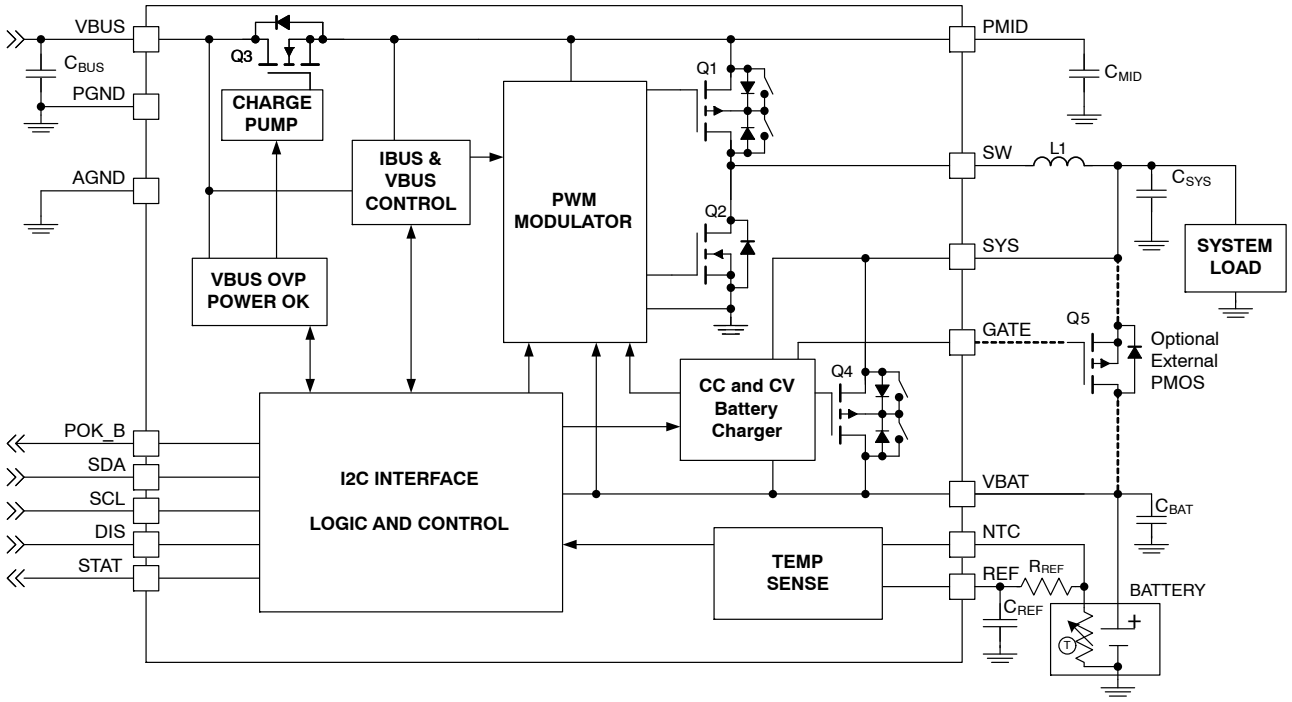


Figure 2. IC and System Block Diagram

Table 2. RECOMMENDED EXTERNAL COMPONENTS

Component	Description	Vendor	Parameter	Typ.	Unit
L1	1 μH, 20%, 4.0 A, 2016	Semco CIGT201610EH1R0M or Equivalent	L	1.0	μH
			DCR (series R)	33	mΩ
C_{BAT}, C_{SYS}	10 μF, 20%, 6.3 V, X5R, 0603	Murata: GRM188R60J106M TDK: C1608X5R0J106M	C	10	μF
C_{MID}	4.7 μF, 10%, 10 V, X5R, 0603	Murata: GRM188R61A475K TDK: C1608X5R1A475K	C (Note 1)	4.7	μF
C_{BUS},	1.0 μF, 10%, 25 V, X5R, 0603	Murata GRM188R61E105K TDK:C1608X5R1E105M	C	1.0	μF
C_{REF}	1 μF, 10%, 6.3 V, X5R, 0402		C	1.0	μF
Q5 (optional)	PMOS,12 V, 16 mΩ, MLP2x2	**onsemi** FDMA905P	$R_{DS(ON)}$	16	mΩ

1. 10 V rating is sufficient for C_{MID} since PMID is protected from over−voltage surges on VBUS by Q3.

Pin Configuration

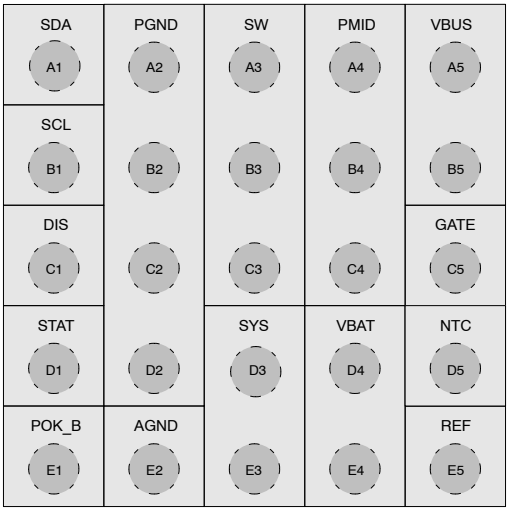


Figure 3. Top View

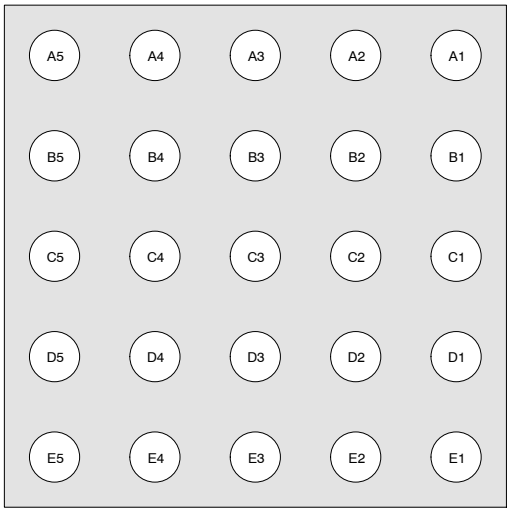


Figure 4. Bottom View

PIN DEFINITIONS

Pin #	Name	Description
A1	SDA	**I²C Interface Serial Data**. This pin should not be left floating
B1	SCL	**I²C Interface Serial Clock**. This pin should not be left floating
C1	DIS	**Disable**. If this pin is held HIGH, Q1 and Q3 are turned off; creating a HIGH Z condition at VBUS and the PWM converter is disabled
D1	STAT	**Status**. Open−drain output indicating charge status. The IC pulls this pin LOW when charge is in progress and is also used to signal the host processor when a fault condition occurs
E1	POK_B	**Power OK**. Open−drain output that pulls LOW when VBUS is plugged in and the battery has risen above V_{LOWV}. This signal is used to signal the host processor that it can begin to draw significant current
A2 – D2	PGND	**Power Ground**. Power return for gate drive and power transistors. The connection from this pin to the bottom of C_{MID} should be as short as possible
E2	AGND	**Analog Ground**. All IC signals are referenced to this node
A3 – C3	SW	**Switching Node**. Connect to output inductor
D3 – E3	SYS	**System Supply**. Output voltage of the switching charger and input to the power path controller. Bypass SYS to PGND with a 10 μF capacitor
A4 – C4	PMID	**Power Input Voltage**. Power input to the charger regulator, bypass point for the input current sense. Bypass with a minimum of a 4.7 μF, 6.3 V capacitor to PGND
D4 – E4	VBAT	**Battery Voltage**. Connect to the positive (+) terminal of the battery pack. Bypass with a 10 μF capacitor to PGND. VBAT is a power path connection
A5 – B5	VBUS	**Charger Input Voltage and USB−OTG Output Voltage**. Bypass with a 1 μF capacitor to PGND
C5	GATE	**External MOSFET Gate**. This pin controls the gate of an optional external P−channel MOSFET transistor used to augment the internal power−path FET (Q4) during battery discsharge. The source of the P−channel MOSFET should be connected to SYS and the drain should be connected to VBAT
D5	NTC	**Thermistor Input**. The IC compares this node with taps on a resistor divider from REF to inhibit auto−charging when the battery temperature is outside of permitted fast−charge limits
E5	REF	**Reference Voltage**. REF is a 1.8 V regulated output

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter			Min.	Max.	Unit
V_{BUS}	Voltage on VBUS Pin	Continuous		−0.3	28.0	V
		Pulsed, 100 ms Maximum Non−Repetitive		−1.0		
V_I	Voltage on PMID, SW, SYS, VBAT, STAT, DIS Pins			−0.3	7.0	V
V_O	Voltage on Other Pins			−0.3	6.5 (Note 2)	V
$\frac{\Delta V_{BUS}}{\Delta t}$	Maximum V_{BUS} Slope Above 5.5 V when Boost or Charger Active				4	V/μs
ESD	Electrostatic Discharge Protection Level	Human Body Model per JESD22−A114		2000		V
		Charged Device Model per JESD22−C101		500		
	IEC 61000−4−2 System ESD (Note 3)	USB Connector Pins (V_{BUS} to GND)	Air Gap	15		kV
			Contact	8		
T_J	Junction Temperature			−40	+150	°C
T_{STG}	Storage Temperature			−65	+150	°C
T_L	Lead Soldering Temperature, 10 Seconds				+260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Lesser of 6.5 V or V_I + 0.3 V.
3. Guaranteed if $C_{BUS} \geq 1$ μF and $C_{MID} \geq 4.7$ μF.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min.	Max.	Unit
V_{BUS}	Supply Voltage		4	6	V
$V_{BAT(MAX)}$	Maximum Battery Voltage when Boost enabled			4.5	V
$-\frac{\Delta V_{BUS}}{\Delta t}$	Negative VBUS Slew Rate during VBUS Short Circuit, $C_{MID} \leqq 4.7$ μF, see VBUS Short While Charging	$T_A \leqq 60°C$		4	V/μs
		$T_A \geqq 60°C$		2	
T_A	Ambient Temperature		−30	+85	°C
T_J	Junction Temperature (see Thermal Regulation and Shutdown)		−30	+120	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

THERMAL PROPERTIES

Junction−to−ambient thermal resistance is a function of application and board layout. This data is measured with four−layer 2s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperature T_A.

Symbol	Parameter	Typical	Unit
θ_{JA}	Junction−to−Ambient Thermal Resistance	50	°C/W
θ_{JB}	Junction−to−PCB Thermal Resistance	20	°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified: according to the circuit of Figure 1; recommended operating temperature range for T_J and T_A; V_{BUS} = 5.0 V; HZ_MODE = “0”; OPA_MODE = “0” (Charge Mode); SCL, SDA = 0 or 1.8 V; and typical values are for T_J = 25°C. Min. and Max. values are not tested in production, but are determined by characterization.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
POWER SUPPLIES						
I_{VBUS}	VBUS Current	PWM Switching		20		mA
		$V_{BAT} > V_{OREG}$ I_{BUSLIM} = 500 mA		6		mA
		0°C < T_J < 85°C, HZ_MODE = “1” or DIS pin HIGH, $V_{BAT} > V_{LOWV}$		190	280	μA
I_{BAT_HZ}	Battery Discharge Current in High−Impedance Mode	DIS pin HIGH, or HZ_MODE = “1”, V_{BAT}=4.35 V		<1.25	10.00	μA
I_{BUS_HZ}	Battery Leakage Current to V_{BUS} in High−Impedance Mode	DIS pin HIGH or HZ_MODE = “1”, V_{BAT} = 4.35 V, V_{BUS} Shorted to Ground	−5.0	−0.2		μA
CHARGER VOLTAGE REGULATION						
V_{OREG}	Charge Voltage Range		3.51		4.45	V
	Charge Voltage Accuracy	T_A = 25°C, V_{OREG} = 4.35 V	−0.5		+0.5	%
		T_J = 0 to 125°C	−1		+1	%
CHARGING CURRENT REGULATION (FAST CHARGE)						
I_{OCHRG}	Output Charge Current Range	IO_LEVEL = “0”	550		1550	mA
		IO_LEVEL = “1” (default)	165	200	230	mA
	Charge Current Accuracy	IO_LEVEL = “0”	−5		+5	%
WEAK BATTERY DETECTION						
V_{LOWV}	Weak Battery Threshold Range		3.4		3.7	V
	Weak Battery Threshold Accuracy		−5		+5	%
	Weak Battery Deglitch Time			32		ms
PWM CHARGING THRESHOLD						
V_{BATMIN}	Rising PWM Charging Threshold		3.1	3.2	3.3	V
$V_{BATFALL}$	Falling PWM Charging Threshold			3.0		V
LOGIC LEVELS: DIS, SDA, SCL						
V_{IH}	High−Level Input Voltage		1.05			V
V_{IL}	Low−Level Input Voltage				0.4	V
I_{IN}	Input Bias Current	Input Tied to GND or V_{BUS}		0.01	1.00	μA
R_{PD}	DIS Pull−Down Resistance	V_{DIS} = 0.4 V		300		kΩ
CHARGE TERMINATION DETECTION						
I_{TERM}	Termination Current Range		50		400	mA
	Termination Current Accuracy	I_{TERM} Setting ≤ 100 mA	−15		+15	%
		I_{TERM} Setting ≥ 200 mA	−5		+5	
	Termination Current Deglitch Time (Note 4)			32		ms

ELECTRICAL SPECIFICATIONS (continued)

Unless otherwise specified: according to the circuit of Figure 1; recommended operating temperature range for T_J and T_A; V_{BUS} = 5.0 V; HZ_MODE = “0”; OPA_MODE = “0” (Charge Mode); SCL, SDA = 0 or 1.8 V; and typical values are for T_J = 25°C. Min. and Max. values are not tested in production, but are determined by characterization.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
POWER PATH (Q4) CONTROL (PRECHARGE)						
I_{PP}	Power Path Maximum Charge Current	IO_LEVEL = “1” (default)	165	200	235	mA
		IO_LEVEL = “0”, IBUSLIM ≤ “01”	165	200	235	mA
		IO_LEVEL = “0”, IBUSLIM >“01”, IOCHARGE ≤ “02”	375	450	520	mA
		IO_LEVEL = “0”, IBUSLIM >“01”, IOCHARGE >“02”	610	730	840	mA
V_{THSYS}	VBAT to SYS Threshold for Q4 and Gate Transition While Charging	(SYS−VBAT) Falling	−6	−5	−3	mV
		(SYS−VBAT) Rising	−1	1	2	mV
PRODUCTION TEST MODE						
$V_{BAT(PTM)}$ (Note 4)	Production Test Output Voltage	1 mA < I_{BAT} < 2 A, V_{BUS} = 5.5 V	4.116	4.200	4.284	V
$I_{BAT(PTM)}$ (Note 4)	Production Test Output Current	20% Duty with Max. Period 10 ms	2.3			A
BATTERY TEMPERATURE MONITOR (NTC)						
T1	T1 (0°C) Temperature Threshold		71.9	73.9	75.9	% of V_{REF}
T2	T2 (10°C) Temperature Threshold		62.6	64.6	66.6	
T3	T3 (45°C) Temperature Threshold		31.9	32.9	34.9	
T4	T4 (60°C) Temperature Threshold		21.3	23.3	25.3	
INPUT POWER SOURCE DETECTION						
$V_{IN(MIN)1}$	VBUS Input Voltage Rising	To Initiate and Pass VBUS Validation		4.35	4.45	V
$V_{IN(MIN)2}$	Minimum VBUS during Charge	During Charging		3.71	3.94	V
t_{VBUS_VALID} (Note 4)	VBUS Validation Time			32		ms
V_{BUS} CONTROL LOOP						
V_{BUSLIM}	VBUS Loop Setpoint Accuracy		−3		+3	%
INPUT CURRENT LIMIT						
I_{BUSLIM}	Charger Input Current Limit Threshold	IBUSLIM = “00”	450	475	500	mA
		IBUSLIM = “01”		760		
		IBUSLIM = “10”	972	1080	1188	
V_{REF} BIAS GENERATOR						
V_{REF}	Bias Regulator Voltage	Charge Mode		1.8		V
	Short−Circuit Current Limit			2.5		mA
BATTERY RECHARGE THRESHOLD						
V_{RCH}	Recharge Threshold	V_{BAT} Below V_{OREG}	100	120	150	mV
	Deglitch Time	V_{BAT} Falling Below V_{RCH} Threshold		130		ms
STAT, POK_B OUTPUTS						
$V_{(OL)}$	Output Low	I_{SINK} = 10 mA			0.4	V
$I_{(OH)}$	Output High Leakage Current	V_{OUTPUT} = 5 V			1	μA

ELECTRICAL SPECIFICATIONS (continued)

Unless otherwise specified: according to the circuit of Figure 1; recommended operating temperature range for T_J and T_A; V_{BUS} = 5.0 V; HZ_MODE = "0"; OPA_MODE = "0" (Charge Mode); SCL, SDA = 0 or 1.8 V; and typical values are for T_J = 25°C. Min. and Max. values are not tested in production, but are determined by characterization.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BATTERY DETECTION						
I_{DETECT}	Battery Detection Current before Charge Done (Sink Current) (Note 5)	Begins after Termination Detected and $V_{BAT} \le V_{OREG} - V_{RCH}$		−1.9		mA
t_{DETECT}	Battery Detection Time			262		ms
SLEEP COMPARATOR						
V_{SLP}	Sleep−Mode Entry Threshold, $V_{BUS} - V_{BAT}$	$V_{IN(MIN)2} \le V_{BAT} \le V_{OREG}$, V_{BUS} Falling	0	0.04	0.10	V
POWER SWITCHES (see Figure 2)						
$R_{DS(ON)}$	Q3 On Resistance (VBUS to PMID)	I_{BUSLIM} = 500 mA		180	340	mΩ
	Q1 On Resistance (PMID to SW)			130	225	
	Q2 On Resistance (SW to GND)			150	225	
	Q4 On Resistance (SYS to VBAT)	V_{BAT} = 4.35 V		70	100	mΩ
I_{SYNC}	Synchronous to Non−Synchronous Current Cut−Off Threshold (Note 6)	Low−Side MOSFET (Q2) Cycle−by−Cycle Current Limit		180		mA
CHARGER PWM MODULATOR						
f_{SW}	Oscillator Frequency		2.7	3.0	3.3	MHz
D_{MAX}	Maximum Duty Cycle				100	%
D_{MIN}	Minimum Duty Cycle			0		%
BOOST MODE OPERATION (OPA_MODE=1)						
V_{BOOST}	Boost Output Voltage at VBUS	2.5 V < V_{BAT} < 4.5 V, I_{LOAD} from 0 to 200 mA	4.80	5.07	5.20	V
		3.0 V < V_{BAT} < 4.5 V, I_{LOAD} from 0 to 500 mA	4.77	5.07	5.20	
$I_{BAT(BOOST)}$	Boost Mode Quiescent Current	PFM Mode, V_{BAT} = 3.6 V, I_{LOAD} = 0 A		250	350	μA
$I_{LIMPK(BST)}$	Q2 Peak Current Limit		1550	1800	2100	mA
$UVLO_{BST}$	Minimum Battery Voltage for Boost Operation	While Boost Active		2.32		V
		To Start Boost Regulator		2.48	2.70	
VBUS LOAD RESISTANCE						
R_{VBUS}	VBUS to PGND Resistance	Normal Operation		500		kΩ
		VBUS Validation		100		Ω
PROTECTION AND TIMERS						
$VBUS_{OVP}$	VBUS Over−Voltage Shutdown	V_{BUS} Rising	6.09	6.29	6.49	V
	Hysteresis	V_{BUS} Falling		100		mV
$I_{LIMPK(CHG)}$	Q1 Cycle−by−Cycle Peak Current Limit	Charge Mode		3		A
V_{SHORT}	Battery Short−Circuit Threshold	V_{BAT} Rising	1.95	2.00	2.07	V
	Hysteresis			100		mV
I_{SHORT}	Linear Charging Current	V_{BAT} < V_{SHORT}		30		mA
$T_{SHUTDWN}$	Thermal Shutdown Threshold (Note 4)	T_J Rising		145		°C
	Hysteresis (Note 4)	T_J Falling		25		
T_{CF}	Thermal Regulation Threshold (Note 4)	Charge Current Reduction Begins		120		°C
t_{INT}	Detection Interval			2		s

ELECTRICAL SPECIFICATIONS (continued)
Unless otherwise specified: according to the circuit of Figure 1; recommended operating temperature range for T_J and T_A; V_{BUS} = 5.0 V; HZ_MODE = "0"; OPA_MODE = "0" (Charge Mode); SCL, SDA = 0 or 1.8 V; and typical values are for T_J = 25°C. Min. and Max. values are not tested in production, but are determined by characterization.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
PROTECTION AND TIMERS						
T_{32S}	32−Second Timer (Note 7)	Charger Enabled	20.5	25.2	28.0	s
		Charger Disabled	18.0	25.2	34.0	
Δt_{LF}	Low−Frequency Timer Accuracy	Charger Inactive	−23		27	%

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
4. Guaranteed by design; not tested in production.
5. Negative current is current flowing from the battery to ground (discharging the battery).
6. Q2 always turns on for 60 ns, then turns off if current is below I_{SYNC}.
7. This tolerance (%) applies to all timers on the IC, including soft−start and deglitching timers.

I^2C TIMING SPECIFICATIONS Guaranteed by design.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{SCL}	SCL Clock Frequency	Standard Mode			100	kHz
		Fast Mode			400	
		Fast Mode Plus			1000	
		High−Speed Mode, $C_B \leq$ 100 pF			3400	
		High−Speed Mode, $C_B \leq$ 400 pF			1700	
t_{BUF}	Bus−free Time between STOP and START Conditions	Standard Mode		4.7		µs
		Fast Mode		1.3		
		Fast Mode Plus		0.5		
$t_{HD;STA}$	START or Repeated START Hold Time	Standard Mode		4		s
		Fast Mode		600		ns
		Fast Mode Plus		260		ns
		High−Speed Mode		160		ns
t_{LOW}	SCL LOW Period	Standard Mode		4.7		µs
		Fast Mode		1.3		µs
		Fast Mode Plus		0.5		µs
		High−Speed Mode, C_B < 100 pF		160		ns
		High−Speed Mode, C_B < 400 pF		320		ns
t_{HIGH}	SCL HIGH Period	Standard Mode		4		µs
		Fast Mode		600		ns
		Fast Mode Plus		260		ns
		High−Speed Mode, C_B < 100 pF		60		ns
		High−Speed Mode, C_B < 400 pF		120		ns
$t_{SU;STA}$	Repeated START Setup Time	Standard Mode		4.7		µs
		Fast Mode		600		ns

I²C TIMING SPECIFICATIONS Guaranteed by design. (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
		Fast Mode Plus		260		ns
		High−Speed Mode		160		ns
$t_{SU;DAT}$	Data Setup Time	Standard Mode		250		ns
		Fast Mode		100		
		Fast Mode Plus		50		
		High−Speed Mode		10		
$t_{HD;DAT}$	Data Hold Time	Standard Mode	0		3.45	μs
		Fast Mode	0		900	ns
		Fast Mode Plus	0		450	ns
		High−Speed Mode, C_B < 100 pF	0		70	ns
		High−Speed Mode, C_B < 400 pF	0		150	ns
t_{RCL}	SCL Rise Time	Standard Mode	$20+0.1C_B$		1000	ns
		Fast Mode	$20+0.1C_B$		300	
		Fast Mode Plus	$20+0.1C_B$		120	
		High−Speed Mode, C_B < 100 pF		10	80	
		High−Speed Mode, C_B < 400 pF		20	160	
t_{FCL}	SCL Fall Time	Standard Mode	$20+0.1C_B$		300	ns
		Fast Mode	$20+0.1C_B$		300	
		Fast Mode Plus	$20+0.1C_B$		120	
		High−Speed Mode, C_B < 100 pF		10	40	
		High−Speed Mode, C_B < 400 pF		20	80	
t_{RCL1}	Rise Time of SCL after a Repeated START Condition and after ACK Bit	High−Speed Mode, C_B < 100 pF		10	80	ns
		High−Speed Mode, C_B < 400 pF		20	160	
t_{RDA}	SDA Rise Time	Standard Mode	$20+0.1C_B$		1000	ns
		Fast Mode	$20+0.1C_B$		300	
		Fast Mode Plus	$20+0.1C_B$		120	
		High−Speed Mode, C_B < 100 pF		10	80	
		High−Speed Mode, C_B < 400 pF		20	160	
t_{FDA}	SDA Fall Time	Standard Mode	$20+0.1C_B$		300	ns
		Fast Mode	$20+0.1C_B$		300	
		Fast Mode Plus	$20+0.1C_B$		120	
		High−Speed Mode, C_B < 100 pF		10	80	
		High−Speed Mode, C_B < 400 pF		20	160	
$t_{SU;STO}$	Stop Condition Setup Time	Standard Mode		4		μs
		Fast Mode		600		ns
		Fast Mode Plus		120		ns
		High−Speed Mode		160		ns
C_B	Capacitive Load for SDA and SCL				400	pF

Timing Diagrams

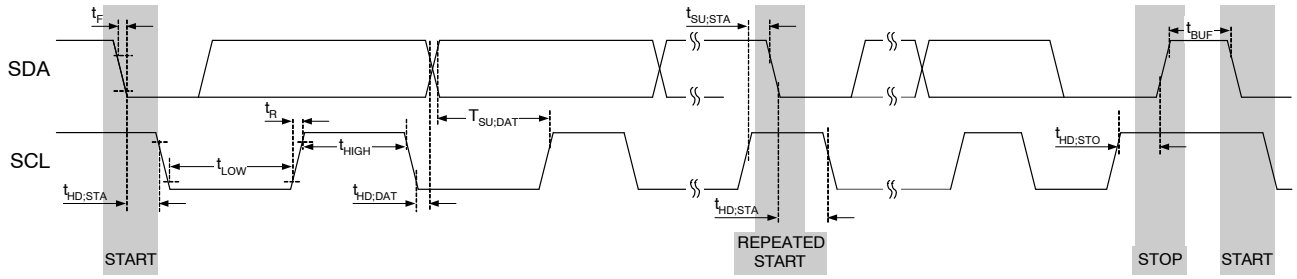
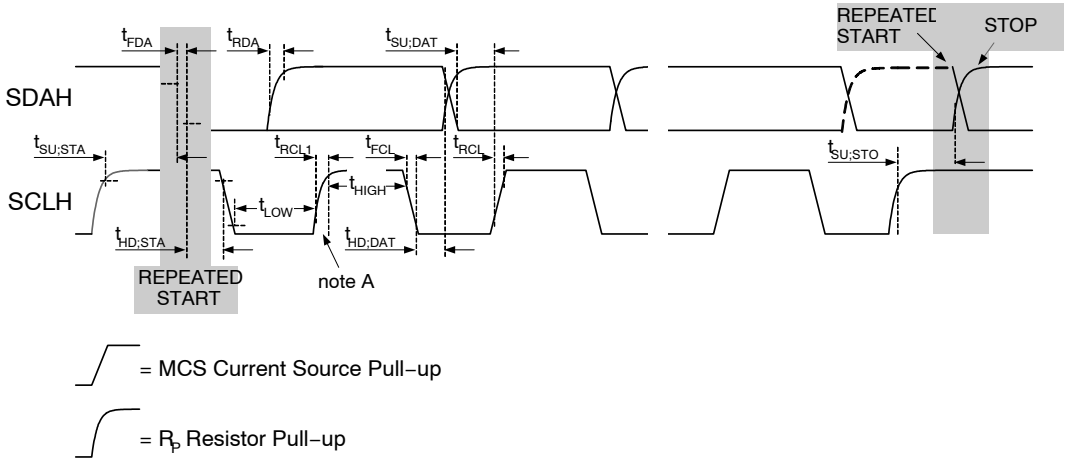


Figure 5. I²C Interface Timing for Fast and Slow Modes



Note A: First rising edge of SCLH after Repeated Start and after each ACK bit.

Figure 6. I²C Interface Timing for High−Speed Mode

CHARGE MODE TYPICAL CHARACTERISTICS

Unless otherwise specified, circuit of Figure 1, V_{OREG} = 4.35 V, $I_{OCHARGE}$ = 950 mA, IO_LEVEL = 0, V_{BUS} = 5.0 V, and T_A = 25°C.

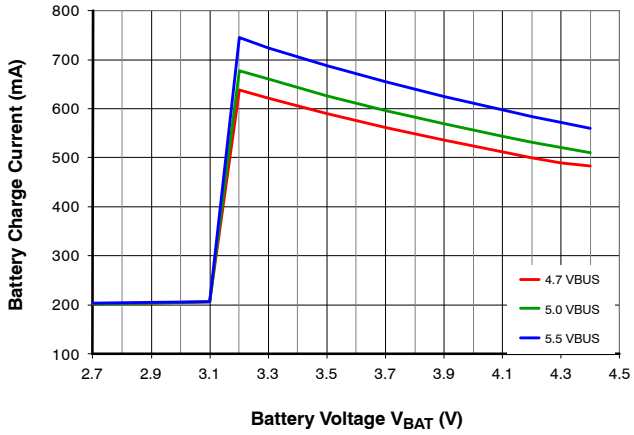


Figure 7. Battery Charge Current vs. V_{BUS} with I_{BUSLIM} = 500 mA

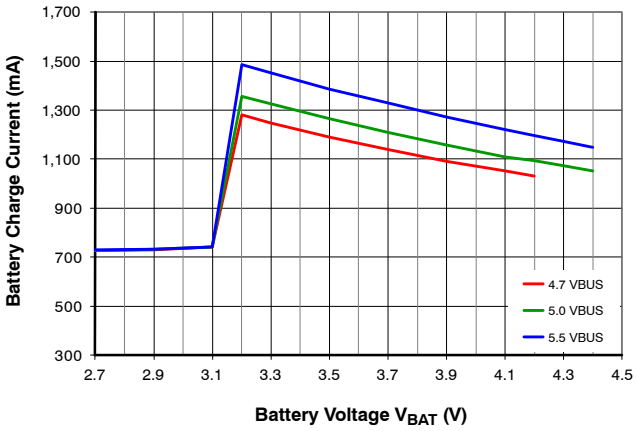


Figure 8. Battery Charge Current vs. V_{BUS} with I_{BUSLIM} = 1100 mA, I_{OCHRG} = 1550 mA

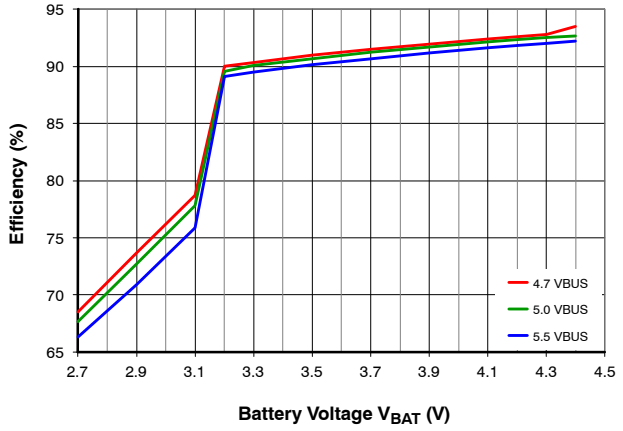


Figure 9. Efficiency vs. V_{BUS}, I_{BUSLIM} = 500 mA, I_{SYS} = 0

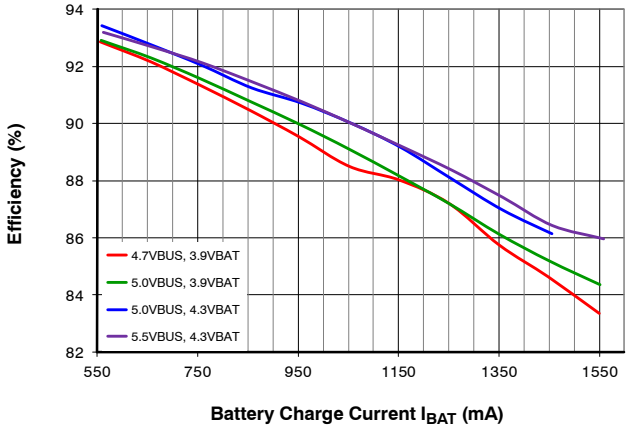


Figure 10. Efficiency vs. Charging Current, I_{BUSLIM} = No Limit

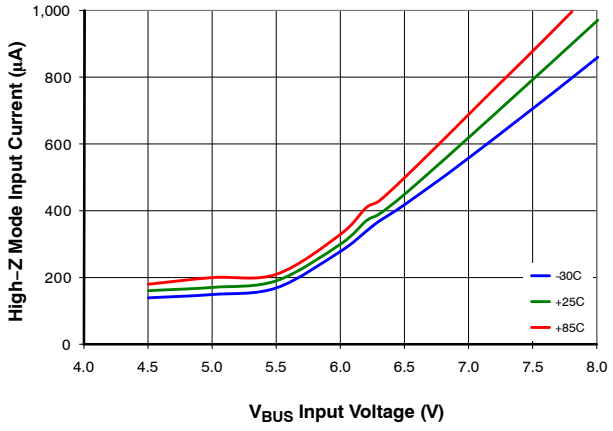


Figure 11. HZ Mode V_{BUS} Current vs. Temperature, 3.7 V_{BAT}

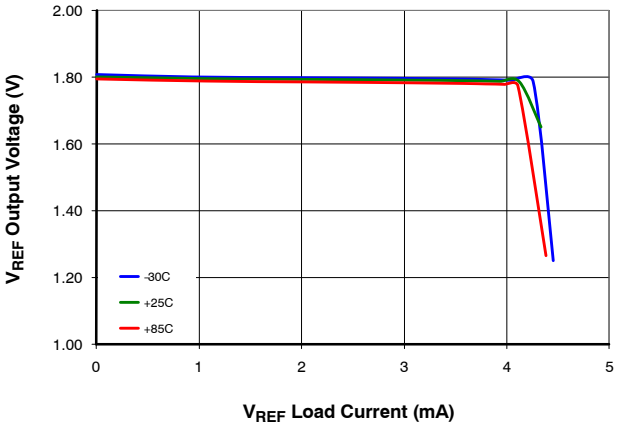


Figure 12. V_{REF} vs. Load Current, Over Temperature

CHARGE MODE TYPICAL CHARACTERISTICS

Unless otherwise specified circuit of Figure 1, V_{OREG} − 4.34 V, $I_{OCHARGE}$ = 950 mA, IO_LEVEL = 0, V_{BUS} = 5.0 V, and T_A = 25°C

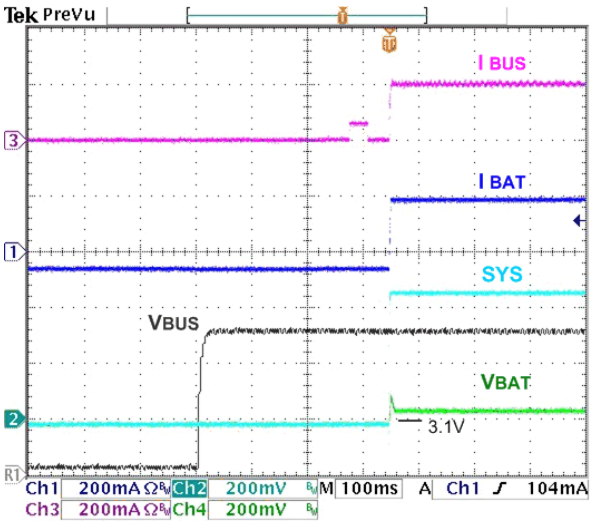


Figure 13. Charger Startup at V_{BUS} Plug−In, 500 mA I_{BUSLIM}, 3.1 V_{BAT}, 50 Ω SYS Load, CE# = 0, IO_LEVEL = 1

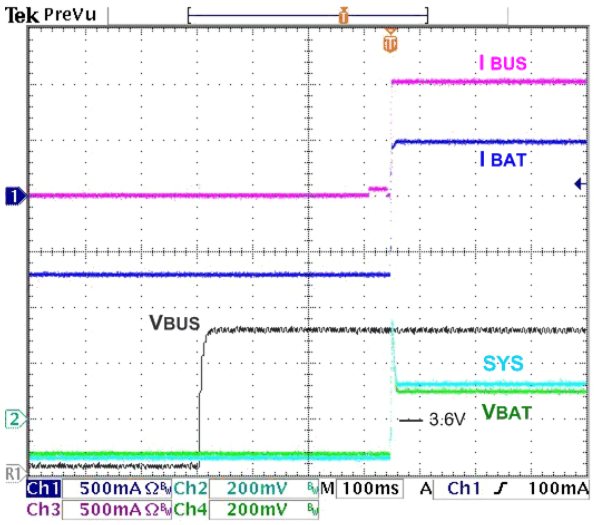


Figure 14. Charger Startup at V_{BUS} Plug−In, 1100 mA I_{BUSLIM}, 3.6 V_{BAT}, 700 mA SYS Load, CE# = 0, IO_LEVEL = 0

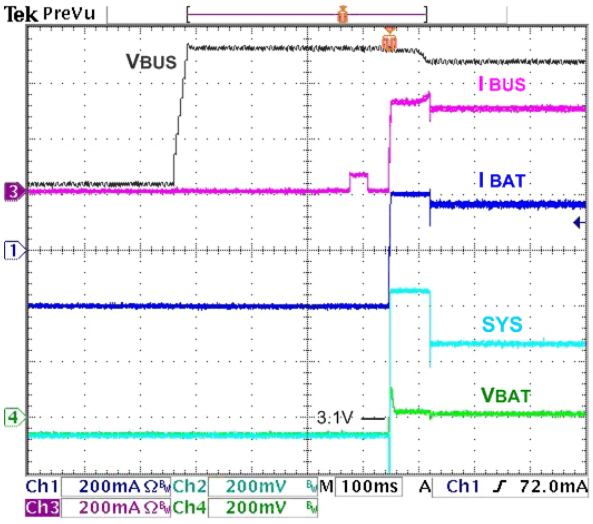


Figure 15. Charger Startup at V_{BUS} Plug−In Using 300 mA Current Limited Source, 500 mA I_{BUSLIM}, 3.1 V_{BAT}, 200 mA SYS Load, CE# = 0, IO_LEVEL=0

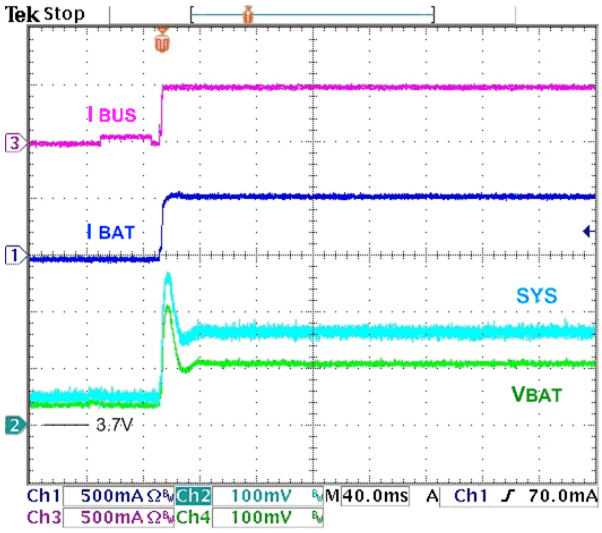


Figure 16. Charger Startup with HZ Bit Reset, 500 mA I_{BUSLIM}, 950 mA I_{CHARGE}, 50 Ω SYS Load, CE# = 0

CHARGE MODE TYPICAL CHARACTERISTICS

Unless otherwise specified circuit of Figure 1, V_{OREG} − 4.34 V, $I_{OCHARGE}$ = 950 mA, IO_LEVEL = 0, V_{BUS} = 5.0 V, and T_A = 25°C

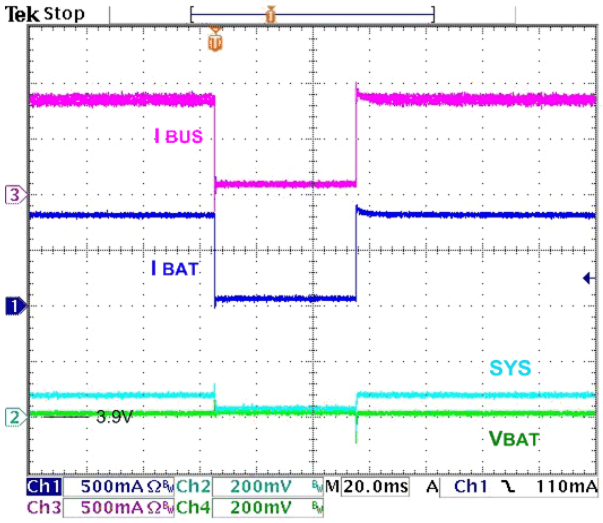


Figure 19. Battery Removal / Insertion while Charging, TE = 0, 3.9 V_{BAT}, I_{CHRG} = 950 mA, I_{BUSLIM} = No Limit, 50 Ω SYS Load

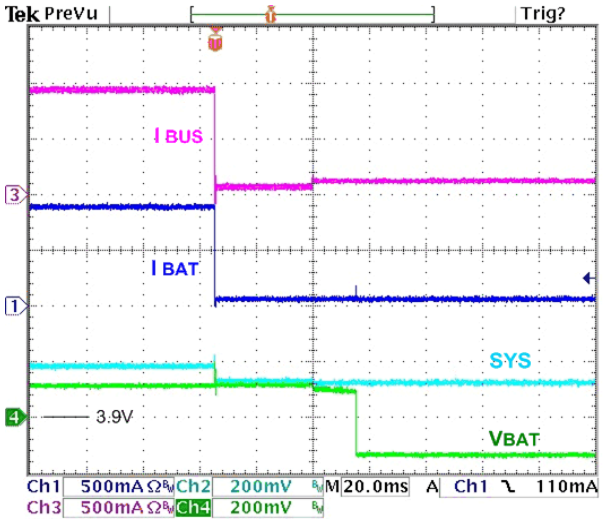


Figure 20. Battery Removal / Insertion when Charging, TE = 1, 3.9 V_{BAT}, I_{BUSLIM} = No Limit, 50 Ω SYS Load

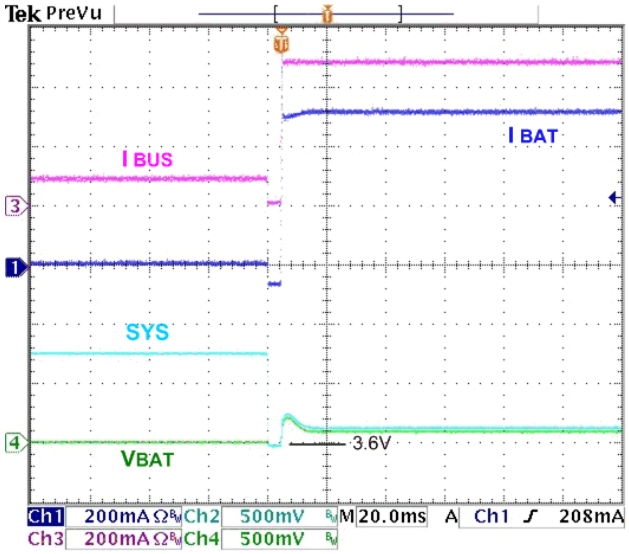


Figure 17. Charger Enable (CE# = 1 to 0) with V_{BUS} Applied, I_{BUSLIM} = 500 mA, 200 mA SYS Load, IO_LEVEL = 0

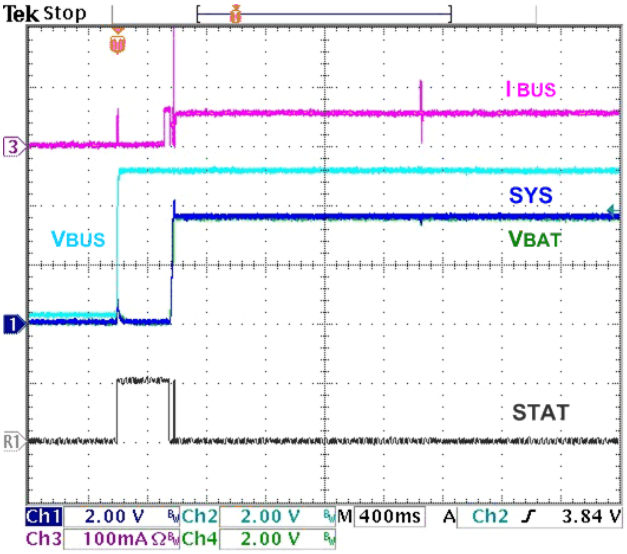


Figure 18. No Battery at V_{BUS} Power−Up, 100 Ω SYS Load, 1 kΩ V_{BAT} Load

GSM TYPICAL CHARACTERISTICS

A 2.0 A GSM pulse applied at V_{BAT} with 5 ms rise / fall time. Simultaneous to GSM pulse, 50Ω additional load applied at SYS

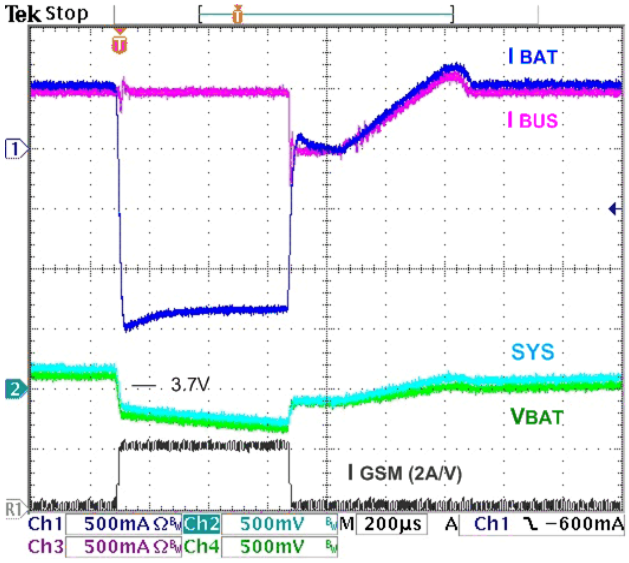


Figure 21. 2.0 A GSM Pulse Response, I_{BUSLIM} = 500 mA Control, I_{CHRG} = 950 mA, 3.7 V_{BAT}, OREG = 4.35 V

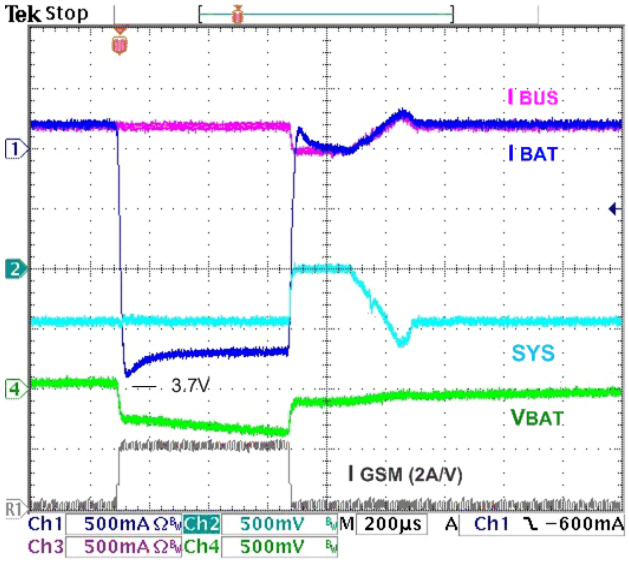


Figure 22. 2.0 A GSM Pulse Response, I_{BUSLIM} = 500 mA, I_{CHRG} = 950 mA, 3.7 V_{BAT}, OREG = 4.35 V, 200 mA Source Current Limit

BOOST MODE TYPICAL CHARACTERISTICS

Unless otherwise specified, using circuit of Figure 1 with optional external PMOS, V_{BAT} = 3.6 V, T_A = 25°C.

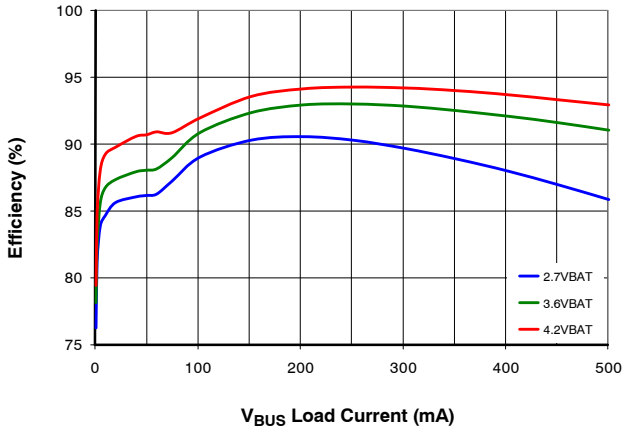


Figure 23. Efficiency vs. I_{BUS} over V_{BAT}

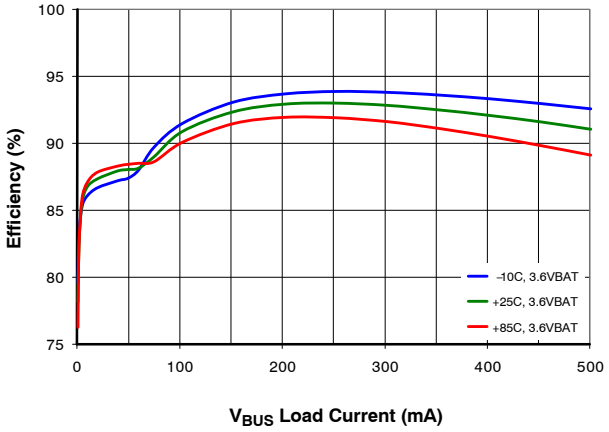


Figure 24. Efficiency vs. I_{BUS} Over−Temperature, 3.6 V_{BAT}

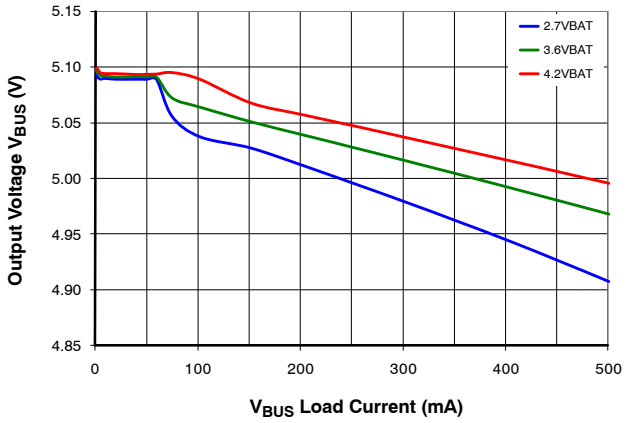


Figure 25. Regulation vs. I_{BUS} over V_{BAT}

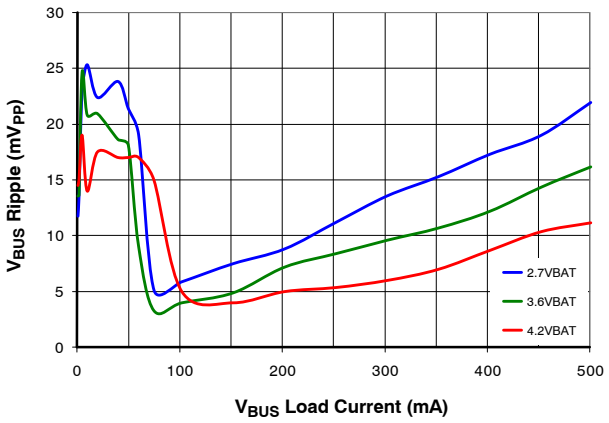


Figure 26. Output Ripple vs. I_{BUS} over V_{BAT}

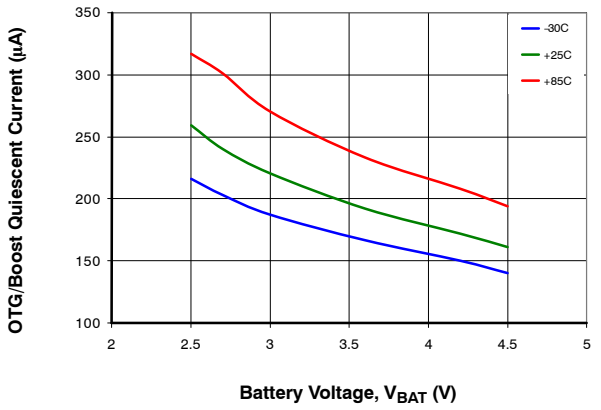


Figure 27. Quiescent Current (I_Q) vs. V_{BAT} Over−Temperature

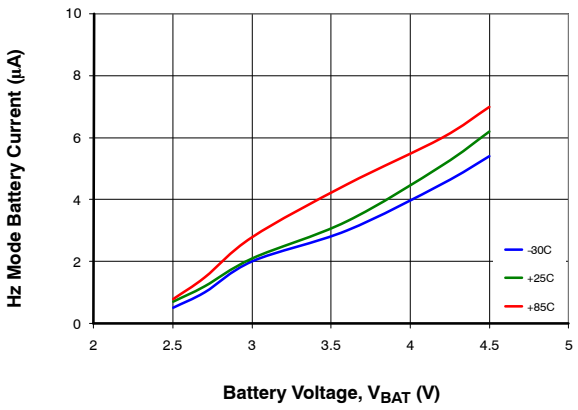


Figure 28. Battery Discharge Current vs. V_{BAT}, Hz/ Sleep Mode

BOOST MODE TYPICAL CHARACTERISTICS

Unless otherwise specified, using circuit of Figure 1 with optional external PMOS, V_{BAT} = 3.6 V, T_A = 25°C.

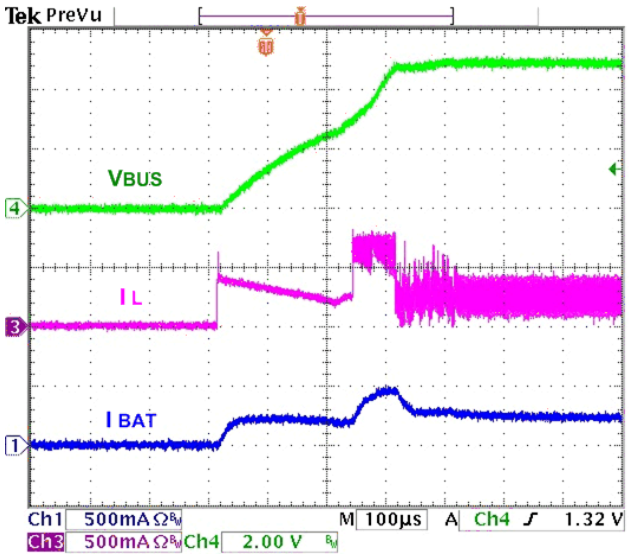


Figure 29. OTG Startup, 50 Ω Load, 3.6 V_{BAT} External / Additional 10 µF on V_{BUS}

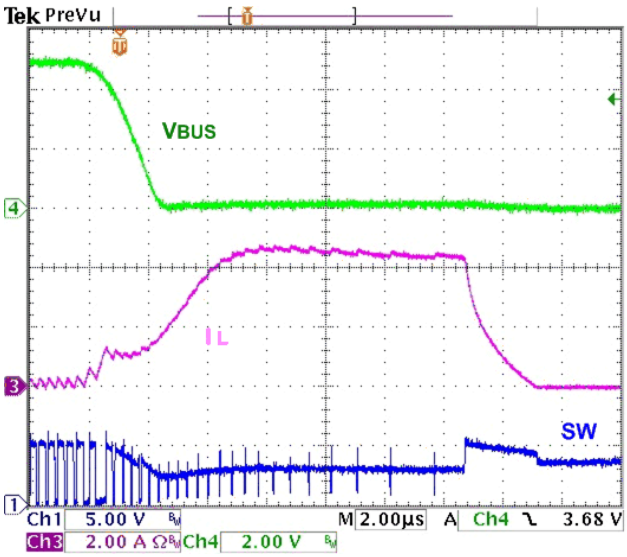


Figure 30. OTG V_{BUS} Overload Response

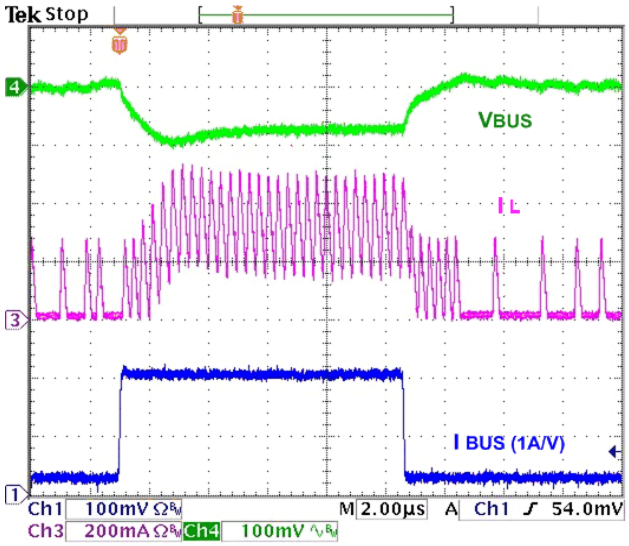


Figure 31. Load Transient, 20–200–20 mA I_{BUS}, $t_{RISE/FALL}$ = 100 ns

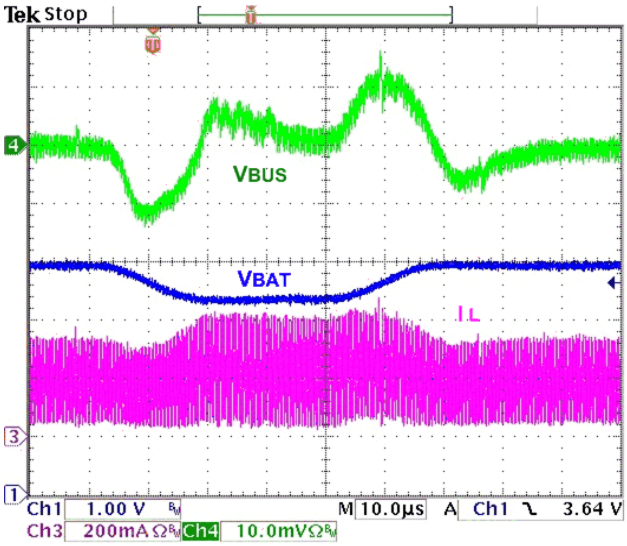


Figure 32. Line Transient, 50 Ω Load, 3.9–3.3–3.9 V_{BAT}, $t_{RISE/FALL}$ = 10 µs

CIRCUIT DESCRIPTION / OVERVIEW

When charging batteries with a current−limited input source, such as USB, a switching charger's high efficiency over a wide range of output voltages minimizes charging time.

FAN54063 combines a highly integrated synchronous buck regulator for charging with a synchronous boost regulator, which can supply 5 V to USB On−The−Go (OTG) peripherals. The FAN54063 employs synchronous rectification for both the charger and boost regulators to maintain high efficiency over a wide range of battery voltages and charge states.

The FAN54063 has four operating modes:

1. Charge Mode:
   Charges a single−cell Li−ion or Li−polymer battery
2. Boost Mode:
   Provides 5 V power to USB−OTG with an integrated synchronous rectification boost regulator, using the battery as input
3. High−Impedance Mode:
   Both the boost and charging circuits are OFF in this mode. Current flow from VBUS to the battery or from the battery to VBUS is blocked in this mode. This mode consumes very little current from VBUS or the battery
4. Production Test Mode:
   This mode provides 4.2 V output on VBAT and supplies a load current of up to 2.3 A

CHARGE MODE AND REGISTERS

Charge Mode

In Charge Mode, FAN54063 employs six regulation loops:

1. Input Current: Limits the amount of current drawn from VBUS. This current is sensed internally and can be programmed through the I^2C interface
2. Charging Current: Limits the maximum charging current. This current is sensed using an internal sense MOSFET
3. VBUS Voltage: This loop is designed to prevent the input supply from being dragged below V_{BUSLIM} (typically 4.5 V) when the input power source is current limited. An example of this would be a travel charger. This loop cuts back the current when V_{BUS} approaches V_{BUSLIM}, allowing the input source to run in current limit
4. Charge Voltage: The regulator is restricted from exceeding this voltage. As the internal battery voltage rises, the battery's internal impedance works in conjunction with the charge voltage regulation to decrease the amount of current flowing to the battery. Battery charging is completed when the current through Q4 drops below the I_{TERM} threshold
5. Pre−charge: When V_{BAT} is below V_{BATMIN}, Q4 operates as a linear current source and modulates its current to ensure that the voltage on SYS stays above 3.4 V
6. Temperature: If the IC's junction temperature reaches 120°C, charge current is reduced until the IC's temperature is below 120°C

PWM Controller in Charge Mode

The IC uses a current−mode PWM controller to regulate the output voltage and battery charge currents. The synchronous rectifier (Q2) has a negative current limit that turns off Q2 at 180 mA to prevent current flow from the battery.

Battery Charging Curve

If the battery voltage is below V_{SHORT}, a linear current source pre−charges the battery until V_{BAT} reaches V_{SHORT}. The PWM charging circuit is then started and the battery is charged with a constant current if sufficient input power is available. The current slew rate is limited to prevent overshoot.

During the current regulation phase of charging, I_{BUSLIM} or the programmed charging current limits the amount of current available to charge the battery and power the system.

During the voltage regulation phase of charging, assuming that V_{OREG} is programmed to the cell's fully charged "float" voltage, the current that the battery accepts with the PWM regulator limiting its output (sensed at VBAT) to V_{OREG} declines.

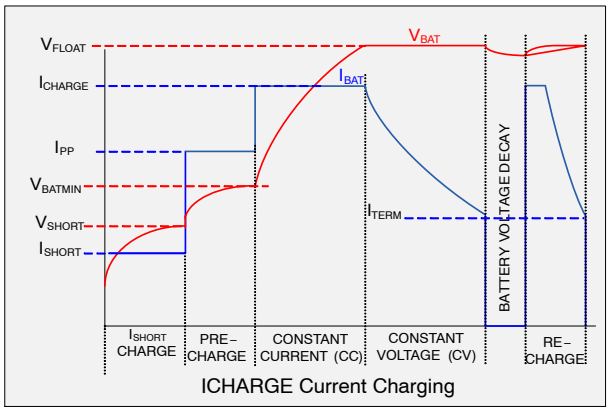


Figure 33. Charge Curve, I_{CHARGE} Not Limited by I_{BUSLIM}

The FAN54063 is designed to work with a current−limited input source at VBUS as shown below:

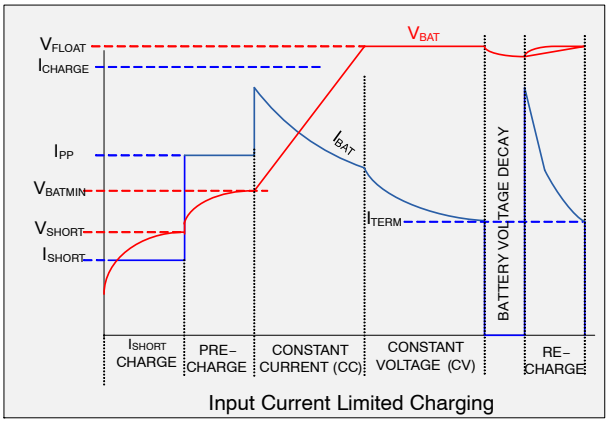


Figure 34. Charge Curve, I_{BUSLIM} Limits I_{CHARGE}

The following charging parameters can be programmed by the host through I^2C:

Table 3. PROGRAMABLE CHARGING PARAMETERS

Parameter	Name	Register
Output Voltage Regulation	V_{OREG}	REG02[7:2]
Battery Charging Current Limit	$I_{OCHARGE}$	REG04[6:3]
Input Current Limit	I_{BUSLIM}	REG01[7:6]
Charge Termination Limit	I_{TERM}	REG04[2:0]
Weak Battery Voltage	V_{LOWV}	REG01[5:4]

Output Voltage Regulation (V_{OREG})

The charger output or "float" voltage can be programmed by the OREG (REG02[7:2]) bits from 3.51 V to 4.45 V in 20 mV increments. The default setting is 3.55 V.

See OREG Register Bit Definitions.(Table 17)

Battery Charging Current Limit ($I_{OCHARGE}$)

When the IO_LEVEL bit is set (default), the IOCHARGE bits are ignored and charge current is set to 200 mA.

See IOCHARGE Register Bit Definitions.(Table 17)

Input Current Limiting (I_{BUSLIM})

To minimize charging time without overloading VBUS current limitations, the IC's input current limit can be programmed by the IBUSLIM (REG01[7:6]) bits.

See I_{BUSLIM} Register Bit Definitions.(Table 17)

Termination Limit (I_{TERM})

Charge current termination can be enabled or disabled using the TE (REG01[3]) bit. By default TE = "0", therefore, termination is disabled and charging does not terminate at the programmed I_{TERM} level.

When TE = "1", and V_{BAT} reaches V_{OREG}, the charging current is reduced, limited by the battery's ESR and its internal cell voltage. When the charge current falls below I_{TERM}; PWM charging stops; but the STAT pin remains LOW. The STAT pin then goes HIGH and the STAT bits change to CHARGE DONE (10), provided the battery and charger are still connected. If V_{BAT} falls to V_{RCH} below V_{OREG}, the Fast Charge cycle starts again.

Post−charging can be enabled to "top−off" the battery to a lower termination current threshold than I_{TERM}. The PC_EN bit (REG07[3]) must be set to "1" before the battery charging current reaches I_{TERM}. The lower termination current is set by the PC_IT (REG07[2:0] bits. Post−charging begins after normal charging is ended (as described above) with the PC_ON (REG11[2]) monitor bit set to "1".

During post−charging, the STAT pin is HIGH, indicating that the charge current is below the I_{TERM} level. Once the current reaches the threshold for post−charging completion (set by the PC_IT bits), PWM charging stops and the PC_ON bit changes back to "0". If the charging current goes above I_{TERM} without first falling to PC_IT, the PC_ON bit can be reset by using any of these methods: V_{BAT} moving below and above V_{BATMIN}, a VBUS POR, or the CE# or HZ_MODE bit cycled. If V_{BAT} falls to V_{RCH} below V_{OREG}, the Fast Charge cycle starts again.

See ITERM Register Bit Definitions.(Table 17)

Weak Battery Voltage (V_{LOWV})

The FAN54063 monitors the level of the battery with respect to a programmable VLOWV (REG01<5:4>) threshold (default 3.7 V). V_{LOWV} defines the voltage level of the battery at which the system is guaranteed to be fully operational when only powered by the battery.

The POK_B pin pulls LOW once V_{BAT} reaches V_{LOWV}, and remains LOW as long as the IC is in Fast Charge. The IC will remain in Fast Charge as long as V_{BAT} > 3.0 V.

See VLOWV Register Bit Definitions.(Table 17)

VBUS Control loop (V_{BUSLIM})

The IC includes a control loop that limits input current in case a current−limited source is supplying V_{BUS}.

The control increases the charging current until either:

- I_{BUSLIM} or $I_{OCHARGE}$ limit is reached OR
- $V_{BUS} = V_{BUSLIM}$

If V_{BUS} collapses to V_{BUSLIM}, the VBUS loop reduces its current to keep $V_{BUS} = V_{BUSLIM}$. When the VBUS control loop is limiting the charge current, the VLIM bit (REG05[3]) is set.

See VBUSLIM Register Bit Definitions.(Table 17)

CHARGER OPERATION

VBUS Plug In and Safety Timer

At VBUS plug in, the TMR_RST (Reg00[7]) bit must be set within 2 seconds of V_{BUS} rising above $V_{(INMIN)1}$ or all registers, except for SAFETY (REG06), are set to their default values. This functionality occurs regardless of the state of the CE# and WD_DIS bit. If plug in occurs with the device in a HZ or Charge Done state and the TMR_RST bit is not set within 2 seconds of V_{BUS} rising above $V_{(INMIN)1}$, all register, except for SAFETY, will reset when the device enters PWM Charging or Recharge.

By default, the safety timers do not run in the FAN54063. A Watchdog (t_{32s}) timer can be enabled by setting the WD_DIS register bit, (REG13[1]) to “0”. When WD_DIS = “0”, charging is controlled by the host with the t_{32S} timer running to ensure that the host is alive. Setting the TMR_RST bit resets the t_{32S} timer. If the t_{32S} timer times out; all registers, except SAFETY, are set to their default values (including WD_DIS and CE#), the FAULT bits are set to “110”, and STAT is pulsed.

V_{BUS} POR / Non−Compliant Charger Rejection

256 ms after VBUS is connected, the IC pulses the STAT pin and sets the VBUS_CON bit. Before starting to supply current, the IC applies a 100 Ω load from VBUS to GND. V_{BUS} must remain above $V_{IN(MIN)1}$ and below $VBUS_{OVP}$ for t_{VBUS_VALID} (32 ms) before the IC initiates charging or supplies power to SYS.

The VBUS validation sequence always occurs before significant current is drawn from VBUS (for example, after a VBUS OVP fault or a recharge initiation. t_{VBUS_VALID} ensures that unfiltered 50/60 Hz chargers and other non−compliant chargers are rejected.

USB−Friendly Boot Sequence

The FAN54063 does not automatically initiate charging at VBUS POR. Instead, prior to receiving host commands, the buck is enabled to provide power to SYS while Q4 and Q5 remain off until register bit CE# (REG01[2]) is set to “0” through the I^2C interface, allowing charging through Q4.

Startup with No Battery

The FAN54063 has Battery Absent Behavior enabled. At VBUS POR with the battery absent, the PWM will run, providing 3.55 V to the system from the input source with current limited by the default I_{BUSLIM} setting.

Startup with a Dead Battery

At VBUS POR, if $V_{BAT} < V_{SHORT}$, all registers, including the SAFETY register, are reset to their default values and the DBAT_B (REG02[1]) bit is reset. CE# = “1”, so charging is disabled.

If the battery’s protection switch is open, the PWM will run, providing 3.55 V to the system from the input source with current limited by the default I_{BUSLIM} setting. This allows the host processor to awaken and establish host control. Once this occurs, the host’s low level software can program the CE# bit to “0” and a linear current source closes the battery protection switch. When V_{BAT} voltage rises above V_{BATMIN} and sufficient power is available, PWM charging begins and the battery is charged through the BATFET, Q4. The IO_LEVEL (REG05[5]) bit is set to “1” by default which limits charge current to 200 mA.

With CE# = “1” once V_{BAT} rises above V_{SHORT}, DBAT_B is set. With CE# = “0” once V_{BAT} rises above V_{BATMIN}, DBAT_B is set.

Power Path Operation

As long as $V_{BAT} < V_{BATMIN}$, Q4 operates as a linear current source, (Precharge) with its current (I_{PP}) limited to 200 mA when IO_LEVEL (REG05[5]) is set to its default value of “1”. If IO_LEVEL is set to “0” and IBUSLIM > “01”, charge current is limited to 450 mA when $I_{OCHARGE} \le 750$ mA, and 730 mA when $I_{OCHARGE} > 750$ mA. Providing the input current is not limited by the I_{BUSLIM} setting or the current available from the source, during precharge, the IC regulates SYS to 3.55 V and provides the I_{PP} limited current to the battery.

System power always has the highest priority when power from the buck is limited ensuring SYS does not fall below 3.4 V. This is managed by folding back the current to charge the battery until charge current is reduced to 0 A.

After V_{BAT} reaches V_{BATMIN}, Q4 fully enhances and is used as a current−sense element to limit current ($I_{OCHARGE}$) per the I^2C register settings. This is accomplished by limiting the PWM modulator’s current (Fast Charge). If SYS drops more than 5 mV (V_{THSYS}) below V_{BAT} and CE# = “0”, Q4 is turned on and GATE is pulled LOW. If CE# = “1”, only GATE is forced LOW. Once SYS voltage becomes higher than V_{BAT}, GATE returns HIGH and Q4, once again, serves as the current−sense element to limit $I_{OCHARGE}$.

If the DIS pin is HIGH or HZ_MODE = “1” while $V_{BAT} > V_{LOWV}$, Q4 is enabled and GATE is forced LOW to prevent the system from crashing. Upon enterring SLEEP Mode ($V_{BUS} < V_{BAT}$), Q4 is turned on and GATE is held LOW.

Optional External Power Path Provisions

Q4 has a typical on−resistance of 70mΩ, which is sufficient for most applications. However, if high system load currents are expected, it is possible to augment Q4 with a parallel external PMOS element, connected as shown by dotted lines in Figure 2. Use of the optional external PMOS reduces the series voltage drop associated with battery discharge during SLEEP mode or supplemental mode operation. For example, the addition of **onsemi**’s FDMA905P can support discharge currents above 10 A.

POK_B (see Table 4)

The POK_B pin and the POK_B (REG11[5]) bit are intended to provide feedback to the processor that the battery is strong enough to allow the system to fully function. Whenever the IC is operating in precharge, POK_B is HIGH. On exiting Precharge, POK_B remains HIGH until $V_{BAT} > V_{LOWV}$. REG01[5:4] sets the V_{LOWV} threshold. POK_B pulls LOW once V_{BAT} reaches V_{LOWV}, and remains LOW as long as the IC is in Fast Charge and the IC will remain in Fast Charge as long as $V_{BAT} > 3.0$ V. If the battery voltage falls below 3.0 V the IC enters Precharge. If WD_DIS = "0" and the t_{32S} timer expires during charging, the POK_B pin will go HIGH.

The POK_B bit can be set via I2C to change the state of the pin to HIGH. This setting of the bit and pin can be used to signal the system into a low−power state, preventing excessive loading from the system while attempting to recharge a depleted battery.

The STAT pin pulses any time the POK_B pin and bit change states.

Table 4. Q4, Q5, POK_B vs. OPERATING MODE

Operating Mode	V_{BUS}	V_{BAT}	CE#	PWM	V_{SYS}	Q4	Q5	GATE	POK_B
VBUS DISCONNECTED									
OFF	< V_{BAT} OR < $V_{IN(MIN)2}$	> V_{SHORT}	X	OFF	≤ V_{BAT}	ON	ON	LOW	HIGH
VBUS PLUG IN WITH BATTERY PROTECTION SWITCH OPEN									
PWM	Valid	OPEN	1	ON	V_{OREG}	OFF	OFF	HIGH	HIGH
			0						Indeterminate (Note 8)
30 mA Linear Charging (Note 8)	Valid	< V_{SHORT}	0	ON	3.55	OFF	OFF	HIGH	HIGH
CHARGE MODE									
Precharge	Valid	> V_{SHORT} and < V_{BATMIN}	0	ON	3.55	Linear	OFF	HIGH	HIGH
Precharge: $I_{SYS} + I_{pp} > I_{PWM}$, $I_{BAT} < I_{PP}$	Valid	< V_{BATMIN}	0	ON	< 3.55	Linear	OFF	HIGH	HIGH
Fast Charge	Valid	> V_{BATMIN} and < V_{LOWV}	0	ON	> V_{BAT}	ON	OFF	HIGH	HIGH
		> V_{LOWV}							LOW
BATTERY VOLTAGE FALLING FROM FAST CHARGE									
Precharge	Valid	$V_{BATFALL}$	0	ON	3.55	ON	OFF	HIGH	HIGH
BATTERY SUPPLEMENTING SYS									
Supplemental Mode : $I_{SYS} > I_{PWM}$	Valid	> V_{BATMIN} and > $V_{SYS} + V_{THSYS}$	X	ON	< V_{BAT}	X	ON	LOW	X

8. When VBAT is open, V_{BAT} can float to V_{SYS}, and POK_B = HIGH when $V_{BAT} < V_{LOWV}$ and POK_B = LOW when $V_{BAT} > V_{LOWV}$. Battery's presence or not (VBAT open) can be monitored by reading NOBAT bit (REG11[3]).
9. 30 mA Linear Charging operating mode assumes the host has programmed CE# = "0" during PWM Operating Mode.

Charger Status / Fault Status

The STAT pin indicates the operating condition of the IC and provides a fault indicator for interrupt driven systems.

Table 5. STAT Pin Function

EN_STAT	Charge State	STAT Pin
0	X	OPEN
X	Normal Conditions	OPEN
1	Charging	LOW
X	Fault (Charging or Boost)	128 μs Pulse, then OPEN

The FAULT bits (REG00[2:0]) indicate the type of fault in Charge Mode.

Monitor Registers (REG10, REG11)

Additional status monitoring bits enable the host processor to have more visibility into the status of the IC. The monitor bits are real−time status indicators and are not internally debounced or otherwise time qualified.

The state of the MONITOR register bits listed in High−Impedance Mode is valid only when V_{BUS} is valid.

Charge Mode Control Bits

The CE# (REG01[2]) bit is set to “1” by default, therefore, charging is disabled.

Setting the RESET (REG04[7]) bit clears all registers (except SAFETY). The CE# bit will only be cleared if RESET occurs with a valid VBUS and $V_{BAT} < V_{LOWV}$. If the HZ_MODE bit was set when the RESET bit is set, this bit is also cleared. Refer to the Register Bit Definitions section for more details.

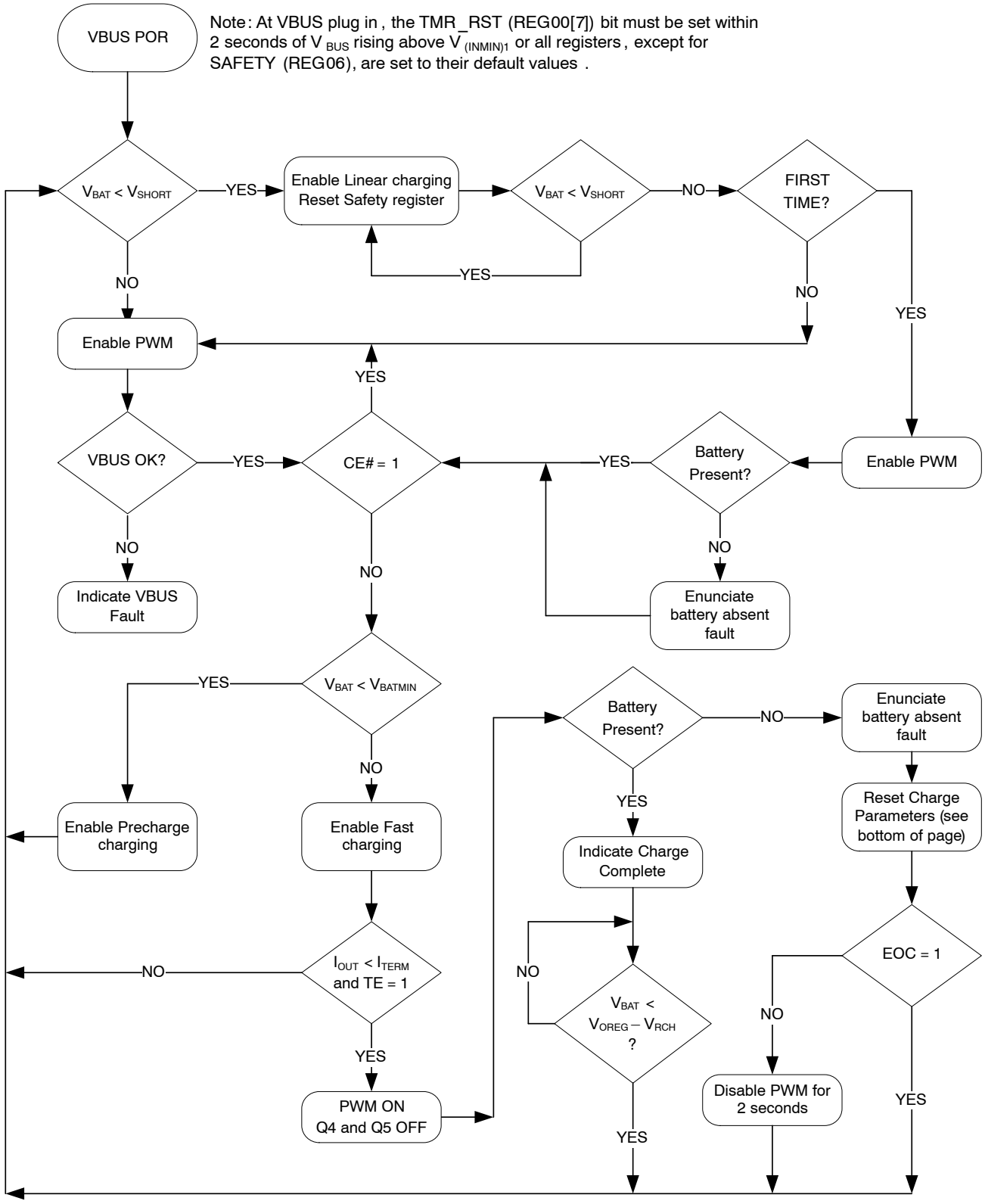
Setting the HZ_MODE bit (REG01[1]) or raising the DIS pin will put the device in High−Impedance Mode, where the buck is disabled. Q4 and Q5 are enabled to prevent the system from crashing. Refer to Table 6 for details.

If the charger is in High−Impedance mode and V_{BAT} drops below V_{LOWV}, or High Impedance mode is entered while $V_{BAT}<V_{LOWV}$, all registers (except SAFETY), including HZ_MODE and CE#, are reset to their default values. If WD_DIS = “0” (REG13[1]), the register resets, including WD_DIS, only occur if the Watch−Dog Timer (t_{32s}) expires. If the DIS pin is HIGH, the IC will remain in High−Impedance Mode. If the DIS pin is LOW, the buck will be enabled.

Table 6. DIS PIN, HZ_MODE AND WD_DIS BIT OPERATION

Conditions	Functionality
WD_DIS = 1 (default) and $V_{BAT} > V_{LOWV}$	Setting either the HZ_MODE bit through I^2C or the DIS pin HIGH will disable the charger and put the IC into High−Impedance Mode. Resetting the HZ_MODE bit or the DIS pin to LOW will allow charging to resume.
WD_DIS = 0 and $V_{BAT} > V_{LOWV}$	Setting either the HZ_MODE bit through I^2C or the DIS pin HIGH will stop the t_{32s} timer from advancing (does not reset it), disable the charger, and put the IC into High−Impedance Mode. Resetting the HZ_MODE bit or the DIS pin LOW allows charging to resume. The t_{32s} timer resuming counting down the remainder of time from where it was suspended, at HZ mode entry.

FLOW CHARTS



Note: Reset Charge Parameters is a condition that results in the O REG, IOCHARGE, IBUSLIM, ITERM, VLOWV, and the Safety register bits resetting. It does not reset the IO _LEVEL, EOC, and TE register bits.

Figure 35. Charge State Flow Chart

NON−CHARGING STATES

Sleep Mode

When V_{BUS} falls below V_{BAT} + V_{SLP} and V_{BUS} is above $V_{IN(MIN)2}$, the IC enters Sleep Mode to prevent the battery from draining into VBUS. During Sleep Mode, reverse current is disabled by body switching Q1.

Idle State

The Idle State is related to the condition of the battery. During Idle mode the Switch Mode Power Supply (SMPS) is operating, but the battery is not being charged for one or more of the following conditions: the Safety Timer expires (CE# reset to 1), charging is complete, or the BATFET is disabled by the Charge Enable bit, CE# = "1".

The PWM Buck continues to supply power to the system, but the Battery is no longer being charged and the BATFET is disabled.

Standby State

The Standby State is an intermediate state where the switch mode supply is off due to either bad input power, the device has been put in High−Impedance Mode, or the die temperature is too hot.

CHARGER PROTECTION

Battery Temperature (NTC) Monitor

The FAN54063 reduces the maximum charge current and termination voltage if an NTC measuring battery temperature (T_{BAT}) indicates that it is outside the fast−charging limits (T2 to T3), as described in the JEITA specification[1]. There are four temperature thresholds that change battery charger operation: T1, T2, T3, and T4, shown below.

Table 7. BATTERY TEMPERATURE THRESHOLDS

For use with 10 kΩ NTC, b = 3380, and R_{REF} = 10 kΩ.

Threshold	Temperature	% of V_{REF}
T1	0°C	73.9
T2	10°C	64.6
T3	45°C	32.9
T4	60°C	23.3

Table 8. CHARGE PARAMETERS VS. TBAT

For use with 10 kΩ NTC, b = 3380, and R_{REF} = 10 kΩ.

T_{BAT} (°C)	I_{CHARGE}	V_{FLOAT}
Below T1	Charging to VBAT Disabled	
Between T1 and T2	$I_{OCHARGE}$ / 2 (Note 10)	4.0 V
Between T2 and T3	$I_{OCHARGE}$	V_{OREG}
Between T3 and T4	$I_{OCHARGE}$ / 2 (Note 10)	4.0 V
Above T4	Charging to VBAT Disabled	

10. If $I_{OCHARGE}$ is programmed to less than 650 mA, the charge current is limited to 340 mA.

Thermistors with other β values can be used, with some shift in the corresponding temperature threshold, as shown in Table 9.

Table 9. THERMISTOR TEMPERATURE THRESHOLDS

R_{REF} = R_{THRM} at 25°C.

Parameter	Various Thermistors			
$R_{THRM(25°C)}$	10 kΩ	10 kΩ	47 kΩ	100 kΩ
β	3380	3940	4050	4250
T1	0°C	3°C	6°C	8°C
T2	10°C	12°C	13°C	14°C
T3	45°C	42°C	41°C	40°C
T4	60°C	55°C	53°C	51°C

[1] Japan Electronics and Information Technology Industries Association (JEITA) and Battery Association of Japan. "A Guide to the Safe Use of Secondary Lithium Ion Batteries in Notebook−type Personal Computers," April 28, 2007.

The host processor can disable temperature−driven control of charging parameters by writing “1” to the TEMP_DIS bit. Since TEMP_DIS is reset whenever the IC resets its registers, the temperature controls are enforced whenever the IC is auto−charging, since auto−charge is always preceded by a reset of registers.

To disable the thermistor circuit, tie the NTC pin to GND. Before enabling the charger, the IC tests to see if NTC is shorted to GND. If NTC is shorted to GND, no thermistor readings occur and the NTC_OK and NTC1−NTC4 is reset.

The IC first measures the NTC immediately prior to entering any PWM charging state, then measures the NTC once per second, updating the result in NTC1−NTC4 bits (REG 12[3:0]).

Table 10. NTC1−NTC4 DECODING

T_{BAT} (°C)	NTC4	NTC3	NTC2	NTC1
Above T4	1	1	1	1
Between T3 and T4	0	1	1	1
Between T2 and T3	0	0	1	1
Between T1 and T2	0	0	0	1
Below T1	0	0	0	0

Safety Register Settings

The IC contains a SAFETY register (REG06) that prevents the values of OREG (REG02[7:2]) and IOCHARGE (REG04[6:3]) from exceeding the values of VSAFE (REG06[3:0]) and ISAFE (REG06[7:4]) in the SAFETY register.

After V_{BAT} rises above V_{SHORT}, the SAFETY register is loaded with its default value and may be written to only before writing to any other register. The same 8−bit value should be written to the SAFETY register twice to set the register value. After writing to any other register, the SAFETY register is locked until V_{BAT} falls below V_{SHORT}.

If the host attempts to write a value higher than VSAFE or ISAFE to OREG or IOCHARGE, respectively; the VSAFE, ISAFE value appears as the OREG, IOCHARGE register value, respectively.

The Safety register is reset when the battery is below V_{SHORT} and power is removed from VBUS.

See VSAFE and ISAFE Register Bit Definitions. (Table 17)

Thermal Regulation and Shutdown

When the IC’s junction temperature reaches T_{CF} (about 120°C), the charger reduces its output current to 550 mA to prevent overheating. If the temperature increases beyond $T_{SHUTDOWN}$; charging is suspended, the FAULT bits are set to 101, and STAT is pulsed high. In Suspend Mode, all timers stop and the state of the IC’s logic is preserved. Charging resumes at programmed current after the die cools to about 120°C.

Note that as power dissipation increases, the effective θ_{JA} decreases due to the larger difference between the die temperature and ambient.

Charge Mode Input Supply Protection

Input Supply Low−Voltage Detection

The IC continuously monitors V_{BUS} during charging. If V_{BUS} falls below $V_{IN(MIN)2}$, the IC:

1. Terminates charging
2. Pulses the STAT pin, sets the STAT bits to “00”, and sets the FAULT bits to “011”

If V_{BUS} recovers above the $V_{IN(MIN)1}$ rising threshold after time t_{INT} (about two seconds), the charging process is repeated. This function prevents the USB power bus from collapsing or oscillating when the IC is connected to a suspended USB port or a low−current−capable OTG device.

Input Over−Voltage Detection

When V_{BUS} exceeds $VBUS_{OVP}$, the IC:

1. Turns off Q3
2. Suspends charging
3. Sets the FAULT bits to “001”, sets the STAT bits to “11”, and pulses the STAT pin

When VBUS falls about 100 mV below $VBUS_{OVP}$, the fault is cleared and charging resumes after VBUS is revalidated.

SYS Short During Discharge / Supplemental Mode

Caution should be taken to ensure the SYS pin is not shorted when connected to a battery. This condition can induce high current flow through the BATFET (Q4) and the external PMOS, if equipped, until the battery’s own safety circuit trips. The resulting high current can damage the IC.

Charge Mode Battery Detection & Protection

V_{BAT} Over−Voltage Protection

The OREG voltage regulation loop prevents V_{BAT} from overshooting V_{OREG} by more than 50 mV when the battery is removed. When the PWM charger runs with no battery, the TE bit is not set and a battery is inserted that is charged to a voltage higher than V_{OREG}; PWM pulses stop. If no further pulses occur for 30 ms, the IC sets the FAULT bits to “100”, sets the STAT bits to “11”, and pulses the STAT pin.

Battery Detection during Charging

The IC can detect the presence, absence, or removal of a battery if the termination bit (TE) is set to “1” and CE# = “0”. During normal charging, once V_{BAT} is close to V_{OREG} and the charge current falls below I_{TERM}; the PWM charger continues to provide power to SYS and Q4 is turned off. It then turns on a discharge current, I_{DETECT}, for t_{DETECT}. If V_{BAT} is still above $V_{OREG} - V_{RCH}$, the battery is present and the IC sets the STAT bits to “10” (Charge Done). If V_{BAT} is below $V_{OREG} - V_{RCH}$, the battery is absent and the IC:

1. Sets the charging parameters to their default values
2. Sets the FAULT bits to “111” (Battery Absent) and sets the NOBAT bit
3. If EOC = “0”, the IC turns off the PWM for t_{INT}, then resumes charging and retries Battery Detection. If the battery is still absent, the process repeats with the “No Battery” fault re−enunciated
4. If EOC = “1”, the PWM remains on to provide power to SYS, but charge termination and the battery absent test are performed every t_{INT}

Linear Charging

If the battery voltage is below the short−circuit threshold (V_{SHORT}); a linear current source, I_{SHORT}, charges V_{BAT} until $V_{BAT} > V_{SHORT}$.

PRODUCTION TEST MODE (PTM)

PTM provides 4.20 V at up to 2.3 A to VBAT when V_{BUS} = 5.5 V ±5%.

The IC enters PTM when the PROD (REG05[6]) bit is set after the NOBAT (REG11[3]) bit has been set. The NOBAT bit indicates that the IC has detected battery absence. A battery absence detection test is performed automatically at current termination. The steps for entering PTM should include: set the TE (REG01[3]) bit high, set the CE# (REG01[2]) bit low, wait for the NOBAT bit to set HIGH, then set the PROD bit to “1” to enter PTM. Battery absence detection is completed within 500 ms from the time that CE# is set.

In PTM, the GATE bit (REG11[7]) is LOW, Q5 is on, and all auxiliary control loops are disabled. Only the OREG loop is active, which controls V_{BAT} to 4.20 V, regardless of the OREG register setting. Thermal shutdown remains active.

During PTM, high current pulses (load currents greater than 1.5 A) must be limited to 20% duty cycle with a minimum period of 10 ms.

BOOST MODE

Boost Mode can be enabled by setting the OPA_MODE REG01[0]) bit HIGH and clearing the HZ_MODE bit.

Table 11. ENABLING BOOST

HZ_MODE	OPA_MODE	BOOST
0	1	Enabled
1	X	Disabled
X	0	Disabled

If WD_DIS = “0”, to remain in Boost Mode, the TMR_RST must be set by the host before the t_{32S} timer times out. If t_{32S} times out in Boost Mode; the IC resets all registers, pulses the STAT pin, sets the FAULT bits to 110, and resets the BOOST bit. VBUS POR or reading REG00 clears the fault condition.

Boost PWM Control

The IC uses a minimum on−time and computed minimum off−time to regulate V_{BUS}. The regulator achieves excellent transient response by employing current−mode modulation. This technique causes the regulator to exhibit a load line. The output voltage drops slightly as the output current rises. With a constant V_{BAT}, this appears as a constant output resistance.

The “droop” caused by the output resistance when a load is applied allows the regulator to respond smoothly to load transients with no undershoot from the load line. This can be seen in Figure 31 and Figure 36.

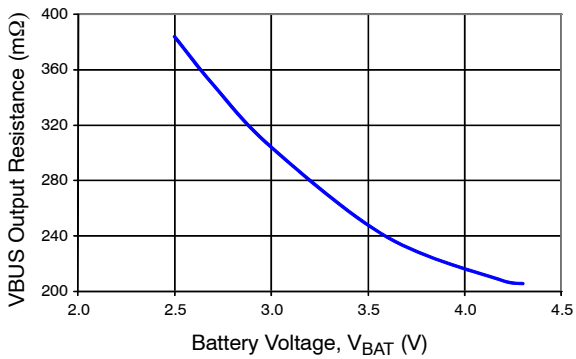


Figure 36. Output Resistance (R_{OUT})

V_{BUS} as a function of I_{LOAD} can be computed when the regulator is in PWM Mode (continuous conduction) as:

$$V_{OUT} = 5.07 - R_{OUT} \times I_{LOAD} \quad \text{(eq. 1)}$$

At V_{BAT} = 3.0 V and I_{LOAD} = 300 mA, V_{BUS} drops to:

$$V_{OUT} = 5.07 - 0.30 \times 0.3 = 4.98\ V \quad \text{(eq. 2)}$$

At V_{BAT} = 3.6 V and I_{LOAD} = 500 mA, V_{BUS} drops to:

$$V_{OUT} = 5.07 - 0.24 \times 0.5 = 4.95\ V \quad \text{(eq. 3)}$$

PFM Mode

If V_{BUS} > $VREF_{BOOST}$ (nominally 5.07 V) when the minimum off−time ends, the regulator enters PFM Mode. Boost pulses are inhibited until V_{BUS} < $VREF_{BOOST}$. The minimum on−time is increased to enable the output to pump up sufficiently with each PFM boost pulse. Therefore, the regulator behaves like a constant on−time regulator, with the bottom of its output voltage ripple at 5.07 V in PFM Mode.

Table 12. BOOST PWM OPERATING STATES

Mode	Description	Invoked When
LIN	Linear Startup	V_{BAT} > V_{BUS}
SS	Boost Soft−Start	V_{BUS} < V_{BST}
BST	Boost Operating Mode	V_{BAT} > $UVLO_{BST}$ and SS Completed

Startup

When the boost regulator is shut down, current flow is prevented from V_{BAT} to V_{BUS}, as well as reverse flow from VBUS to VBAT.

LIN State

When the boost is enabled by setting OPA_MODE = 1 and HZ_MODE = 0, if V_{BAT} > $UVLO_{BST}$, the regulator first attempts to bring PMID to within approximately 500 mV of V_{BAT} using an internal 1100 mA limited current source from V_{BAT}. If PMID has not achieved V_{BAT}−500 mV after 8 ms, a fault state is declared.

SS State

Once PMID > V_{BAT} − 500 mV, Q3 begins to close, connecting VBUS to PMID, and the boost regulator begins switching with a reduced peak current limit of 50% of it nominal current limit for up to 128 μs. After the 128 μs, the peak current limit is increased to 100%.

If the output fails to achieve 95% of its setpoint within 4 ms, while the peak current limit is 100%, a restart cycle is initiated. Up to 15 restart attempts will be made before a fault is declared.

Once the voltage reaches 95%, the device begins to increment the voltage in 50 mV steps, every 512 μsec, until full regulation is achieved.

During the soft start state, the high−side FET (Q1) is operated asynchronously until PMID > V_{BAT}.

BST State

This is the normal operating mode of the regulator. The regulator uses a calculated t_{OFF}, modulated t_{ON} scheme. The calculated t_{OFF} is proportional to V_{IN}/V_{OUT}, which keeps the regulator's switching frequency reasonably constant in CCM. $t_{ON(MIN)}$ is proportional to V_{BAT} and is a higher value if the inductor current reached 0 before $t_{OFF(MIN)}$ in the prior cycle.

To ensure V_{BUS} does not overshoot the regulation point, the boost switch remains off as long as V_{BUS} > $VREF_{BOOST}$.

If a USB peripheral hot insertion causes VBUS to dip below V_{BAT}, the device will commence a restart without faulting.

Boost Faults

If a BOOST fault occurs:

1. The STAT pin pulses
2. OPA_MODE bit is reset
3. The power stage is in High−Impedance Mode
4. The FAULT bits (REG0[2:0]) are set per Table 13.

Restart After Boost Faults

OPA_MODE is reset on boost faults. Boost Mode can only be re−enabled by setting the OPA_MODE bit.

Table 13. FAULT BITS DURING BOOST MODE

Fault Bit			Fault (REG00h[2:0]) Description
B2	B1	B0	
0	0	0	Normal (no fault)
0	0	1	V_{BUS} > $VBUS_{OVP}$
0	1	0	V_{BUS} fails to achieve the voltage required to advance to the next state during soft−start or sustained (> 50 μs) current limit during the BST state
0	1	1	V_{BAT} < $UVLO_{BST}$
1	0	0	NA: This code does not appear
1	0	1	Thermal shutdown
1	1	0	Timer fault; all registers reset
1	1	1	NA: This code does not appear

I²C INTERFACE

The FAN54063's serial interface is compatible with Standard, Fast, Fast Plus, and High−Speed Mode I²C bus specifications. The FAN54063 SCL line is an input and the SDA line is a bi−directional open−drain output; it can only pull down the bus when active. The SDA line only pulls LOW during data reads and when signaling ACK. All data is shifted in MSB (bit 7) first.

Slave Address

Table 14. I²C SLAVE ADDRESS BYTE

7	6	5	4	3	2	1	0
1	1	0	1	0	1	1	R/$\overline{W}$

In hex notation, the slave address assumes a 0 LSB. The hex slave address is D6 for all parts in the family. Other slave addresses can be accommodated upon request. *Contact a* ***onsemi*** *representative.*

Bus Timing

Shown in Figure 37, data is normally transferred when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL to allow ample time for the data to set up before the next SCL rising edge.

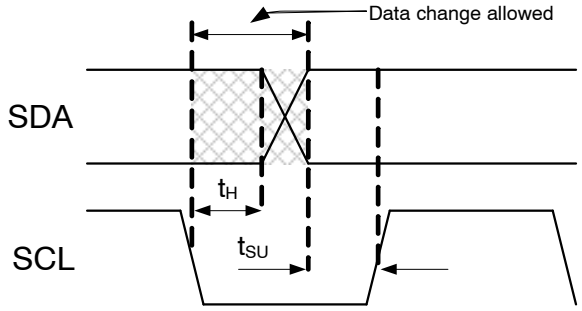


Figure 37. Data Transfer Timing

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a START condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH, as shown in Figure 38.

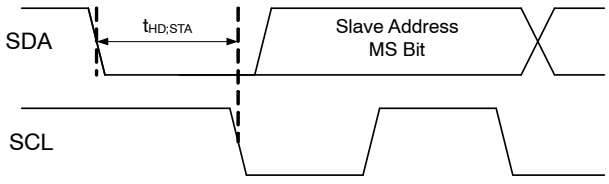


Figure 38. Start Bit

Transactions end with a STOP condition, which is SDA transitioning from 0 to 1 with SCL HIGH, as shown in Figure 39.

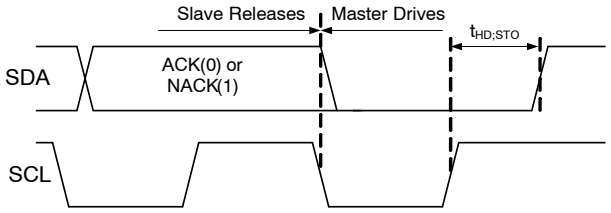


Figure 39. Stop Bit

During a read from the FAN54063, the master issues a Repeated Start after sending the register address and before resending the slave address. The Repeated Start is a 1−to−0 transition on SDA while SCL is HIGH, as shown in Figure 40.

High−Speed (HS) Mode

The protocols for High−Speed (HS), Low−Speed (LS), and Fast−Speed (FS) Modes are identical except the bus speed for HS Mode is 3.4 MHz. HS Mode is entered when the bus master sends the HS master code 00001XXX after a start condition. The master code is sent in Fast or Fast Plus Mode (less than 1 MHz clock); slaves do not ACK the transmission.

The master then generates a repeated start condition that causes all slaves on the bus to switch to HS Mode. The master then sends I²C packets, as described above, using the HS Mode clock rate and timing.

The bus remains in HS Mode until a stop bit is sent by the master. While in HS Mode, packets are separated by repeated start conditions (Figure 40).

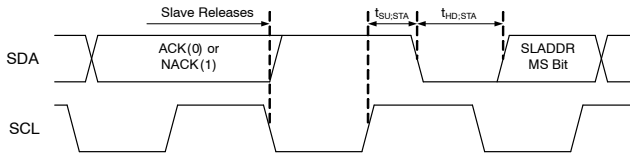


Figure 40. Repeated Start Timing

Read and Write Transactions

The figures below outline the sequences for data read and write. Bus control is signified by the shading of the packet, defined as Master Drives Bus and Slave Drives Bus. All addresses and data are MSB first.

Table 15. BIT DEFINITIONS FOR FIGURE 41– FIGURE 44

Symbol	Definition
S	START, see Figure 38
A	ACK. The slave drives SDA to 0 to acknowledge the preceding packet
$\overline{A}$	NACK. The slave sends a 1 to NACK the preceding packet
R	Repeated START, see Figure 40
P	STOP, see Figure 39

Multi−Byte (Sequential) Read and Write Transactions

Sequential Write

The Slave Address, Reg Addr address, and the first data byte are transmitted to the FAN54063 in the same way as in a byte write Figure 41. However, instead of generating a Stop condition, the master transmits additional bytes that are written to consecutive sequential registers after the falling edge of the eighth bit. After the last byte written and its ACK bit received, the master issues a STOP bit. The IC contains an 8−bit counter that increments the address pointer after each byte is written.

Sequential Read

Sequential reads are initiated in the same way as a single−byte read , except that once the slave transmits the first data byte, the master issues an acknowledge instead of a STOP condition. This directs the slave's I^2C logic to transmit the next sequentially addressed 8−bit word. The FAN54063 contains an 8−bit counter that increments the address pointer after each byte is read, which allows the entire memory contents to be read during one I^2C transaction.

Figure 41. Single−Byte Write Transaction

Figure 42. Single−Byte Read Transaction

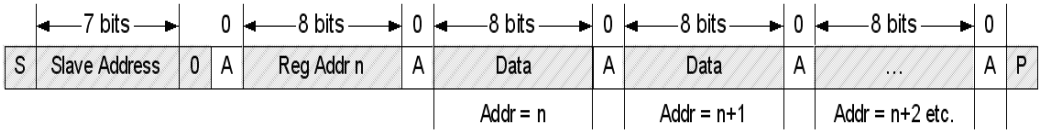


Figure 43. Multi−Byte (Sequential) Write Transaction

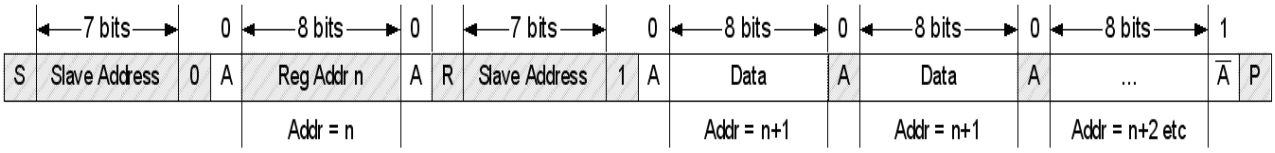


Figure 44. Multi−Byte (Sequential) Read Transaction

REGISTER DESCRIPTIONS

The Twelve user−accessible IC registers are defined in Table 17.

Table 16. I²C REGISTER MAP

Register		BIT NAME							
Name	**REG#**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CONTROL0	0H	TMR_RST	EN_STAT	STAT		BOOST	FAULT		
CONTROL1	1H	IBUSLIM		VLOWV		TE	CE#	HZ_MODE	OPA_MODE
OREG	2H	OREG						DBAT_B	EOC
IC_INFO	3H	Vendor Code		PN			REVISION		
IBAT	4H	RESET	IOCHARGE				ITERM		
VBUS_CONTROL	5H	Reserved	PROD	IO_LEVEL	VBUS_CON	VLIM	VBUSLIM		
SAFETY	6H	ISAFE				VSAFE			
POST_CHARGING	7H	Reserved	Reserved	VBUS_LOAD		PC_EN	PC_IT		
MONITOR0	10H	ITERM_CMP	VBAT_CMP	LINCHG	T_120	ICHG	IBUS	VBUS_VALID	CV
MONITOR1	11H	GATE	VBAT	POK_B	DIS_LEVEL	NOBAT	PC_ON	Reserved	Reserved
NTC	12H	Reserved		TEMP_DIS	NTC_OK	NTC4	NTC3	NTC2	NTC1
WD_CONTROL	13H	Reserved	Reserved	Reserved	Reserved	Reserved	EN_REG	WD_DIS	Reserved
RESTART	FA	RESTART							

Table 17. REGISTER BIT DEFINITIONS

This table defines the operation of each register bit. Default values are in **bold** text.

Bit	Name	Value	Type	Description
CONTROL0				**REGISTER ADDRESS: 00H** **DEFAULT VALUE = 0100 0000 (40h)**
7	TMR_RST	**0**	W	Writing a 1 resets the t_{32S} timer; writing a 0 has no effect. Reading this bit always returns 0
6	EN_STAT	0	R/W	Prevents STAT pin from going LOW during charging; STAT pin still pulses to enunciate faults
		1		Enables STAT pin to be LOW when IC is charging
5:4	STAT	**00**	R	**Bit 5 / Bit 4 / STAT Description** **0 / 0 / Standby** 0 / 1 / PWM enabled. Charging is occurring if CE# = 0 1 / 0 / Charge Done 1 / 1 / Fault
3	BOOST	**0**	R	IC is not in Boost Mode
		1		IC is in Boost Mode
2:0	FAULT	**000**	See table to the right.	**Fault Bit 2 / Fault Bit 1 / Fault Bit 0 / Type / FAULT Description** 0 / 0 / 0 / R / Normal (No Fault) 0 / 0 / 1 / R / VBUS OVP 0 / 1 / 0 / RC / Sleep Mode 0 / 1 / 1 / R / Poor Input Source 1 / 0 / 0 / R / Battery OVP 1 / 0 / 1 / R / Thermal Shutdown 1 / 1 / 0 / RC / Timer Fault 1 / 1 / 1 / RC / No Battery For Boost Mode faults, see Table 13.
CONTROL1				**REGISTER ADDRESS: 01H** **DEFAULT VALUE = 0011 0100 (34h)**
7:6	IBUSLIM	**00**	R/W	Input current limit **Bit 7 / Bit 6 / I_{BUSLIM} (mA)** **0 / 0 / 475** 0 / 1 / 760 1 / 0 / 1080 1 / 1 / No Limit
5:4	VLOWV	**11**	R/W	Weak battery voltage threshold **Bit 5 / Bit 4 / V_{LOWV} (V)** 0 / 0 / 3.4 0 / 1 / 3.5 1 / 0 / 3.6 **1 / 1 / 3.7**
3	TE	**0**	R/W	Setting the TE bit to a 1 will enable Charge Termination.
2	CE#	**1**	R/W	This is an active low bit and by setting the bit to a “0” will enable Charging. When the bit is reset, it will return to the “1” state and charging will be disabled.
1	HZ_MODE	**0**	R/W	Setting this bit to a “1” puts the device in High Impedance mode.	See Table 11
0	OPA_MODE	**0**	R/W	The device is in Charge Mode when the OPA_MODE bit = 0 and in Boost Operation when the bit = 1.	

Table 17. REGISTER BIT DEFINITIONS (continued)

This table defines the operation of each register bit. Default values are in **bold** text.

Bit	Name	Value	Type	Description
OREG				**REGISTER ADDRESS: 02H** **DEFAULT VALUE = 0000 1000 (08h)**
7:2	OREG	**000010**	R/W	Charger output "float" voltage; programmable from 3.51 to 4.45 V in 20 mV increments. **Dec / Hex / V_{OREG}**: 0/00/3.51; 1/01/3.53; **2/02/3.55**; 3/03/3.57; 4/04/3.59; 5/05/3.61; 6/06/3.63; 7/07/3.65; 8/08/3.67; 9/09/3.69; 10/0A/3.71; 11/0B/3.73; 12/0C/3.75; 13/0D/3.77; 14/0E/3.79; 15/0F/3.81; 16/10/3.83; 17/11/3.85; 18/12/3.87; 19/13/3.89; 20/14/3.91; 21/15/3.93; 22/16/3.95; 23/17/3.97; 24/18/3.99; 25/19/4.01; 26/1A/4.03; 27/1B/4.05; 28/1C/4.07; 29/1D/4.09; 30/1E/4.11; 31/1F/4.13; 32/20/4.15; 33/21/4.17; 34/22/4.19; 35/23/4.21; 36/24/4.23; 37/25/4.25; 38/26/4.27; 39/27/4.29; 40/28/4.31; 41/29/4.33; 42/2A/4.35; 43/2B/4.37; 44/2C/4.39; 45/2D/4.41; 46/2E/4.43; 47–63/2F–3F/4.45
1	DBAT_B	**0**	R/W	Indicates that the IC detected a dead battery after VBUS_POR.
		1		The IC sets this bit to 1 if a dead battery ($V_{BAT} < V_{SHORT}$) was not detected at VBUS_POR. Writing a "1" or a "0" to this bit does not affect charger operation. The bit state will not change until the next VBUS POR.
0	EOC	**0**	R/W	If TE = "1", and no battery is detected at I_{TERM}, the IC turns off the PWM for t_{INT}, then resumes charging and retries Battery Detection. If the battery is still absent, the process repeats with the "No Battery" fault re−enunciated, and sets the charging parameters to the default values (see Charge State Flow Chart)
		1		If no battery is detected when a full battery (end of charge) is reached, the PWM charger stays on, allowing the host processor to continue to run with no battery.
IC_INFO				**REGISTER ADDRESS: 03H** **DEFAULT VALUE = 1001 0XXX (9Xh)**
7:6	Vendor Code	**10**	R	Identifies **onsemi** as the IC supplier
5:3	PN	**010**	R	Part number bits, *see Ordering Information*
2:0	REV		R	IC Revision bits
IBAT				**REGISTER ADDRESS: 04H** **DEFAULT VALUE = 1000 0001 (81h)**
7	RESET	1	W	**Conditions** / **Functionality** Valid V_{BUS}, $V_{BAT} > V_{LOWV}$: Setting the RESET bit clears all registers (except SAFETY and CE#) including WD_DIS and HZ_MODE. Valid V_{BUS}, $V_{BAT} < V_{LOWV}$: Setting the RESET bit clears all registers (except SAFETY) including WD_DIS, HZ_MODE and CE#. Absent V_{BUS}: Setting the RESET bit clears all registers (except SAFETY and CE#) including WD_DIS and HZ_MODE. Writing a 0 has no effect; read returns 1
6:3	IOCHARGE	**0000**	R/W	Programs the typical charge current (550 mA default) **Bit 6 5 4 3 / $I_{OCHARGE}$ (mA)** **0 0 0 0 / 550**; 0 0 0 1 / 650; 0 0 1 0 / 750; 0 0 1 1 / 850; 0 1 0 0 / 950; 0 1 0 1 / 1,050; 0 1 1 0 / 1,150; 0 1 1 1 / 1,250; 1 0 0 0 / 1,350; 1 0 0 1 / 1,450; 1010–1111 / 1,550

Table 17. REGISTER BIT DEFINITIONS (continued)

This table defines the operation of each register bit. Default values are in **bold** text.

Bit	Name	Value	Type	Description
IBAT				**REGISTER ADDRESS: 04H** **DEFAULT VALUE = 1000 0001 (81h)**
2:0	ITERM	**001**	R/W	Sets the current used for charging termination **Bit 2 / 1 / 0 — I_{TERM} (mA)** 0 0 0 — 50 **0 0 1 — 100** 0 1 0 — 150 0 1 1 — 200 1 0 0 — 250 1 0 1 — 300 1 1 0 — 350 1 1 1 — 400
VBUS_CONTROL				**REGISTER ADDRESS: 05H** **DEFAULT VALUE = 001X X100**
7	Reserved	**0**	R	This bit always returns 0
6	PROD	**0**	R/W	Charger operates in Normal Mode.
		1		Charger operates in Production Test Mode.
5	IO_LEVEL	0	R/W	Battery current is controlled by IOCHARGE and IBUSLIM bits while Fast Charging. During Precharge Mode, battery current is limited to 450 mA when $I_{OCHARGE} \leq 750$ mA and 730 mA when $I_{OCHARGE} > 750$ mA. IBUSLIM bits must be set to “10” or “11” or IO_LEVEL current will remain at 200 mA.
		1		Battery current control is set to 200 mA for Fast Charge and Precharge Mode.
4	VBUS_CON		R	1 Indicates that V_{BUS} is above 4.4 V (rising) or 3.7 V (falling). When VBUS_CON changes from 0 to 1, a STAT pulse occurs.
3	VLIM	0	R	VBUS control loop is not active (V_{BUS} is able to stay above V_{BUSLIM})
		1		VBUS control loop is active and V_{BUS} is being regulated to V_{BUSLIM}
2:0	VBUSLIM	**100**	R/W	VBUS control voltage reference **Bit 2 / 1 / 0 — VBUSLIM (V)** 0 0 0 — 4.213 0 0 1 — 4.293 0 1 0 — 4.373 0 1 1 — 4.453 **1 0 0 — 4.533** 1 0 1 — 4.613 1 1 0 — 4.693 1 1 1 — 4.773
SAFETY				**REGISTER ADDRESS: 06H** **DEFAULT VALUE = 0100 1010 (4Ah)**
7:4	ISAFE	**0100**	R/W	Sets the maximum IOCHARGE value used by the control circuit **Bit 7 / 6 / 5 / 4 — IOCHARGE(MAX) (mA)** 0 0 0 0 — 550 0 0 0 1 — 650 0 0 1 0 — 750 0 0 1 1 — 850 **0 1 0 0 — 950** 0 1 0 1 — 1,050 0 1 1 0 — 1,050 0 1 1 1 — 1,250 1 0 0 0 — 1,350 1 0 0 1 — 1,450 1010−1111 — 1,550

Table 17. REGISTER BIT DEFINITIONS (continued)
This table defines the operation of each register bit. Default values are in **bold** text.

Bit	Name	Value	Type	Description
SAFETY			**REGISTER ADDRESS: 06H**	**DEFAULT VALUE = 0100 1010 (4Ah)**
3:0	VSAFE	**1010**	R/W	Sets the maximum V_{OREG} used by the control circuit **Bit 3 2 1 0 — VOREG(MAX) (V)** 0 0 0 0 — 4.21 0 0 0 1 — 4.23 0 0 1 0 — 4.25 0 0 1 1 — 4.27 0 1 0 0 — 4.29 0 1 0 1 — 4.31 0 1 1 0 — 4.33 0 1 1 1 — 4.35 1 0 0 0 — 4.37 1 0 0 1 — 4.39 **1 0 1 0 — 4.41** 1 0 1 1 — 4.43 1100–1111 — 4.45
POST_CHARGING			**REGISTER ADDRESS: 07H**	**DEFAULT VALUE = 0000 0001 (01h)**
7:6	Reserved	**00**	R	These bits always return 0
5:4	VBUS_LOAD	**00**	R/W	After charger termination, in the charge done state, these bits control VBUS loading to improve detection of AC power removal from the AC adapter. **[5:4] VBUS Loading in Charge Done State:** 00 None 01 Load VBUS for 4 ms every two seconds 10 Load VBUS for 131 ms every two seconds 11 Load VBUS for 135 ms every two seconds
3	PC_EN	**0**	R/W	Post charging or background charging feature is disabled
		1		Post charging or background charging feature is enabled
2:0	PC_IT	**001**	R/W	Sets the termination current for post charging **Bit 2 1 0 — PC_IT (mA)** 0 0 0 — 50 **0 0 1 — 100** 0 1 0 — 150 0 1 1 — 200 1 0 0 — 250 1 0 1 — 300 1 1 0 — 350 1 1 1 — 400
MONITOR0			**REGISTER ADDRESS: 10H**	**DEFAULT VALUE = XXXX XXXX**
7	ITERM_CMP		R	ITERM comparator output, 1 when $I_{CHARGE} > I_{TERM}$ reference
6	VBAT_CMP		R	Output of VBAT comparator, 1 when $V_{BAT} < V_{BUS}$
5	LINCHG		R	1 when 30 mA linear charger ON ($V_{BAT} < V_{SHORT}$)
4	T_120		R	Thermal regulation comparator, 1 when the die temperature is greater than 120°C. If battery is being charged in Precharge mode, the charge current is limited to 200 mA and in Fast Charge, 550 mA.
3	ICHG		R	0 indicates the ICHARGE loop is controlling the battery charge current.
2	IBUS		R	0 indicates the IBUS (input current) loop is controlling the battery charge current.
1	VBUS_VALID		R	1 indicates V_{BUS} has passed validation and is capable of charging.
0	CV		R	1 indicates the constant−voltage loop (OREG) is controlling the charger and all current limiting loops have released.
MONITOR1			**REGISTER ADDRESS: 11H**	**DEFAULT VALUE = XX1X XX00**
7	GATE		R	The GATE bit indicates the state of the GATE pin. If the bit is “0”, the pin is low, driving the PFET, Q5 on. A “1” will disable Q5, but current can still flow from battery to the system through Q5’s body diode.
6	VBAT		R	A “1” indicates $V_{BAT} > V_{LOWV}$. A “0” indicates $V_{BAT} < V_{LOWV}$ in fast charging.

Table 17. REGISTER BIT DEFINITIONS (continued)
This table defines the operation of each register bit. Default values are in **bold** text.

Bit	Name	Value	Type	Description	
MONITOR1				**REGISTER ADDRESS: 11H**	**DEFAULT VALUE = XX1X XX00**
5	POK_B	**1**	R/W	POK_B indicates the state of the POK_B pin (see section on POK_B). This bit can be set to a 1 if VBAT has fallen below V_{LOWV}, in turn the open drain $\overline{POK}$_B pin will be Hi−Z.	
4	DIS_LEVEL		R	This pin indicates the state of the DIS pin. A “1” indicates the DIS pin is high and the device is in a Hi−Z state on the input and the PWM controller is not running.	
3	NOBAT		R	A “1” on this bit indicates that the device has determined there is no battery connected.	
2	PC_ON		R	A “1” on this bit indicates that Post charging (background charging) is in progress.	
1:0	Reserved	00	R	These bits always return 0.	
NTC				**REGISTER ADDRESS: 12H**	**DEFAULT VALUE = 000X XXXX**
7:6	Reserved	00	R	These bits always return 0.	
5	TEMP_DIS	**0**	R/W	NTC Temperature measurement results affect charge parameters.	
		1		NTC Temperature measurement results do not affect charge. Temperature measurements continue to be updated every second in the NTC1−4 monitor bits.	
4	NTC_OK		R	0 if NTC is either shorted to GND, open, or shorted to REF.	
3	NTC4		R	1 indicates that NTC is above the T4 threshold.	See Battery Temperature (NTC) Monitor
2	NTC3		R	1 indicates that NTC is above the T3 threshold.	
1	NTC2		R	1 indicates that NTC is above the T2 threshold.	
0	NTC1		R	1 indicates that NTC is above the T1 threshold.	
WD_CONTROL				**REGISTER ADDRESS: 13H**	**DEFAULT VALUE = 0110 1110 (6Eh)**
7	Reserved	**0**	R	This bit always returns 0	
6	Reserved	**1**	R	This bit always returns 1	
5	Reserved	**1**	R	This bit always returns 1	
4	Reserved	**0**	R	This bit always returns 0	
3	Reserved	**1**	R	This bit always returns 1	
2	EN_VREG	**1**	R/W	The EN_VREG defaults to a “1” enabling the regulator. To disable the regulator, set the bit to a “0”.	
1	WD_DIS	**1**	R/W	A “1” disables the Watchdog (t_{32s}) timer. Setting the bit to a “0” will enable the timers (See Safety Timer Section for further information).	
0	Reserved	0	R	This bit always returns 0	
RESTART				**REGISTER ADDRESS: FAH**	**DEFAULT VALUE = 1111 1111 (FFh)**
7:0	RESTART		W	Writing B5h restarts charging when the IC is in the charge done state. This register reads back FF.	

PCB LAYOUT RECOMMENDATION

Bypass capacitors should be placed as close to the IC as possible. In particular, the total loop length for CMID should be minimized to reduce overshoot and ringing on the SW, PMID, and VBUS pins. Power and ground pins should be routed directly to their bypass capacitors using the top copper layer. The copper area connecting to the IC should be maximized to improve thermal performance.

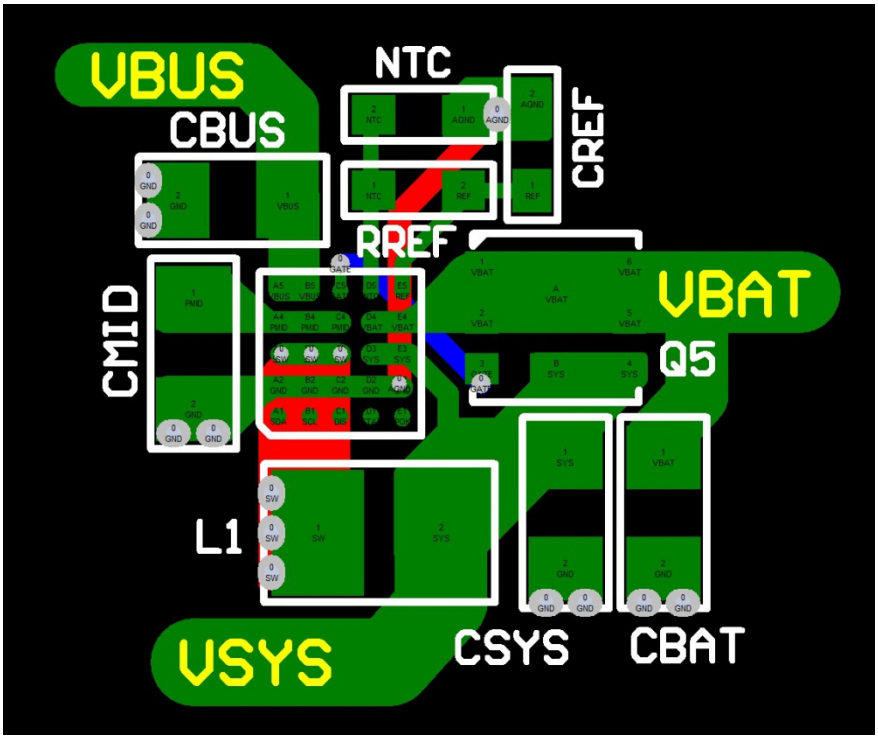


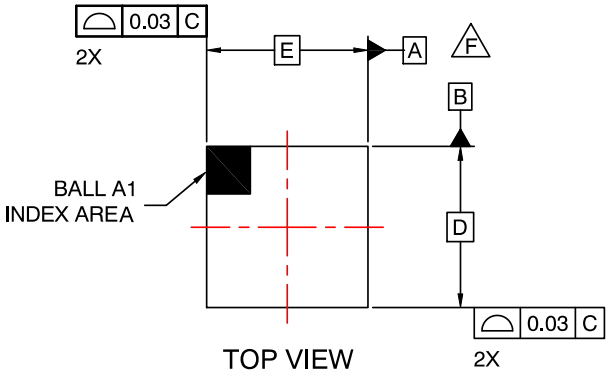
Figure 45. PCB Layout Recommendation

PRODUCT−SPECIFIC DIMENSIONS

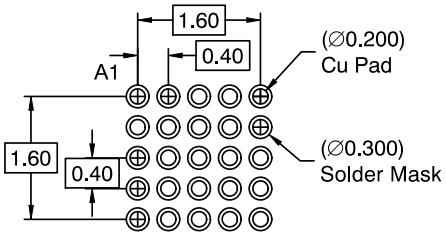
Product	D	E	X	Y
FAN54063UCX	2.40 ±0.030	2.00 ±0.030	0.180	0.380

WLCSP25 2.4x2.0x0.586
CASE 567SQ
ISSUE O

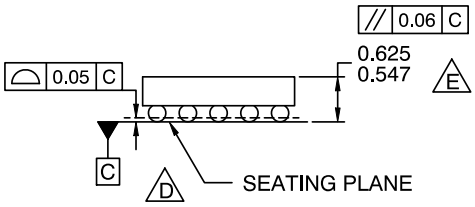
DATE 30 NOV 2016

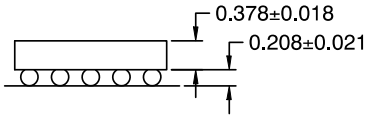


TOP VIEW

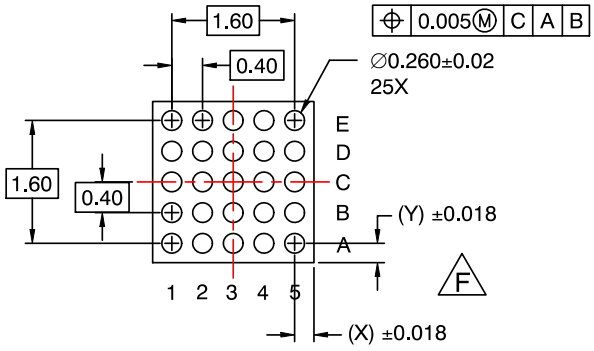


RECOMMENDED LAND PATTERN
(NSMD PAD TYPE)





SIDE VIEWS



BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 1994.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547–625 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

DOCUMENT NUMBER:	**98AON16612G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**WLCSP25 2.4x2.0x0.586**		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales