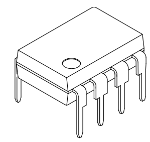
Green-Mode Power Switch

GF001H



PDIP8 9.59x6.6, 2.54P
CASE 646CN

Description

The GF001H is a next−generation, Green−Mode Power Switch. It integrates an advanced current−mode Pulse Width Modulator (PWM) and an avalanche−rugged 700 V SENSEFET® in a single package, allowing auxiliary power designs with higher standby energy efficiency, reduced size, improved reliability, and lower system cost than previous solutions.

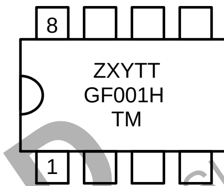
A new frequency modulation reduces EMI emission and built−in synchronized slope compensation allows stable peak−current−mode control over a wide range of input voltage.

Requiring a minimum number of external components, the GF001H provides a solid platform for cost−effective flyback converter design with low standby power consumption.

Features

- Advanced Burst Mode Operation at No−Load Condition
- 700 V High−Voltage JFET Startup Circuit
- Internal Avalanche−Rugged 700 V SENSEFET
- Built−in 5 ms Soft−Start
- Peak−Current−Mode Control
- Cycle−by−Cycle Current Limiting
- Leading−Edge Blanking (LEB)
- Synchronized Slope Compensation
- Frequency Modulation to Attenuating EMI
- Internal Overload / Open−Loop Protection (OLP)
- V_{DD} Under−Voltage Lockout (UVLO)
- V_{DD} Over−Voltage Protection (OVP)
- Internal Auto−Restart Circuit (OLP, VDD OVP)
- Adjustable Peak Current Limit
- This Device is Pb−Free, Halide Free and are RoHS Compliant

MARKING DIAGRAM



Z = Plant Code
X = 1−Digit Year Code
Y = 1−Digit Week Code
TT = 2−Digit Die Run Code
T = Package Type (N: DIP)
M = Manufacture Flow Code
GF001H = Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

APPLICATION DIAGRAM

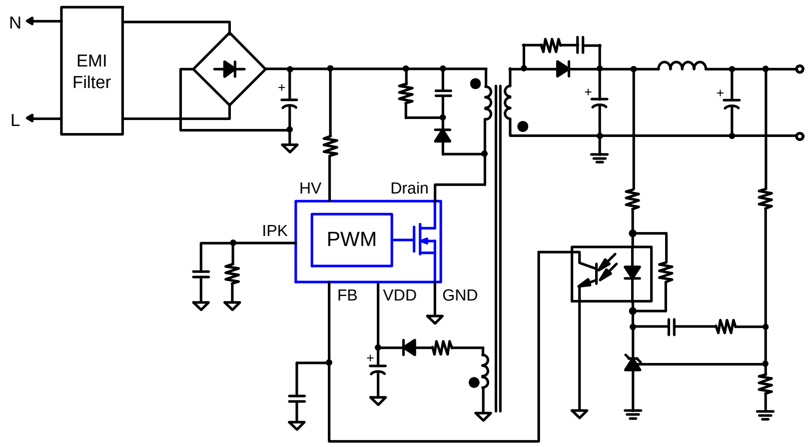


Figure 1. Typical Flyback Application

OUTPUT POWER TABLE (Note 1)

Product	230 V_{AC} ±15% (Note 2)		85 − 265 V_{AC}	
	Adapter (Note 3)	**Open−Frame** (Note 4)	**Adapter** (Note 3)	**Open−Frame** (Note 4)
GF001HN	14 W	20 W	11 W	16 W

1. The maximum output power can be limited by junction temperature.
2. 230 V_{AC} or 100/115 V_{AC} with voltage doublers.
3. Typical continuous power in a non−ventilated enclosed adapter, with sufficient drain pattern of printed circuit board (PCB) as a heat sink, at 50°C ambient.
4. Maximum practical continuous power in an open−frame, design with sufficient drain pattern of printed circuit board (PCB) as a heat sink, at 50°C ambient.

BLOCK DIAGRAM

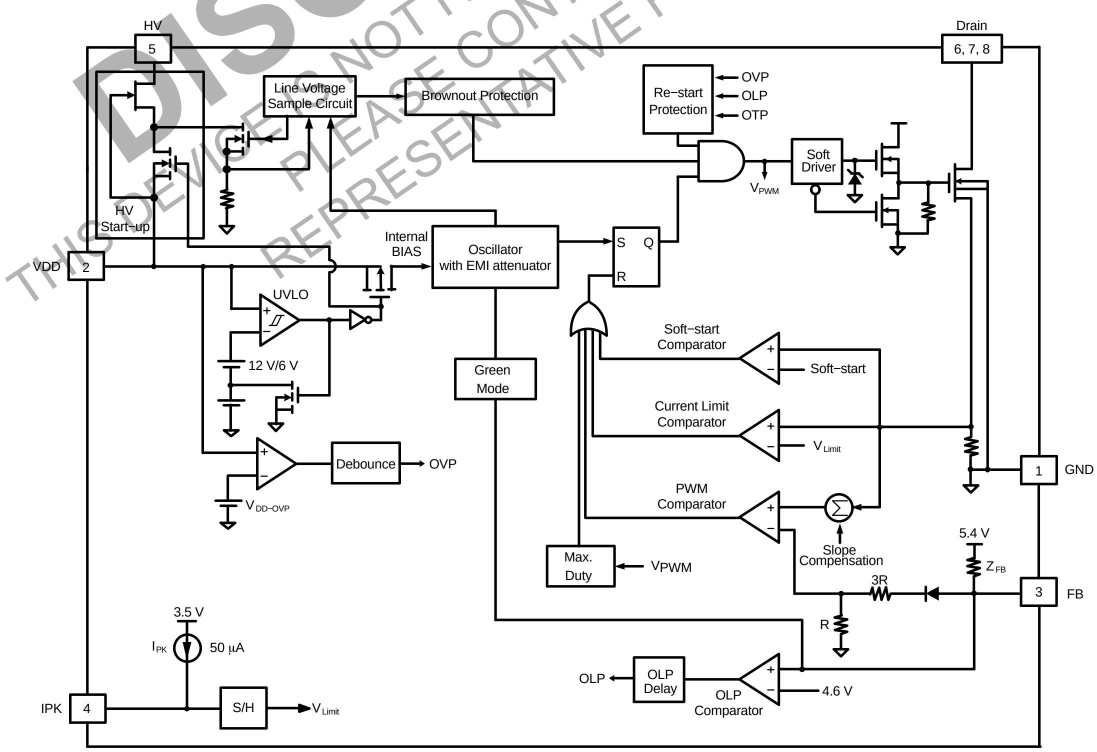


Figure 2. Internal Block Diagram

PIN CONFIGURATION

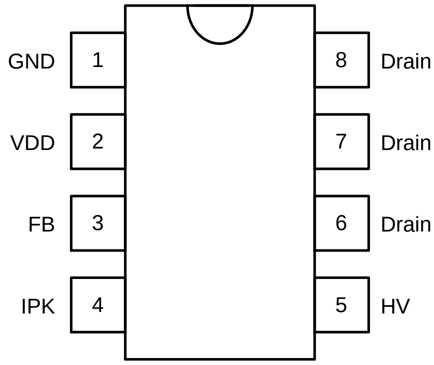


Figure 3. Pin Assignment

PIN DEFINITIONS

Pin #	Name	Description
1	GND	*Ground*. This pin internally connects to the SENSEFET source and signal ground of the PWM controller.
2	VDD	*Supply Voltage of the IC*. Typically the hold−up capacitor connects from this pin to ground. A rectifier diode in series with the transformer auxiliary winding connects to this pin to supply bias during normal operation.
3	FB	*Feedback*. The signal from the external compensation circuit connects to this pin. The PWM duty cycle is determined by comparing the signal on this pin and the internal current−sense signal.
4	IPK	*Adjust Peak Current*. Typically a resistor connects from this pin to the GND pin to program the current−limit level. The internal current source (50 μA) introduces voltage drop across the resistor, which determines the current−limit level of pulse−by−pulse current limit.
5	HV	*Startup*. Typically, resistors in serious from DC line connect to this pin to supply internal bias and to charge the external capacitor connected between the VDD pin and the GND pin during startup. This pin is also used to sense the line voltage for brownout protection.
6	Drain	*SENSEFET Drain*. This pin is designed to directly drive the transformer.
7		
8		

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V_{DRAIN}	Drain Pin Voltage (Note 5, 6)	−	700	V
I_{DM}	Drain Current Pulsed (Note 7)	−	8.0	A
E_{AS}	Single Pulsed Avalanche Energy (Note 8)	−	140	mJ
V_{DD}	DC Supply Voltage	−	25	V
V_{FB}	FB Pin Input Voltage	−0.3	6.0	V
V_{IPK}	IPK Pin Input Voltage	−0.3	6.0	V
V_{HV}	HV Pin Input Voltage	−	700	V
P_D	Power Dissipation (T_A < 50°C)	−	1.5	W
T_J	Operating Junction Temperature	−40	Internally Limited (Note 9)	°C
T_{STG}	Storage Temperature Range	−55	+150	°C
T_L	Lead Soldering Temperature (Wave Soldering or IR, 10 Seconds)	−	+260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
5. All voltage values, except differential voltages, are given with respect to the network ground terminal.
6. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
7. Non−repetitive rating: pulse width is limited by the maximum junction temperature.
8. L = 51 mH, starting T_J = 25°C.
9. Internally limited by Over−Temperature Protection (OTP). Refer to T_{OTP}.

THERMAL RESISTANCE TABLE

Symbol	Parameter	Value	Unit
θ_{JA}	Junction−to−Air Thermal Resistance	86	°C/W
Ψ_{JT}	Junction−to−Package Thermal Resistance (Note 10)	20	°C/W

10. Measured on the package top surface.

ESD CAPABILITY

Symbol	Parameter		Value	Unit
ESD	Human Body Model, JESD22−A114 (Note 11)	All Pins Excluding HV Pin	7	kV
		All Pins Including HV Pin	3	
	Charged Device Model, JESD22−C101 (Note 11)	All Pins Excluding HV Pin	2	
		All Pins Including HV Pin	2	

11. Meets JEDEC standards JESD 22−A114 and JESD 22−C101.

ELECTRICAL CHARACTERISTICS (V_{DD} = 15 V, and T_A = 25°C unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
SENSEFET SECTION (Note 12)						
BV_{DSS}	Drain−Source Breakdown Voltage	V_{DS} = 700 V, V_{GS} = 0 V	700	−	−	V
I_{DSS}	Zero−Gate−Voltage Drain Current	V_{DS} = 700 V, V_{GS} = 0 V	−	−	50	μA
		V_{DS} = 560 V, V_{GS} = 0 V, T_C = 125°C	−	−	200	
$R_{DS(ON)}$	Drain−Source On−State Resistance (Note 12)	V_{GS} = 10 V, I_D = 0.5 A	−	6.0	7.2	Ω
C_{ISS}	Input Capacitance	V_{GS} = 0V, V_{DS} = 25 V, f = 1 MHz	−	550	715	pF
C_{OSS}	Output Capacitance	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	−	38	50	pF
C_{RSS}	Reverse Transfer Capacitance	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	−	17	26	pF
$t_{d(on)}$	Turn−On Delay	V_{DS} = 350 V, I_D = 1.0 A	−	20	50	ns
t_r	Rise Time	V_{DS} = 350 V, I_D = 1.0 A	−	15	40	ns
$t_{d(off)}$	Turn−Off Delay	V_{DS} = 350 V, I_D = 1.0 A	−	55	120	ns
t_f	Fall Time	V_{DS} = 350 V, I_D = 1.0 A	−	25	60	ns
CONTROL SECTION						
VDD SECTION						
V_{DD-ON}	UVLO Start Threshold Voltage		11	12	13	V
$V_{DD-OFF1}$	UVLO Stop Threshold Voltage		5	6	7	V
$V_{DD-OFF2}$	I_{DD-OLP} Enable Threshold Voltage		8	9	10	V
V_{DD-OLP}	V_{DD} Voltage Threshold for HV Startup Turn−On at Protection Mode		5	6	7	V
I_{DD-ST}	Startup Supply Current	V_{DD-ON} − 0.16 V	−	−	30	μA
I_{DD-OP1}	Operating Supply Current with Normal Switching Operation	V_{DD} = 15 V, V_{FB} = 3 V	−	−	3.8	mA
I_{DD-OP2}	Operating Supply Current without Switching Operation	V_{DD} = 15 V, V_{FB} = 1 V	−	−	1.8	mA
I_{DD-OLP}	Internal Sinking Current	V_{DD-OLP} + 0.1 V	40	60	100	μA
V_{DD-OVP}	V_{DD} Over−Voltage Protection		23	24	25	V
$t_{D-VDDOVP}$	V_{DD} Over−Voltage Protection Debounce Time		40	105	170	μs
HV SECTION						
I_{HV}	Supply Current Drawn from HV Pin	HV = 120 V_{DC}, V_{DD} = 0 V with 10 μF	1.2	−	4.7	mA
V_{HV}	Minimum HV Voltage for V_{DD} being charged to V_{DD-ON}	R_{HV} = 0 Ω, T_A = −40°C to 105°C	30	−	−	V
I_{HV-LC}	Leakage Current after Startup	HV = 700 V, V_{DD} = $V_{DD-OFF1}$ + 1 V	−	−	10	μA
V_{DC-ON}	Brown−in Threshold Level (V_{DC})	DC Voltage Applied to HV Pin Through 200 kΩ Resistor	104	114	124	V
V_{DC-OFF}	Brownout Threshold Level (V_{DC})		89	99	109	V
t_{UVP}	Brownout Protection Time		0.8	1.2	1.6	s
OSCILLATOR SECTION						
f_{OSC}	Frequency in Nominal Mode	Center Frequency	94	100	106	kHz
f_M	Frequency Modulation		−	±6	−	kHz
f_{OSC-G}	Green−Mode Frequency		20	23	26	kHz
f_{DV}	Frequency Variation vs. V_{DD} Deviation	V_{DD} = 11 V to 22 V	−	−	5	%
f_{DT}	Frequency Variation vs. Temperature Deviation (Note 12)	T_A = −40°C to 105°C	−	−	5	%

ELECTRICAL CHARACTERISTICS (V_{DD} = 15 V, and T_A = 25°C unless otherwise specified.) (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
FEEDBACK INPUT SECTION						
A_V	Internal Voltage Dividing Factor of FB Pin (Note 12)		1/4.5	1/4.0	1/3.5	V/V
Z_{FB}	Pull−Up Impedance of FB Pin		15	21	27	kΩ
$V_{FB-OPEN}$	FB Pin Pull−Up Voltage	FB Pin Open	5.2	5.4	5.6	V
V_{FB-OLP}	FB Voltage Threshold to Trigger Open−Loop Protection		4.3	4.6	4.9	V
t_{D-OLP}	Delay of FB Pin Open−Loop Protection		46	56	66	ms
V_{FB-N}	FB Voltage Threshold to Exit Green Mode	V_{FB} is Rising	2.4	2.6	2.8	V
V_{FB-G}	FB Voltage Threshold to Enter Green Mode	V_{FB} is Falling	−	V_{FB-N} − 0.2	−	V
V_{FB-ZDC}	FB Voltage Threshold to Enter Zero−Duty State	V_{FB} is Falling	1.1	1.2	1.3	V
$V_{FB-ZDCR}$	FB Voltage Threshold to Exit Zero−Duty State	V_{FB} is Rising	−	V_{FB-ZDC} + 0.1	−	V
IPK PIN SECTION						
$V_{IPK-OPEN}$	IPK Pin Open Voltage		3.0	3.5	4.0	V
V_{IPK-H}	Internal Upper Clamping Voltage of IPK Pin (Note 12)		−	−	3	V
V_{IPK-L}	Internal Lower Clamping Voltage of IPK Pin (Note 12)		1.5	−		V
I_{PK}	Internal Current Source of IPK Pin	T_A = −40°C to 105°C, V_{IPK} = 2.25 V	45	50	55	μA
I_{LMT-H}	Flat Threshold Level of Current Limit for the Highest IPK Level	V_{IPK} = 3 V	0.90	1.00	1.10	A
I_{LMT-L}	Flat Threshold Level of Current Limit for the Lowest IPK Level	V_{IPK} = 1.5 V	0.45	0.50	0.55	A
CURRENT−SENSE SECTION (Note 13)						
t_{PD}	Current Limit Turn−Off Delay (Note 14)		−	100	200	ns
t_{LEB}	Leading−Edge Blanking Time (Note 14)		160	210	260	ns
t_{SS}	Soft−Start Time (Note 12)		−	5	−	ms
GATE SECTION (Note 13)						
DCY_{MAX}	Maximum Duty Cycle		70	−	−	%
OVER TEMPERATURE PROTECTION SECTION (OTP)						
T_{OTP}	Junction Temperature to Trigger OTP (Note 12)		140	−	−	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

12. Guaranteed by design; not 100% tested in production.
13. Pulse test: pulse width ≤ 300 μs, duty ≤ 2%.
14. These parameters, although guaranteed, are tested in wafer−sort process.

TYPICAL CHARACTERISTICS

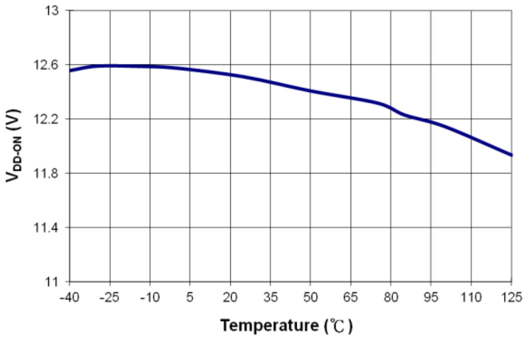


Figure 4. V_{DD-ON} vs. Temperature

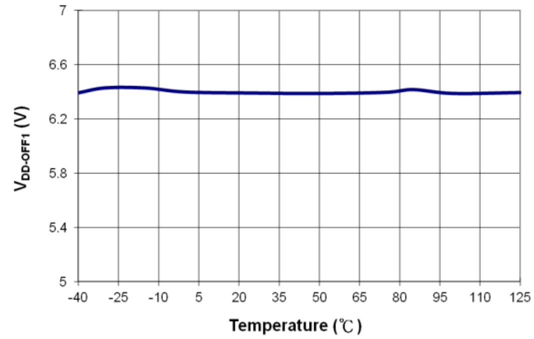


Figure 5. $V_{DD-OFF1}$ vs. Temperature

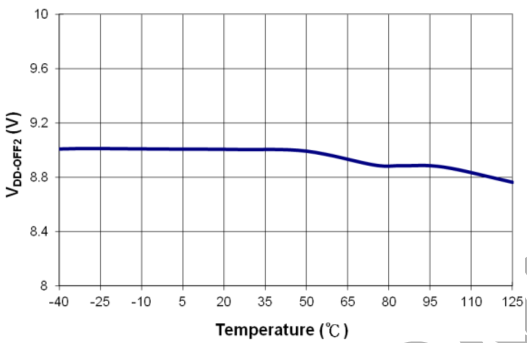


Figure 6. $V_{DD-OFF2}$ vs. Temperature

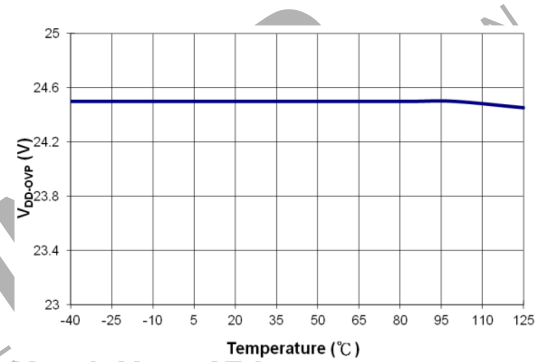


Figure 7. V_{DD-OVP} vs. Temperature

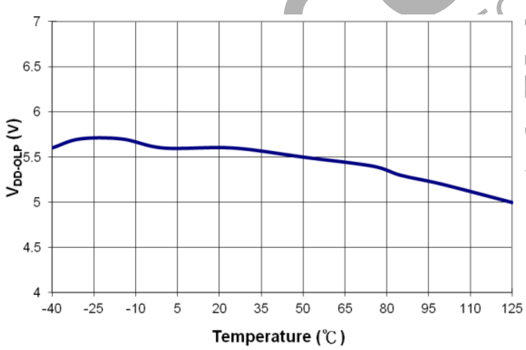


Figure 8. V_{DD-OLP} vs. Temperature

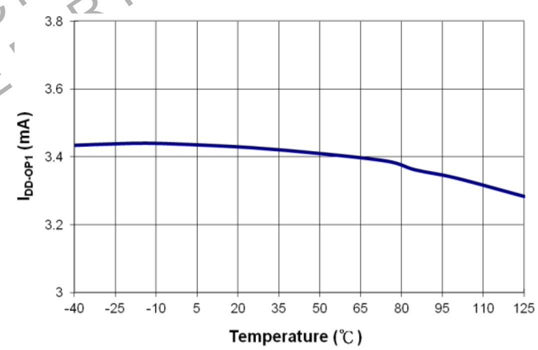


Figure 9. I_{DD-OP1} vs. Temperature

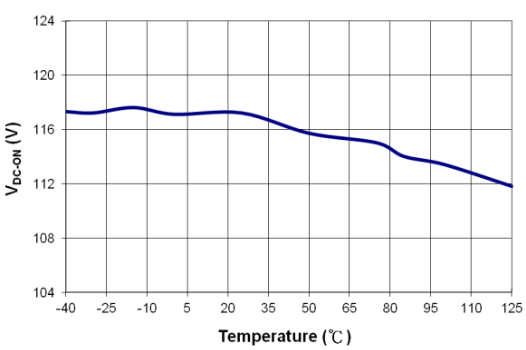


Figure 10. V_{DC-ON} vs. Temperature

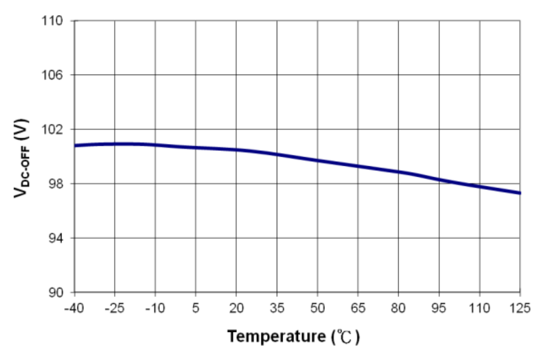


Figure 11. V_{DC-OFF} vs. Temperature

TYPICAL CHARACTERISTICS (Continued)

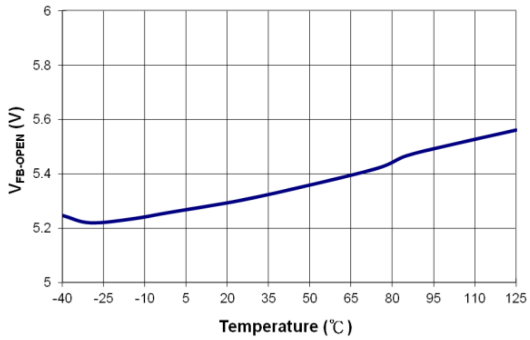


Figure 12. $V_{FB-OPEN}$ vs. Temperature

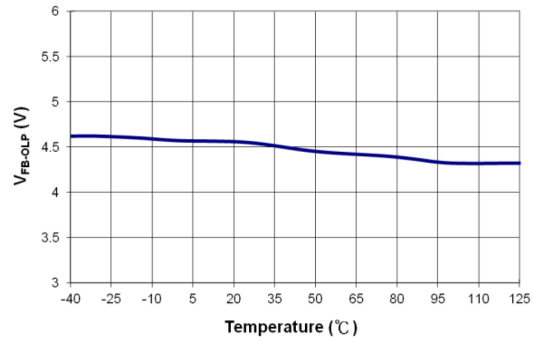


Figure 13. V_{FB-OLP} vs. Temperature

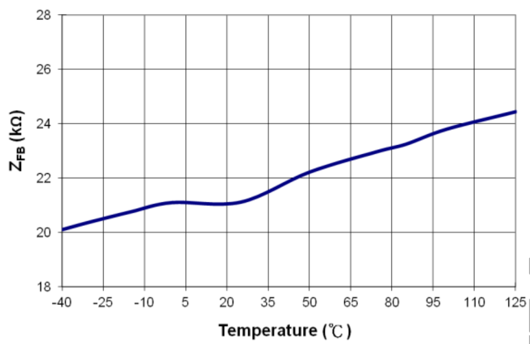


Figure 14. Z_{FB} vs. Temperature

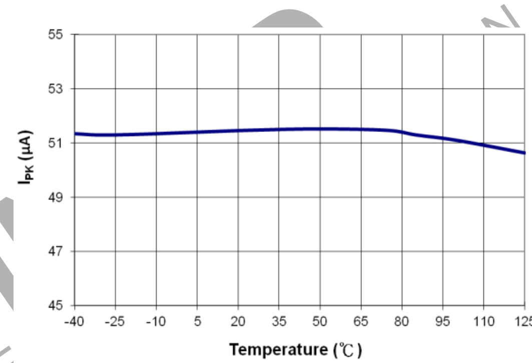


Figure 15. I_{PK} vs. Temperature

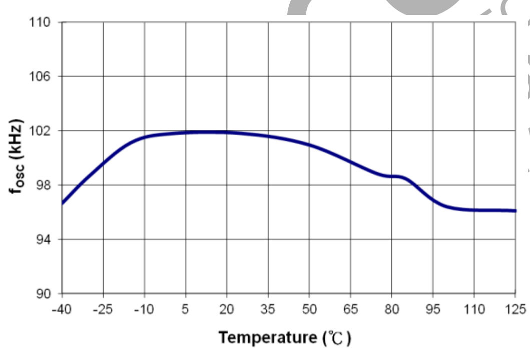


Figure 16. f_{OSC} vs. Temperature

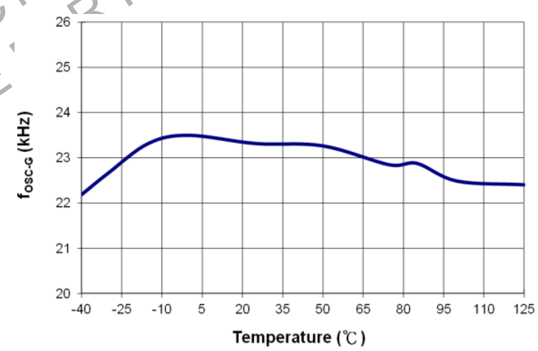


Figure 17. f_{OSC-G} vs. Temperature

FUNCTIONAL DESCRIPTION

Startup Operation

The HV pin is typically connected to the DC link input through one resistor (RHV), as shown in Figure 18. When the DC input voltage is applied, the V_{DD} hold−up capacitor is charged by the line voltage through the resistor. After V_{DD} voltage reaches the turn−on threshold voltage (V_{DD-ON}), the startup circuit charging the V_{DD} capacitor is switched off and V_{DD} is supplied by the auxiliary winding of the transformer. Once the GF001H starts, it continues operation until V_{DD} drops below 6 V ($V_{DD-OFF1}$). The IC startup time with a given DC input voltage is:

$$t_{STARTUP} = R_{HV} \cdot C_{DD} \cdot \ln \frac{V_{DC}}{V_{DC} - V_{DD-ON}} \qquad \text{(eq. 1)}$$

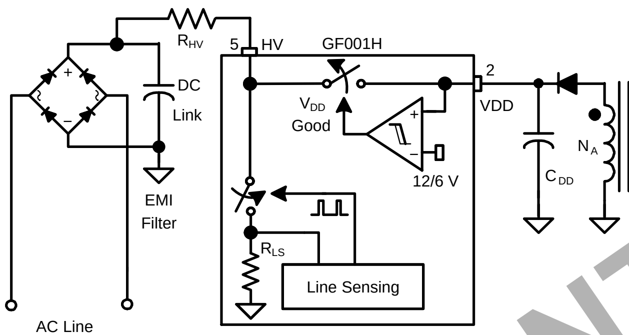


Figure 18. Functional Description

Brown−in/out Function

The HV pin can detect the DC link voltage using a switched voltage divider that consists of external resistor (R_{HV}) and internal resistor (R_{LS}), as shown in Figure 18. The internal DC input voltage sensing circuit detects the input voltage using a sampling circuit and peak− detection circuit. Since the voltage divider causes power consumption when it is switched on, the switching is driven by a signal with a very narrow pulse width to minimize power loss. The sampling frequency is adaptively changed according to the load condition to minimize power consumption in light−load condition.

Based on the detected DC input voltage, brown−in and brownout thresholds are determined. Since the internal resistor (R_{LS}) of the voltage divider is much smaller than R_{HV}, the thresholds are given:

$$V_{BROWN-IN} = \frac{R_{HV}}{200\ k} \cdot V_{DC\_ON} \qquad \text{(eq. 2)}$$

$$V_{BROWNOUT} = \frac{R_{HV}}{200\ k} \cdot V_{DC\_OFF} \qquad \text{(eq. 3)}$$

PWM Control

The GF001H employs current−mode control, as shown in Figure 19. An opto−coupler (such as the H11A817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the R_{sense} resistor makes it possible to control the switching duty cycle. A synchronized positive slope is added to the SENSEFET current information to guarantee stable current−mode control over a wide range of input voltage. The built−in slope compensation stabilizes the current loop and prevents sub−harmonic oscillation.

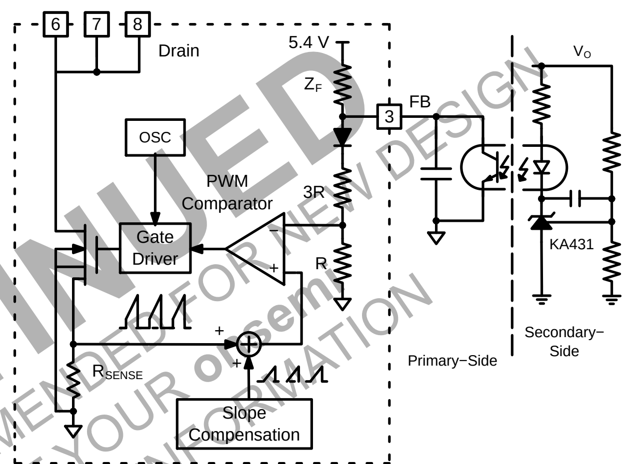


Figure 19. Current Mode Control

Soft−Start

The GF001H has an internal soft−start circuit that progressively increases the pulse−by−pulse current limit level of MOSFET during startup to establish the correct working conditions for transformers and capacitors, as shown in Figure 20. The current limit levels have nine steps, as shown in Figure 21. This prevents transformer saturation and reduces stress on the secondary diode during startup.

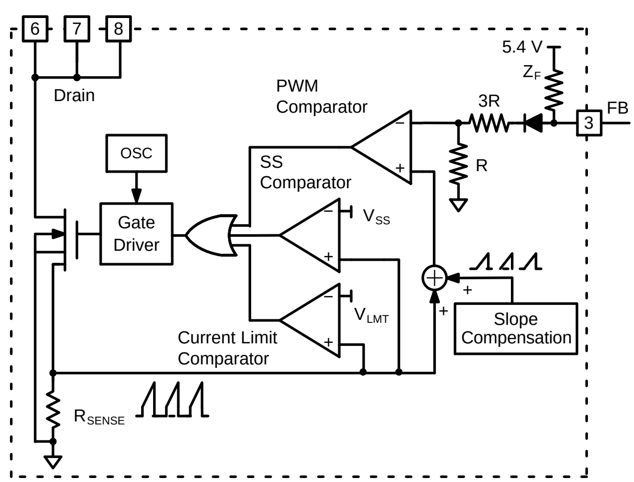


Figure 20. Soft−Start and Current−Limit Circuit

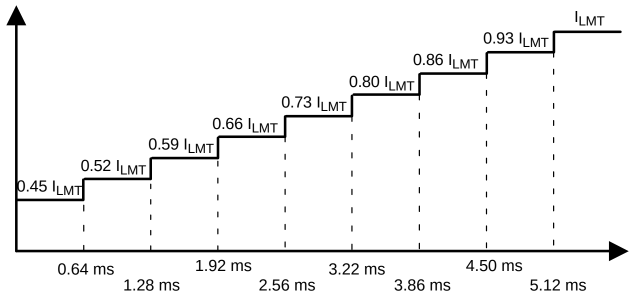


Figure 21. Current Limit Variation During Soft−Start

Adjustable Peak Current Limit

The peak current limit is programmable using a resistor on the IPK pin. The internal current 50 μA source for the IPK pin generates voltage drop across the resistor. The voltage of the IPK pin determines the current−limit level. Since the upper and lower clamping voltage of the IPK pin are 3 V and 1.5 V, respectively; the suggested resistor value is from 30 kΩ to 60 kΩ.

Green Mode

As output load condition is reduced, the switching loss becomes the largest power loss factor. GF001H uses the FB pin voltage to monitor output load condition. As output load decreases, V_{FB} decreases and switching frequency declines, show in Figure 22. Once V_{FB} falls to 2.4 V, the switching frequency varies between 21.5 kHz and 24.5 kHz before Burst Mode operation. At Burst Mode operation, random frequency fluctuation still functions.

As V_{FB} falls below V_{FB-ZDC}, the GF001H enters Burst Mode, where PWM switching is disabled. The output voltage starts to drop, causing the feedback voltage to rise. Once V_{FB} rises above $V_{FB-ZDCR}$, switching resumes. Burst Mode alternately enables and disables switching, thereby reducing switching loss to reduce power consumption, shown in Figure 23.

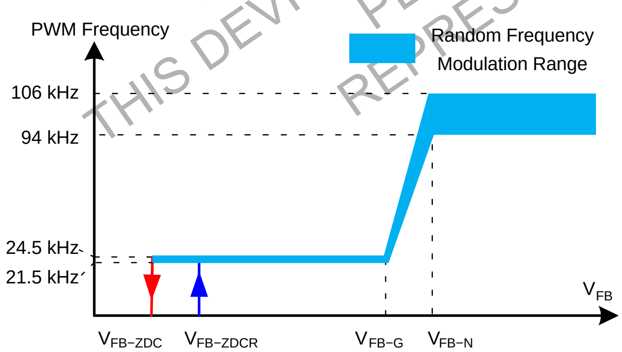


Figure 22. PWM Frequency

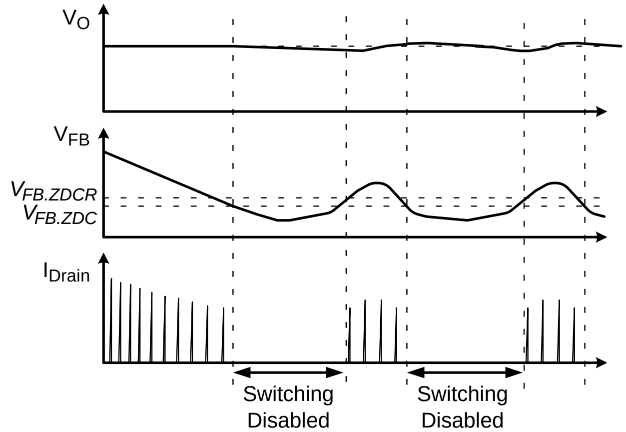


Figure 23. Burst−Mode Operation

Protections

The GF001H provides protection functions that include Overload / Open−Loop Protection (OLP) and Over−Voltage Protection (OVP). All the protections are implemented as Auto−Restart Mode. Once the fault condition is detected, switching is terminated and the SENSEFET remains off, this causes V_{DD} to fall. When V_{DD} falls to 6 V, the protection is reset and HV startup circuit charges V_{DD} up to 12 V voltage, allowing restart.

Open−Loop / Overload Protection (OLP)

Because of the pulse−by−pulse current−limit capability, the maximum peak current through the SENSEFET is limited and maximum input power is limited. If the output consumes more than the limited maximum power, the output voltage (V_O) drops below the set voltage. The current through the opto−coupler LED and the transistor become virtually zero and FB voltage is pulled HIGH, shown in Figure 24. If feedback voltage is above 4.6 V for longer than 56 ms, OLP is triggered. This protection is also triggered when the feedback loop is open due to a soldering defect.

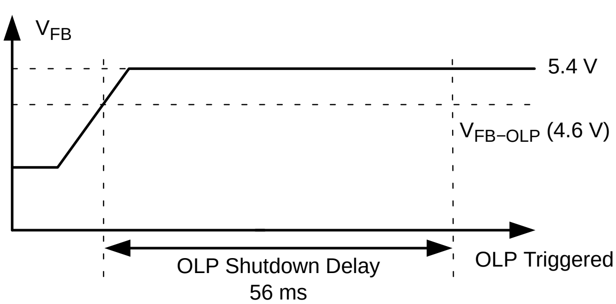


Figure 24. OLP Operation

V_{DD} Over−Voltage Protection (OVP)

If the secondary−side feedback circuit malfunctions or a solder defect causes an opening in the feedback path, the current through the opto−coupler transistor becomes virtually zero. Feedback voltage climbs in a similar manner to the overload situation, forcing the preset maximum current to be supplied to the SMPS until the overload protection triggers. Since more energy than required is provided to the output, the output voltage may exceed the rated voltage before the overload protection triggers, resulting in the breakdown of the devices in the secondary side. To prevent this situation, an OVP circuit is employed. Since V_{DD} voltage is proportional to the output voltage by the transformer coupling, the over−voltage of output is indirectly detected using V_{DD} voltage. The OVP is triggered when V_{DD} voltage reaches 24 V. Debounce time (typically 105 μs) is applied to prevent false triggering by switching noise.

Two−Level UVLO

Since all the protections of the GF001H are auto−restart, the power supply repeats shutdown and restart until the fault condition is removed. GF001H has two−level UVLO, which is enabled when protection is triggered, to delay the re−startup by slowing down the discharge of V_{DD}. This effectively reduces the input power of the power supply during the fault condition, minimizing the voltage/current stress of the switching devices. Figure 25 shows the normal UVLO operation and two−step UVLO operation. When V_{DD} drops to 6 V without triggering the protection, PWM stops switching and V_{DD} is charged up by the HV startup circuit. Meanwhile, when the protection is triggered, GF001H has a different V_{DD} discharge profile. Once the protection is triggered, the IC stops switching and V_{DD} drops. When V_{DD} drops to 9 V, the operating current becomes very small and V_{DD} is slowly discharged. When V_{DD} is naturally discharged down to 6 V, the protection is reset and V_{DD} is charged up by the HV startup circuit. Once V_{DD} reaches 12 V, the IC resumes switching operation.

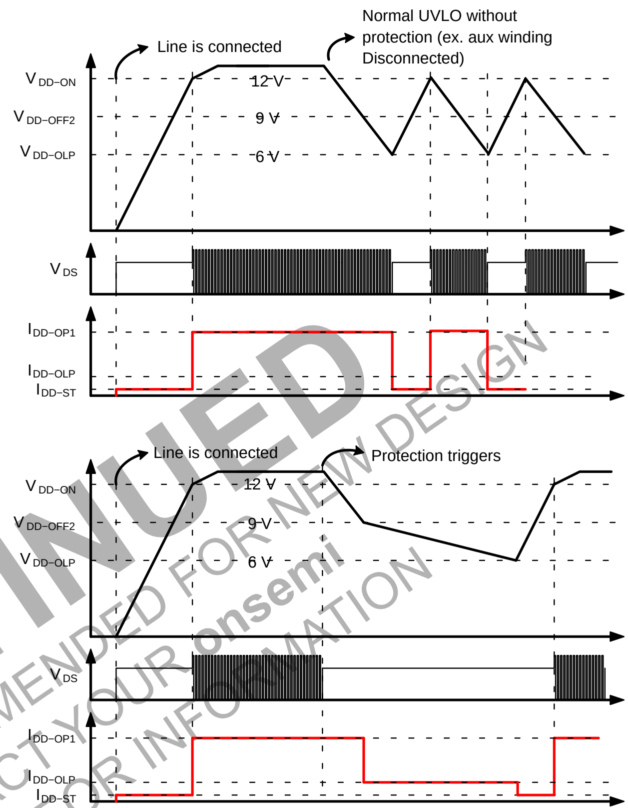


Figure 25. Two−Level UVLO

ORDERING INFORMATION

Part Number	SENSEFET	Operating Temperature Range	Package	Shipping
GF001HN	2 A 700 V	−40°C to +105°C	8−Pin, Dual Inline Package (DIP) (Pb−Free, Halide Free)	3000 Units / Tube

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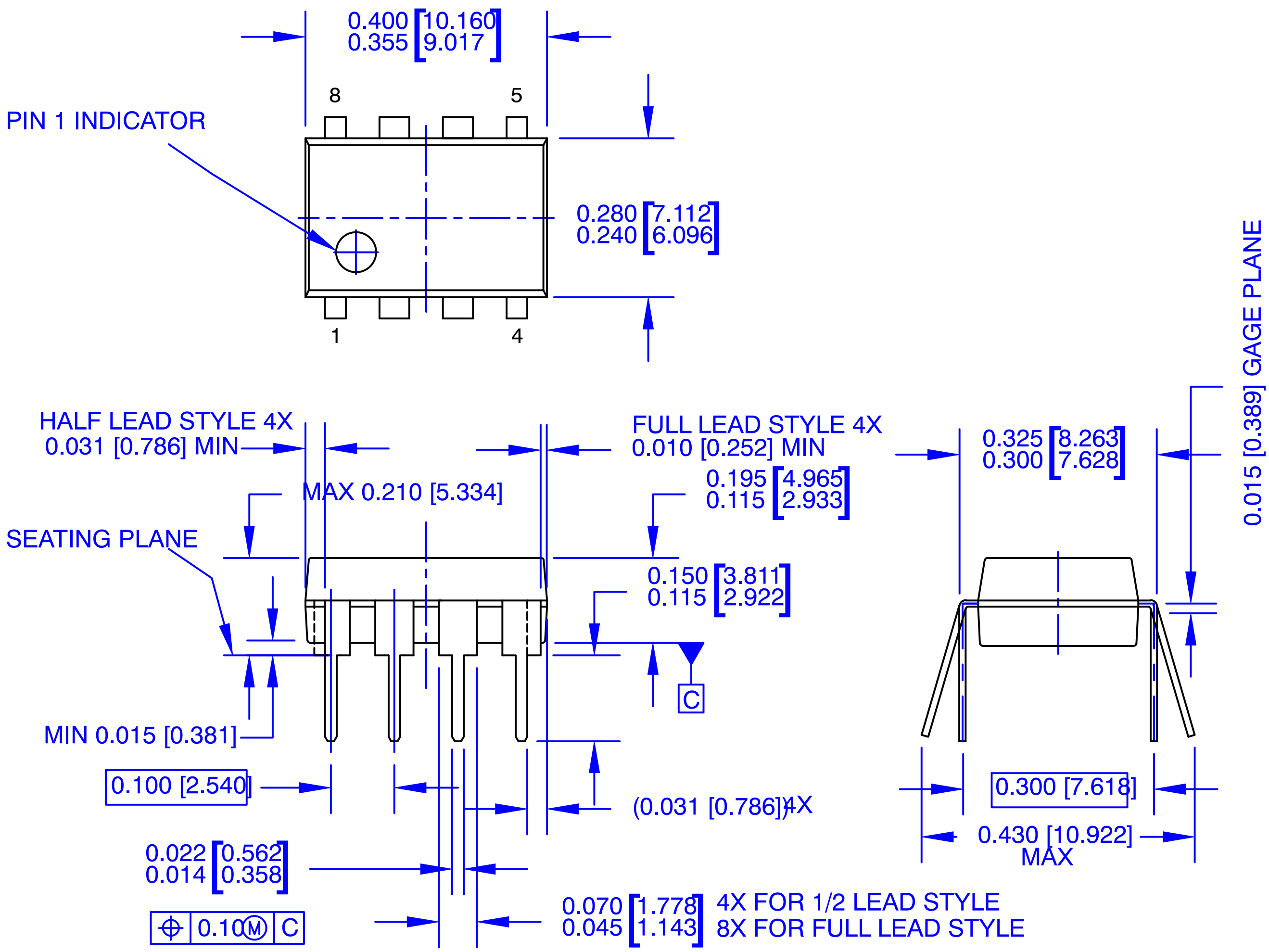

NOTES:

A) THIS PACKAGE CONFORMS TO JEDEC MS−001 VARIATION BA WHICH DEFINES 2 VERSIONS OF THE PACKAGE TERMINAL STYLE WHICH ARE SHOWN HERE.
B) CONTROLING DIMS ARE IN INCHES
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D) DIMENSIONS AND TOLERANCES PER ASME Y14.5M−2009

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