GLF1201Q

Nano Current Power I_QSmart™ Switch with True Reverse Current Blocking

Product Specification

DESCRIPTION

The GLF1201Q is an advanced technology fully integrated I_QSmart™ load switch device with True Reverse Current Blocking (TRCB) technology and the slew rate control of the output voltage. The best in class efficiency makes it an ideal choice for electronics requiring operation under the high temperature up to 125 °C.

The GLF1201Q offers an industry leading True Reverse Current Blocking (TRCB) performance, featuring an ultra-low threshold voltage. It minimizes reverse current flow in an event that the VOUT pin voltage exceeds the VIN voltage.

An integrated slew rate control can also enhance system reliability by mitigating bus voltage swings during switching events. Where uncontrolled switches can generate high inrush currents that result in voltage droop and/or bus reset events, the GLF slew rate control specifically limits inrush currents during turn-on to minimize voltage droop.

The GLF1201Q load switch device supports an industry leading wide input voltage range and helps to improve operating life and system robustness. Furthermore, one device can be used in multiple voltage rail applications which helps to simplify inventory management and reduces operating cost.

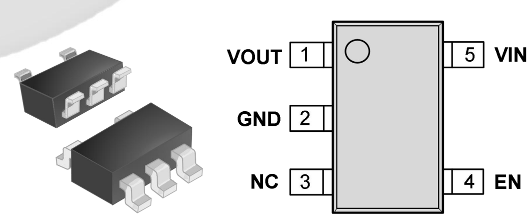
FEATURES

- AEC-Q100 Qualified
- Qualified for Automotive Applications:
  Temperature Grade 1: Ambient Operating
  Temperature Range: - 40 °C ~ +125 °C
- Wide Input Range: 1.5 V to 5.5 V
  6 V abs max
- True Reverse Current Blocking
- R_{ON}: 60 mΩ Typ at 5.5 V_{IN}
- I_{OUT} Max: 2 A
- Ultra-Low I_Q: 0.48 µA Typ at 5.5 V_{IN}
- Ultra-Low I_{SD}: 25 nA Typ at 5.5 V_{IN}
- Controlled Rise Time: 600 µs at 3.3V_{IN}
- Internal EN Pull-Down Resistor on
- Integrated Output Discharge Switch
- ESD Performance Tested per AEC Q100
  HBM: 4 kV, CDM: 2 kV
- Moisture Sensitivity Level: MSL-3 and 260 °C Peak Reflow Temp
- Lead-free, Halogen-free, and Adhere to RoHS Directive

APPLICATIONS

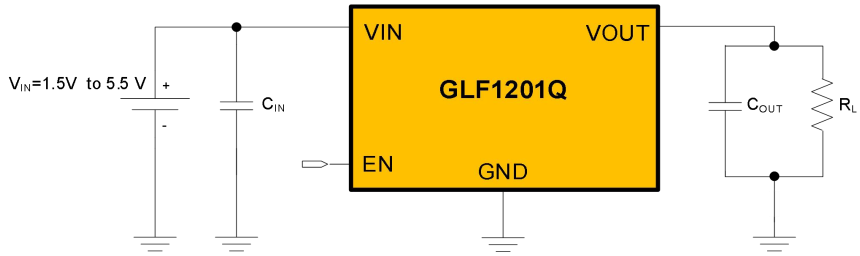
- Automotive Electronics
- Infotainment Systems
- Diagnosis System

PACKAGE



SOT23-5L

APPLICATION DIAGRAM



ALTERNATE DEVICE OPTIONS

Part Number	Top Mark	R_{ON} (Typ) at 5.5 V_{IN}	TRCB	Output Discharge	EN Activity
GLF1201Q-T1G7	DN	60 mΩ	Yes	85 Ω	High

FUNCTIONAL BLOCK DIAGRAM

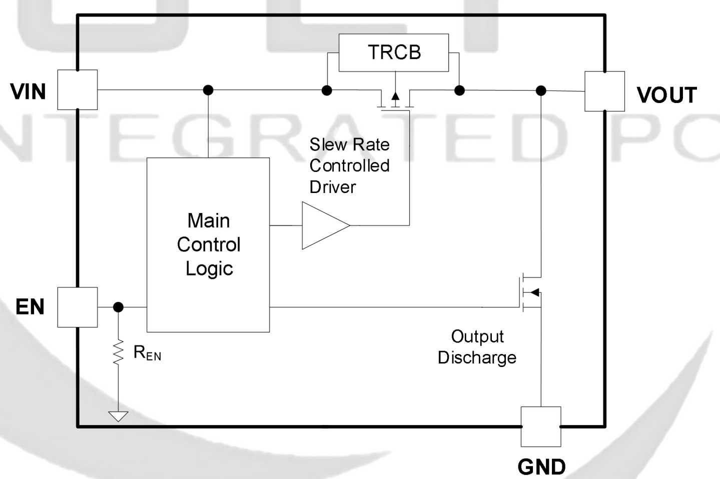


Figure 1. Functional Block Diagram

PIN CONFIGURATION

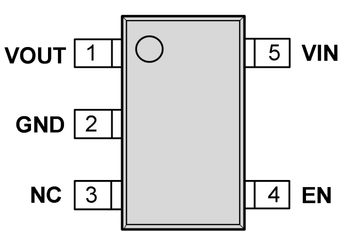


Figure 2. SOT23-5L

PIN DEFINITION

Pin #	Name	Description
1	VOUT	Switch Output
2	GND	Ground
3	NC	No connection
4	EN	Enable to control the switch
5	VIN	Switch Input. Supply Voltage for IC

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions; extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}	V_{IN}, V_{OUT}, V_{EN} to GND		-0.3	6	V
I_{OUT}	Maximum Continuous Switch Current			2	A
T_{STG}	Storage Junction Temperature		-65	150	°C
T_J	Operating Temperature Range			150	°C
θ_{JC}	Thermal Resistance, Junction to Case			90	°C/W
θ_{JA}	Thermal Resistance, Junction to Ambient			180	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, per AEC Q100-002	4		kV
		Charged Device Model, per AEC Q100-011	2		

Note. The θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Supply Voltage	1.5	5.5	V
T_A	Ambient Operating Temperature	-40	+125	°C

ELECTRICAL CHARACTERISTICS

Values are at V_{IN} = 3.3V and T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Basic Operation						
I_Q	Quiescent Current [1]	V_{IN} = V_{EN} =5.5 V, I_{OUT}=0 mA		0.48	0.60	μA
		V_{IN}=V_{EN}=5.5 V, I_{OUT}=0 mA, T_A= 125 °C		0.60		
I_{SD}	Shut Down Current	V_{IN}=1.5 V, V_{EN} = 0 V, I_{OUT}=0 mA		2	20	nA
		V_{IN}=1.5 V, V_{EN} = 0 V, I_{OUT}=0 mA		3		
		V_{IN}=4.2 V, V_{EN} = 0 V, I_{OUT}=0 mA		10		
		V_{IN}=5.5 V, V_{EN} = 0 V, I_{OUT}=0 mA		25	35	
		V_{IN}=5.5 V, V_{EN} = 0 V, I_{OUT}=0 mA, T_A=85 °C [4]		0.30	0.45	μA
		V_{IN}=5.5 V, V_{EN} = 0 V, I_{OUT}=0 mA, T_A=125 °C		2.30	3.00	
R_{ON}	On-Resistance	V_{IN}=5.5 V, I_{OUT}= 500 mA, T_A=25 °C		60	68	mΩ
		V_{IN}=5.5 V, I_{OUT}= 500 mA, T_A= 125 °C		76		
		V_{IN}=3.3 V, I_{OUT}= 500 mA, T_A=25 °C		70	79	
		V_{IN}=3.3 V, I_{OUT}= 500 mA, T_A= 125 °C		90		
		V_{IN}=1.8 V, I_{OUT}= 300 mA, T_A=25 °C		110	124	
		V_{IN}=1.8 V, I_{OUT}= 300 mA, T_A= 125 °C		132		
		V_{IN}=1.5 V, I_{OUT}= 100 mA, T_A=25 °C		120	135	
		V_{IN}=1.5 V, I_{OUT}= 100 mA, T_A= 125 °C		155		

R_{DSC}	Output Discharge Resistance	V_{EN}=Low , I_{FORCE}= 10 mA		85		Ω
		V_{EN}=Low , I_{FORCE}= 10 mA, T_A= 125 °C		90		
V_{IH}	EN Input Logic High Voltage	V_{IN}=1.5 V to 1.8 V, T_A= -40 °C to +125 °C	1.1			V
		V_{IN}=1.8 V to 5.5 V, T_A= -40 °C to +125 °C	1.3			
V_{IL}	EN Input Logic Low Voltage	V_{IN}=1.5 V to 1.8 V, T_A= -40 °C to +125 °C			0.3	
		V_{IN}=1.8 V to 5.5 V, T_A= -40 °C to +125 °C			0.4	
R_{EN}	EN Internal Resistance	Internal Pull-down Resistance		10		MΩ
I_{EN}	EN Current	V_{EN}=5.5 V		0.5		µA
V_{RCB_TH}	RCB Protection Threshold Voltage	V_{OUT} - V_{IN}		42		mV
		V_{OUT} - V_{IN}, T_A= 125 °C		50		
V_{RCB_RL}	RCB Protection Release Voltage	V_{IN} - V_{OUT}		22		
		V_{IN} - V_{OUT} ,T_A= 125 °C		32		
Switching Characteristics (2), (3)						
t_{dON}	Turn-On Delay	R_L=150 Ω, C_{OUT}=0.1 µF		450		µs
t_R	V_{OUT} Rise Time			600		
t_{dOFF}	Turn-Off Delay (4)	R_L=150 Ω, C_{OUT}=0.1 µF		17		
t_F	V_{OUT} Fall Time (3), (4)			12		

Notes:
1. I_Q does not include the pull-down current of the enable pin through the R_{EN}.
2. t_{ON} = t_{dON} + t_R, t_{OFF} = t_{dOFF} + t_F
3. Output discharge path is enabled when the device is enabled.
4. By design; characterized, not production tested.

TIMING DIAGRAM

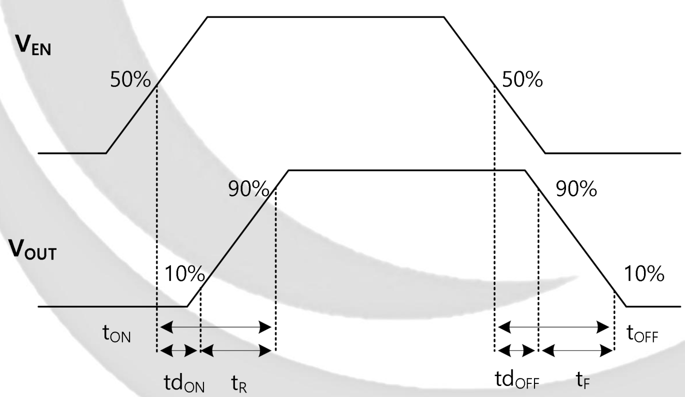


Figure 3. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

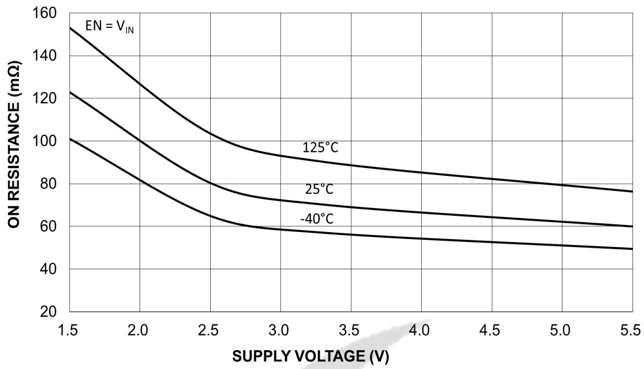


Figure 4. On-Resistance vs. Supply Voltage

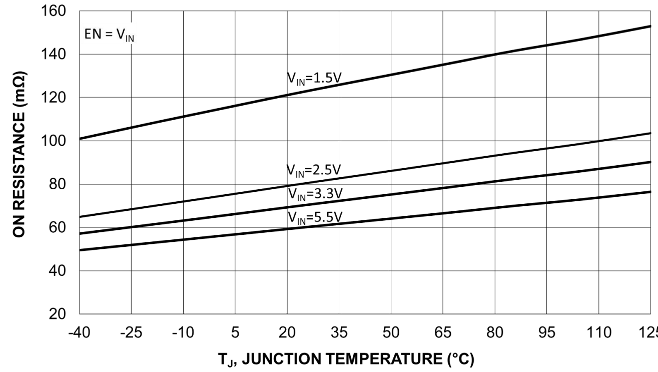


Figure 5. On-Resistance vs. Temperature

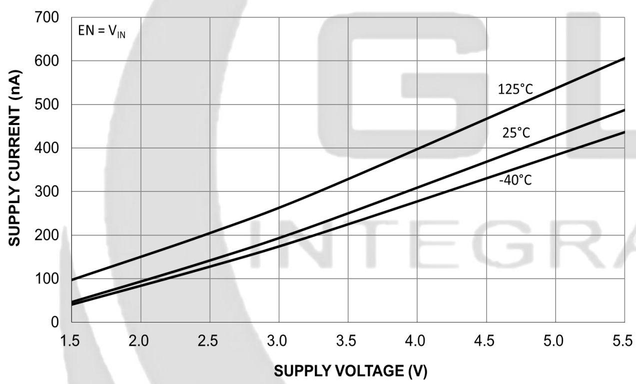


Figure 6. Quiescent Current vs. Supply Voltage

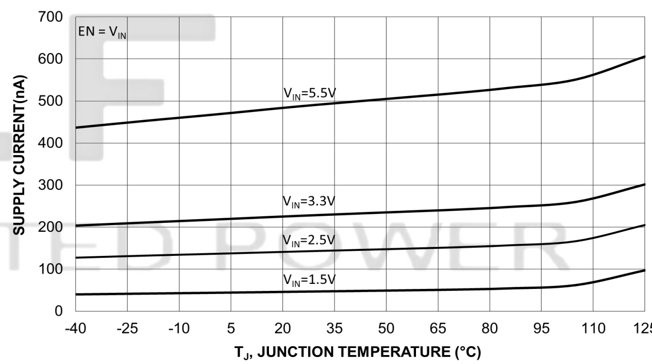


Figure 7. Quiescent Current vs. Temperature

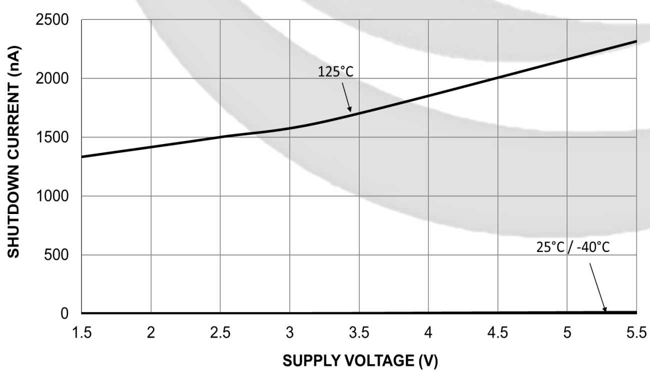


Figure 8. Shutdown Current vs. Supply Voltage

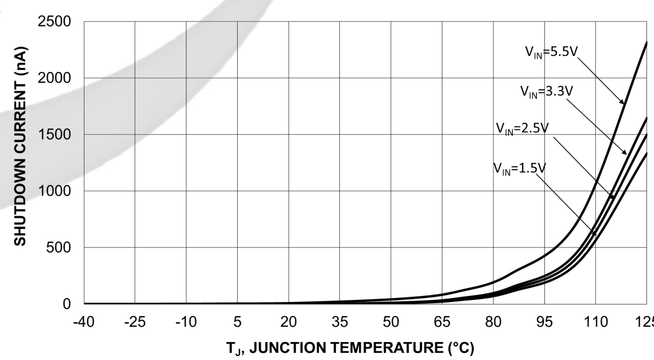


Figure 9. Shutdown Current vs. Temperature

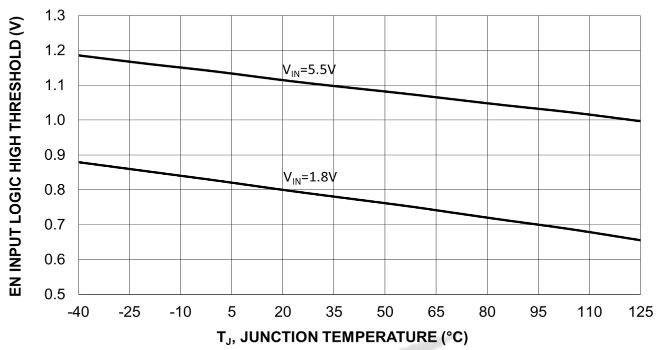


Figure 10. EN Input Logic High Threshold Vs. Temperature

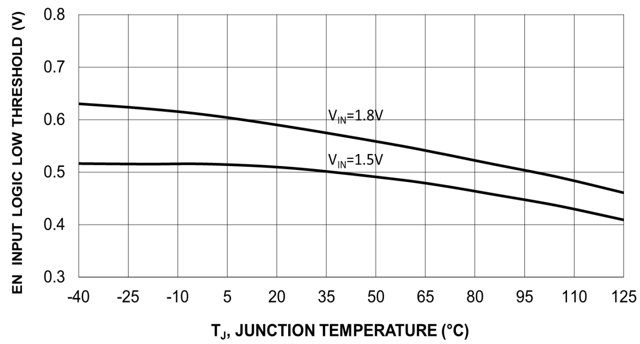


Figure 11. EN Input Logic Low Threshold Vs. Temperature

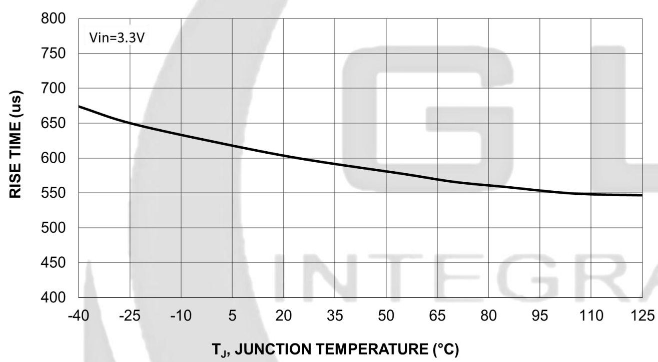


Figure 12. V_{OUT} Rise Time vs. Temperature

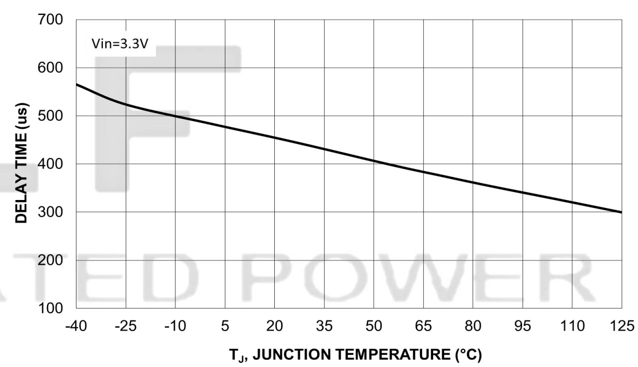


Figure 13. Turn-On Delay Time vs. Temperature

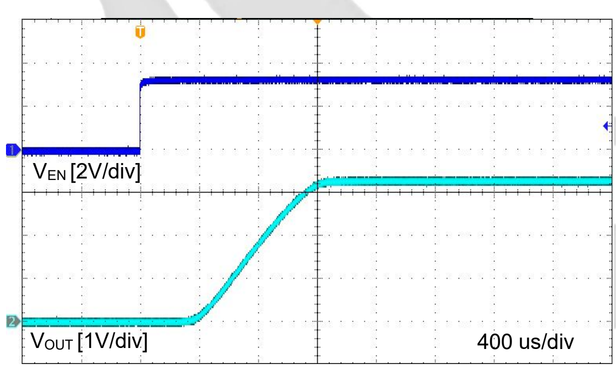


Figure 14. Turn-On Response
V_{IN}=3.3 V, C_{IN}=C_{OUT}=0.1 µF, R_L=150 Ω

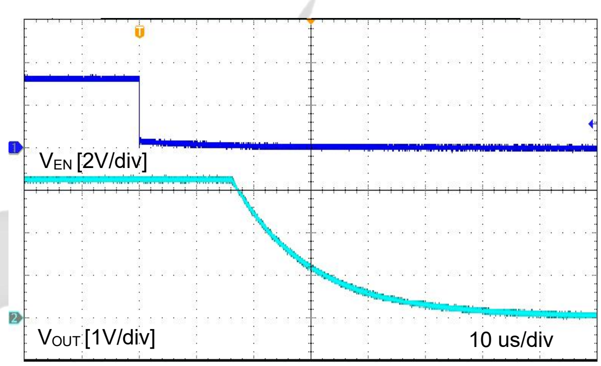


Figure 15. Turn-Off Response
V_{IN}=3.3 V, C_{IN}=C_{OUT}=0.1 µF, R_L=150 Ω

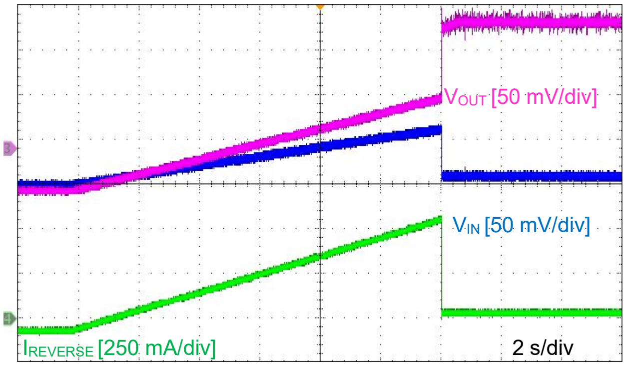


Figure 16. Reverse Current Blocking Threshold
V_{IN}=3.3 V, V_{OUT}=Up to 3.4 V, C_{IN}=C_{OUT}=0.1 μF, R_L=150 Ω

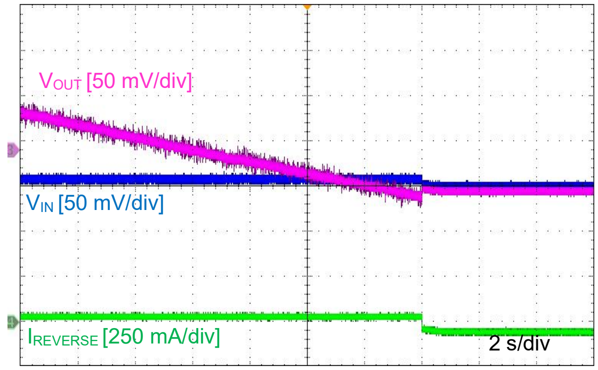


Figure 17. Reverse Current Blocking Release
V_{IN}=3.3 V, V_{OUT}=Down to 3.2 V, C_{IN}=C_{OUT}=0.1 μF, R_L=150 Ω

APPLICATION INFORMATION

The GLF1201Q integrated 2 A, ultra-efficient I_QSmart™ load switch devices with a fixed slew rate control to limit the inrush current during turn on. It is capable of operating over a wide input range from 1.5 V to 5.5 V with low on-resistance to reduce conduction loss. In the off state, it consumes very low leakage current to lengthen the lifespan of a battery.

Input Capacitor

The GLF1201Q does not require an input capacitor. However, to reduce the voltage drop on the input power rail caused by transient inrush current at start-up, a 0.1 μF capacitor is recommended to be placed close to the V_{IN} pin. A higher input capacitor value can be used to further attenuate the input voltage drop.

Output Capacitor

The GLF1201Q does not require an output capacitor. However, use of an output capacitor is recommended to mitigate voltage undershoot on the output pin when the switch is turning off. Undershoot can be caused by parasitic inductance from board traces or intentional load inductances. If load inductances do exist, use of an output capacitor can improve output voltage stability and system reliability. The C_{OUT} capacitor should be spaced close to the VOUT and GND pins.

EN pin

The GLF1201Q can be activated by forcing EN pin high level. Note that the EN pin has an internal pull-down resistor to help pull the main switch to a known “off state” when no EN signal is applied from an external controller.

True Reverse Current Blocking

The GLF1201Q has a built-in true reverse current blocking protection (TRCB) which always monitors the output voltage level regardless of the status of EN pin to check if it is greater than the input voltage. When the output voltage goes beyond the input voltage by 42 mV, the TRCB turns off the device immediately. Note that some reverse current can occur until the V_{RCB} is triggered. The main switch will resume normal operation when the output voltage drops below the input source by the TRCB protection release voltage.

Output Discharge Function

The GLF1201Q has an internal discharge NFET switch on the VOUT pin. When an EN signal turns off the main power switch, the NFET switch turns on to discharge an output capacitor quickly.

Thermal Consideration

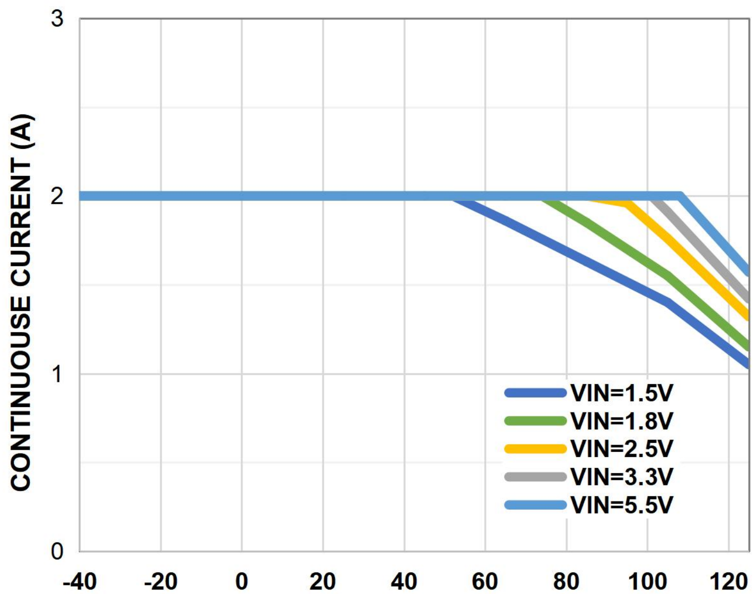
The maximum power dissipation ($P_{D(MAX)}$) depends on specific temperature conditions such as ambient temperature, a silicon junction temperature, printed circuit board conditions, and a thermal resistance of an IC. It can be calculated by the following equation The maximum junction temperature of the GLF1201Q is not allowed to exceed the maximum rating, 150 °C to insure normal functionality.

The continuous output current given in Figure 18 shows current capability at the ambient temperature, T_A. It is limited by the maximum junction temperature, the thermal resistance, and the rise of the R_{ON} at the ambient temperature condition.

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\theta_{JA}}$$

$$I_{D(DC)} = \sqrt{\frac{T_{J(max)} - T_A}{R_{DS} \cdot \theta_{JA}}}$$

Where
- $T_{J(max)}$: Maximum junction temperature
- T_A : Ambient temperature
- θ_{JA} : Thermal resistance between junction and ambient



Note. This graph is based on a high effective thermal conductivity four-layer test board per JEDEC 51-7.

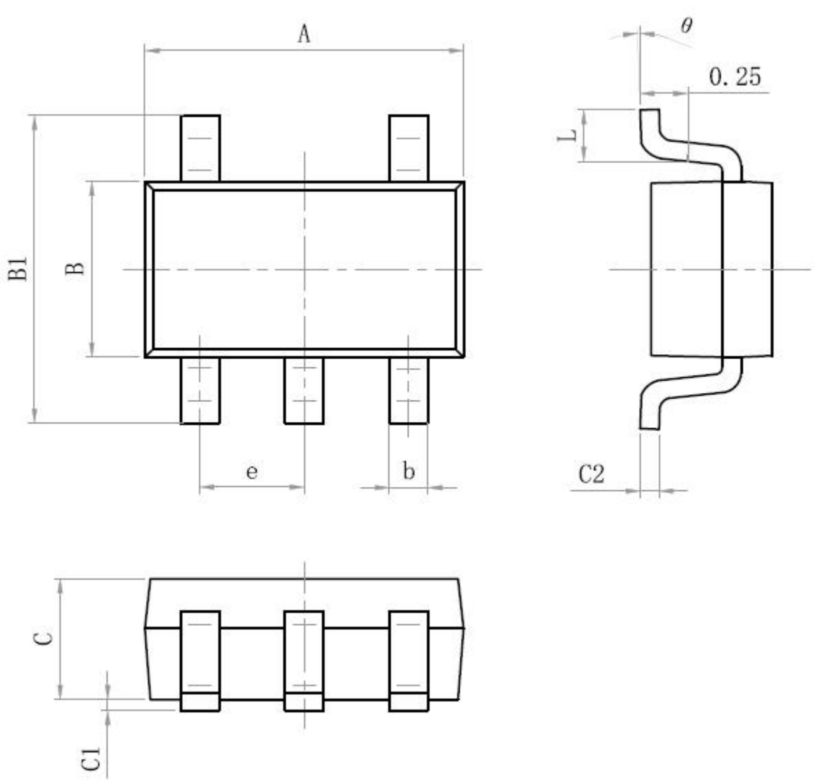
Figure 18. Continuous Current vs. Ambient Temperature

Board Layout

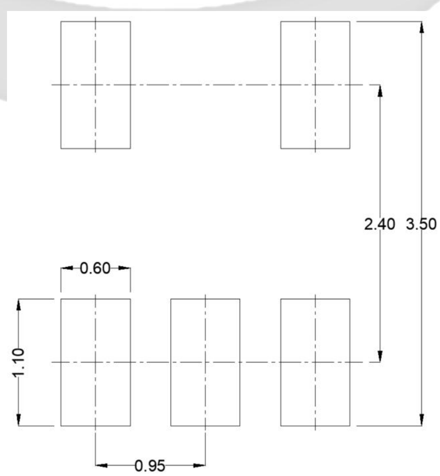
All traces should be as short as possible to minimize parasitic inductance effects. Wide traces for VIN, VOUT, and GND will help reduce signal degradation and parasitic effects during dynamic operation as well as improve the thermal performance at high load current.

PACKAGE OUTLINE

Mark \ Size	Min (mm)	Max (mm)	Mark \ Size	Min (mm)	Max (mm)
A	2.82	3.02	C	1.05	1.15
e	0.95 (BSC)		C1	0.03	0.15
b	0.28	0.45	C2	0.12	0.23
B	1.50	1.70	L	0.35	0.55
B1	2.60	3.00	θ	0°	8°

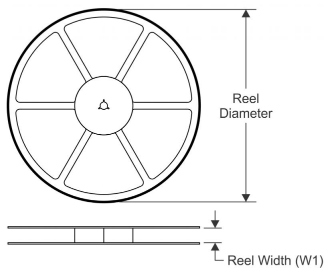


Recommended Footprint

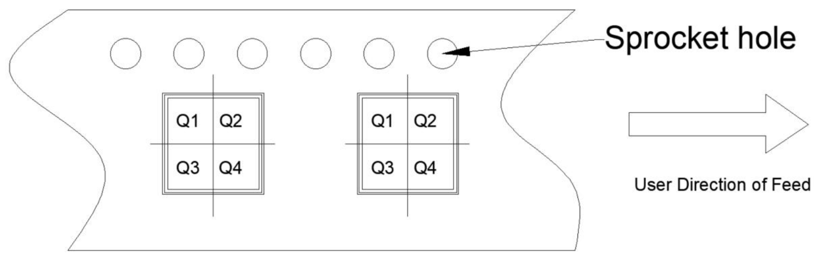


TAPE AND REEL INFORMATION

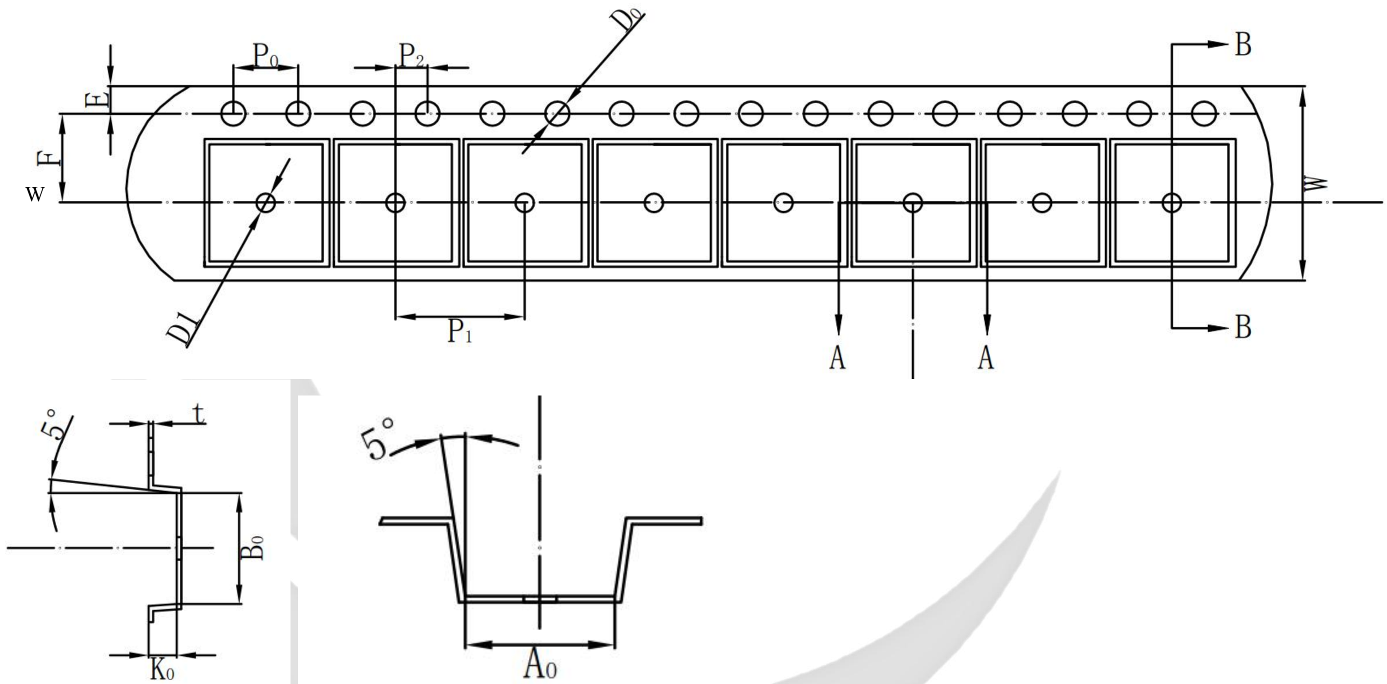
REEL DIMENSIONS



QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE



TAPE DIMENSIONS



Device	Package	Pins	SPQ	Reel Diameter (mm)	Reel Width W1	A0	B0	K0	P1	W	Pin1
GLF1201Q-T1G7	SOT23-5	5	3000	178	9	3.25	3.30	1.38	4	8	Q3

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

C0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

P1:   Pitch between successive cavity centers

SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Spec limits including typical, minimum, and maximum values are desired, or target, limits. GLF reserves the right to change limits at any time without warning or notification. A target specification in no way guarantees future production of the device in question.	Design / Development
Preliminary Specification	This is a draft version of a product specification. The specification is still under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification in no way guarantees future production of the device in question.	Qualification
Product Specification	This document represents the anticipated production performance characteristics of the device.	Production

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