

## Quad low-side intelligent power switch



HTSSOP20



### Product status link

[IPS4260LM](#)

### Product label



## Features

- 8 V to 50 V operating voltage range
- Four independent protected channels
- $V_{CC}$  undervoltage lock-out
- High speed operation ( $t_r, t_f < 1 \mu s$ )
- Programmable load current limitation level by external resistor
- Typical operating load current: 0.5 A (per channel) / 2 A (one channel)
- Thermally independent junction overtemperature protections
- Programmable non-dissipative short-circuit protection (cut-off) by external resistor
- Open load (off-state) and short-to-ground activated by external pull-down resistors
- Fast demagnetization of inductive loads with integrated catch diodes clamping turn-off transients
- Ground and  $V_{CC}$  wire break protection
- $V_{CC}$  overvoltage protection
- Common open load diagnostic
- Common thermal shutdown and overload diagnostic
- Per channel thermal shutdown diagnostic
- Designed to meet IEC 61131-2, IEC61000-4-2, IEC61000-4-4 and IEC61000-4-5
- Miniaturized HTSSOP20 package

## Application

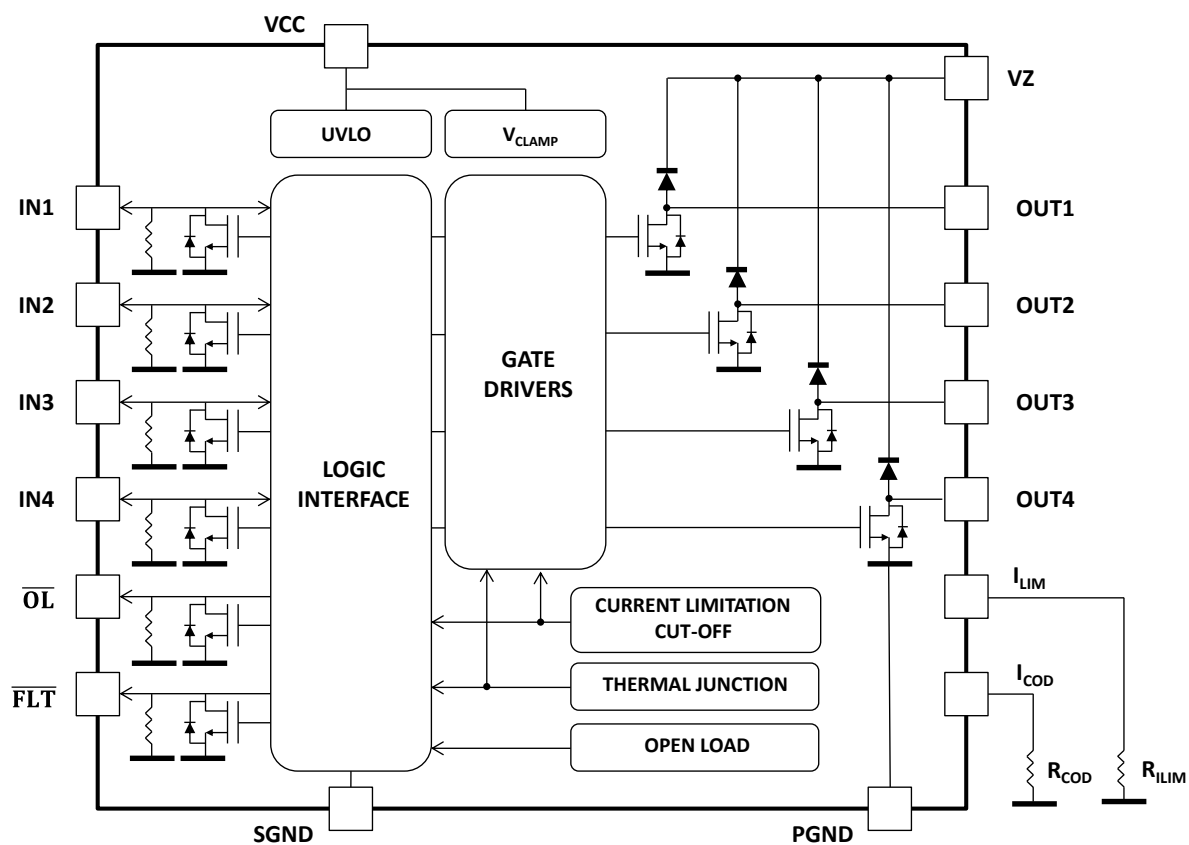
- Programmable logic control
- Industrial PC peripheral input/output
- Numerical control machines
- General low-side switch applications

## Description

The **IPS4260LM** is a monolithic high speed ( $f_{SW}$  up to 250 kHz) device, which can drive four independent capacitive, resistive or inductive loads with one side connected to supply voltage. The channels can be parallelized to reduce power dissipation. When connected to  $V_{CC}$  rail, four integrated catch diodes clamp the turn-off transients generated by inductive loads even with huge inductance; combined with proper external TVS connected to  $V_{CC}$  or to GND the IC allows fast decay, too. Each channel is protected against overload or short circuit event: the intervention level can be set by an external resistor on  $I_{LIM}$  pin. Built-in thermal shutdown protects the chip against overtemperature even in case of short-circuit. If enabled, the integrated cut-off protection features a non-dissipative protection in case of overload; it limits both the output average current value and, consequently, the device overheating. Cut-off delay/restart can be programmed by external resistors on CoD pin; it can be disabled by shorting CoD to GND. Two common diagnostic open drains pins (OL, for open load and FLT for cut-off and thermal shutdown) together with the four open drain on each  $INx$  pin (cut-off and thermal shutdown) feature an extensive diagnostic of the chip.

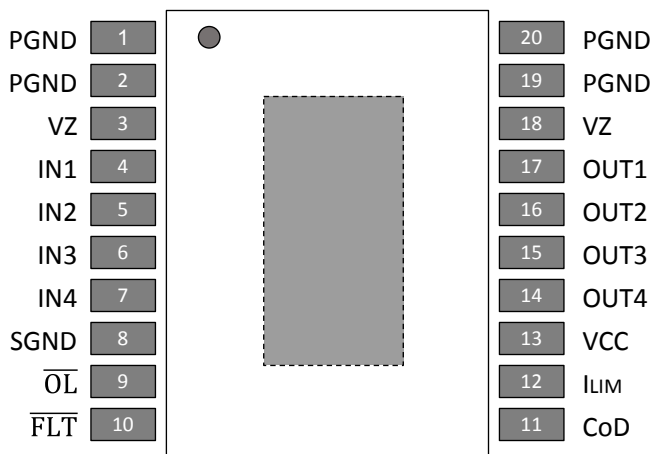
## 1

### Figure 1. Block diagram



## 2 Pin description

**Figure 2. Pin connection (top view)**



**Table 1. Pin configuration**

Number	Name	Function	Type
1, 2, 19, 20	PGND	Integrated power switch ground	Supply
3, 18	VZ	Load clamp voltage pins. Pins 3 and 18 must be shorted on the application board and then connected directly to the supply rail, or by an external Zener or TVS diode to the supply rail or to PGND (see <a href="#">Section 2.3</a> )	Analog Output
4	IN1	Channel 1 input / cut-off and thermal shutdown diagnostic	Input/output open drain
5	IN2	Channel 2 input / cut-off and thermal shutdown diagnostic	Input/output open drain
6	IN3	Channel 3 input / cut-off and thermal shutdown diagnostic	Input/output open drain
7	IN4	Channel 4 input / cut-off and thermal shutdown diagnostic	Input/output open drain
8, exposed pad	SGND	Logic interface block ground	Supply
9	$\overline{OL}$	Cumulative power stage open load or short ground common diagnostic	Output open drain
10	$\overline{FLT}$	Cut-off and thermal shutdown pin. Common diagnostic pin both for thermal shutdown and cut-off	Output open drain
11	CoD	Programmable cut-off intervention delay during overcurrent operation. It cannot be left floating: connect to PCB SGND ground plane to disable the cut-off function or connect a resistor between CoD and PCB ground plane to set the delay (see <a href="#">Section 6.3 Current limitation and cut-off</a> )	Analog Output
12	$I_{LIM}$	Limitation current adjustment. It cannot be left floating: connect a resistor between $I_{LIM}$ and SGND to set the current limit threshold (see <a href="#">Section 6.3 Current limitation and cut-off</a> )	Analog Output
13	VCC	Supply voltage. Connect to the supply rail	Supply
14	OUT4	Power stage, channel 4	Analog Output
15	OUT3	Power stage, channel 3	Analog Output
16	OUT2	Power stage, channel 2	Analog Output
17	OUT1	Power stage, channel 1	Analog Output

## 2.1 VCC

IC supply voltage. This pin has to be connected to the supply rail of the application.

## 2.2 PGND, SGND

PGND stands for power ground and it is internally connected to the source of the integrated switches. SGND stands for signal ground and it is the reference level for the logic interface. SGND and PGND pins must be shorted on the application board. In order to reduce as much as possible the switching noises from PGND to SGND, the application board has to be designed with two different ground planes for SGND and PGND. The two ground planes have to be shorted by a dedicated net.

## 2.3 VZ

These two pins (corresponding to the cathodes of the clamp diodes) must be shorted together on the application and connected directly to supply rail or, alternatively, connected by a Zener or TVS diode to supply rail or PGND. Connecting VZ pins directly to the supply rail implies that the inductive loads are demagnetized without fast decay option: in fact the  $V_{OUTx}$  (voltage on OUTx pin) is forced to the forward voltage of the integrated clamp diodes. The connection by a Zener or TVS allows to drive loads requiring fast current decay (fast demagnetization). For the proper selection of the external Zener or TVS, please refer to [Section 7.1 Fast current decay with TVS between VZ and supply rail](#) and [Section 7.2 Fast current decay with TVS between VZ and PGND](#)

*Note:* Leaving VZ pins floating, the integrated output voltage clamp is activated and the fast current decay capability is limited by the heatsink capability of the IC. See  $E_{AS}$  in [Table 2. Absolute maximum ratings](#).

## 2.4 IN1, IN2, IN3, IN4

These pins drive the power stage on pins OUT1, OUT2, OUT3 and OUT4. Besides an internal weak pull-down resistor, each IN1, IN2, IN3, IN4, is internally wired to an open drain transistor, used for diagnostic purposes, and must be driven through a series resistor. The open drain transistor is turned-on in case of thermal shutdown or cut-off protection of the relative channel (see [Section 6.2 Overtemperature](#) and [Section 6.3 Current limitation and cut-off](#) ).

## 2.5 OUT1, OUT2, OUT3, OUT4

Power stage load connection pins: integrated power transistor are in low-side configuration, so the load has to be connected between OUTx pin and supply rail. The power stage channels can be paralleled.

## 2.6 Open load in off-state

OL pin is used for diagnostic purpose and it is internally wired to an open drain transistor. If the open load feature is enabled (see [Section 6.4 Open load in off-state](#)) the open drain transistor is activated when OUTx is in off state and the open load threshold (VOLoff) is triggered (see [Table 8. Protection and diagnostic](#) ).

## 2.7 FLT

This pin is used for diagnostic purpose and it is internally wired to an open drain transistor. The open drain transistor is turned on in case of junction thermal shutdown or during the cut-off protection.

## 2.8 I<sub>LIM</sub>

This pin cannot be left floating and can be used to program the limitation current value through an external resistor  $R_{ILIM}$  (see [Table 8. Protection and diagnostic](#)). The resistor  $R_{ILIM}$  has to be connected between I<sub>LIM</sub> and SGND pins. When more than one ICs are used in the same application, their I<sub>LIM</sub> pins cannot be wired together: each IC must be connected to its own resistor (see [Section 6.3 Current limitation and cut-off](#) )

## 2.9 CoD

This pin cannot be left floating and can be used to program the cut-off delay time  $t_{coff}$  (see [Table 7. Logic inputs](#)) through an external resistor ( $R_{CoD}$ ). The resistor  $R_{CoD}$  has to be connected between CoD and SGND pins. The cut-off function can be completely disabled by shorting CoD pin to SGND: in this condition the power stage channel remains ON in limitation condition, supplying the current to the load until the input is forced LOW or the thermal shutdown threshold is triggered (see [Table 8. Protection and diagnostic](#) ).

### 3 Absolute maximum ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply voltage	-0.3 to 55	V
V <sub>Z</sub>	Internal clamp diode supply	-0.3 to 55	V
V <sub>OUTx</sub>	Power stage (OUTx channel) voltage	-0.3 to V <sub>DEMAG</sub>	V
V <sub>INx</sub>	INx pin voltage	-0.3 to 5.5	V
I <sub>INx</sub>	INx pin current	-10 to +10	mA
V <sub>CoD</sub> , V <sub>ILIM</sub>	CoD and I <sub>LIM</sub> pin voltage	5.5	V
I <sub>CoD</sub> , I <sub>ILIM</sub>	CoD and I <sub>LIM</sub> pin current	-1/+5	mA
V <sub>OD</sub>	Open drain fault pins (FLT and OL) voltage	-0.3 to 5.5	V
I <sub>OD</sub>	Open drain fault pins (FLT and OL) current	-10/10	mA
I <sub>CC</sub>	Maximum DC reverse current (from GND to V <sub>CC</sub> )	-250	mA
I <sub>OUTHx</sub>	Power stage (OUTx channel) current	Internally limited	A
-I <sub>OUTHx</sub>	DC Reverse current on OUTx channel	5	A
I <sub>Z</sub>	DC current on V <sub>Z</sub> (pins 3 and 18 connected together in the application board)	5	A
EAS	Single pulse avalanche energy per channel not simultaneously @T <sub>AMB</sub> = 125 °C, I <sub>OUT</sub> = 500 mA, V <sub>Z</sub> pins floating	0.9	J
P <sub>TOT</sub>	Power dissipation at T <sub>C</sub> = 25 °C	Internally limited	W
T <sub>STG</sub>	Storage temperature range	-55 to 150	°C
T <sub>J</sub>	Junction temperature	-40 to 150	°C

**Note:** Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All voltages are referenced to GND.

**Table 3. Thermal data**

Symbol	Thermal resistance	Conditions	Value	Unit
R <sub>TH(JA)</sub>	Junction to ambient	2s2p (4L) board Natural convection <sup>(1)</sup>	43	°C/W
R <sub>TH(J-C)</sub>	Junction to case	Cold plate (infinite headsink like) <sup>(2)</sup>	3	°C/W

1. JESD51-7.

2. JESD51-12.01

## 4 Electrical characteristics

(8 V < V<sub>CC</sub> < 50 V; -40 °C < T<sub>J</sub> < 125 °C, unless otherwise specified)

**Table 4. Supply**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Operating voltage range		V <sub>UVON</sub>		50	V
V <sub>UVON</sub>	Undervoltage on threshold	V <sub>CC</sub> increasing	7		8	V
V <sub>UVOFF</sub>	Undervoltage off threshold	V <sub>CC</sub> decreasing	6.5		7.5	V
V <sub>UVH</sub>	Undervoltage hysteresis		0.2	0.5		V
I <sub>S</sub>	Supply current in off-state	V <sub>CC</sub> = 24 V; all INx OFF		1		mA
		V <sub>CC</sub> = 50 V; all INx OFF		1.2	1.6	
	Supply current in on-state	V <sub>CC</sub> = 24 V; all INx ON, OUTx open load [x = 1..4]		2		mA
		V <sub>CC</sub> = 50 V; all INx ON, OUTx open load [x = 1..4]		2.4	3	

**Table 5. Output stage**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R <sub>DS(ON)</sub>	On-state resistance	R <sub>LOAD</sub> = 48 Ω, V <sub>CC</sub> = 24 V @ T <sub>J</sub> = 25 °C		260		mΩ
		R <sub>LOAD</sub> = 48 Ω, V <sub>CC</sub> = 24 V @ T <sub>J</sub> = 125 °C			560	
V <sub>OUT(OFF)</sub>	Off-state power stage voltage	V <sub>IN</sub> = 0 V and I <sub>OUT</sub> = 0 A	V <sub>CC</sub> -2			V
I <sub>OUT(OFF)</sub>	Off-state power stage current	V <sub>IN</sub> = 0 V, V <sub>OUT</sub> = V <sub>CC</sub> = 24 V		0.5		μA
		V <sub>IN</sub> = 0 V, V <sub>OUT</sub> = V <sub>CC</sub> = 50 V			5	
V <sub>FCD</sub>	Catch diodes forward voltage	I <sub>forward</sub> = 500 μA	0.21	0.50	0.73	V
I <sub>RRM</sub>	Catch diodes reverse current	V <sub>rrm</sub> = 55 V			1	μA

**Table 6. Switching (V<sub>CC</sub> = 24 V; R<sub>LOAD</sub> = 24 Ω, input rise time < 0.1 μs )**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t <sub>r</sub>	Rise time	see Figure 3. t <sub>rise</sub> and t <sub>fall</sub> and Figure 4. t <sub>PD(L-H)</sub> and t <sub>PD(H-L)</sub>		450	700	ns
t <sub>f</sub>	Fall time			500	600	
t <sub>PD(H-L)</sub>	Propagation delay time INx to OUTx, low to high			500	700	
t <sub>PD(L-H)</sub>	Propagation delay time INx to OUTx, high to low			400	600	

Figure 3.  $t_{\text{rise}}$  and  $t_{\text{fall}}$

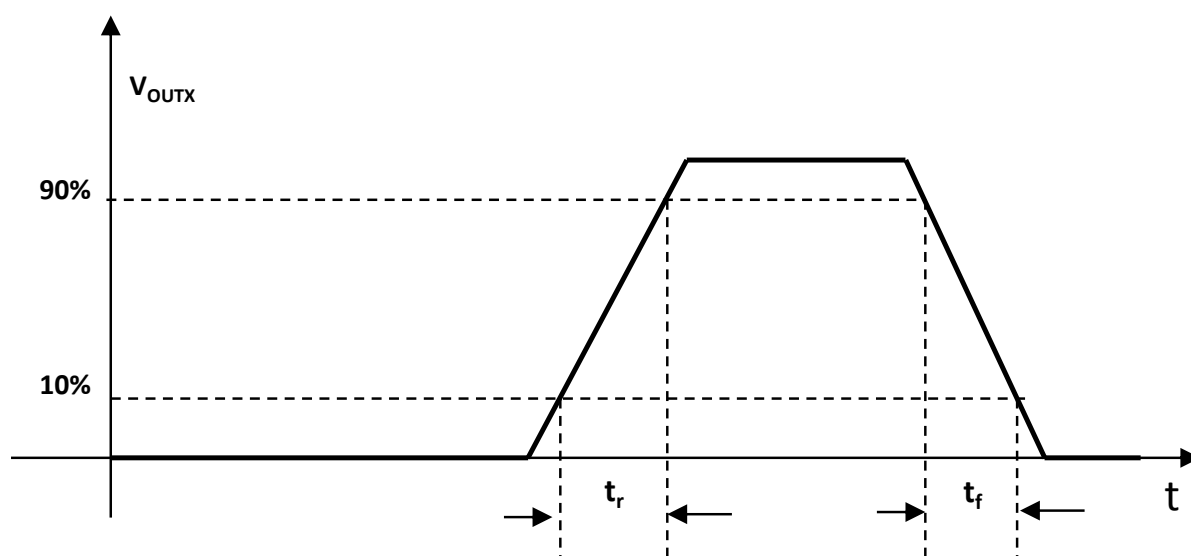
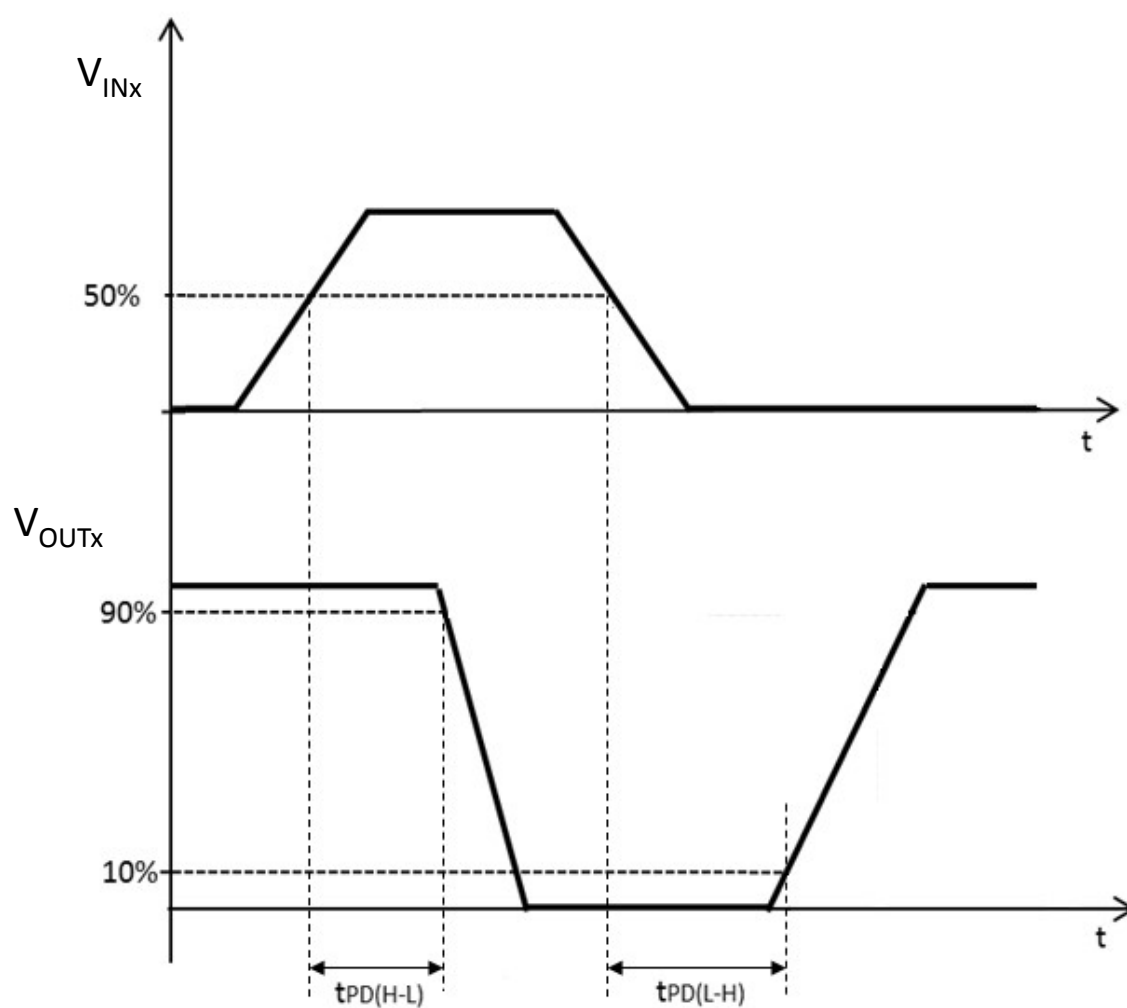


Figure 4.  $t_{\text{PD(L-H)}}$  and  $t_{\text{PD(H-L)}}$



**Table 7. Logic inputs**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>IL</sub>	Input low level voltage	V <sub>IN</sub> decreasing			0.8	V
V <sub>IH</sub>	Input high level voltage	V <sub>IN</sub> increasing	2.0			
V <sub>I(HYST)</sub>	Input hysteresis voltage			0.4		
V <sub>OL</sub>	Voltage drop on OL pin	I <sub>OL</sub> = 5 mA, V <sub>INx</sub> = 0 V, OUTx = open load, R <sub>PD</sub> between OUTx and GND			0.1	
V <sub>FAULT</sub>	Voltage drop on FAULT pin or INx pin	I <sub>FLT</sub> = 5 mA, V <sub>INx</sub> = 0 V, (T <sub>JX</sub> > T <sub>JSD</sub> or cut-off event)			0.1	
I <sub>INX</sub>	All digital input/output pin current	V <sub>IN</sub> = 5 V			70	μA

**Table 8. Protection and diagnostic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>clamp</sub>	V <sub>CC</sub> clamp voltage	I <sub>CC</sub> ≤ 10 mA	55	58	60	V
V <sub>demag</sub>	Demagnetization voltage	I <sub>OUT</sub> = 0.5 A; load ≥10 mH	55	58	60	
I <sub>peak</sub>	Current limitation activation threshold.	I <sub>OUT</sub> increasing from 0 A to short circuit.		I <sub>LIM</sub> +20%		A
I <sub>LIM</sub>	Current limitation level	30 kΩ ≤ R <sub>ILIM</sub> < 120 kΩ	60/R <sub>ILIM</sub> [kΩ] ± 30%			A
		0 < R <sub>ILIM</sub> < 30 kΩ	3 ± 30%			
t <sub>coff</sub>	Cut-off current delay time	Programmable by external resistor on "cut-off" pin (valid in the range from 60 kΩ to 240 kΩ).	R <sub>CoD</sub> [kΩ]/120 ± 15%			ms
		R <sub>CoD</sub> = 0 Ω cut-off disabled	The IC is protected against overheating by the thermal shutdown only.			
t <sub>res</sub>	Power stage restart delay time		31*t <sub>coff</sub> ± 15%			ms
t <sub>BKT</sub>	Open load blanking time		10	16	22	μs
I <sub>VD</sub>	V <sub>CC</sub> wire break power stage current	V <sub>INx</sub> = V <sub>CC</sub> =0 V; V <sub>OUTx</sub> = 24 V, V <sub>Z</sub> floating			50	μA
T <sub>JSD</sub>	Junction temperature shutdown			160		°C
T <sub>JHYST</sub>	Junction temperature thermal hysteresis			20		°C
V <sub>OLoff</sub>	Open load (off-state) or short-to-ground detection threshold		V <sub>CC</sub> -4.5	V <sub>CC</sub> -3.5	V <sub>CC</sub> -2.5	V

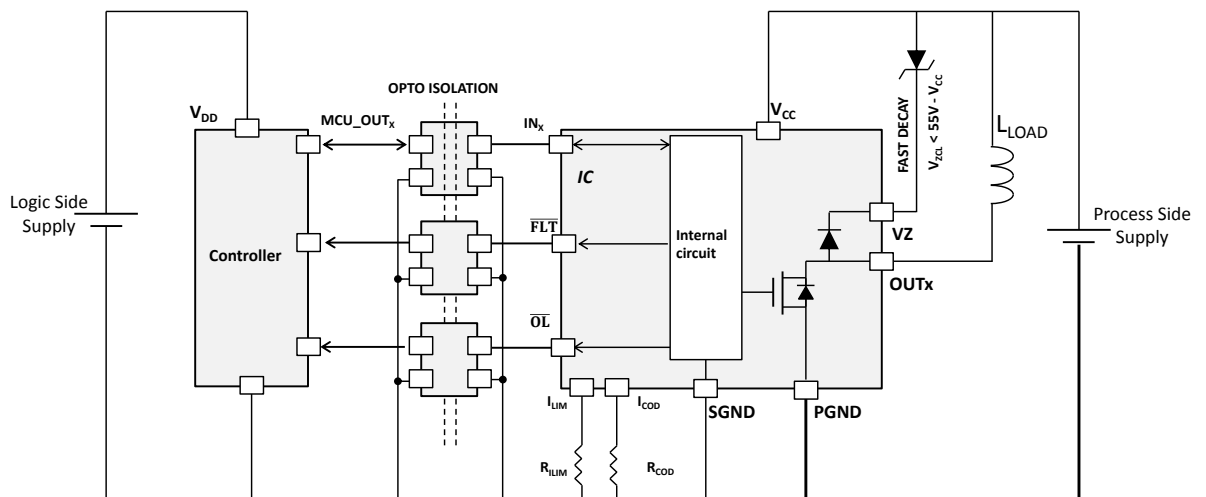


## 5 Power stage logic

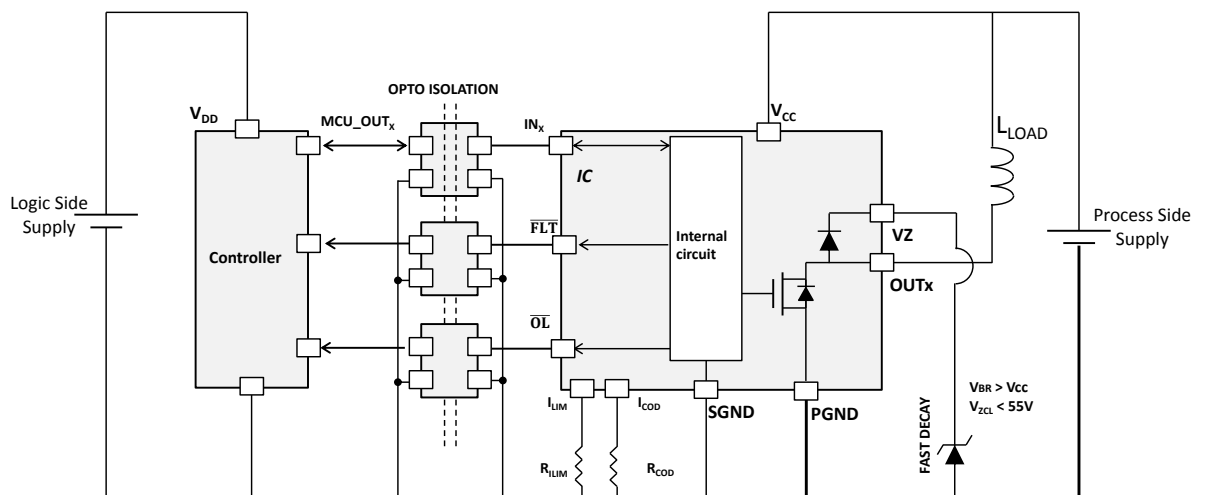
**Table 9.** Power stage (OUTx pin) truth table

Operation	MCU_OUTx	INx	OUTx	$\overline{\text{FLT}}$	$\overline{\text{OL}}$
Normal	L	L	H	H	H
	H	H	L	H	H
Cut-off	L	L	H	L	H
	H	L	H	L	H
UVLO	L	L	H	X	X
	H	H	H	X	X
Open load / short-to-GND	L	L	L	H	L
	H	H	L	H	H
Overtemperature	L	L	H	L	H
	H	L	H	L	H

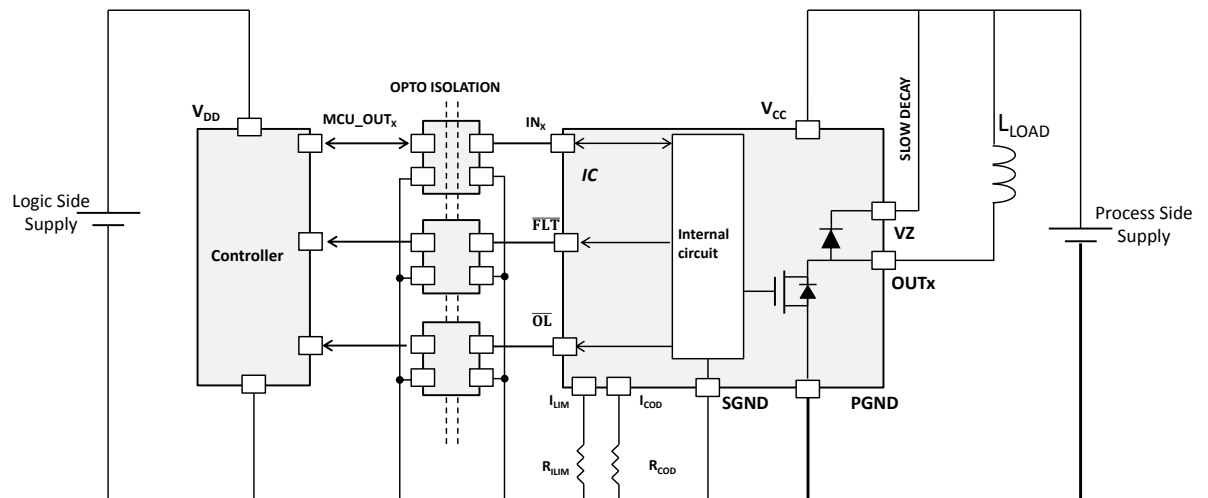
**Figure 5.** Application circuit (fast decay enabled by TVS between Vz and supply rail)



**Figure 6.** Application circuit (fast decay enabled by TVS between Vz and PGND).



**Figure 7. Application circuit (fast decay disabled by Vz shorted to supply rail) .**



## 6 Protection and diagnostic

The IC integrates several protections to ease the design of a robust application.

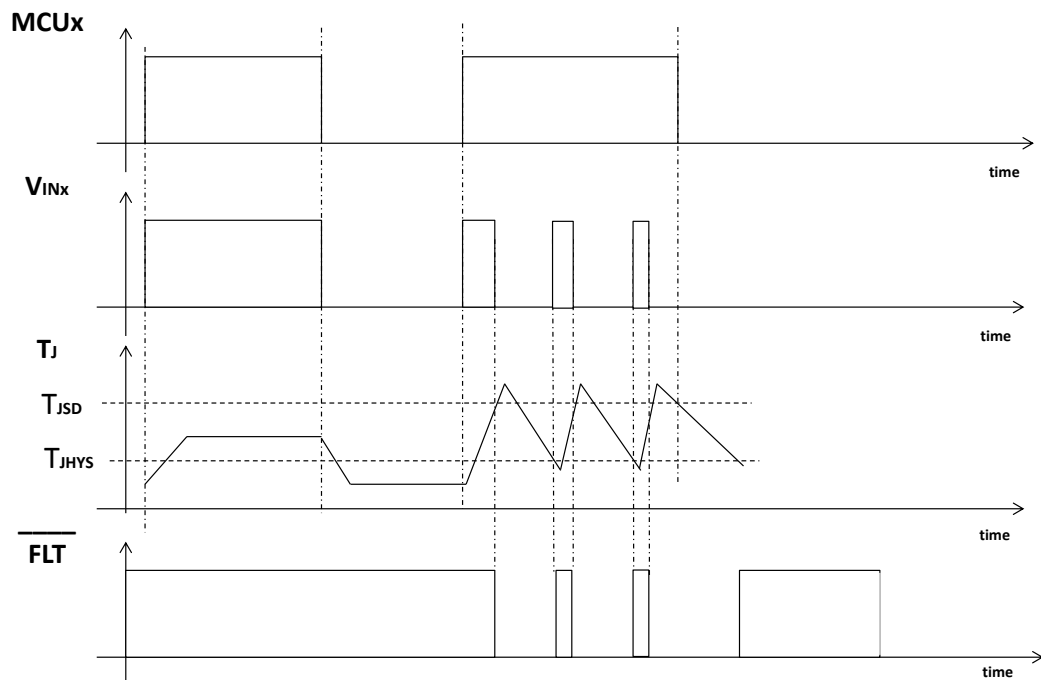
### 6.1 Undervoltage lock-out

The device turns off if the supply voltage falls below the turn-off threshold ( $V_{UV(off)}$ ). Normal operation restarts after  $V_{CC}$  exceeds the turn-on threshold ( $V_{UV(on)}$ ). Turn-on and turn-off thresholds are defined in [Table 4. Supply](#).

### 6.2 Overtemperature

The power stage of each channel is turned off as its internal junction temperature ( $T_J$ ) exceeds the shutdown threshold ( $T_{JSD}$ ). Normal operation restarts when  $T_J$  comes back below the reset threshold (see [Table 8. Protection and diagnostic](#)). The internal fault signal is set when the channel is OFF due to thermal protection. The thermal fault is reported both on the FLT pin and on the INx pin of the corresponding OUTx in fault. Note that the FLT pin reports the logic OR of the four output channels faults.

Figure 8. Thermal protection signalization behavior on  $\overline{FLT}$



### 6.3 Current limitation and cut-off

The load current flows through the integrated power stage and it is internally limited by the specific  $I_{LIM}$  threshold that can be set by an external resistor ( $R_{ILIM}$ ) placed between  $I_{LIM}$  and SGND ground plane. The design rule for the  $R_{ILIM}$  resistor is:

Equation 1:

$$I_{LIM} = 60 / R_{ILIM} [k\Omega] \quad (1)$$

The above design rule is valid in the range  $30 \text{ k}\Omega \leq R_{ILIM} \leq 120 \text{ k}\Omega$ . For  $0 \Omega \leq R_{ILIM} < 30 \text{ k}\Omega$ , the current is internally limited up to 3 A (typical). For  $R_{ILIM} > 120 \text{ k}\Omega$  the current is anyway limited but the linearity is not guaranteed.

The IC implements the cut-off feature which limits the duration of the current limitation condition. The duration of the current limitation condition ( $T_{Coff}$ ) can be set by a resistor ( $R_{CoD}$ ) placed between CoD and SGND ground plane. The design rule for  $R_{CoD}$  is:

**Equation 2:**

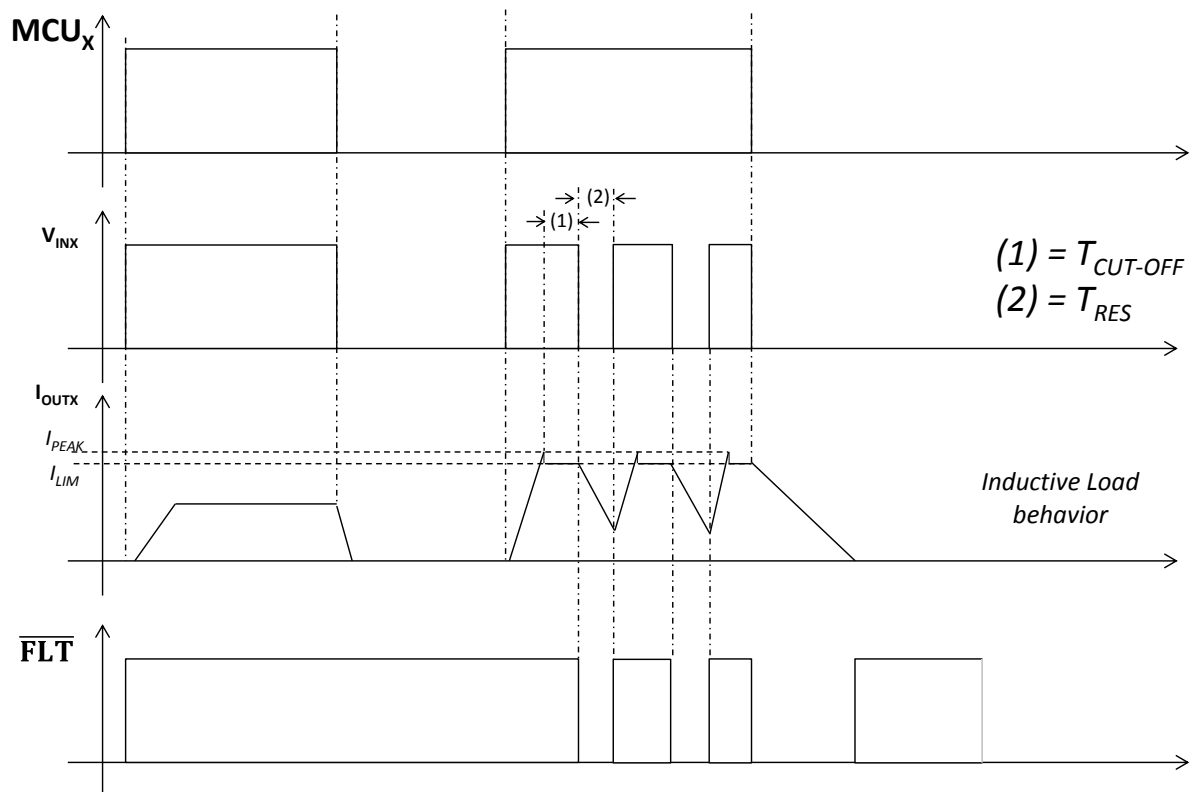
$$T_{\text{coff}} = R_{\text{CoD}}[k\Omega] / 120 \quad (2)$$

The above design rule is valid in the range  $60\text{ k}\Omega \leq R_{\text{CoD}} \leq 240\text{ k}\Omega$ . As  $0\text{ }\Omega < R_{\text{CoD}} < 60\text{ k}\Omega$ ,  $T_{\text{coff}}$  anyway decreases but the linearity of the above design rule is not guaranteed. As  $R_{\text{CoD}} = 0\text{ }\Omega$  (short-to-ground plane) the cut-off feature is disabled, by means the IC is protected by thermal shutdown only. Concerning  $R_{\text{CoD}} > 240\text{ k}\Omega$ ,  $T_{\text{coff}}$  increases but linearity of equation 2 is not guaranteed.

In case  $I_{\text{LIM}}$  threshold is triggered, the power stage remains in the current limitation condition ( $I_{\text{OUTx}} = I_{\text{LIM}}$ ) at least for  $t_{\text{coff}}$ . When  $t_{\text{coff}}$  elapses, the power stage is turned off and restarted after the  $t_{\text{res}}$  restart time. The fault condition is reported both on  $\overline{\text{FLT}}$  pin and on the input pin ( $\text{INx}$ ) corresponding to the channel in fault. The internal cut-off flag signal is latched at power stage switch-off and released after the time  $t_{\text{res}}$ . The same behavior is reported on  $\overline{\text{FLT}}$  pin and on the  $\text{INx}$  pins related to the  $\text{OUTx}$  in fault. If one of the four channels is in overload protection, the other channels (in operating conditions) work properly. The status of  $\overline{\text{FLT}}$  is independent of the  $\text{INx}$  pin status, and is low during the whole cut-off time ( $t_{\text{res}}$ ). The same behavior has to be respected on fault signals on input pins.

If CoD pin is shorted to SGND ground plane (cut-off feature disabled) then the output channel remains ON, in current limitation condition, until the related input becomes LOW or the thermal protection threshold is triggered.

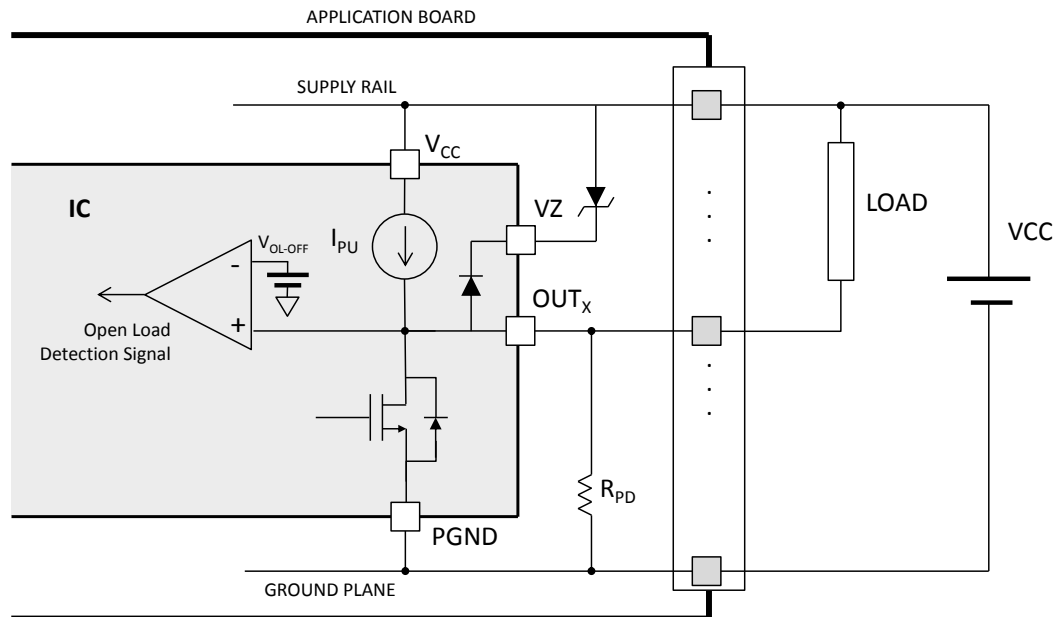
**Figure 9. Cut-off signalization behavior on  $\overline{\text{FLT}}$**



## 6.4 Open load in off-state

The IC provides the open load detection feature, which detects if the load is disconnected (wire break) from the  $\text{OUTx}$  pin when in OFF-state ( $\text{INx} = \text{LOW}$ ). This feature can be activated by placing a proper resistor ( $R_{\text{PD}}$ ) between  $\text{OUTx}$  and PGND ground plane.

Figure 10. Open load off-state



The voltage on OUTx pin ( $V_{OUTx}$ ) is internally compared with the  $V_{OLOFF}$  threshold: if the related INx pin is LOW and the  $V_{OUTx}$  goes lower than  $V_{OLOFF}$  then the open load condition is triggered. The fault condition is reported on the OL pin and the fault reset occurs when load is reconnected. If the channel is switched ON by the related INx pin, the fault condition is no longer detected.

In OFF state, the IC achieves the open load detection feature by forcing the internally generated current  $I_{PU}$  ( $= 20 \mu A$ ) on the external pull-down resistor  $R_{PD}$ . The following design rule has to be followed in order to set the proper value of  $R_{PD}$ :

**Equation 3:**

$$R_{PD} < \frac{V_{OLOFF(min)}}{I_{PU}} = \frac{V_{CC} - 4.5}{I_{PU}} \quad (3)$$

**Note:** When the load is connected the open load detection threshold must not be triggered:

**Equation 4:**

$$V_{OUTx} = V_{CC} * \frac{R_{PD}}{(R_{PD} + R_{LOAD})} > V_{OLOFF(max)} \quad (4)$$

Therefore:

**Equation 5:**

$$R_{PD} > R_{LOAD} * \left[ \frac{V_{OLOFF(max)}}{(V_{CC} - V_{OLOFF(max)})} \right] \quad (5)$$

**Note:** if two or more channels are parallelized then  $R_{PD}$  must be calculated according to the  $n \cdot I_{pu}$  (e.g. in case of 4 channels in parallel the total  $I_{pu}$  becomes  $80 \mu A$ ).

## 6.5 GND wire break protection

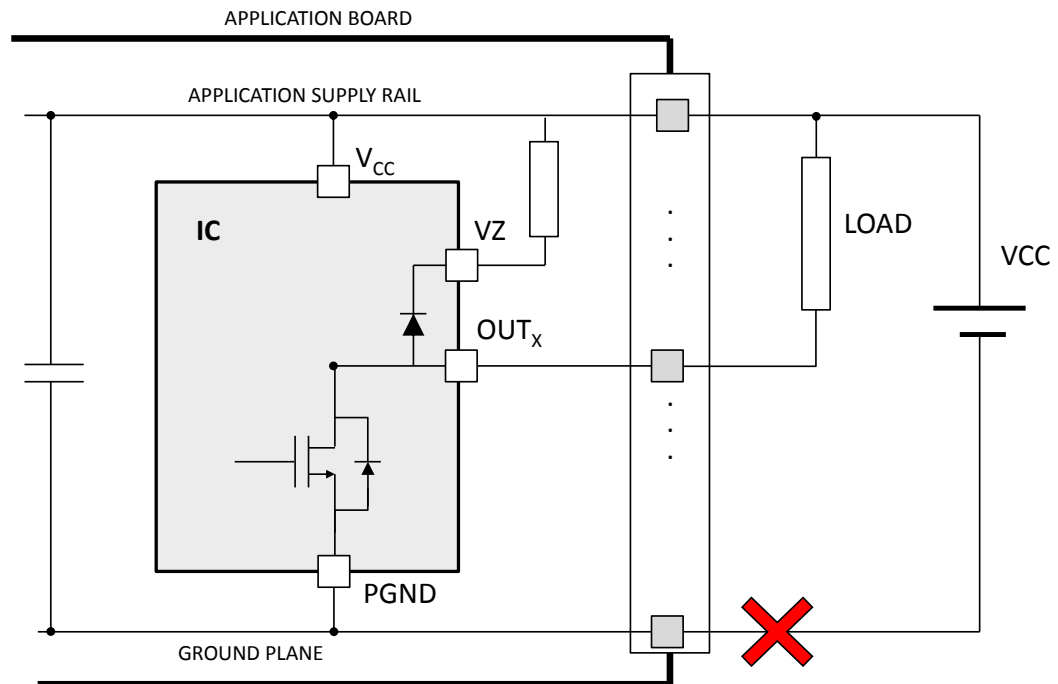
GND wire break is intended as the disconnection event of the application board ground (where both SGND and PGND signals are connected) from the system ground of the external supply rail (see Figure 11. GND wire break where the shape between VZ and supply rail represents one of the application configurations: open circuit, short circuit or an external TVS).

When this event happens, the supply voltage at Vcc pin decreases until  $V_{uvoff}$  is triggered and then all power stages are turned off independently of the input status.

In case of inductive load, if the ground disconnection event happens while one or more channels are active:

- in case of Vz pins floating, the residual current in the inductor flows through the integrated power switch, which is activated by active clamp as if the input had been deactivated.
- in case of Vz pins connected to supply rail (by short circuit or by TVS), the residual current in the inductor flows through the catch diodes. Similarly, the catch diodes allows the proper ground disconnection protection even in case of Vz pins connected by a TVS to ground layer.

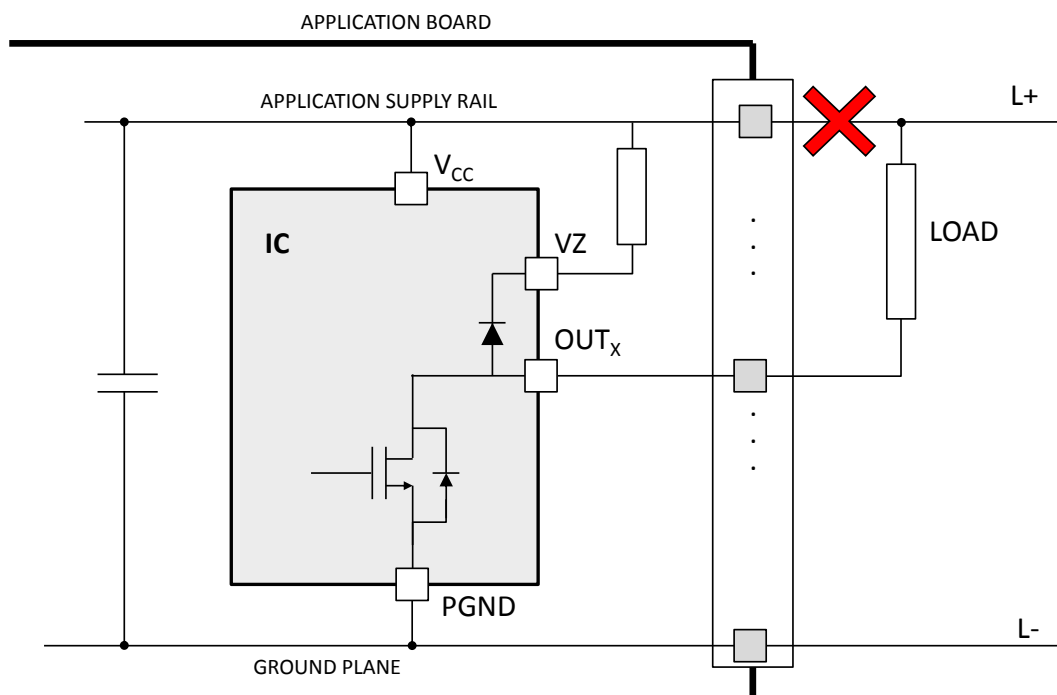
Figure 11. GND wire break



## 6.6 VCC wire break protection

VCC wire break is intended as the disconnection of the application board from rail supply (see Figure 12. VCC wire break), where the shape between VZ and supply rail represents one of the application configurations: open circuit, short circuit or an external TVS). When this condition is detected, all power stage channels are turned off independently of the input status. The maximum steady-state current measured through a channel in short to the supply voltage is not greater than  $I_{VD}$  (see Table 7. Logic inputs). The same behavior is guaranteed when all channels are simultaneously in short to the supply voltage. In case of inductive load, if the VCC is disconnected while one or more channels are active, the current flows through the power, which is activated by the active clamp as if the input had been deactivated.

Figure 12. VCC wire break



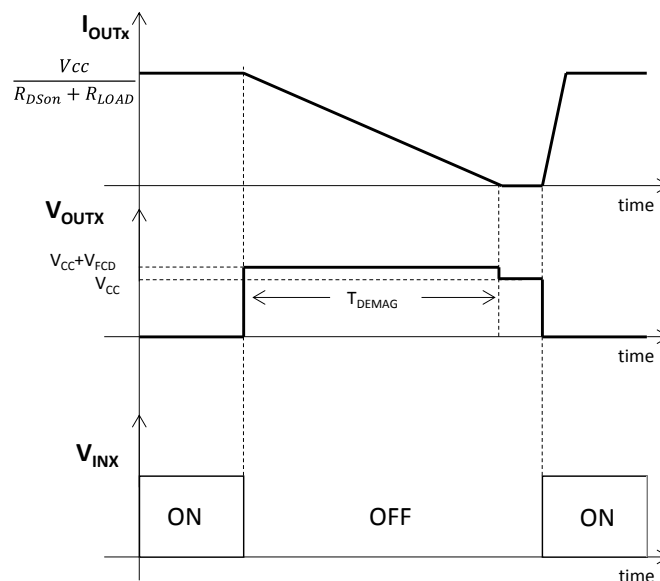
VCC wire break protection is guaranteed when VZ floats or when VZ is connected to GND by a proper TVS, while it is limited (see below) when VZ is shorted to V<sub>CC</sub>.

If VZ is connected to V<sub>CC</sub> by a TVS (with clamping voltage = V<sub>CL</sub>), then VCC wire break protection is limited by the following design rule:  $V_{CL} > V_{L+} - (V_{OUT} + V_D + V_{UVLO})$ .

## 7 Active clamp

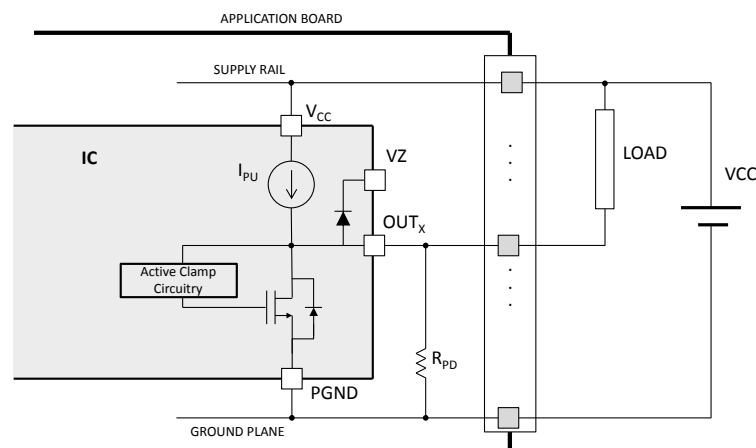
Active clamp is also known as fast demagnetization of inductive loads or fast current decay. When a low-side driver turns off an inductance, an overvoltage on load is detected. If VZ pins are directly shorted to the supply rail (see Figure 7) then the fast current decay is disabled: the inductive load is demagnetized slowly and according to the forward voltage of the integrated clamp diodes ( $V_{FCD}$ ). The figure below shows the typical waveforms of the load voltage and current in case of slow demagnetization.

Figure 13.  $V_{OUT}$  and  $I_{OUT}$  in case of slow demagnetization



If VZ pins are left floating (see Figure 14) or connected by a Zener or TVS diode to supply rail (see Figure 5) or PGND (see Figure 6) then the fast decay is activated. When VZ pins are left floating the integrated clamping circuit protects the IC despite overvoltages: the conduction state of the integrated switches is modulated in order to keep the OUTx pin voltage  $< V_{demag}$  until the energy in the load has been dissipated. The demagnetization energy is dissipated in the IC and it is limited by the internal heatsink capability, see EAS in Table 2. Absolute maximum ratings .

Figure 14. Active clamp equivalent principle schematic.

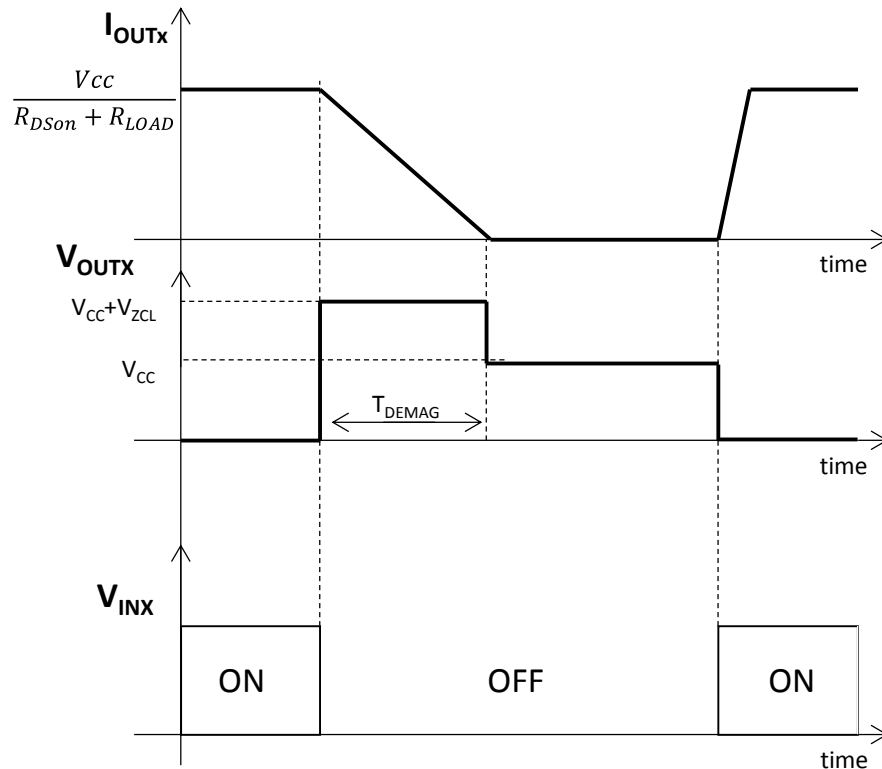




## 7.1 Fast current decay with TVS between VZ and supply rail

Being  $V_{CLZ}$  the clamping voltage of the external TVS, when the inductive load is turned off the OUTx pin is pulled up to  $V_{CC} + V_{CLZ}$ . In order to avoid any damage to the IC, the external diode must be selected such that  $V_{CLZ} < (V_{DEMAG(MIN)} - V_{CC})$ . Furthermore, the external diode must be selected such that it is able to dissipate the power due to the demagnetization currents flowing from the active channels.

**Figure 15.**  $V_{OUT}$  and  $I_{OUT}$  in case of fast demagnetization (fast decay)



## 7.2 Fast current decay with TVS between VZ and PGND

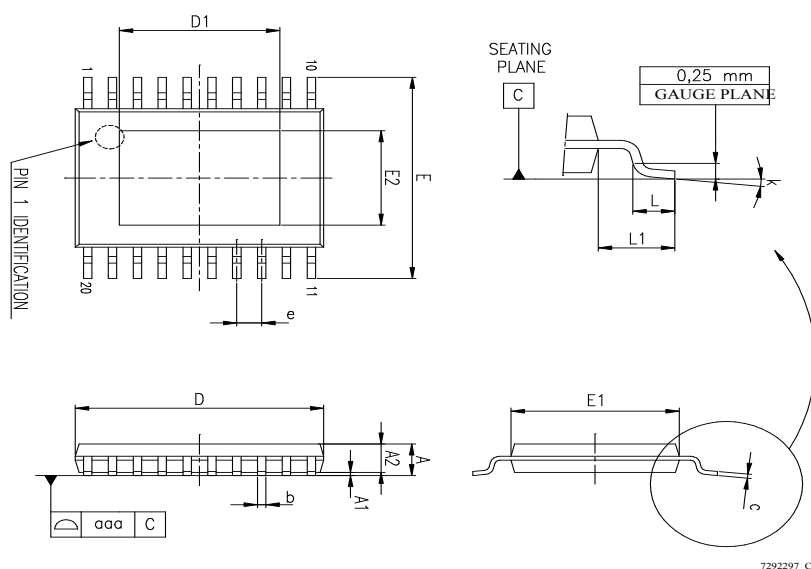
Being  $V_{CLZ}$  the clamping voltage of the external TVS, when the inductive load is turned off the OUTx pin is clamped by the lower voltage between  $V_{CLZ}$  and  $V_{DEMAG(MIN)}$ . In order to avoid any leakage current on the external TVS has to be selected such that its  $V_{BR}$  results  $> V_{CC}$ , while in order to avoid any damage to the IC the  $V_{CLZ}$  of the external TVS must be selected such that  $V_{CLZ} < V_{DEMAG(MIN)}$ . Further, the external diode must be selected such that it is able to dissipate the power due to the demagnetization currents flowing from the active channels.

## 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 8.1 HTSSOP20 package information

**Figure 16. HTSSOP20 package outline**



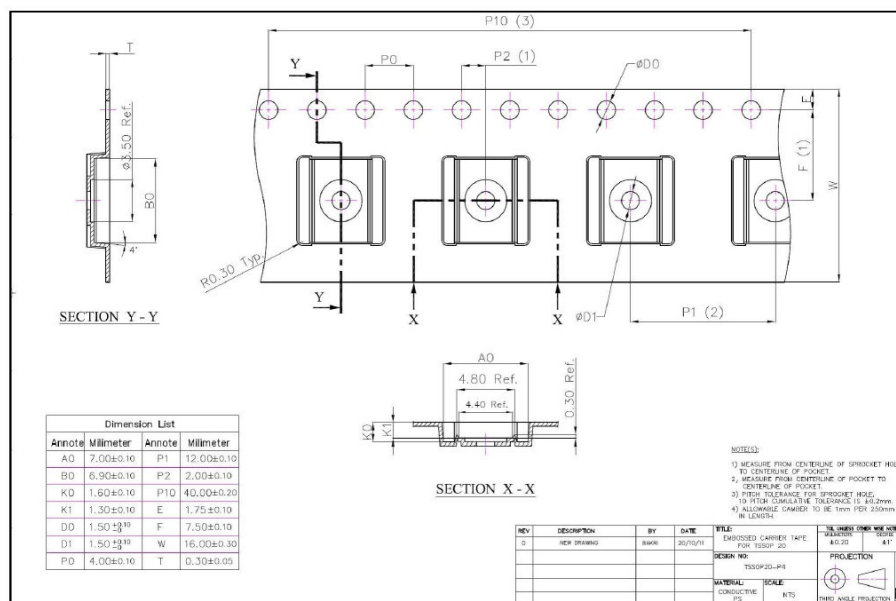
**Table 10. HTSSOP20 mechanical data**

Dim.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1			0.15		0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	6.4	6.5	6.6	0.252	0.256	0.260
D1	4.1	4.2	4.3	0.161	0.165	0.169
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.5	0.169	0.173	0.177
E2	2.9	3.0	3.1	0.114	0.118	0.122
e		0.65			0.0256	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

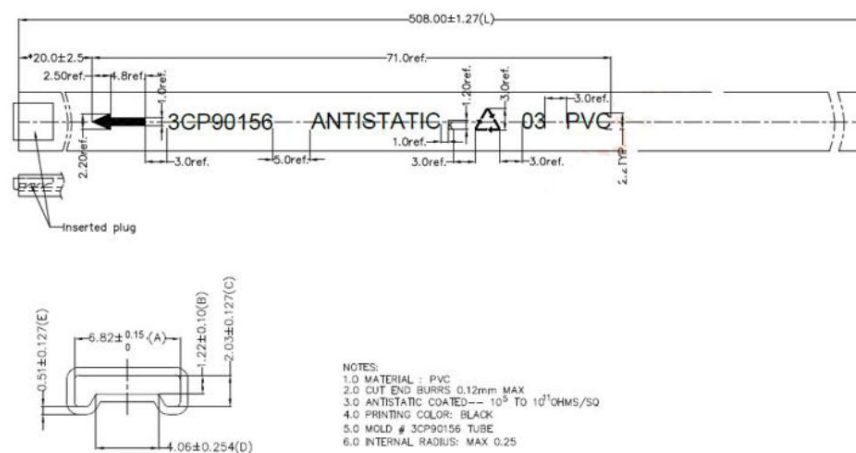
## 9 Packaging information

## 9.1 HTSSOP20 packaging information

**Figure 17. Carrier Tape for HTSSOP20 20L**



### Figure 18. HTSSOP20 Shipping Tube



## 10 Order information

**Table 11. Ordering information**

Order code	Package	Packing
IPS4260LM	HTSSOP20	Tube
IPS4260LMTR		Tape and reel

## Revision history

**Table 12. Document revision history**

Date	Revision	Changes
07-Nov-2023	1	Initial release.

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