ISOSD61

Datasheet

High accuracy isolated Sigma-Delta modulator

Product status link
ISOSD61

Product label
SUSTAINABLE TECHNOLOGY

Features

- Up to 25 MHz external clock input
- ±320 mV full scale analog input range
- 16 bits resolution, no missing codes
- 86 dB typical SNR
- -83 dB typical THD
- 13 bits typical ENOB
- Low Voltage Differential Signaling (LVDS) and Single - ended (TTL/CMOS) options
- –40°C to +125°C extended industrial temperature range
- SO-16 wide package
- 30 kV/µs typical High Common-mode transient immunity
- 5000 V_{PEAK} Isolation Voltage V_{IOTM}
- 1700 V_{PEAK} Working Voltage V_{IORM}
- Safety and Regulatory approvals:
  - IEC 60747-17 certified in SO16W package, File Number: 5022192-4880-0002/300335
  - UL1577 certified, File Number: E362869

Applications

Current or voltage sensing in:

- Industrial motor control
- Solar inverter
- UPS
- Electric vehicle charger
- Telecom and server power supply

Description

The ISOSD61 is a galvanic isolated second order Sigma-Delta modulator based on embedded transformer coupling technology. It converts an analog input signal with maximum range of ±320 mV into a high speed, 25 Msps, 1-bit digital data stream. The signal information can be rebuilt by means of a digital filtering. The modulator is isolated from the digital I/O section through a high-speed isolated data coupling, whose performances are far better than other isolated transceivers like optocouplers.

1 Device overview

Figure 1. **ISOSD61L Block diagram**

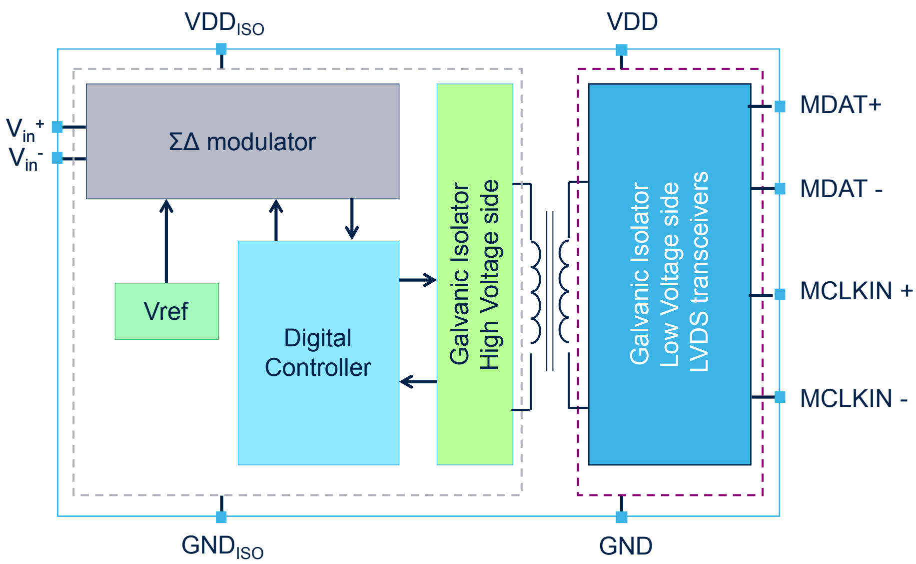
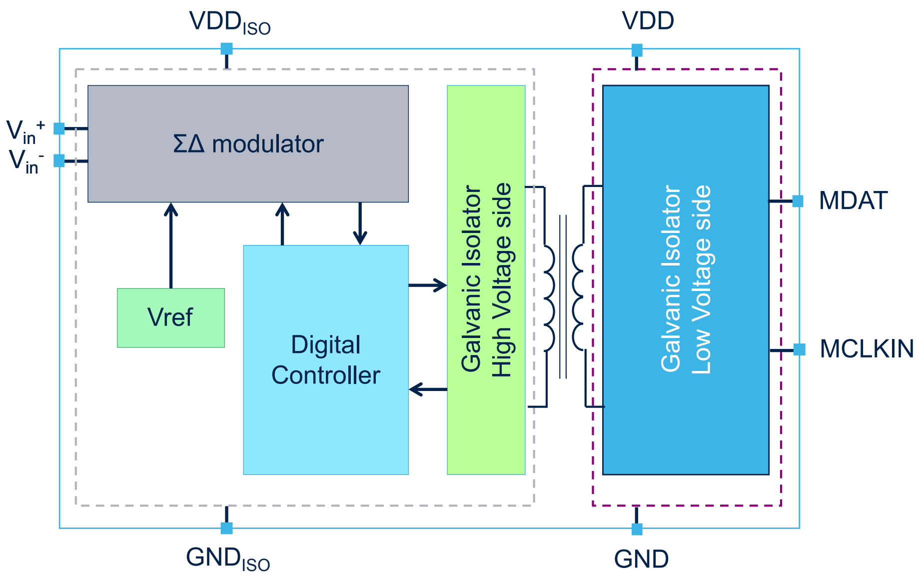
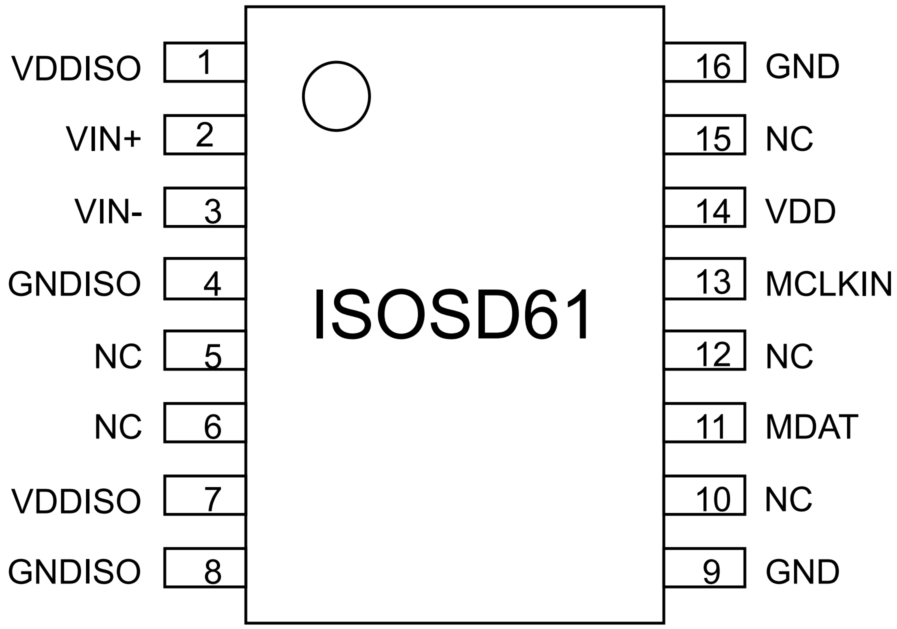


Figure 2. **ISOSD61 Block diagram**



2 Pin description



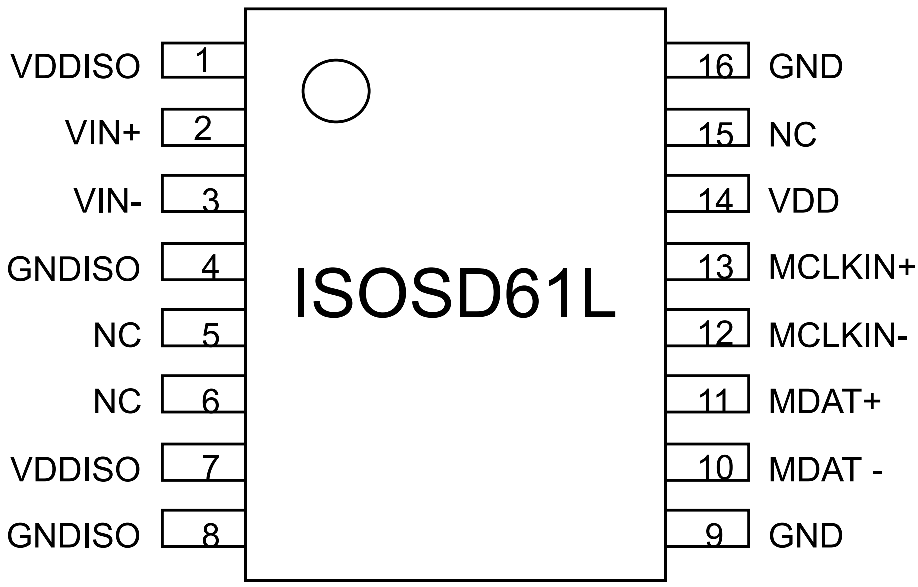


Figure 3. Pin connection

Table 1. Pin description

Pin No.	Pin name	Pin description (ISOSD61L)	Pin description (ISOSD61)
1	VDDISO	VDD high voltage side	VDD high voltage side
2	VIN+	Positive analog input	Positive analog input
3	VIN-	Negative analog input	Negative analog input
4	GNDISO	GND high voltage side	GND high voltage side
5	NC(1)		
6	NC(1)		
7	VDDISO	VDD high voltage side	VDD high voltage side
8	GNDISO	GND high voltage side	GND high voltage side
9	GND	GND low voltage side	GND low voltage side
10	MDAT-	Serial data output-	NC
11	MDAT+/MDAT	Serial data output+	Serial data output
12	MCLKIN-	Clock input-	NC
13	MCLKIN+/MCLKIN	Clock input+	Clock input
14	VDD	VDD low voltage side	VDD low voltage side
15	NC		
16	GND	GND low voltage side	GND low voltage side

1. *For test purpose only; it must be connected to GND in functional mode.*

3 Device specifications

Table 2. DIN EN IEC 60747-17 (VDE 0884-17) Isolation characteristics

Description	Symbol	Test Conditions	Characteristic	Unit
Maximum Repetitive Isolation Voltage	V_{IORM}	AC voltage	1500	V_{PEAK}
Maximum Working Isolation Voltage	V_{IOWM}	AC voltage (sinewave)	1060	V_{RMS}
		DC voltage	1500	V_{PEAK}
Partial Discharge test voltage	V_{PR}	Method a, Type and sample test $V_{PR} = V_{IORM} \times 1.6$, $t_m = 10$ s Partial discharge < 5 pC	2400	V_{PEAK}
		Method b1, 100 % Production test $V_{PR} = V_{IORM} \times 1.85$, $t_m = 1$ s Partial discharge < 5 pC	2812	V_{PEAK}
Maximum Transient Isolation Voltage	V_{IOTM}	Method a, Type an sample test $t_{ini} = 60$ s	5000	V_{PEAK}
Transient Isolation Voltage test	$V_{IOTM,test}$	Method b1, 100% Production test $V_{IOTM,test} = V_{IOTM} \times 1.2$ $t_{ini} = 1$ s	6000	V_{PEAK}
Maximum Impulse Voltage	V_{IMP}	Type test; tested in air 1.2/50 µs waveform per IEC 62368-1	4600	V_{PEAK}
Maximum Surge Isolation Voltage	V_{IOSM}	Type test; tested in oil 1.2/50 µs waveform per IEC 62368-1 $V_{IOSM} \geq V_{IMP} \times 1.3$	6000	V_{PEAK}
Isolation Resistance	R_{IO}	Type test; $V_{IO} = 500$ V $T_{amb} = 25$ °C	$>10^{12}$	Ω
		Type test; $V_{IO} = 500$ V 100 °C ≤ $T_{amb} \leq T_S$	$>10^{11}$	Ω
		Type test; $V_{IO} = 500$ V $T_{amb} = T_S = 150$ °C	$>10^{9}$	Ω

Table 3. UL 1577 Isolation characteristics

Descripion	Symbol	Test Conditions	Characteristic	Unit
Isolation Withstand Voltage	V_{ISO}	60 s; Type test	3540/5000	V_{RMS}/ V_{PEAK}
Isolation Voltage Test	$V_{ISO,test}$	1 S; 100% production	4240/6000	V_{RMS}/ V_{PEAK}

Table 4. Safety-limiting values (maximum values allowed in the event of a failure)

Description	Symbol	Value	Unit
Safety temperature	T_s	150	°C
Input current	$I_{S, INPUT}$	100	mA
Output power	$P_{S, OUPUT}$	1400	mW

Table 5. Isolation and safety-related specifications

Parameter	Symbol	Value	Unit	Conditions
Minimum External Air Gap (External Clearance)	CLR	8	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (External Creepage)	CPG	8	mm	Measured from input terminals to output terminals, shortest distance path along body
Tracking Resistance (Comparative Tracking Index)	CTI	≥ 400	V	IEC 60112
Isolation Group	-	II	-	according to IEC 60664-1
Overvoltage Category per IEC 60664-1		I - IV	-	Rated Mains voltages ≤ 150 V_{RMS}
		I - III	-	Rated Mains voltages ≤ 300 V_{RMS}
		I - II	-	Rated Mains voltages ≤ 600 V_{RMS}
		I	-	Rated Mains voltages ≤ 1000 V_{RMS}

Table 6. Absolute maximum ratings

Parameter	Symbol	Min.	Max.	Units
Storage temperature	T_S	-55	150	°C
Operating temperature	T_A	-40	125	°C
Supply voltage	V_{DD}, V_{DDISO}	-0.3	6	V
Steady-state input voltage	V_{IN+}, V_{IN-}	-0.3	V_{DDISO} + 0.5	V
Digital input/output voltages	MDAT+, MDAT- MCLKIN+, MCLKIN-	-0.3	V_{DD} + 0.5	V
Lead solder temperature			260 for 10 s.	°C

Table 7. Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Ambient operating temperature	T_A	-40	125	°C
VDD supply voltage	V_{DD}	3	5.5	V
VDDISO supply voltage	V_{DDISO}	4.5	5.5	V
Analog input voltage	V_{IN+}, V_{IN-}	-200	200	mV

Table 8. Electrical specifications

V_{DD}=3 V to 5.5 V, V_{DDISO} = 4.5 to 5.5 V, V_{IN+} = -200 mV to +200 mV, T_A=-40 to 125 °C, f_{MCLKIN}=5 to 25MHz unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test conditions
STATIC CHARACTERISTICS						
Resolution			16		bits	with SINC3 filter with OSR=256 and V_{IN+} - V_{IN-}=200 mV
Integral nonlinearity	INL		±3		LSB	

Parameter	Symbol	Min.	Typ.	Max.	Units	Test conditions
Differential nonlinearity	DNL		±0.2		LSB	No missing codes
Offset error	V_{VOS}		-0.8		mV	
Offset drift vs. temperature	TCV_{VOS}		1.5	4.5	μV/°C	
Offset drift vs. V_{DDISO}			200		μV/V	
Gain error	G_E			±1.0	%	
Gain error drift vs. Temperature	TCG_E		60		ppm/°C	
Gain error drift vs. V_{DDISO}			600		μV/V	
ANALOG INPUTS						
Full-scale differential voltage input range	FSR	-320		+320	mV	$V_{IN} = V_{IN+} - V_{IN-}$
Average input bias current	I_{INA}		–0.5		μA	V_{DDISO} = 5V, V_{DD} = 5V, V_{IN+} = 0 V;
	I_{INA}		40	50	μA	V_{DDISO} = 5 V, V_{DD} = 5 V, V_{IN+} = 300 mV;
Input capacitance	C_{INA}		10		pF	Across V_{IN+} or V_{IN-} to GNDISO
DYNAMIC CHARACTERISTICS						
Signal-to-noise ratio	SNR		86		dB	V_{IN+}=-200 mV to +200 mV f_{MCLKIN} = 5 to 15 MHz
						V_{IN+}=-250 mV to +250 mV f_{MCLKIN} = 20 MHz
Signal-to-(noise + distortion) ratio	SNDR		80		dB	
Effective number of bits	ENOB		13		bits	
Spurious free dynamic Range	SFDR		83		dB	
Total harmonic distortion	THD		-83		dB	
Common-mode transient immunity(1)	CMTI	25	30		kV/μs	Transient Pulse repetition frequency up to 100 KHz
POWER SUPPLY						
VDDISO supply current	I_{DDISO}		35		mA	@ 25 MHz
			30		mA	@ 10 MHz
VDD supply current	I_{DD}		13		mA	V_{DD} = 5 V, f_{MCLKIN} = 25 MHz
			11		mA	V_{DD} = 5 V, f_{MCLKIN} = 10 MHz
			12.5		mA	V_{DD} = 3.3 V, f_{MCLKIN} = 25 MHz
			10.5		mA	V_{DD} = 3.3 V, f_{MCLKIN} = 10 MHz

1. *Guaranteed by characterization*

Table 9. Timing specifications

Parameter	Symbol	Min.	Typ.	Max.	Units	Test conditions
Modulator clock input frequency	f_{CK}	5		25	MHz	Clock duty cycle 48% to 52%

Parameter	Symbol	Min.	Typ.	Max.	Units	Test conditions
Data delay after rising edge of CK	t_D	5		20	ns	CL = 15 pF

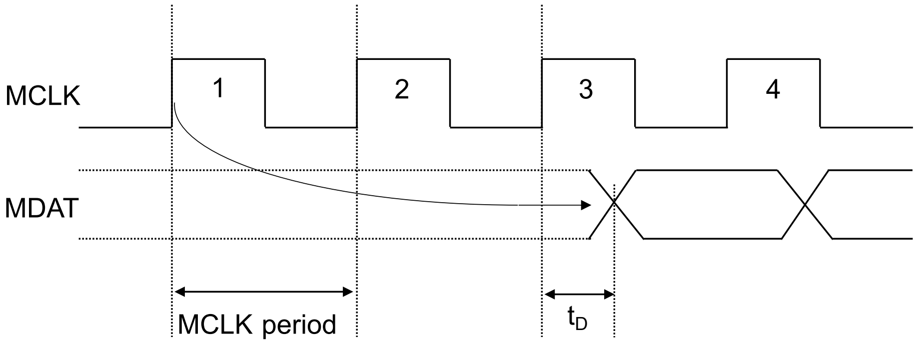


Figure 4. Timing sequence diagram

The data is provided to the MDAT output 2 clock cycles after the effective sampling instant.

Table 10. LVDS transmitter signaling specifications (ISOSD61L)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Output voltage high	V_{OH}	-0.3		1475	mV	R_{LOAD} = 110 Ω +/- 20%
Output voltage low	V_{OL}	925			mV	R_{LOAD} = 110 Ω +/- 20%
Output differential voltage	$\|V_{OD}\|$	240		420	mV	R_{LOAD} = 110 Ω +/- 20%
Output offset voltage	V_{OS}	1125	1200	1275	mV	R_{LOAD} = 110 Ω +/- 20%
Output current	I_O	2.2		3.7	mA	R_{LOAD} = 110 Ω +/- 20%
LVDS load impedance, single ended	R_L	80	110	140	Ω	V_{CM} = 1 V and 1.4 V
R_L mismatch between both channels	ΔR_L			10	%	
MDAT rise time	t_{LH}	0.5		5	ns	R_{LOAD} = 110 Ω +/- 20% C_{LOAD} = 30 pF
MDAT fall time	t_{HL}	0.5		5	ns	R_{LOAD} = 110 Ω +/- 20% C_{LOAD} = 30pF

Table 11. LVDS receiver signaling specifications

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Voltage range	V_R	-0.3		3.6	V	R_{LOAD} = 110 Ω +/- 20%
Common mode voltage(1)	V_C	0.05		2.4(2)	V	R_{LOAD} = 110 Ω +/- 20%
Differential input voltage(3)	$\|V_i\|$	100			mV	R_{LOAD} = 110 Ω +/- 20%
Differential input hysteresis voltage(4)	$\|V_{HYS}\|$	25			mV	R_{LOAD} = 110 Ω +/- 20%
Differential input capacitance	C_i			5	pF	R_{LOAD} = 110 Ω +/- 20%
Bias resistors(5)	$R_{PULLUP/PULLDOWN}$	140	200	260	k Ω	

1. *V_c is defined as the voltage that is mid-way between VH and VL.*
2. *This parameter is guaranteed with Vdd > 4 V.*
3. *$|V_i|$ defines the minimum differential voltage that is guaranteed to be recognized as a valid input, 1 or 0, by the receiver.*

4. $|V_{hys}|$ *defines the minimum voltage separation between the actual |Vi| rising and falling thresholds.*
5. *A pullup resistor is present between the minus LVDS input and V3.3, and a pulldown resistor is present between plus LVDS input and GND in order to force a '0' value if the LVDS input is floating.*

Table 12. Single-ended input and output signaling specifications (ISOSD61)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input high voltage	V_{IH}	2			V	V_{DD} = 3.3 V
		V_{DD} x 0.7			V	V_{DD} = 5 V
Input low voltage	V_{IL}			0.8	V	V_{DD} = 3.3 V
				V_{DD} x 0.3	V	V_{DD} = 5 V
Input current	I_{IND}		±0.5		µA	
Input capacitance	C_{IND}		6		pF	
Output high voltage	V_{OH}	V_{DD} – 0.06	V_{DD} – 0.04		V	V_{DD} = 5 V, I_{OUT} = -0.2 mA
		V_{DD} – 0.05	V_{DD} – 0.03			V_{DD} = 3.3 V, I_{OUT} = -0.2 mA
Output low voltage	V_{OL}		0.01	0.02	V	I_{OUT} = 0.2 mA

Table 13. Package characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test conditions
IC junction-to-ambient thermal resistance	θ_{JA}		80		°C/W	On a 2s2p JEDEC board in free air as per JEDEC JESD51, TA = 25°C

4 Terminology

Differential Nonlinearity (DNL)

DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Integral Nonlinearity (INL)

INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Offset error

Offset error is the deviation of the center scale code from the ideal scale code corresponding to 0 V differential input voltage.

Gain error

The gain is the derivative of the digital output code vs. the input signal. Graphically, for the output code vs. input signal transfer function (an ideal straight line), the gain is the slope of such function. The gain error is the % difference between the measured slope and the expected one.

Signal-to-Noise-and-Distortion Ratio (SINAD or SNDR)

SINAD is the measured ratio of signal to noise and distortion at the output of the ADC. The signal is the RMS value of the sine wave, and noise is the RMS sum of all non-fundamental AC signals up to half the sampling frequency (fS / 2), including harmonics.

Signal-to-Noise Ratio (SNR)

SNR is the measured ratio of signal to noise at the output of the ADC. The signal is the RMS amplitude of the fundamental. Noise is the RSM sum of all non-fundamental AC signals up to half the sampling frequency ($f_S/2$).

The ratio is dependent on the number of quantization levels in the conversion: the greater the number of levels, the smaller the quantization noise. The theoretical signal-to-noise ratio for an ideal N-bit converter with a sine wave input is given by

Signal-to-Noise Ratio = (6.02N + 1.76) [dB]

Therefore, for a 12-bit converter, the SNR is 74 dB.

Isolation transient immunity

The isolation transient immunity specifies the rise and fall speed of a transient pulse applied across the isolation barrier, beyond which clock or data is corrupted.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of harmonics to the fundamental. The THD stated in this datasheet is defined as:

$$\mathrm{THD} = 20\log\frac{\sqrt{V_2{}^2 + V_3{}^2 + V_4{}^2 + V_5{}^2 + V_6{}^2}}{V_1}$$

where: V_1 is the RMS amplitude of the fundamental. V_2, V_3, V_4, V_5, and V_6 are the RMS amplitudes of the second through the sixth harmonics. The result is in dB.

Spurious Free Dynamic Range (SFDR)

SFDR is defined as the ratio of the RMS value of the AC Noise Peak (up to f_S / 2) to the RMS value of the fundamental.

Effective Number of Bits (ENOB)

ENOB is defined by:

ENOB = (SINAD - 1.76) / 6.02 [bits]

Noise free code resolution

Noise free code resolution represents the resolution in bits for which there is no code flicker. The noise free code resolution for an N-bit converter is defined as

$$Noisefree\ \ code\,resolution = \log_2\left(\frac{2^N}{Peak - to - Peak\ Noise}\right)[bits]$$

The peak-to-peak noise in LSBs is measured with VIN+ = VIN− = 0 V.

Common-Mode Rejection Ratio (CMRR)

CMRR is defined as the ratio of the power in the ADC output with an input differential sine wave, PD, to the power of an input peak-to-peak sine wave applied to the common-mode voltage of VIN+ and VIN−, P_{CM}, as:

$$CMRR\ (dB) = 10\ log(P_D/P_{CM})$$

Power Supply Rejection Ratio (PSRR)

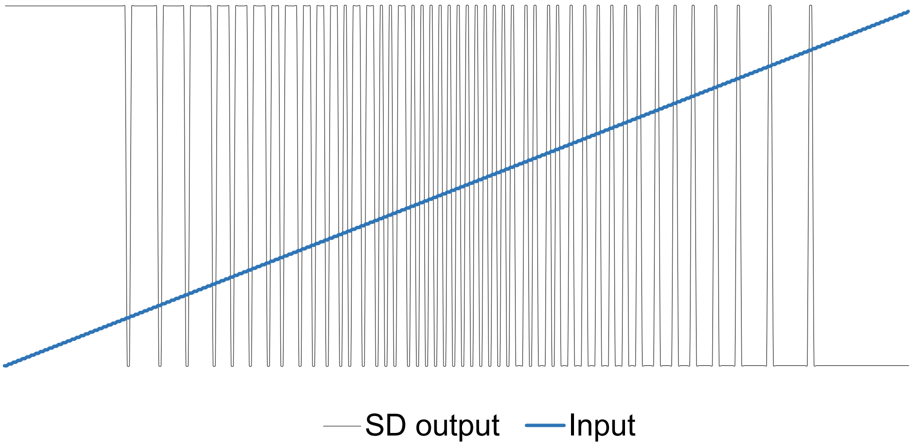
Variations in power supply affect the full-scale transition but not the linearity of the converter. PSRR is the maximum change in the specified full-scale transition point due to a change in power supply voltage from the nominal value.

$$PSRR = 20\ log\ (change\ in\ supply/change\ in\ output\ voltage)$$

5 Theory of operation

The differential analog input of the ISOSD61 implements a second-order modulator stage that digitizes the input signal into a 1-bit output stream. The sample clock (MCLKIN) provided externally, is the clock signal for the conversion process as well as the output data-framing clock. The analog input signal is continuously sampled by the modulator and compared to an internal voltage reference. A digital stream that accurately represents the analog input over time appears at the output of the converter.

Figure 5. **Sigma-Delta data stream vs. differential input voltage ramp**



A differential signal of 0 V results (ideally) in a stream of alternating 1s and 0s at the MDAT output pin. This output is high 50% of the time and low 50% of the time. Any differential input voltage produces a stream whose ratio between 1s and the total number of pulses of the time is proportional to the ratio between the input voltage and the full-scale differential range (+320 mV - -320 mV= 640 mV). The correspondent equation is:

$$\frac{nr\ of\ 1s}{tot\ nr\ of\ pulses} = 0.5 + \frac{Vin}{640}$$

Where: Vin: input differential voltage [mV]; nr of 1s: count of 1 bit over a given time; tot nr of pulses: count of the total 1 and 0 bits over the given time.

This means for a maximum positive differential input signal +320 mV there would be only 1s (signal stuck at 1) and for a maximum negative of -320 mV only 0s (signal stuck at 0).

To decode the original information, the digital output stream must be digitally filtered and decimated. A recommended filter is the SINC3 3rd order decimator. The SINC3 filter can be easily realized, for instance, with a FPGA or an MCU like STM32.

5.1 Analog inputs

The analog front-end of the modulator implements a differential switched capacitor circuitry, whose purpose is to sample and hold the analog signal every clock cycle. Like any A/D converter, to prevent the conversion of aliasing signal, in accordance to the Nyquist-Shannon theorem, a low-pass filter should be added at the analog inputs. Its cut- frequency should be below half the sampling frequency. The capacitors of this LP filter help to smooth the undershoots and overshoots of the internal switching capacitors. Every switching has a charge current injected, and the effective impedance of the analog inputs decreases with the clock frequency increasing. To avoid undesired signal voltage drops, the LP filter resistors should have a value in the order of tenth of ohms.

5.2 Digital filtering

A typical filtering technique for sigma-delta modulators is the implementation af an SINC3 digital filter. The code below is an example of a generic SINC3 filter written for GNU Octave that can be easily ported to other languages or systems:

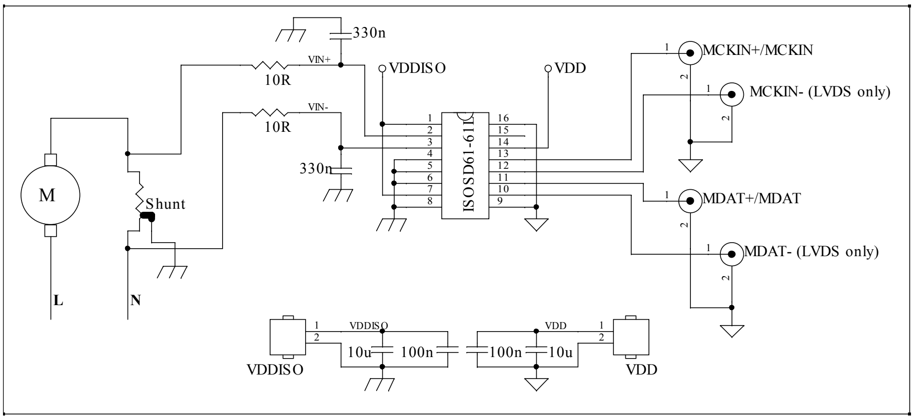
```
function [output, output_dec]=sinc3_generic(in)
%in is 1xsamples
%output is 1xsamples
```

```
%output_dec is 1x(samples/dec_fact)
nbits = 25;
accbits = 46; %minimum accumulator size
dutbits = 16;
stages = 3;
dec_fact = 256;
dim = size(in);
samples = dim(2);
feed_state = zeros(1,stages);
fwd_state = zeros(1, stages);
i = 1;
out_feed_state = 0;
for k=1:samples
if ( i > 1 )
output(k) = round(out_feed_state * 2^((dutbits-1)));
else
output(k) = 0;
end
if ( k == dec_fact*i )
output_dec(i) = round(out_feed_state * 2^((dutbits-1)));
in_fwd = feed_state(stages);
fwd_sum = 0;
for s=1:stages
fwd_sum += fwd_state(s);
end
out_feed_state = in_fwd - fwd_sum;
si = stages;
while(si > 1)
fwd_sum = 0;
for s=1:(si-1)
fwd_sum += fwd_state(s);
end
fwd_state(si) = in_fwd - fwd_sum;
si--;
end
fwd_state(1) = in_fwd;
i++;
end
si = stages;
while(si > 1)
feed_state(si) = feed_state(si) + feed_state(si-1);
si--;
end
feed_state(1) = feed_state(1) + in(k)* 2^(-(nbits-1));
end
end
```

5.3 Application design tips

In Figure 6 below a typical application schematics is shown:

Figure 6. Typical application schematics



Large use of capacitors on both VDDiso and VDD supply pins for decoupling is strongly recommended.

Though the device can withstand high transients across the isolation barrier, the application designer must take care of board coupling between the analog front-end and the digital back-end domains. They must also take design actions in order to avoid any loss of clearance and creepage distances. Failure to ensure these can lead to severe permanent damage.

The analog input tracks should be kept symmetrical and equalized in impedance, to minimize additional offset.

The use of ground planes for noise reduction is recommended.

For LVDS digital interfacing, the use of termination resistors (typically 100 ohm) is recommended.

6 Package description

The ISOSD61/61L is hosted in an SO-16 wide package. The mechanical drawing is shown below.

Figure 7. Mechanical drawing

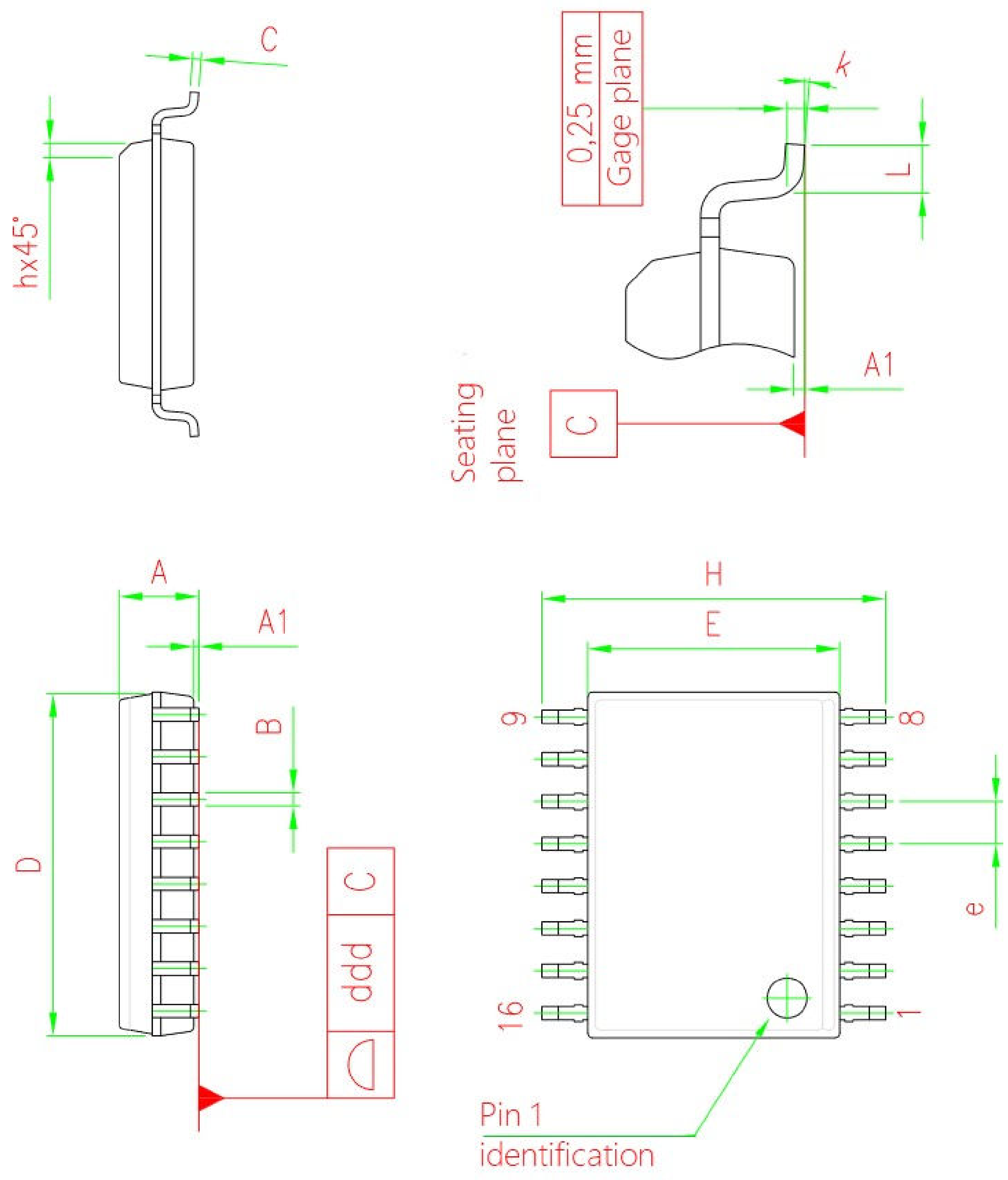
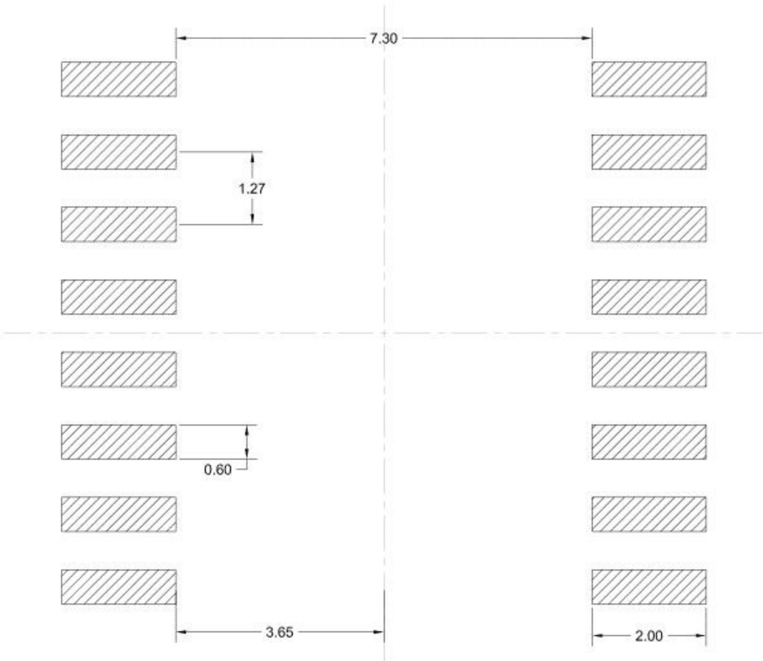


Table 14. **Package dimensions**

Dimensions							
	Databook (mm)			Drawing (mm)			
Param.	Min.	Typ.	Max.	Min.	Typ.	Max.	Notes
A	2.35		2.65	2.36		2.50	
A1	0.10		0.30	0.12	0.15	0.18	
B	0.33		0.51	0.375	0.40	0.425	
C	0.23		0.32			0.292	
D	10.10		10.50	10.35	10.38	10.41	(1)
E	7.40		7.60	7.52	7.55	7.58	
e		1.27			1.27		
H	10		10.65	10.20	10.30	10.40	
h	0.25		0.75		0.35		
L	0.40		1.27	0.60		0.75	
k	0		8	2	4	6	DEGREES
ddd			0.10			0.06	

1. *Dimension D does not include mold flash, protrusions or gate burrs.*
   Mold flash, protrusions, or gate burrs shall not exceed 0.15mm per side.

Figure 8. Recommended footprint



7 Ordering information

Table 15. **Device summary**

Order code	Package	Package Marking	Packing
ISOSD61	SO16W	ISOSD61	Tray
ISOSD61TR	SO16W	ISOSD61	Tape and Reel
ISOSD61L	SO16W	ISOSD61L	Tray
ISOSD61LTR	SO16W	ISOSD61L	Tape and Reel

Revision history

Table 16. **Document revision history**

Date	Version	Changes
11-Jan-2021	1	Initial release.
26-Jan-2021	2	Added Table 15. Device summary
10-Mar-2021	3	Deleted wrong hyperlinks.
03-May-2021	4	Modified Section Features and Figure 8. Recommended footprint
21-Jun-2021	5	Modified Table 2. DIN EN IEC 60747-17 (VDE 0884-17) Isolation characteristics and added Table 3. UL 1577 Isolation characteristics
01-Dec-2021	6	Modified Section 3: Device specifications
12-Apr-2022	7	Modified Section Features, Section Applications, Table 8. Electrical specifications and Section 5: Theory of operation
05-Jul-2022	8	Updated UL1577 certification status from "pending" to "certified" in Section Features
24-Sep-2024	9	Updated Table 2. DIN EN IEC 60747-17 (VDE 0884-17) Isolation characteristics and Section Features, in accordance to VDE certification; updated Figure 7 and Figure 8.
28-Nov-2024	10	Modified Section 3: Device specifications
24-Mar-2025	11	Modified Table 2

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