LM2698 SIMPLE SWITCHER® 1.35-A Boost Regulator

1 Features

- 1.9-A, 0.2-Ω Internal Switch (Typical)
- Operating Voltage as Low as 2.2 V
- 600 kHz to 1.25 MHz Adjustable Frequency Operation
- Switchers Made Simple® Software
- 8-Pin VSSOP Package

2 Applications

- 3.3 V to 5 V and 5 V to 12 V Conversion
- Distributed Power
- Set-Top Boxes
- DSL Modems
- Diagnostic Medical Instrumentation
- Boost Converters
- Flyback Converters
- SEPIC Converters

3 Description

The LM2698 device is a general purpose PWM boost converter. The 1.9-A, 18-V, 0.2-Ω internal switch enables the LM2698 to provide efficient power conversion to outputs ranging from 2.2 V to 17 V. It can operate with input voltages as low as 2.2 V and as high as 12 V. Current-mode architecture provides superior line and load regulation and simple frequency compensation over the device's 2.2 V to 12 V input voltage range. The LM2698 sets the standard in power density and is capable of supplying 12 V at 400 mA from a 5-V input. The LM2698 can also be used in flyback or SEPIC topologies.

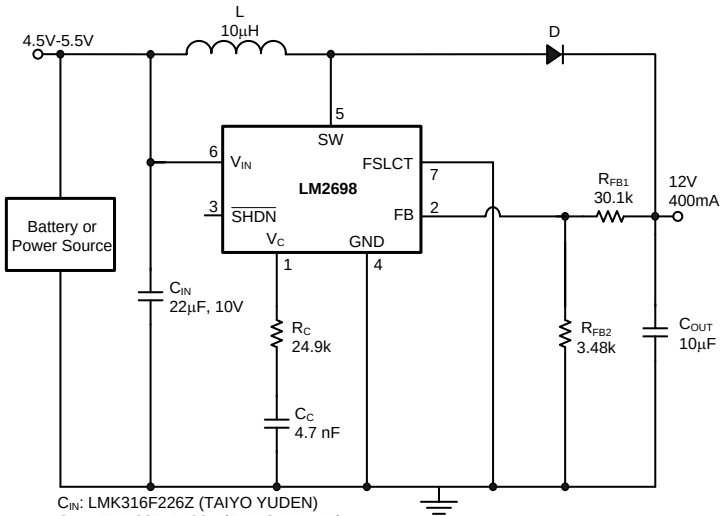
The LM2698 SIMPLE SWITCHER® features a pin selectable switching frequency of either 600 kHz or 1.25 MHz. This promotes flexibility in component selection and filtering techniques. A shutdown pin is available to suspend the device and decrease the quiescent current to 5 µA. An external compensation pin gives the user flexibility in setting frequency compensation, which makes possible the use of small, low-ESR ceramic capacitors at the output. Switchers Made Simple® software is available to ensure a quick, easy, and assured design. The LM2698 is available in a low-profile, 8-pin VSSOP (DGK) package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM2698	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



C_{IN}: LMK316F226Z (TAIYO YUDEN)
C_{OUT}: EMK325B5106K (TAIYO YUDEN)
L: DO3316-103 (COILCRAFT)
D: 0MQ040N (MOTOROLA)

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (April 2013) to Revision F **Page**

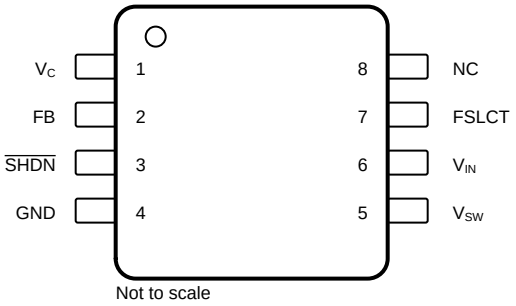
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Ordering Information* table, see POA at the end of the datasheet. ... 1
- Changed values in the *Thermal Information* table to align with JEDEC standards ... 5

Changes from Revision D (April 2013) to Revision E **Page**

- Changed layout of National Semiconductor Data Sheet to TI format ... 1

5 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View



Not to scale

Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	V_C	A	Compensation network connection. Connected to the output of the voltage error amplifier.
2	FB	A	Output voltage feedback input.
3	$\overline{SHDN}$	I	Shutdown control input, active low.
4	GND	G	Analog and power ground.
5	V_{SW}	A	Power switch input. Switch connected between SW pin and GND pin.
6	V_{IN}	P	Analog power input.
7	FSLCT	I	Switching frequency select input. V_{IN}= 1.25 MHz. Ground = 600 kHz.
8	NC	—	Connect to ground.

(1) A = Analog, G = Ground, I = Input, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
V_{IN}	–0.3	12	V
SW voltage	–0.3	18	V
FB voltage	–0.3	7	V
V_C voltage	0.965	1.565	V
$\overline{SHDN}$ voltage(2)	–0.3	7	V
FSLCT(2)	–0.3	12	V
Power dissipation(3)	Internally limited		°C
Lead temperature		300	°C
Vapor phase temperature (60 s)		215	°C
Infrared temperature (15 s)		220	°C
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Shutdown and voltage frequency select must not exceed V_{IN}.
(3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J(MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. See the *Electrical Characteristics* for the thermal resistance of various layouts. The maximum allowable power dissipation at any ambient temperature is calculated using P_D (MAX) = ($T_{J(MAX)}$ – T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation causes excessive die temperature, and the regulator goes into thermal shutdown.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage	2.2		12	V
SW voltage	0		17.5	V
Operating junction temperature(1)	–40		125	°C

(1) All limits are specified at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% tested or specified through statistical analysis. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

6.4 Thermal Information

THERMAL METRIC[1]		LM2698 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	142.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	67.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_J = 25°C, V_{IN} =2.2 V, and I_L = 0 A (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN[1]	TYP[2]	MAX[1]	UNIT
I_Q	Quiescent current	FB = 0 V (not switching)	T_J = 25°C		1.3		mA
			T_J = –40°C to 125°C			2	
		$V_{\overline{SHDN}}$ = 0 V	T_J = 25°C		5		µA
			T_J = –40°C to 125°C			10	
V_{FB}	Feedback voltage	T_J = 25°C			1.26		V
		T_J = –40°C to 125°C		1.23		1.29	
I_{CL}	Switch current limit	V_{IN} = 2.7 V[3]	T_J = 25°C		1.9		A
			T_J = –40°C to 125°C	1.35		2.4	
$\%V_{FB}/\Delta V_{IN}$	Feedback voltage line regulation	2.2 V ≤ V_{IN} ≤ 12 V	T_J = 25°C		0.013%		V
			T_J = –40°C to 125°C			0.1%	
I_B	FB pin bias current[4]	T_J = 25°C			0.5		nA
		T_J = –40°C to 125°C				20	
V_{IN}	Input voltage range	T_J = –40°C to 125°C		2.2		12	V
g_m	Error amp transconductance	ΔI = 5 µA	T_J = 25°C		135		µmho
			T_J = –40°C to 125°C	40		290	
A_V	Error amp voltage gain				120		V/V
D_{MAX}	Maximum duty cycle	FSLCT = Ground	T_J = 25°C		85%		
			T_J = –40°C to 125°C	78%			
D_{MIN}	Minimum duty cycle	FSLCT = Ground			15%		
		FSLCT = V_{IN}			30%		
f_S	Switching frequency	FSLCT = Ground	T_J = 25°C		600		kHz
			T_J = –40°C to 125°C	480		720	
		FSLCT = V_{IN}	T_J = 25°C		1.25		MHz
			T_J = –40°C to 125°C	1		1.5	
$I_{\overline{SHDN}}$	Shutdown pin current	$V_{\overline{SHDN}}$ = V_{IN}	T_J = 25°C		0.01		µA
			T_J = –40°C to 125°C			0.1	
		$V_{\overline{SHDN}}$ = 0 V	T_J = 25°C		–0.5		
			T_J = –40°C to 125°C			–1	

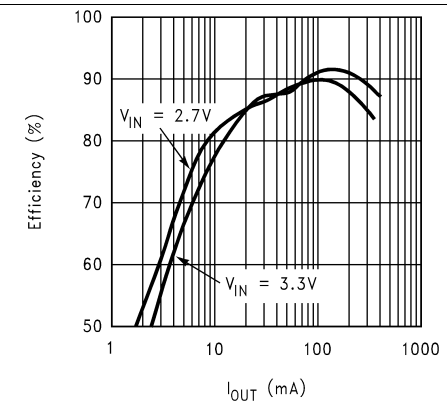
(1) All limits are specified at room temperature and at temperature extremes. All room temperature limits are 100% tested or specified through statistical analysis. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely norm.
(3) This is the switch current limit at 0% duty cycle. The switch current limit changes as a function of duty cycle. See *Typical Characteristics* for I_{CL} vs V_{IN}.
(4) Bias current flows into FB pin.

Electrical Characteristics (continued)

T_J = 25°C, V_{IN} =2.2 V, and I_L = 0 A (unless otherwise noted)

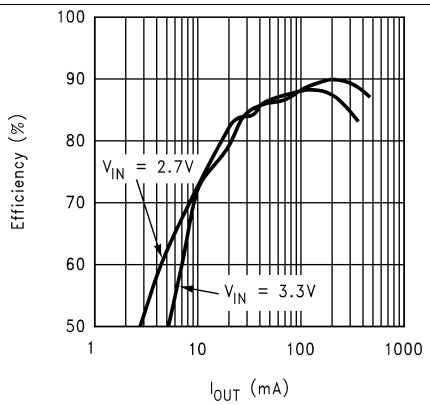
PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
I_L	Switch leakage current	V_{SW} = 18 V	T_J = 25°C		0.01		µA
			T_J = –40°C to 125°C			3	
$R_{DS(ON)}$	Switch $R_{DS(ON)}$	V_{IN} = 2.7 V, I_{SW} = 1 A	T_J = 25°C		0.2		Ω
			T_J = –40°C to 125°C			0.4	
TH_{SHDN}	$\overline{SHDN}$ threshold voltage	Output high	T_J = 25°C		0.6		V
			T_J = –40°C to 125°C			0.9	
		Output low	T_J = 25°C		0.6		
			T_J = –40°C to 125°C	0.3			
UVP	On threshold	T_J = 25°C			2.05		V
		T_J = –40°C to 125°C		1.95		2.2	
	Off threshold	T_J = 25°C			1.95		V
		T_J = –40°C to 125°C		1.85		2.1	

6.6 Typical Characteristics



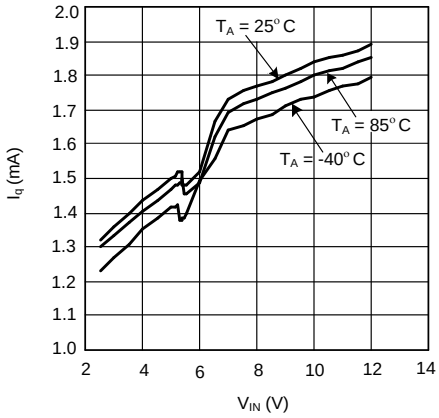
V_{OUT} = 8 V f_S = 600 kHz

Figure 1. Efficiency vs Load Current



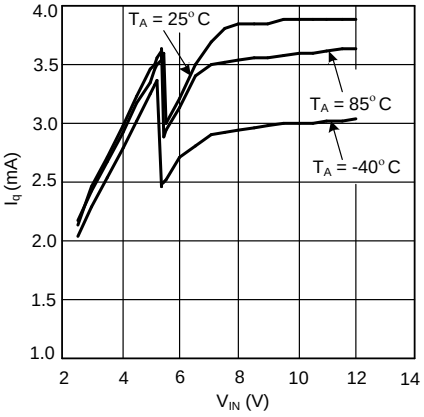
V_{OUT} = 8 V f_S = 1.25 MHz

Figure 2. Efficiency vs Load Current



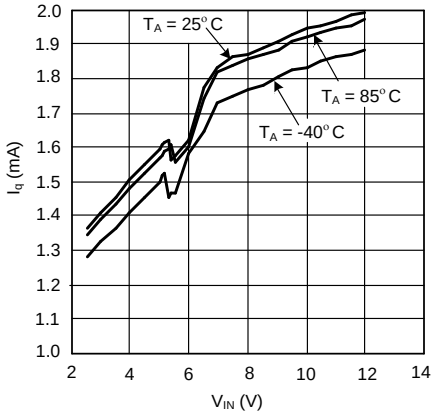
600 kHz Non-Switching

Figure 3. I_q vs V_{IN}



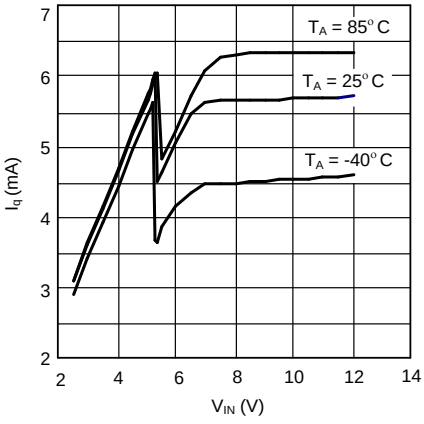
600 kHz Switching

Figure 4. I_q vs V_{IN}



1.25 MHz Non-Switching

Figure 5. I_q vs V_{IN}



1.25 MHz Switching

Figure 6. I_q vs V_{IN}

Typical Characteristics (continued)

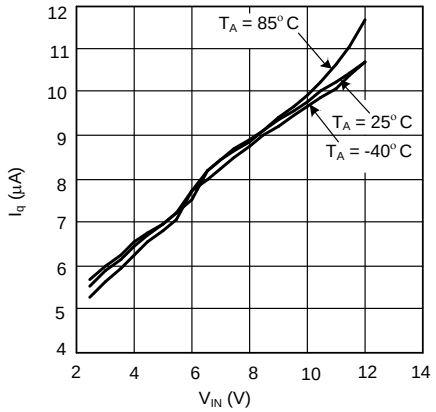


Figure 7. $I_{q(SHDN)}$ vs V_{IN}

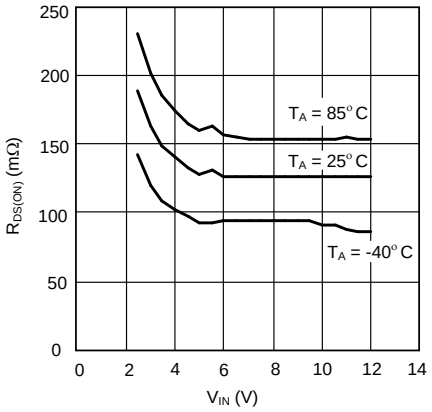


Figure 8. $R_{DS(ON)}$ vs V_{IN}

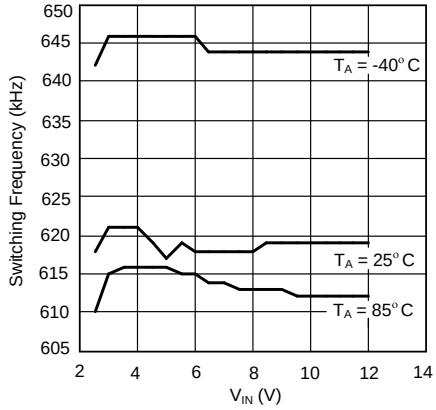


Figure 9. Switching Frequency vs V_{IN} (600 kHz)

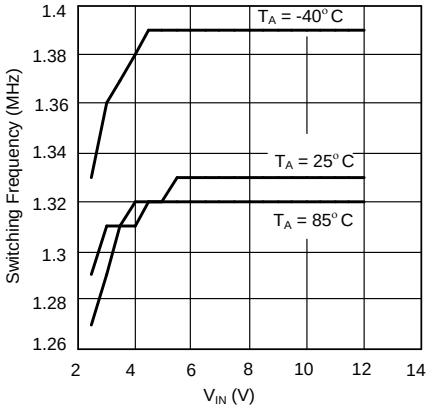
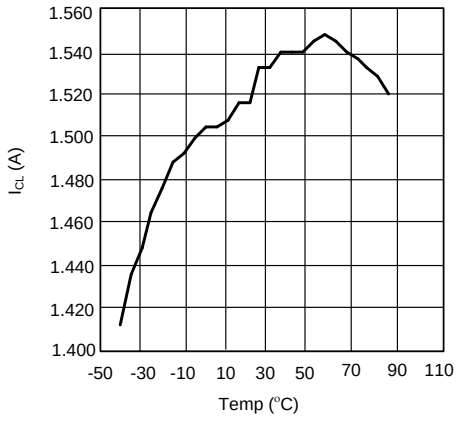


Figure 10. Switching Frequency vs V_{IN} (1.25 MHz)



V_{IN} = 3.3 V V_{OUT} = 8 V

Figure 11. I_{CL} vs Ambient Temperature

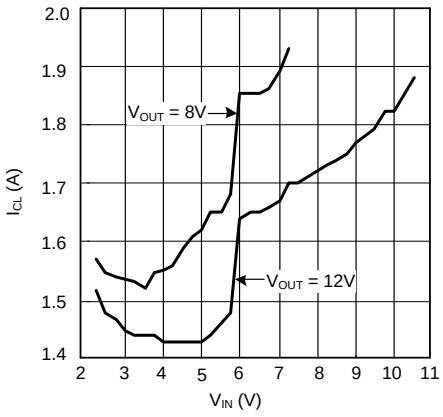


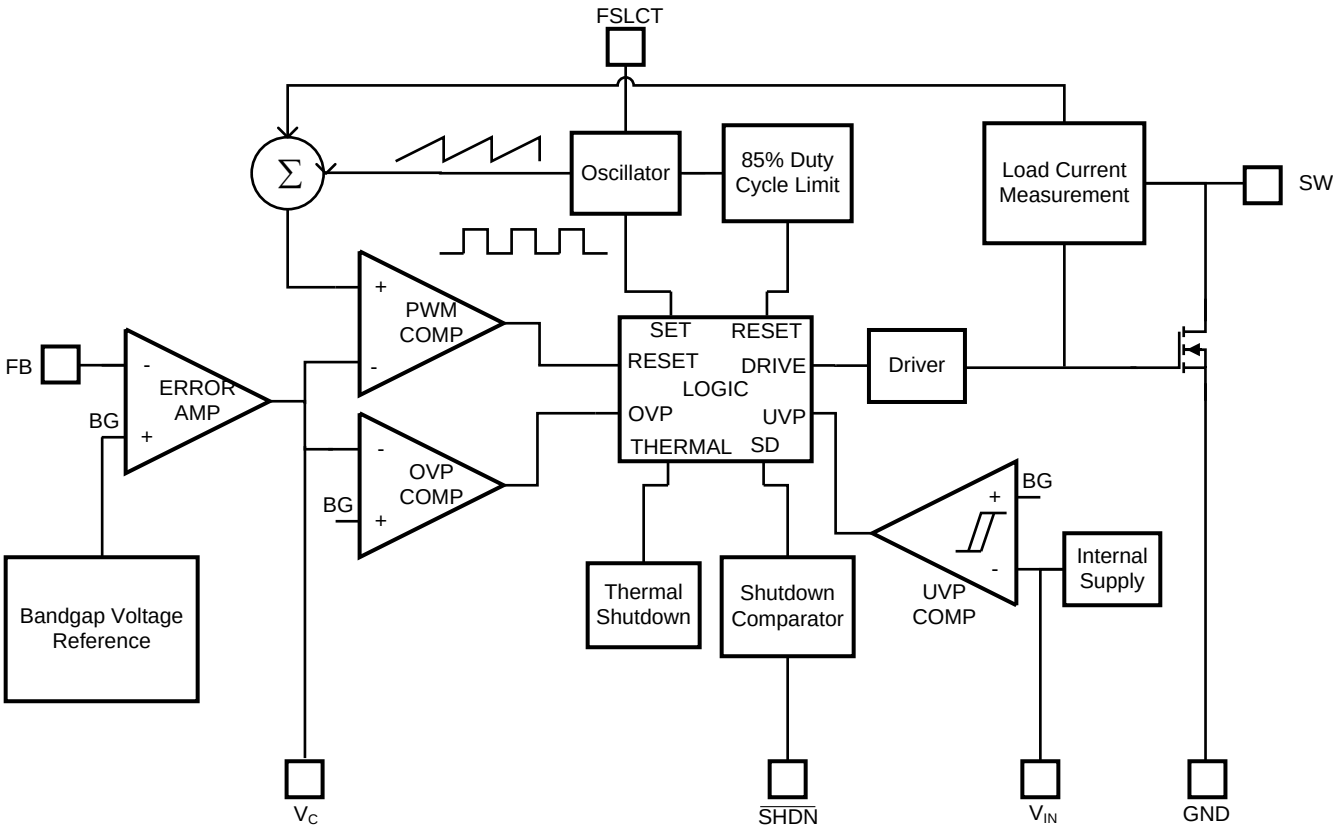
Figure 12. I_{CL} vs V_{IN}

7 Detailed Description

7.1 Overview

The LM2698 is a boost controller with integrated primary switch. The LM2698 functions in current mode control by sensing the current into the integrated switch and adding a slope to the signal for slope compensation purpose. The device provides a cycle by cycle current limiting and the duty cycle is limited to 85% to ensure an additional level of protection. A frequency selection pin FSLCT allows the designer to choose between two switching frequencies (600 kHz or 1250 kHz). A shutdown pin is available to suspend the device and decrease the quiescent current to 5 µA by pulling the pin to a logic high.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Inductor

The inductor is one of the two energy storage elements in a boost converter. Figure 13 shows how the inductor current varies during a switching cycle. The current through an inductor is quantified with Equation 1.

Feature Description (continued)

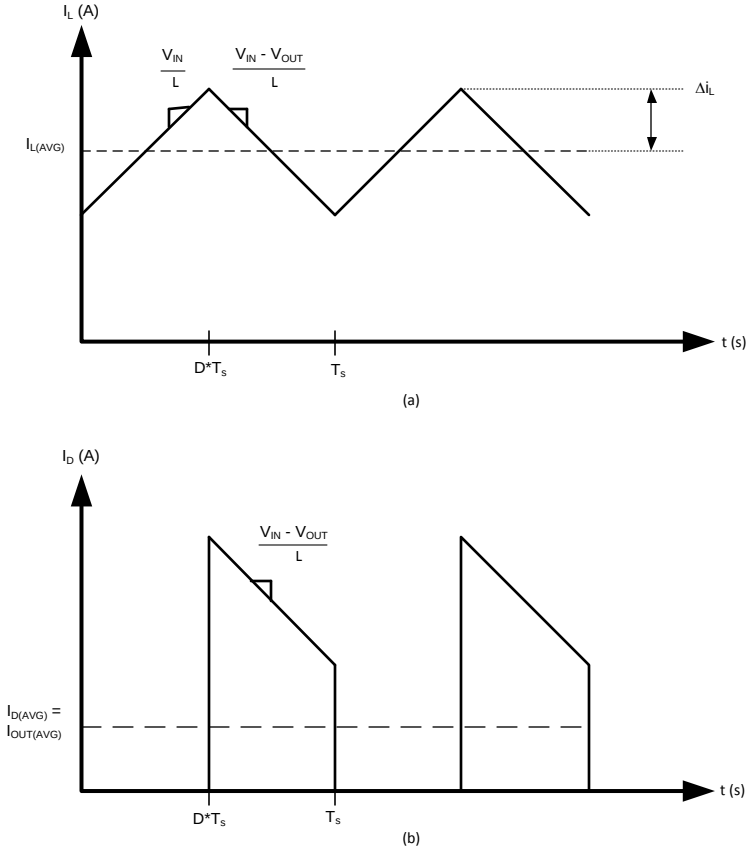


Figure 13. (a) Inductor Current (b) Diode Current

$$V_L(t) = L \frac{di_L(t)}{dt} \quad (1)$$

If $V_{L(t)}$ is constant, di_L / dt must be constant, thus the current in the inductor changes at a constant rate. This is the case in DC/DC converters since the voltages at the input and output can be approximated as a constant. The current through the inductor of the LM2698 boost converter is shown in Figure 13(a). The important quantities in determining a proper inductance value are $I_{L(AVG)}$ (the average inductor current) and Δi_L (the inductor current ripple). If Δi_L is larger than $I_{L(AVG)}$, the inductor current drops to zero for a portion of the cycle and the converter operates in discontinuous conduction mode. If Δi_L is smaller than $I_{L(AVG)}$, the inductor current stays above zero and the converter operates in continuous conduction mode (CCM). All the analysis in this datasheet assumes operation in continuous conduction mode. To operate in CCM, use Equation 2, Equation 3, and Equation 4.

$$I_{L(AVG)} > \Delta i_L \quad (2)$$

$$\frac{I_{OUT(AVG)}}{1-D} > \frac{V_{IN} \times D}{2 \times f_S \times L} \quad (3)$$

$$L > \frac{V_{IN} \times D \times (1-D)}{2 \times f_S \times I_{OUT(AVG)}} \quad (4)$$

Choose the minimum I_{OUT} to determine the minimum L for CCM operation. A common choice is to set Δi_L to 30% of $I_{L(AVG)}$.

The inductance value also affects the stability of the converter. Because the LM2698 utilizes current mode control, the inductor value must be carefully chosen. See *Compensation* for recommended inductance values.

Feature Description (continued)

Choosing an appropriate core size for the inductor involves calculating the average and peak currents expected through the inductor. In a boost converter, use Equation 5 and Equation 6 (where Equation 7 calculates Δi_L).

$$I_{L(AVG)} = \frac{I_{OUT(AVG)}}{1-D}$$

, (5)

$$I_{L(Peak)} = I_{L(AVG)} + \Delta i_L \quad (6)$$

$$\Delta i_L = \frac{DV_{IN}}{2Lf_s} \quad (7)$$

A core size with ratings higher than these values must be chosen. If the core is not properly rated, saturation dramatically reduces overall efficiency.

7.3.2 Current Limit

The current limit in the LM2698 is referenced to the peak switch current. The peak currents in the switch of a boost converter is always higher than the average current supplied to the load. To determine the maximum average output current that the LM2698 can supply, use Equation 8.

$$I_{OUT(MAX)} = (I_{CL} - \Delta i_L) \times (1 - D) = (I_{CL} - \Delta i_L) \times V_{IN} / V_{OUT} \quad (8)$$

where

- I_{CL} is the switch current limit (see *Electrical Characteristics*)

Hence, as V_{IN} increases, the maximum current that can be supplied to the load increases, as shown in Figure 14.

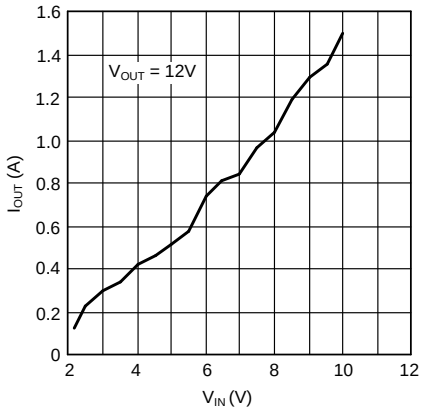


Figure 14. Maximum Output Current vs Input Voltage

7.3.3 Diode

The diode in a boost converter such as the LM2698 acts as a switch to the output. During the first cycle, when the transistor is closed, the diode is reverse biased and current is blocked; the load current is supplied by the output capacitor. In the second cycle, the transistor is open and the diode is forward biased; the load current is supplied by the inductor.

Observation of the boost converter circuit shows that the average current through the diode is the average load current, and the peak current through the diode is the peak current through the inductor. The diode must be rated to handle more than its peak current. To improve efficiency, a low forward drop Schottky diode is recommended.

7.3.4 Input Capacitor

Due to the presence of an inductor at the input of a boost converter, the input current waveform is continuous and triangular. The inductor ensures that the input capacitor sees fairly low ripple currents. However, as the inductor gets smaller, the input ripple increases. The rms current in the input capacitor is given by Equation 9.

Feature Description (continued)

$$I_{CIN(RMS)} = \Delta i_L/\sqrt{3} = \frac{1}{2\sqrt{3}}\left(\frac{V_{in}V_o - V_{in}^2}{f_s L V_o}\right) \quad (9)$$

The input capacitor must be capable of handling the rms current. Although the input capacitor is not so critical in boost applications, a 10 µF or higher value, good quality capacitor prevents any impedance interactions with the input supply.

A 0.1-µF or 1-µF ceramic bypass capacitor is also recommended on the V_{IN} pin (pin 6) of the IC. This capacitor must be connected very close to pin 6 to effectively filter high frequency noise. When operating at 1.25-MHz switching frequency, a minimum bypass capacitance of 0.22 µF is recommended.

7.3.5 Output Capacitor

The output capacitor in a boost converter provides all the output current when the switch is closed and the inductor is charging. As a result, it sees very large ripple currents. The output capacitor must be capable of handling the maximum RMS current. The RMS current in the output capacitor is calculated with Equation 10 (where Equation 11 calculates Δi_L).

$$I_{COUT(RMS)} = \sqrt{(1-D)\left[I_{OUT}^2\frac{D}{(1-D)^2} + \frac{\Delta i_L^2}{3}\right]}$$

where

- $D = (V_{OUT} - V_{IN}) / V_{OUT}$ (10)

$$\Delta i_L = \frac{DV_{IN}}{2Lf_s} \quad (11)$$

The ESR and ESL of the output capacitor directly control the output ripple. Use capacitors with low ESR and ESL at the output for high efficiency and low ripple voltage. Surface mount tantalums, surface mount polymer electrolytic, and polymer tantalum, Sanyo OS-CON, or multi-layer ceramic capacitors are recommended at the output.

7.4 Device Functional Modes

7.4.1 Continuous Conduction Mode

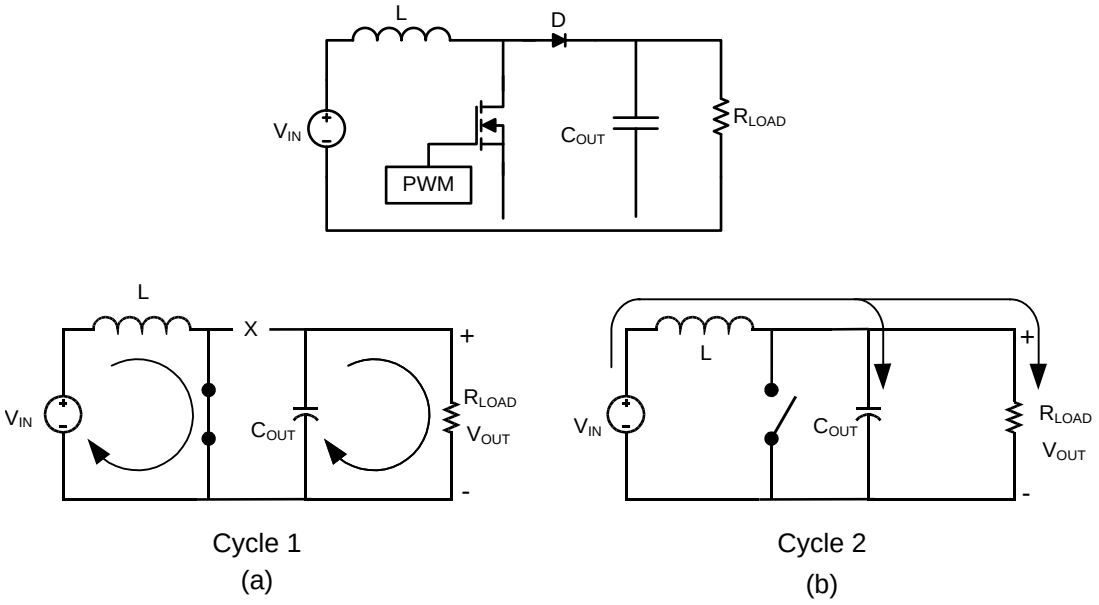


Figure 15. Simplified Boost Converter Diagram
(a) First Cycle of Operation (b) Second Cycle Of Operation

Device Functional Modes (continued)

The LM2698 is a current-mode, PWM boost regulator. A boost regulator steps the input voltage up to a higher output voltage. In continuous conduction mode (when the inductor current never reaches zero at steady state), the boost regulator operates in two cycles.

In the first cycle of operation, shown in Figure 15 (a), the transistor is closed and the diode is reverse biased. Energy is collected in the inductor and the load current is supplied by C_{OUT}.

The second cycle is shown in Figure 15 (b). During this cycle, the transistor is open and the diode is forward biased. The energy stored in the inductor is transferred to the load and output capacitor.

The ratio of these two cycles determines the output voltage. The output voltage is defined with Equation 12.

$$V_{OUT} = \frac{V_{IN}}{1-D} \quad (12)$$

where

- D is the duty cycle of the switch

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The following sections detail typical applications for this device with Boost and SEPIC converters. The SEPIC converter allows step-up and step-down operation and provides a decoupling of the input voltage to the output voltage through the central capacitor which can help protect the input or output in case of faults. The WEBENCH® Design Tool may be used to generate a complete design. This tool utilizes an iterative design procedure and has access to a comprehensive database of components. This allows the tool to create an optimized design and allows the user to experiment with various design options.

8.2 Typical Applications

8.2.1 1.25-MHz Boost Converter

Figure 16 shows the LM2698 boosting 3.3 V to 10 V at 300 mA.

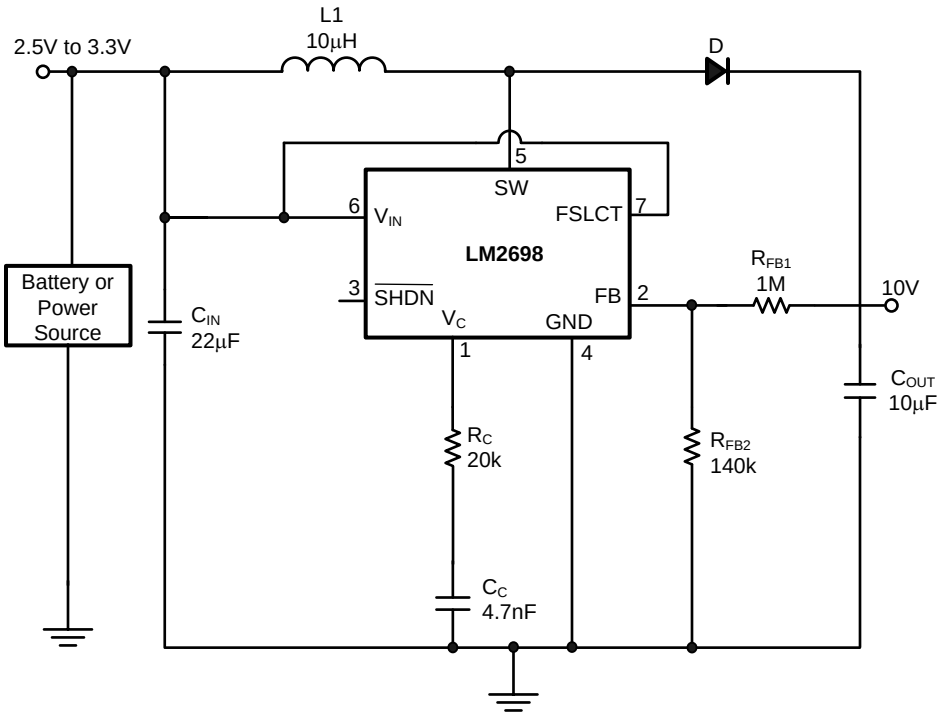


Figure 16. 3.3-V to 10-V Boost Converter

8.2.1.1 Design Requirements

The minimum input voltage for this application is 2.5 V. Absolute Maximum switch node voltage is 18 V which limits the maximum output voltage to less than 17 V. For high output voltage applications (>12 V) proper layout is critical to avoid excessive voltage ringing of the switch node and subsequent damage to the part each time the internal switch turns OFF. In general, proper layout is critical for the efficient operation of the converter. The maximum voltage for VIN is 12 V. If the input of the converter exceeds 12 V, VIN must be connected to another rail or to the input through a linear regulator or similar circuit. *Level-Shifted SEPIC* shows such an example of a step-down voltage circuit for the VIN pin.

Typical Applications (continued)

8.2.1.2 Detailed Design Procedure

As discussed in *Compensation*, the $R_{DS(ON)}$ of the internal FET in the LM2698 raises as the input voltage drops below 5 V (see *Typical Characteristics*). The minimum input voltage for this application is 2.5 V, at which point the $R_{DS(ON)}$ is approximately 200 mΩ. Substituting these values in for Equation 13, it is found that either a 10 µH (1.25-MHz operation) or a 22 µH (600-kHz operation) is necessary for a stable design. The circuit is operated at 1.25 MHz to allow for a smaller inductance. From the *Quick Compensator Design* equations, R_C is calculated as 18.6 kΩ, and a 20-kΩ resistor is used.

8.2.1.2.1 Compensation

This section presents a step-by-step procedure to design the compensation network at pin 1 (V_C) of the LM2698. These design methods produce a conservative and stable control loop.

There is a minimum inductance requirement in any current mode converter. This is a function of V_{OUT}, duty cycle, and switching frequency, among other things. Figure 18 plots the recommended inductance range vs duty cycle for V_{OUT} = 12 V. The two lines represent the upper and lower bounds of the recommended inductance range. The simplified compensation procedure that follows assumes that the inductance never drops below the Q = 5 line. Figure 18 is plotted with Equation 13.

$$L = \frac{V_{OUT} \times R_{DSON}}{Se}\left(\frac{1}{\pi Q} + D - 0.5\right) \quad (13)$$

where

- R_{DSON} = 0.15
- Se = 0.072 × f_S
- Q = 0.5 and 5

Use Q = 5 to calculate the minimum inductance recommended for a stable design. Choosing an inductor between the Q = 0.5 and Q = 5 values provides a good tradeoff between size and stability. Note that as V_{IN} drops less than 5 V, $R_{DS(ON)}$ increases, as shown in Figure 8. The worst case $R_{DS(ON)}$ must be used when choosing the inductance. To view plots for different Vout, multiply the Y axis by a factor of V_{OUT} / 12, or plot Equation 13 for the respective output voltage.

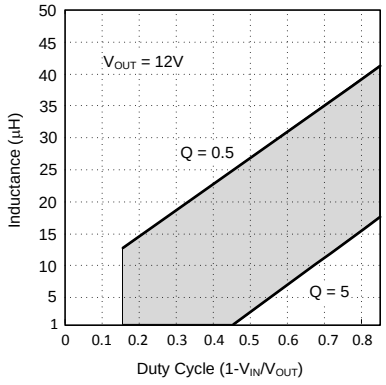


Figure 17. Minimum Inductance Requirements for (a) f_S = 600 kHz

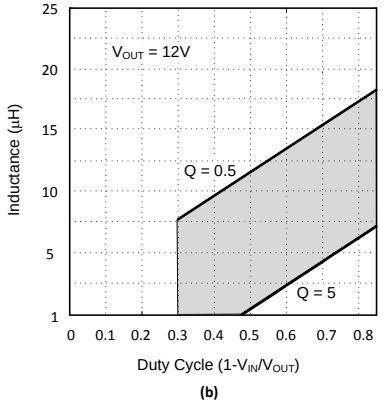


Figure 18. Minimum Inductance Requirements for (b) f_S = 1.25 MHz

The goal of the compensation network is to provide the best static and dynamic performance while insuring stability over line and load variations. The relationship of stability and performance can be best analyzed by plotting the magnitude and phase of the open loop frequency response in the form of a bode plot. A typical bode plot of the LM2698 open loop frequency response is shown in Figure 19.

Typical Applications (continued)

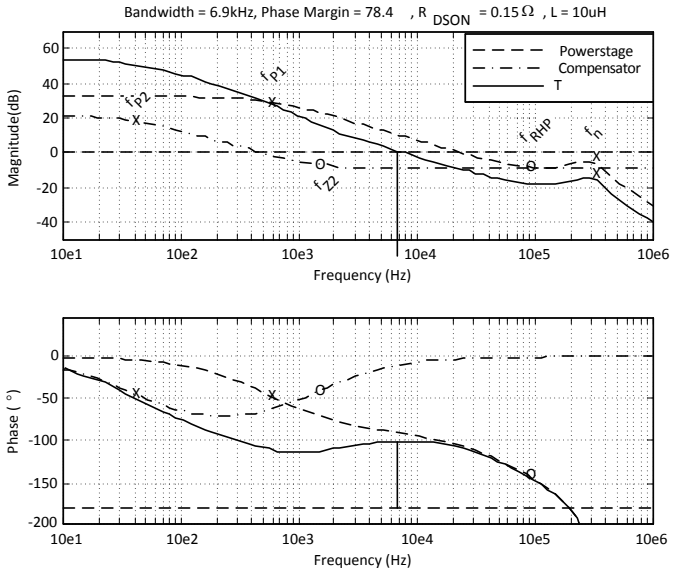


Figure 19. Bode Plot of the LM2698 Frequency Response Using the Typical Application Circuit

Poles are marked with an *X*, and zeros are marked with a *O*. The bolded O labeled f_{RHP} is a right-half plane zero. Right half plane zeros act like normal zeros to the magnitude (20 dB / decade slope influence) and like poles to the phase (–90° shift). Three curves are shown. The powerstage curve is the frequency response of the powerstage, which includes the switch, diode, inductor, output capacitor, and load. The compensator curve is the frequency response of the compensator, which is the error amp combined with the compensation network. T is the product of the powerstage and the compensator and is the complete open loop frequency response. The power stage response is fixed by line and load constraints, while the compensator is set by the external compensation network at pin 1. The compensator can be designed in a few simple steps as follows.

Typical Applications (continued)

8.2.1.2.1.1 Quick Compensator Design

Calculate the quick compensator design using Equation 14 through Equation 19 (where Equation 15 calculates $R_{LOAD(MIN)}$ and Equation 20 calculates A_{DC}).

$$\omega_{PI(MAX)} \approx \frac{1}{C_{OUT} R_{LOAD(MIN)}} \text{ (rad/s)} \tag{14}$$

$$R_{LOAD(MIN)} = \frac{V_{OUT}}{I_{OUT(MAX)}} \tag{15}$$

$$\omega_{RHP(MIN)} = \frac{R_{LOAD(MIN)} \left(\frac{V_{IN(MIN)}}{V_{OUT}} \right)^2}{L} \text{ (rad/s)} \tag{16}$$

$$\text{Set } \omega_{P2} = 2\pi(40)\text{(rad/s)} \approx \frac{1}{C_{C1} R_{OUT}} \text{ (rad/s)}$$

where

- R_{OUT} = 875 kΩ (17)

Choose C_{C1} = 4.7 nF

$$\omega_{z2} = 10 \text{ x } \omega_{P1(max)} \frac{A_{DC} \omega_{P2}}{\omega_{RHP(MIN)}} = \frac{1}{C_{C1} R_C} \text{ (rad/s),} \tag{18}$$

$$R_C = \frac{\omega_{RHP(MIN)}}{10 \text{ x } A_{DC} C_{C1} \omega_{P1(max)} \omega_{P2}} \Omega \tag{19}$$

$$A_{DC} = \frac{118 * R_{LOAD(MIN)}}{R_{DSON(MIN)}} \text{ x } \frac{(1 - D_{MAX})}{\frac{(1 - D_{MAX})^3 R_{LOAD(MIN)}}{2Lf_S} \left(1 + \frac{0.144 * f_S L}{V_{IN} R_{DSON(MIN)}} \right) + 1 + D_{MAX}} \tag{20}$$

If the output capacitor is of high ESR (0.1 Ω or higher), it may be necessary to use C_{C2}. A rule of thumb is that if $1 / (2\pi C_{OUT} ESR)$ (Hz) is lower than $f_S / 2$ (Hz), C_{C2} must be used. Choose C_{C2} with Equation 21.

$$(R_C + R_{OUT})(C_{OUT} \times ESR) / (R_C \times R_{OUT})(F)$$

where

- R_{OUT} = output impedance of the error amp (875 kΩ) (21)

8.2.1.2.1.2 Improving Transient Response Time

The above compensator design provides a loop gain with high phase margin for a large stability margin. The transient response time of this loop is limited by the lower mid-frequency gain necessary to achieve a high phase margin. If it is desired to increase the transient response time, C_{C1} may be decreased. Decreasing C_{C1} by 2x, 4x, and 6x yields increasingly shorter transient response times, however the loop phase margin becomes progressively lower as C_{C1} is decreased. When optimizing the loop gain for transient response time, it is recommended to keep the phase margin above 40°.

8.2.1.2.1.3 Additional Comments on the Open Loop Frequency Response

The procedure used here to pick the compensation network provides a good starting point. In most cases, these values is sufficient for a stable design. It is always recommended to check the design in a real test setup. This is easy to do with the aid of a dynamic load. Set the high and low load values to your system requirements and switch between the two at about 1kHz. View the output voltage with an oscilloscope using AC coupling, and zoom in enough to see the waveform react to the load change. Use Table 1 to determine if your design is stable. Remember to use worst case conditions ($V_{IN(MIN)}$, $R_{OUT(MIN)}$, $R_{OUT(MAX)}$).

Typical Applications (continued)

Table 1. Compensation Troubleshooting Chart

RESPONSE	CONCLUSION	WHAT TO CHANGE
Underdamped, weak attenuation	Nearing instability	Make C_{C1} larger
Underdamped, strong attenuation	Stable	Nothing
Critically damped	Stable	Nothing
Overdamped	Stable	Nothing

8.2.1.3 Application Curves

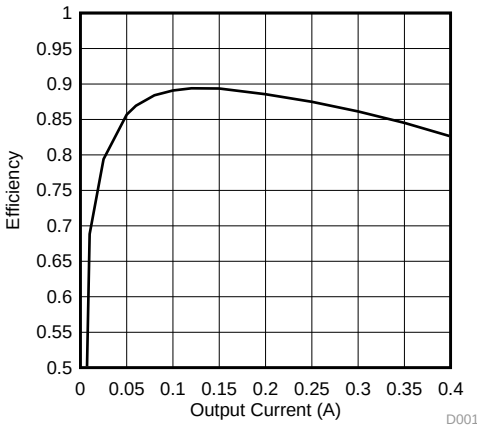


Figure 20. Efficiency Vin = 3.3 V, Vout = 10 V (With Sumida CDRH6D38-100 Inductor)

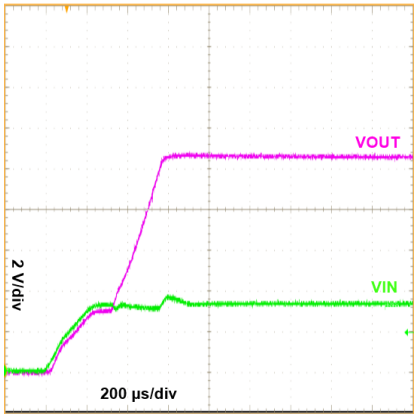


Figure 21. Start-up Waveform

8.2.2 3.3-V SEPIC

The LM2698 can be used to implement a SEPIC technology. The advantages of the SEPIC topology are that it can step up or step down an input voltage, and it has low input current ripple.

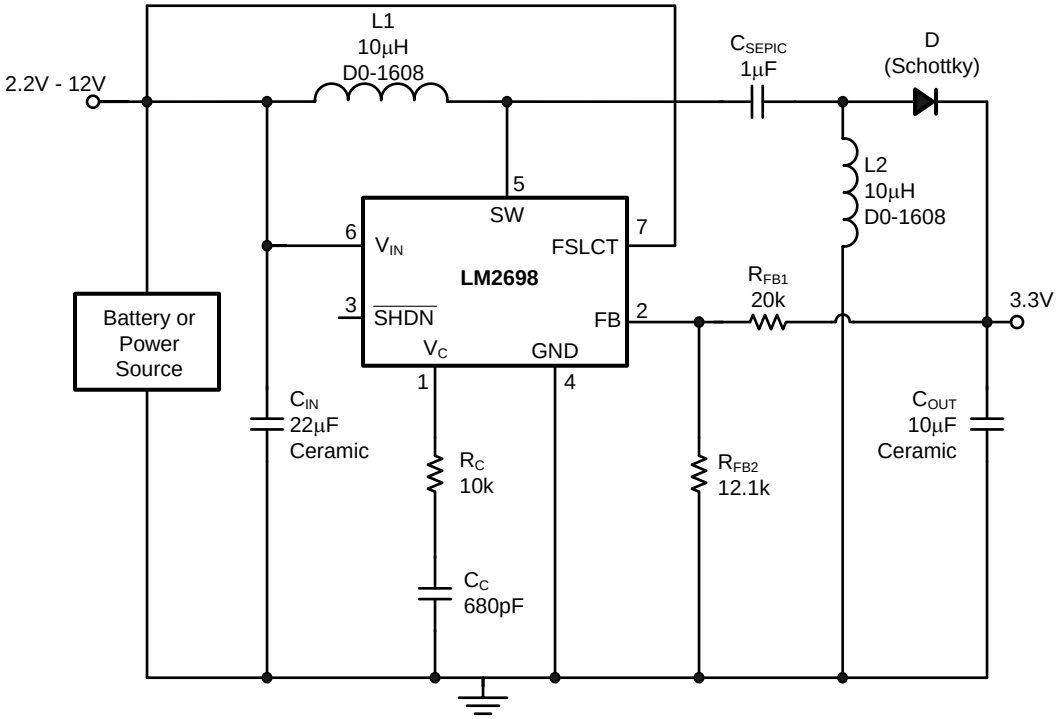


Figure 22. 3.3-V SEPIC Converter

8.2.2.1 Design Requirements

The input voltage, output voltages, and load currents are necessary to properly design the SEPIC converter. The maximum current that the converter can deliver depends on the internal peak current limit set by the LM2698 and the choice of inductor and switching frequency. See details of the design procedure in the next section. Do not exceed absolute maximum ratings for the pin. The switch node voltage swings between 0 V and VIN+Vout+Vfd, where Vfd is the forward voltage of the diode. In addition to this voltage, the ringing at the switch node could increase the voltage stress on the SW pin and lead to a violation of the absolute maximum voltage on that pin.

8.2.2.2 Detailed Design Procedure

The conversion ratio for the SEPIC is Equation 22.

$$\frac{V_{OUT}}{V_{IN}} = \frac{D}{D'}$$

where

- $D' = 1 - D$ (22)

Solving for D yields Equation 23.

$$D = \frac{1}{1 + V_{IN} / V_{OUT}} \quad (23)$$

To avoid subharmonic oscillations, it is recommended that inductors L1 and L2 be the same inductance. Currents conducted by the inductors are:

$I_1 = I_{OUT}(V_{OUT} / V_{IN})$

$\Delta i_1 = V_{IN} D / (2 \times L1 \times fs)$

$I_2 = I_{OUT}$

$\Delta i_1 = V_{IN}D / (2 \times L2 \times fs)$

The switch sees a maximum current of $I_1 + I_2 + \Delta i_1 + \Delta i_2$. If L1 = L2 = L, the maximum switch current is given by Equation 24.

$$I_{OUT}(1 + V_{OUT} / V_{IN}) + V_{IN}D / (L \times fs) \quad (24)$$

The maximum load current is limited by this relationship to the switch current.

The polarity of C_{SEPIC} changes between each cycle, so a ceramic capacitor must be used here. A high-quality, low-ESR capacitor directly improves efficiency because all load currents pass through C_{SEPIC}.

C_{IN} must be chosen using the same relationship as in the boost converter. C_{IN} must be able to provide the necessary RMS current.

8.2.2.3 Application Curve

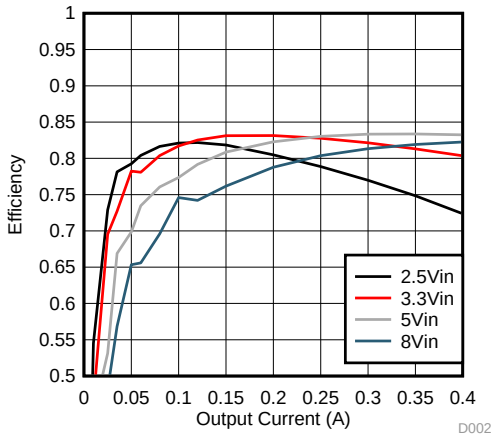


Figure 23. Efficiency

8.2.3 Level-Shifted SEPIC

The circuit shown in Figure 24 is similar to the SEPIC shown in Figure 22, except that it is level shifted to provide a negative output voltage. This is achieved by connecting the ground of the LM2698 to the output.

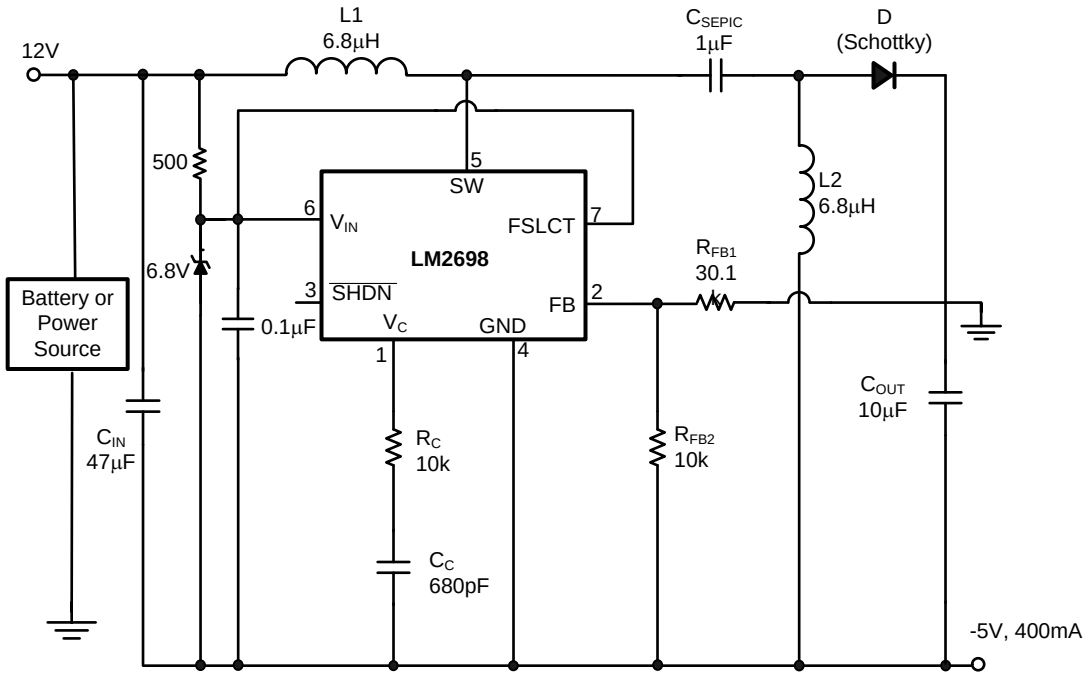


Figure 24. Level-Shifted SEPIC Converter

8.2.3.1 Design Requirements

The circuit analysis for the level-shifted SEPIC is the same as the SEPIC. The voltage at the input of the LM2698 must be clamped if the absolute value of the output voltage plus the input voltage exceeds 12 V, the absolute maximum rating for the V_{IN} pin. The simplest way to do this is with a Zener diode, as shown in Figure 24. Likewise, if the FSLCT pin is pulled high to operate at 1.25 MHz, its voltage must not exceed 12 V. To prevent any high frequency noise from entering the LM2698's internal circuitry, a high-frequency bypass capacitor must be placed as close to pin 6 as possible. A good choice for this capacitor is a 0.1-µF ceramic capacitor.

9 Power Supply Recommendations

The output power of the LM2698 is limited by its maximum power dissipation. The maximum power dissipation is determined by Equation 25.

$$P_D = (T_{jmax} - T_A) / R_{\theta JA} \quad (25)$$

where

- T_{jmax} is the maximum specified junction temperature (125°C)
- T_A is the ambient temperature
- $R_{\theta JA}$ is the thermal resistance of the package

$R_{\theta JA}$ is dependant on the layout of the board as shown in *Layout Examples*.

10 Layout

10.1 Layout Guidelines

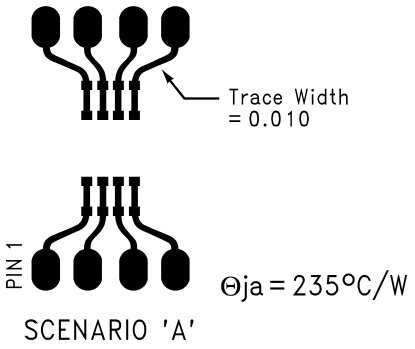
The GND pin and the NC pin is recommended to be connected by a short trace as shown in *Layout Examples*.

Table 2 shows the thermal resistance using different scenarios.

Table 2. Thermal Resistance

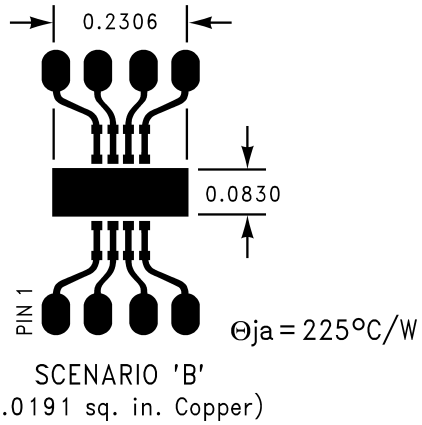
PARAMETER			TYP	UNIT
θ_{JA}	Thermal Resistance	Junction to Ambient Figure 25	235	°C/W
		Junction to Ambient Figure 26	225	°C/W
		Junction to Ambient Figure 27	220	°C/W
		Junction to Ambient Figure 28	200	°C/W
		Junction to Ambient Figure 29	195	°C/W

10.2 Layout Examples



Junction to ambient thermal resistance (no external heat sink) for the MSO8 package with minimal trace widths (0.010 inches) from the pins to the circuit.

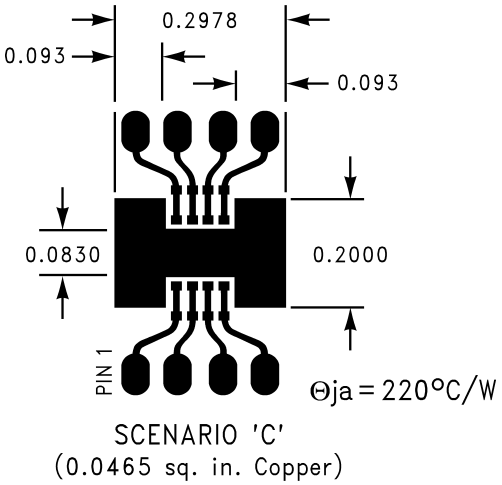
Figure 25. Pad Layout Scenario 'A'



Junction to ambient thermal resistance for the MSO8 package with minimal trace widths (0.010 inches) from the pins to the circuit and approximately 0.0191 sq. in. of copper heat sinking.

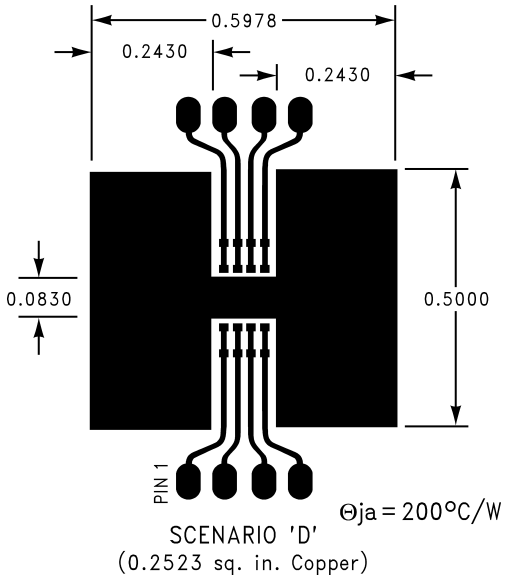
Figure 26. Pad Layout Scenario 'B'

Layout Examples (continued)



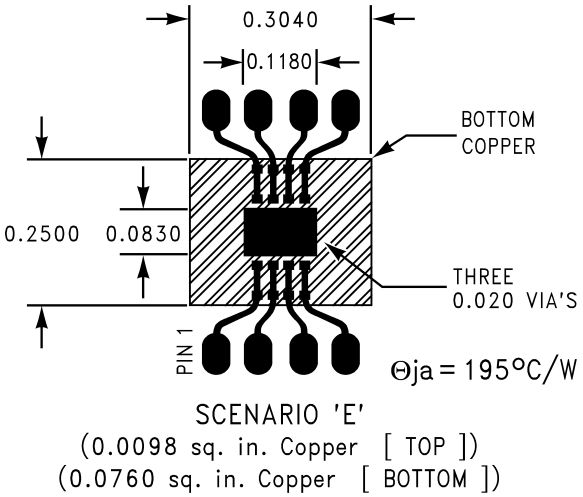
Junction to ambient thermal resistance for the MSO8 package with minimal trace widths (0.010 inches) from the pins to the circuit and approximately 0.0465 sq. in. of copper heat sinking.

Figure 27. Pad Layout Scenario 'C'



Junction to ambient thermal resistance for the MSO8 package with minimal trace widths (0.010 inches) from the pins to the circuit and approximately 0.2523 sq. in. of copper heat sinking.

Figure 28. Pad Layout Scenario 'D'



Junction to ambient thermal resistance for the MSO8 package with minimal trace widths (0.010 inches) from the pins to the circuit and approximately 0.0098 sq. in. of copper heat sinking on the top layer and 0.0760 sq. in. of copper heat sinking on the bottom layer, with three 0.020 in. vias connecting the planes.

Figure 29. Pad Layout Scenario 'E'

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
SIMPLE SWITCHER is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2698MM-ADJ/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	S22B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

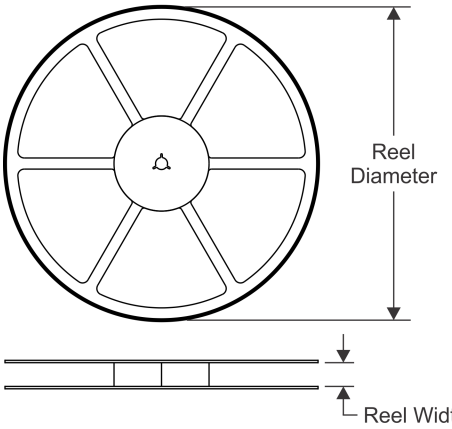
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

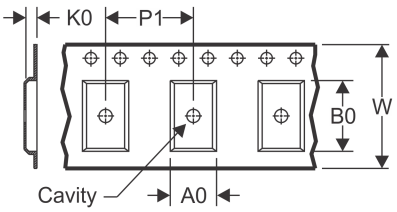
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

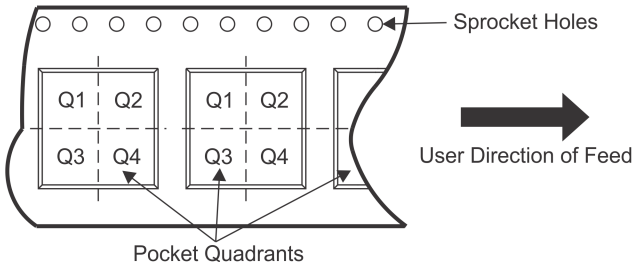


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

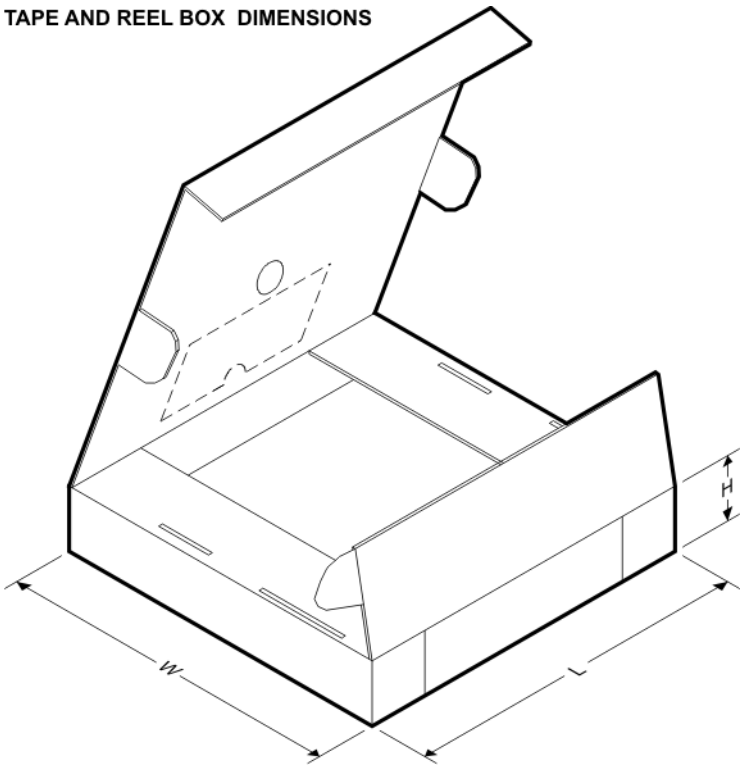
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2698MM-ADJ/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

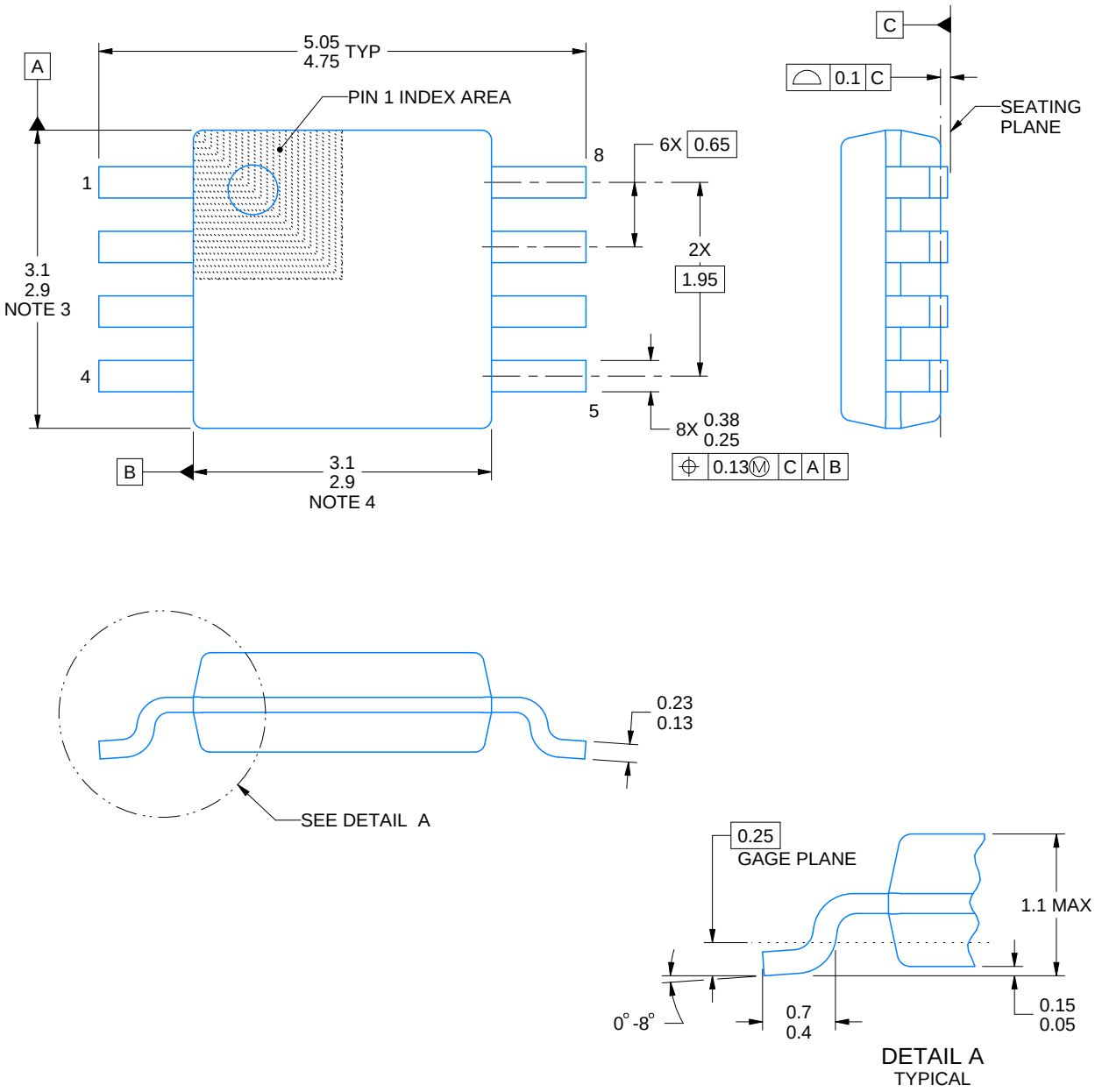
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2698MM-ADJ/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

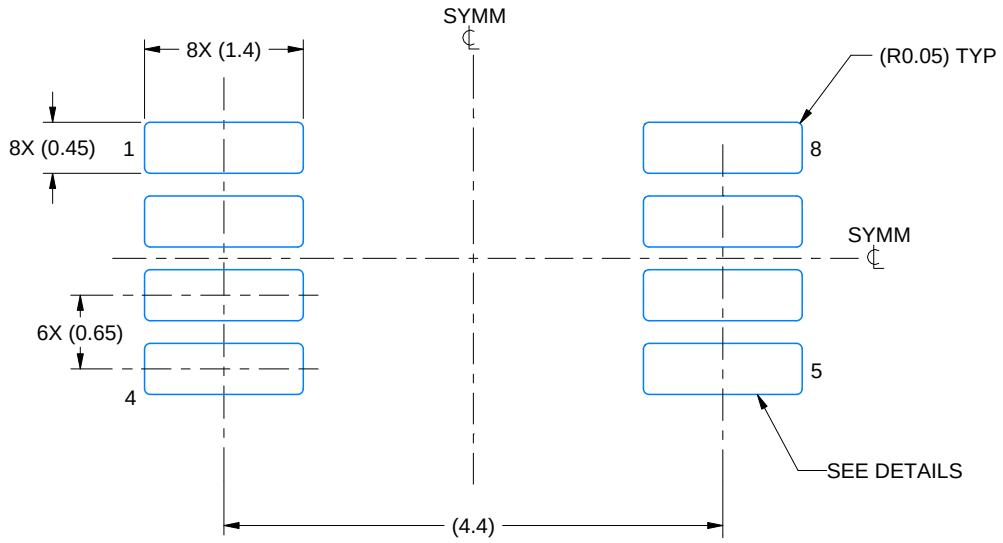
SMALL OUTLINE PACKAGE



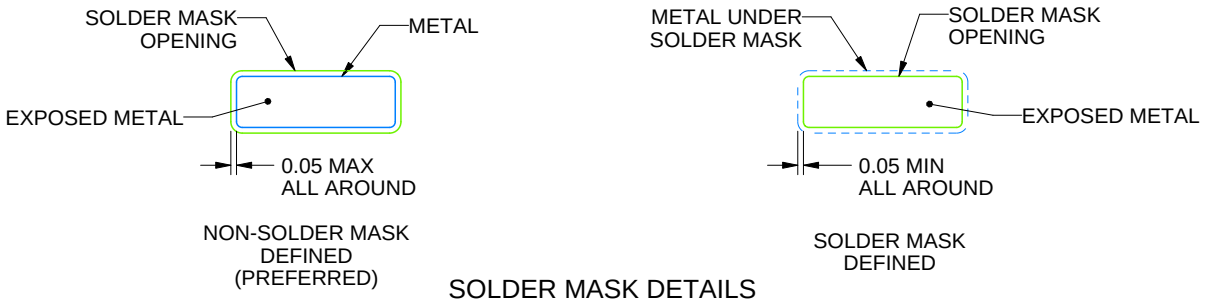
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

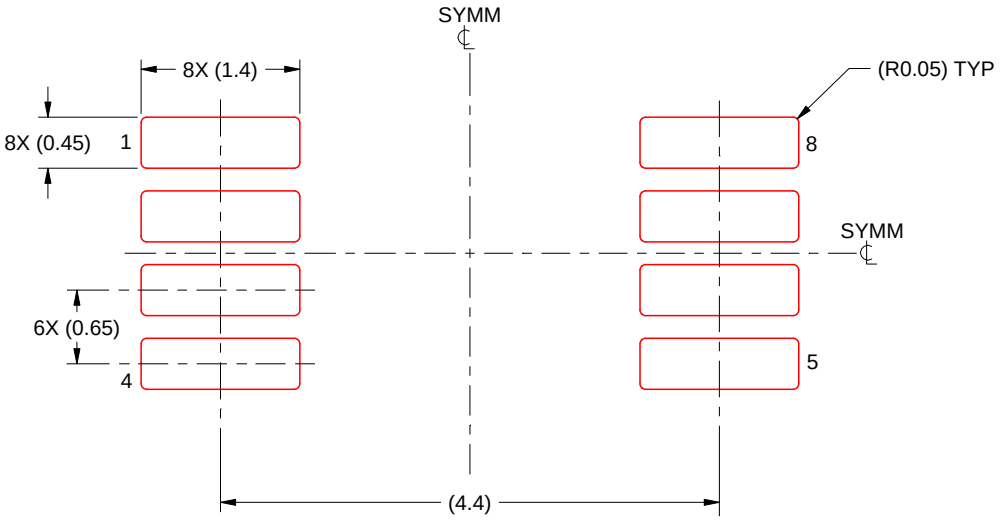


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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