LM2755 Charge Pump LED Controller with I²C-Compatible Interface in DSBGA Package

Check for Samples: LM2755

FEATURES

- **90% Peak Efficiency**
- **Total solution size < 13mm²**
- **No Inductor Required: Only 4 Inexpensive Ceramic Caps**
- **3 Independently Controlled Constant Current Outputs**
- **Programmable Trapezoidal Dimming Waveform on Each Output**
- **Programmable Timing Control Via Internal Registers and External Clock Synchronization Input**
- **32 Exponential Dimming Steps with 800:1 Dimming Ratio**
- **Programmable Brightness Control via I²C-Compatible Interface**
- **Hardware Enable Pin**
- **Wide Input Voltage Range: 2.7V to 5.5V**
- **Tiny 18-bump Thin DSBGA : 1.8mm x 1.6mm x 0.6mm**

APPLICATIONS

- **Indicator LEDs**
- **Keypad LED Backlight**
- **Display LED Backlight**
- **Fun-light LEDs**

DESCRIPTION

The LM2755 is a charge-pump-based, constant current LED driver capable of driving 3 LEDs with a total output current up to 90mA. The diode current waveforms of each LED can be trapezoidal with timing and level parameters (rise time, fall time, high level, low level, delay, high time, low time) programmed via an I²C-compatible interface. The 32 brightness levels found on the LM2755 are exponentially spaced (as opposed to linearly spaced) to better match the response of the human eye to changing brightness levels.

The device requires only four small and low-cost ceramic capacitors. The LM2755 provides excellent efficiency without the use of an inductor by operating the charge pump in a gain of 3/2 or in a gain of 1. Maximum efficiency is achieved over the input voltage range by actively selecting the proper gain based on the LED forward voltage requirements.

The pre-regulation scheme used by the LM2755 is optimized to ensure low conducted noise on the input. An internal soft-start circuitry eliminates high inrush current at start-up. The LM2755 consumes 3µA (typ.) of supply current in shut-down.

The LM2755 is available in Texas Instruments' tiny 18-bump thin DSBGA package.

TYPICAL APPLICATION CIRCUIT

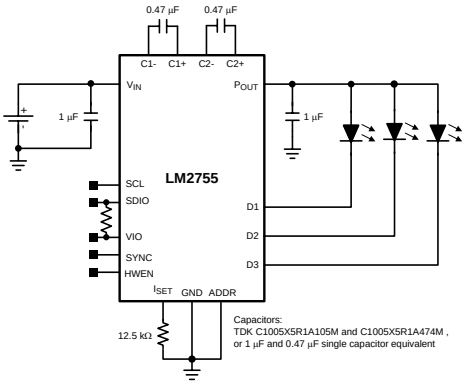


Figure 1. Typical Application Circuit

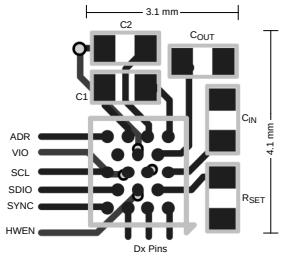


Figure 2. Minimum Solution Size

Connection Diagram

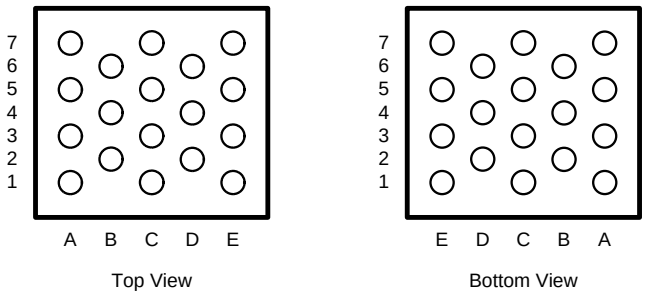


Figure 3. 18-Bump Thin DSBGA Package
1.615mm × 1.807mm × 0.6mm
(See Package Number YFQ0018AAA)

PIN DESCRIPTIONS

Pin #s	Pin Names	Pin Descriptions
A1	ID1	LED Driver 1
A3	ID2	LED Driver 2
A5	ID3	LED Driver 3
A7	SYNC	External clock synchronization input
B2	ISET	LED Driver Current Set Pin
B4	HWEN	Hardware EN Pin. Low '0' = RESET, High '1' = Normal Operation
B6	SDIO	Serial data Input/Output pin
C1	V_{IN}	Input Voltage Connection
C3	GND	Ground Connection.
C5	VIO	Serial Bus Voltage Level Input
C7	SCL	Serial Clock Pin
D2	P_{OUT}	Charge Pump Output
D4	C2-	Flying Capacitor Connect
D6	GND	Ground connection
E1	C1+	Flying Capacitor Connect
E3	C2+	Flying Capacitor Connect
E5	C1-	Flying Capacitor Connect
E7	ADDR	Chip Address Select Input. VIN = 0x67. Ground = 0x18.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS (1)(2)(3)

V_{IN} pin voltage	−0.3V to 6.0V
SCL, SDIO, VIO, ADDR, SYNC pin voltages	−0.3V to (V_{IN}+0.3V) w/ 6.0V max
I_{Dx} Pin Voltages	−0.3V to (V_{POUT}+0.3V) w/ 6.0V max
Continuous Power Dissipation (4)	Internally Limited
Junction Temperature (T_{J-MAX})	150°C
Storage Temperature Range	−65°C to +150°C
Maximum Lead Temperature (Soldering)	(5)
ESD Rating(6) Human Body Model	2.5kV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply verified performance limits. For verified performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 160°C (typ.) and disengages at T_J = 155°C (typ.).
(5) For detailed soldering specifications and information, please refer to STET Application Note 1112: DSBGA Wafer Level Chip Scale Package (AN-1112 SNVA009).
(6) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. (MIL-STD-883 3015.7)

OPERATING RATINGS (1)(2)

Input Voltage Range	2.7V to 5.5V
Junction Temperature (T_J) Range	−30°C to 105°C
Ambient Temperature (T_A) Range(3)	−30°C to +85°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply verified performance limits. For verified performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 105°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.

THERMAL PROPERTIES

Junction-to-Ambient Thermal Resistance (θ_{JA}), YFQ0018 Package (1)	56°C/W

(1) Junction-to-ambient thermal resistance is highly dependent on application and board layout. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. For more information, please refer to Texas Instruments STET Application Note 1112: DSBGA Wafer Level Chip Scale Package (AN-1112 SNVA009).

ELECTRICAL CHARACTERISTICS (1)(2)

Limits in standard typeface are for T_J = 25°C, and limits in boldface type apply over the full operating temperature range. Unless otherwise specified: V_{IN} = 3.6V; V_{D1} = 0.4V; V_{D2} = 0.4V; V_{D3} = 0.4V; R_{SET} = 12.5kΩ; D1, D2, and D3 = Fullscale Current; EN1, EN2, and EN3 Bits = "1"; CLK bit = '0'; C1 = C2 = 0.47µF, C_{IN} = C_{OUT} = 1µF; Specifications related to output current(s) and current setting pins (I_{Dx} and I_{SET}) apply to D1, D2 and D3. (3)

Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{Dx}	Output Current Regulation	3.0V ≤ V_{IN} ≤ 5.5V		**18.7**	20.7	**22.7**	mA
I_{MATCH}	Output Current Matching	3.0V ≤ V_{IN} ≤ 5.5V (4)			1		%
I_Q	Quiescent Supply Current	Gain = 3/2 D_{1-3} = OPEN, R_{SET} = OPEN			1.0	**1.3**	mA
I_{SD}	Shutdown Supply Current	3.0V ≤ V_{IN} ≤ 5.5V EN1 = EN2 = EN3 = 0			5	**9.5**	µA
V_{SET}	I_{SET} Pin Voltage	3.0V ≤ V_{IN} ≤ 5.5V			1.25		V
I_{DX} / I_{SET}	Output Current to Current Set Ratio	(5)			200		
V_{DxTH}	V_{Dx} 1x to 3/2x Gain Transition Threshold	V_{D1} and/or V_{D2} and/or V_{D3}Falling			350		mV
V_{HR}	Current Source Headroom Voltage Requirement (6)	I_{Dx} = 95% ×I_{Dx} (nom.) (I_{Dx} (nom) ≈ 20mA) Gain = 3/2			200		mV
f_{SW}	Switching Frequency			**0.975**	1.25	**1.525**	MHz
t_{START}	Start-up Time	P_{OUT} = 90% steady state			300		µs
f_{PWM}	Internal Diode Current PWM Frequency				20		kHz
f_{SYNC}	Maximum External Sync Frequency				1.0		MHz
V_{HWEN}	HWEN Voltage Thresholds	2.7V ≤ V_{IN} ≤ 5.5V	Reset	**0**		**0.5**	V
			Normal Operation	**1.23**		**VIN**	
I^2C-Compatible Interface Voltage Specifications (SCL, SDIO, VIO)							
V_{IO}	Serial Bus Voltage Level	2.7V ≤ V_{IN} ≤ 5.5V (7)		**1.44**		**V_{IN}**	V
V_{IL}	Input Logic Low "0"	2.7V ≤ V_{IN} ≤ 5.5V, VIO = 3.0V		**0**		**0.35 × V_{IO}**	V
V_{IH}	Input Logic High "1"	2.7V ≤ V_{IN} ≤ 5.5V, VIO = 3.0V		**0.65 × V_{IO}**		**V_{IO}**	V
V_{OL}	Output Logic Low "0"	I_{LOAD} = 3mA				**400**	mV
I^2C-Compatible Interface Timing Specifications (SCL, SDIO, VIO) (8)							
t_1	SCL (Clock Period)			**2.5**			µs
t_2	Data In Setup Time to SCL High			**100**			ns
t_3	Data Out stable After SCL Low			**0**			ns
t_4	SDIO Low Setup Time to SCL Low (Start)			**100**			ns

(1) All voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are ensured by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.
(3) C_{IN}, C_{POUT}, C_1, and C_2 : Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.
(4) For the current sinks on a part, the following are determined: the maximum sink current in the group (MAX), the minimum sink current in the group (MIN), and the average sink current of the group (AVG). Two matching numbers are calculated: (MAX-AVG)/AVG and (AVG-MIN)/AVG. The larger number of the two (worst case) is considered the matching figure. The typical specification provided is the most likely norm of the matching figure for all parts
(5) The maximum total output current for the LM2755 should be limited to 90mA. The total output current can be split among any of the three banks (I_{D1} = I_{D2} = I_{D3} = 30mA Max.). Under maximum output current conditions, special attention must be given to input voltage and LED forward voltage to ensure proper current regulation. See MAXIMUM OUTPUT CURRENT, MAXIMUM LED VOLTAGE, MINIMUM INPUT VOLTAGE of the datasheet for more information.
(6) For each I_{Dx} output pin, headroom voltage is the voltage across the internal current sink connected to that pin. For V_{HR} = V_{OUT} -V_{Dxx}. If headroom voltage requirement is not met, LED current regulation will be compromised.
(7) SCL and SDIO signals are referenced to VIO and GND for minimum VIO voltage testing.
(8) SCL and SDIO should be glitch-free in order for proper brightness control to be realized.

ELECTRICAL CHARACTERISTICS [1][2] (continued)

Limits in standard typeface are for T_J = 25°C, and limits in boldface type apply over the full operating temperature range. Unless otherwise specified: V_{IN} = 3.6V; V_{D1} = 0.4V; V_{D2} = 0.4V; V_{D3} = 0.4V; R_{SET} = 12.5kΩ; D1, D2, and D3 = Fullscale Current; EN1, EN2, and EN3 Bits = "1"; CLK bit = '0'; C1 = C2 = 0.47µF, C_{IN} = C_{OUT} = 1µF; Specifications related to output current(s) and current setting pins (I_{Dx} and I_{SET}) apply to D1, D2 and D3. [3]

Symbol	Parameter	Condition	Min	Typ	Max	Units
t_5	SDIO High Hold Time After SCL High (Stop)		**100**			ns

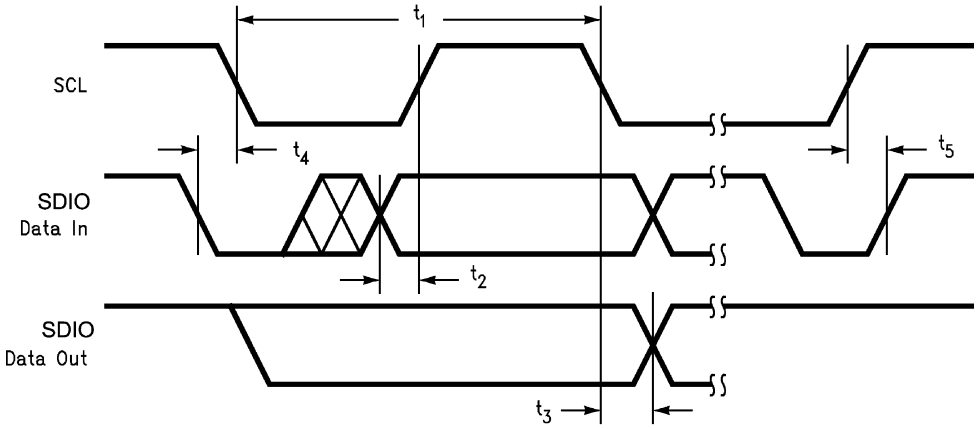


Figure 4. I²C Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified: T_A = 25°C; V_{IN} = 3.6V; V_{HWEN} = V_{IN}; V_{D1} = V_{D2} = V_{D3} = 3.6V; R_{SET} = 12.5kΩ; C_1=C_2= 0.47µF, C_{IN} = C_{VOUT} = 1µF; ENA = ENB = ENC = '1'.

LED Drive Efficiency vs Input Voltage

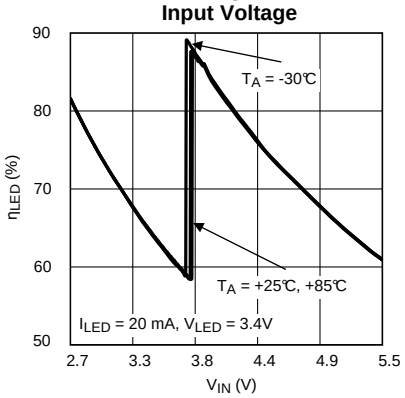


Figure 5.

Diode Current vs Input Voltage

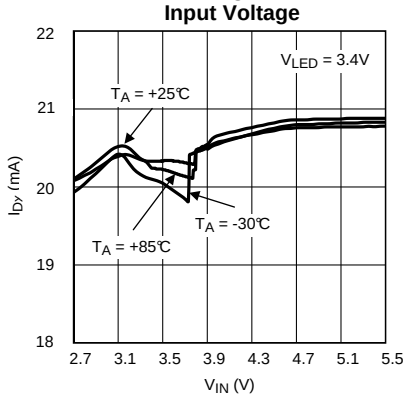


Figure 6.

Current Matching vs Input Voltage 3 LEDs

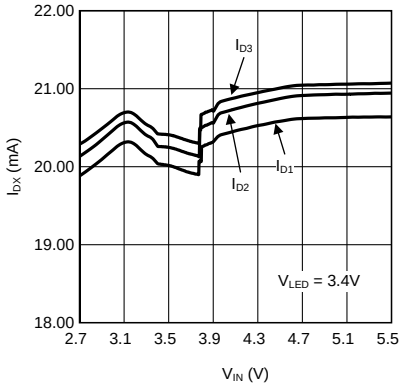


Figure 7.

Diode Current vs Brightness Code

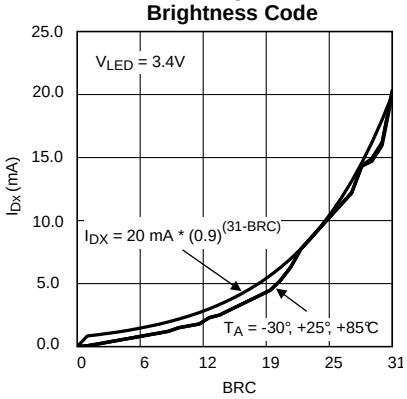


Figure 8.

Quiescent Current vs Input Voltage

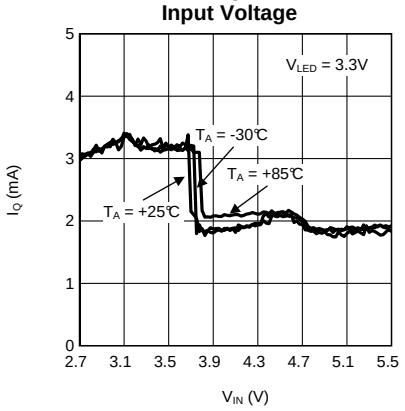


Figure 9.

Shutdown Current vs Input Voltage

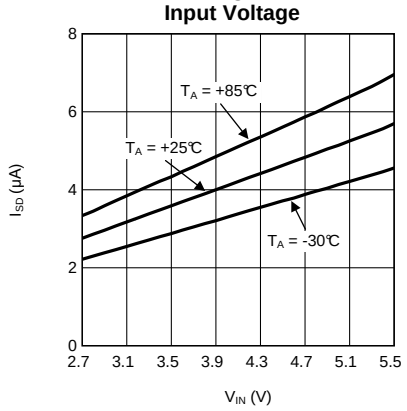
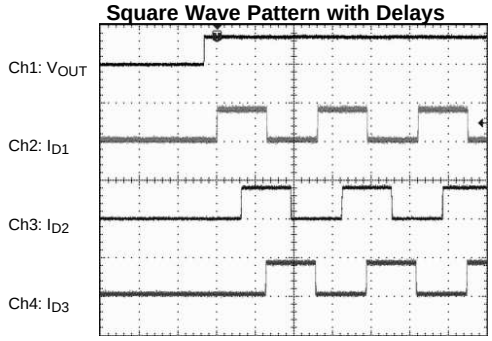


Figure 10.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: T_A = 25°C; V_{IN} = 3.6V; V_{HWEN} = V_{IN}; V_{D1} = V_{D2} = V_{D3} = 3.6V; R_{SET} = 12.5kΩ; C_1=C_2= 0.47µF, C_{IN} = C_{VOUT} = 1µF; ENA = ENB = ENC = '1'.

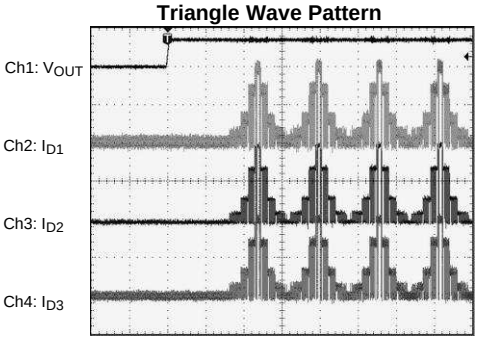
Square Wave Pattern with Delays



Time: 10 msec./div
Ch1: 5V/div Ch2: 10 mA/div
Ch3: 10 mA/div Ch4: 10 mA/div

Figure 11.

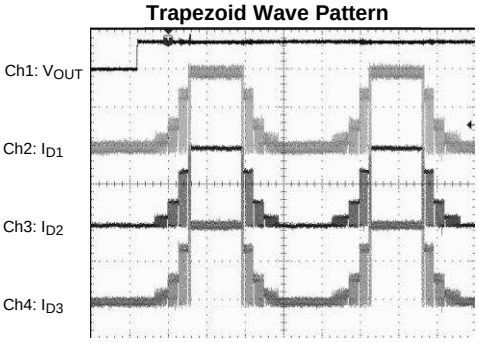
Triangle Wave Pattern



Time: 2 msec./div
Ch1: 5V/div Ch2: 10 mA/div
Ch3: 10 mA/div Ch4: 10 mA/div

Figure 12.

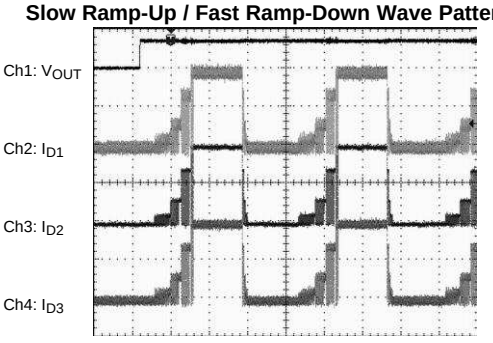
Trapezoid Wave Pattern



Time: 10 msec./div
Ch1: 5V/div Ch2: 10 mA/div
Ch3: 10 mA/div Ch4: 10 mA/div

Figure 13.

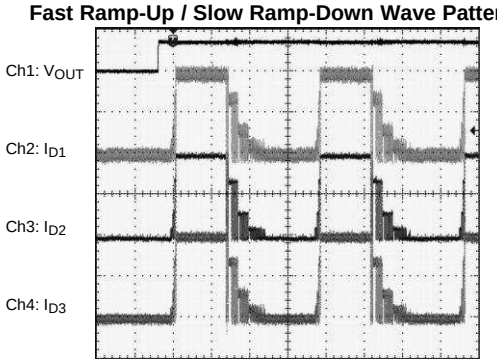
Slow Ramp-Up / Fast Ramp-Down Wave Pattern



Time: 10 msec./div
Ch1: 5V/div Ch2: 10 mA/div
Ch3: 10 mA/div Ch4: 10 mA/div

Figure 14.

Fast Ramp-Up / Slow Ramp-Down Wave Pattern



Ch1: 5V/div Ch2: 10 mA/div
Ch3: 10 mA/div Ch4: 10 mA/div

Figure 15.

BLOCK DIAGRAM

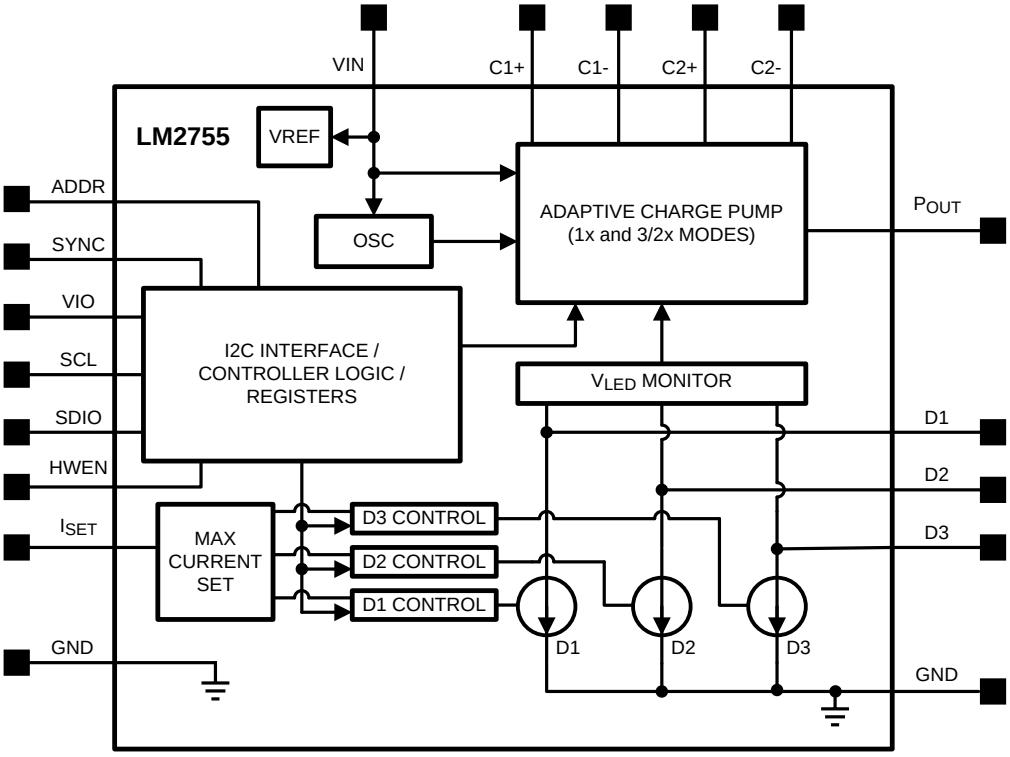


Figure 16. Block Diagram

CIRCUIT COMPONENTS

CHARGE PUMP

The input to the 3/2× - 1x charge pump is connected to the V_{IN} pin, and the regulated output of the charge pump is connected to the P_{OUT} pin. The recommended input voltage range of the LM2755 is 3.0V to 5.5V. The device's regulated charge pump has both open loop and closed loop modes of operation. When the device is in open loop, the voltage at V_{OUT} is equal to the gain times the voltage at the input. When the device is in closed loop, the voltage at V_{OUT} is regulated to 4.6V (typ.). The charge pump gain transitions are actively selected to maintain regulation based on LED forward voltage and load requirements. This allows the charge pump to stay in the most efficient gain (1x) over as much of the input voltage range as possible, reducing the power consumed from the battery.

LED FORWARD VOLTAGE MONITORING

The LM2755 has the ability to switch converter gains (1x or 3/2x) based on the forward voltage of the LED load. This ability to switch gains maximizes efficiency for a given load. Forward voltage monitoring occurs on all diode pins. At higher input voltages, the LM2755 will operate in pass mode, allowing the P_{OUT} voltage to track the input voltage. As the input voltage drops, the voltage on the Dx pins will also drop ($V_{DX} = V_{POUT} – V_{LEDx}$). Once any of the active Dx pins reaches a voltage approximately equal to 350mV, the charge pump will then switch to the gain of 3/2x. This switch-over ensures that the current through the LEDs never becomes pinched off due to a lack of headroom on the current sources.

Only active Dx pins will be monitored. For example, if only D1 is enabled, the LEDs connected to D2 and D3 will not affect the gain transition point. If all Dx pins are enabled, all diodes will be monitored, and the gain transition will be based upon the diode with the highest forward voltage.

HWEN PIN

The LM2755 has a hardware enable/reset pin (HWEN) that allows the device to be disabled by an external controller without requiring an I^2C write command. Under normal operation, the HWEN pin should be held high (logic '1') to prevent an unwanted reset. When the HWEN is driven low (logic '0'), all internal control registers reset to the default states and the part becomes disabled. Please see Electrical Characteristics for required voltage thresholds.

SYNC PIN

The SYNC pin allows the LM2755 to use an external clock to generate the timing within. This allows the LM2755's current-sinks to pulse-width modulate (PWM) and transition at a user controlled frequency. The PWM frequency and the step-time increment can be set by feeding a clock signal into the SYNC pin and enabling bit 6 in the General Purpose register (See Electrical Characteristics for more details.). The maximum frequency allowed to ensure current level accuracy is 1MHz. This external clock is divided down by 32x to create the minimum time-step and PWM frequency. For a 1MHz external clock, the PWM frequency becomes 31.25KHz, and the minimum step time becomes 32µseconds. If not used, it is recommended that the SYNC pin be tied to ground.

ADDR PIN

The ADDR pin allows the user to choose between two different I^2C chip addresses for the LM2755. Tying the ADDR pin high sets the chip address to hex 67 (0x67 or 67h), while tying the ADDR pin low sets the chip address to hex 18 (0x18 or 18h). This feature allows multiple LM2755's to be used within a system in addition to providing flexibility in the event another chip in the system has a chip address similar to the default LM2755 address (0x18).

I^2C-Compatible Interface

DATA VALIDITY

The data on SDIO line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when CLK is LOW.

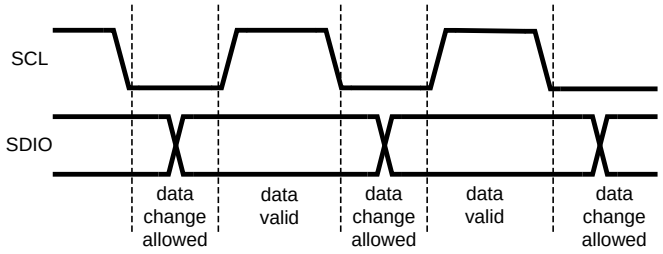


Figure 17. Data Validity Diagram

A pull-up resistor between VIO and SDIO must be greater than [**(VIO-V_{OL}) / 3mA**] to meet the V_{OL} requirement on SDIO. Using a larger pull-up resistor results in lower switching current with slower edges, while using a smaller pull-up results in higher switching currents with faster edges.

START AND STOP CONDITIONS

START and STOP conditions classify the beginning and the end of the I^2C session. A START condition is defined as SDIO signal transitioning from HIGH to LOW while SCL line is HIGH. A STOP condition is defined as the SDIO transitioning from LOW to HIGH while SCL is HIGH. The I^2C master always generates START and STOP conditions. The I^2C bus is considered to be busy after a START condition and free after a STOP condition. During data transmission, the I^2C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise. The data on SDIO line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when CLK is LOW.

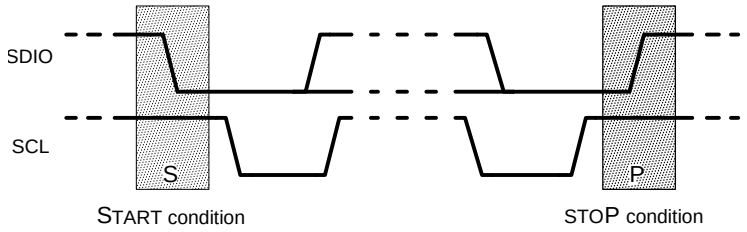
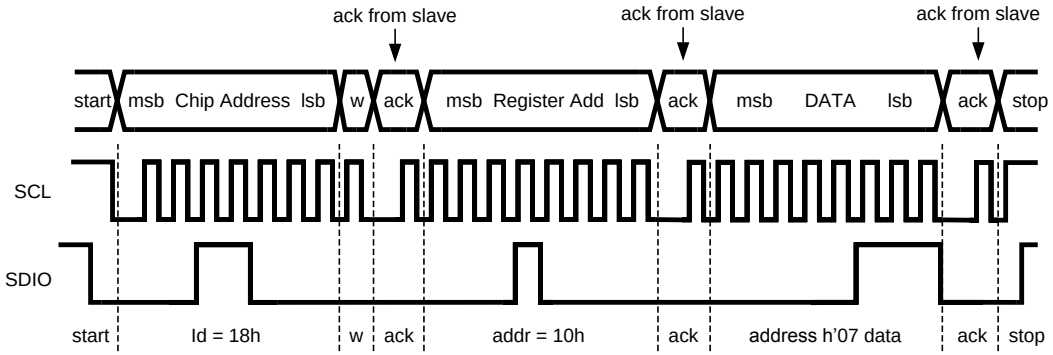


Figure 18. Start and Stop Conditions

TRANSFERRING DATA

Every byte put on the SDIO line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The master releases the SDIO line (HIGH) during the acknowledge clock pulse. The LM2755 pulls down the SDIO line during the 9th clock pulse, signifying an acknowledge. The LM2755 generates an acknowledge after each byte has been received.

After the START condition, the I^2C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LM2755 address is 18h is ADDR if tied low and 67h if ADDR is tied high . For the eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.



w = write (SDIO = "0")
r = read (SDIO = "1")
ack = acknowledge (SDIO pulled down by either master or slave)
rs = repeated start
id = chip address, 18h if ADDR = '0' or 67h if ADDR = '1' for LM2755

Figure 19. Write Cycle

I²C-COMPATIBLE CHIP ADDRESS

The chip address for LM2755 is 0011000 (0x18) when ADDR = '0' or 1100111(0x67) when ADDR = '1'.

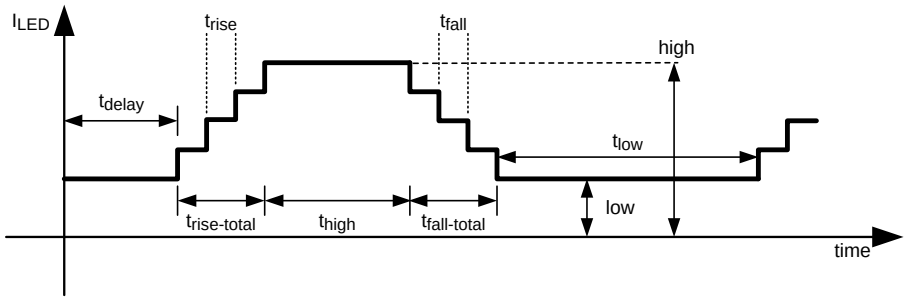


Figure 20. Dimming Waveform

Internal Registers

Table 1. Internal Registers of LM2755

Register Name	Internal Hex Address	Power On Value
General Purpose	x10	0000 0000
Time Step: n_{STEP}	x20	1000 1000
D1 High Level: n_{ID1H}	xA9	1110 0000
D1 Low Level: n_{ID1L}	xA8	1110 0000
D1 Delay: n_{delay1}	xA1	0000 0000
D1 Ramp-Up Step Time: n_{rise1}	xA5	0000 0000 (1)
D1 Time High: n_{high1}	xA3	0000 0000
D1 Ramp-Down Step Time: n_{fall1}	xA4	0000 0000 (1)
D1 Timing: n_{low1}	xA2	0000 0000
D2 High Level: n_{ID2H}	xB9	1110 0000
D2 Low Level: n_{ID2L}	xB8	1110 0000
D2 Delay: n_{delay2}	xB1	0000 0000
D2 Ramp-Up Step Time: n_{rise2}	xB5	0000 0000 (1)

(1) **n_{risex} or n_{fallx} = 0 or 1 are not valid and should not be used**

Table 1. Internal Registers of LM2755 (continued)

Register Name	Internal Hex Address	Power On Value
D2 Time High: n_{high2}	xB3	0000 0000
D2 Ramp-Down Step Time: n_{fall2}	xB4	0000 0000 (1)
D2 Timing: n_{low2}	xB2	0000 0000
D3 High Level: n_{ID3H}	xC9	1110 0000
D3 Low Level: n_{ID3L}	xC8	1110 0000
D3 Delay: n_{delay3}	xC1	0000 0000
D3 Ramp-Up Step Time: n_{rise3}	xC5	0000 0000 (1)
D3 Time High: n_{high3}	xC3	0000 0000
D3 Ramp-Down Step Time: n_{fall3}	xC4	0000 0000 (1)
D3 Timing: n_{low3}	xC2	0000 0000

GENERAL PURPOSE REGISTER DESCRIPTION

- Bit 0: enable output D1 with high current level.
- Bit 1: enable output D2 with high current level.
- Bit 2: enable output D3 with high current level.
- Bit 3: enable dimming waveform on output D1.
- Bit 4: enable dimming waveform on output D2.
- Bit 5: enable dimming waveform on output D3.
- Bit 6: enable external clock. '1' = External Clock Sync, '0' = Internal Clock Used
- Bit 7: If Bit 7 = 0 the charge pump is powered on before any dimming waveform is enabled. It is recommended that Bit7 be set to a '0' if an external clock is used. If Bit 7 = 1 the dimming waveform can be enabled before charge pump is powered on.

Application Information

SETTING FULL-SCALE LED CURRENT

The current through the LEDs connected to D1, D2 and D3 can be set to a desired level simply by connecting an appropriately sized resistor (R_{SET}) between the ISET pin of the LM2755 and GND. The LED currents are proportional to the current that flows through the ISET pin and are a factor of 200 times greater than the I_{SET} currents. The feedback loop of the internal amplifier sets the voltage of the ISET pin to 1.25V (typ.). The statement above is simplified in the equation below:

$$I_{Dx\ (Full\text{-}Scale)} = 200 \times (V_{ISET} / R_{SET}) \quad (1)$$

Please refer to **I²C-Compatible Interface** for detailed instructions on how to adjust the brightness control registers.

BRIGHTNESS LEVEL CONTROL

Once the desired R_{SET} value has been chosen, the LM2755 can internally dim the LEDs by modulating the currents with an internally set 20kHz PWM signal. The PWM duty cycle percentage is independently set for each LED through the I²C-compatible interface. The 32 brightness levels follow a exponentially increasing pattern rather than a linearly increasing one in order to better match the human eye's response to changing brightness. The brightness level response is modeled in the following equations.:

$$I_{Dx\ LOW} = (0.9)^{(31-n_{IDxL})} \times I_{Dx\ Fullscale} \quad (2)$$

$$I_{Dx\ HIGH} = (0.9)^{(31-n_{IDxH})} \times I_{Dx\ Fullscale} \quad (3)$$

n_{IDxH} and n_{IDxL} are numbers between 0 and 31 stored in the Brightness Level registers. When the waveform enable bits are set to '1', n_{IDxH} and n_{IDxL} are the brightness level boundaries. These equations apply to all Dx outputs and their corresponding registers. A '0' code in the Brightness Control register sets the current to an "off-state" (0mA).

TIME STEP CONTROL

Bit 0 to Bit 2: The value of these 3 bits is equal to N, which is used in the timing control equations ($0 \le N \le 7$). The minimum internal time step (N=0) is 50µs. Setting the time-step to N=7 results in a maximum time step of 6.4msec.

$t_{STEP} = 50\mu sec \times 2^{NSTEP}$ if the internal clock is used. (4)

$t_{STEP} = 2^{NSTEP} \times (32 \div f_{SYNC})$ if the external clock on the SYNC pin is used. (5)

Bit 3 to Bit 7: Not used

DELAY CONTROL

The LM2755 allows the programmed current waveform on each diode pin to independently start with a delay upon enabling the waveform dimming bits in the general purpose register. There are 256 delay levels available. The delay time is set by the following equation:

For $n_{STEP} = 0$, (6)

$t_{delayx} = t_{STEP} \times (n_{delayx} + n_{risex})$ (7)

By default, $n_{delayx} = 0$ with a range of $0 \le n_{delay} \le 255$. (8)

For $1 \le n_{STEP} \le 7$, $t_{delayx} = t_{STEP} \times [(n_{delayx}-1) + (n_{risex}-1)]$

where

- $1 \le n_{delay} \le 255$.
- If $n_{delay} = 0$, $t_{delayx} = 0s$.
- n_{delayx} is stored in the Dx Delay registers. (9)

TIMING CONTROL

n_{risex} n_{fallx}, n_{highx}, n_{lowx} are numbers between 0 and 255, stored in the timing control registers. The durations of the rise, high, fall and low times are given by:

For $n_{STEP} = 0$, (10)

(11)

$t_{rise/fall} = t_{STEP} \times (n_{IDxH} - n_{IDxL} - 1) \times n_{risex/fallx}$

where

- $2 \le n_{risex/fallx} \le 255$
- **n_{risex} or n_{fallx} = 0 or 1 are not valid and should not be used** (12)

For $1 \le n_{STEP} \le 7$, (13)

$t_{rise/fall} = t_{STEP} \times (n_{IDxH} - n_{IDxL} - 1) \times (n_{risex/fallx} - 1)$

where

- $2 \le n_{risex/fallx} \le 255$
- **n_{risex} or n_{fallx} = 0 or 1 are not valid and should not be used** (14)

For $n_{STEP} = 0$, (15)

$t_{highx} = t_{STEP} \times (n_{highx} + n_{fallx})$ $t_{lowx} = t_{STEP} \times (n_{lowx} + n_{risex})$

where

- $1 \le n_{highx/lowx} \le 255$
- For $n_{highx/lowx}=0$, $t_{high\ or\ low} = t_{STEP}$ (16)

For $1 \le n_{STEP} \le 7$, (17)

$t_{highx} = t_{STEP} \times ((n_{highx} - 1) + (n_{fallx} - 1))$ (18)

$t_{lowx} = t_{STEP} \times ((n_{lowx} - 1) + (n_{risex} - 1))$

where

- $2 \le n_{highx/lowx} \le 255$
- For $n_{highx/lowx} = 0$ or 1, $t_{highx} = t_{STEP} \times (n_{fallx} - 1)$
- $t_{lowx} = t_{STEP} \times (n_{risex} - 1)$ (19)

SYNC PIN TIMING CONTROL

It is possible to replace the internal clock with an external one placed on the external SYNC pin. Writing a '1' to bit 6 in the General Purpose register switches the system clock from being internally generated to externally generated. The frequency of the PWM modulating signal becomes:

$$f_{PWM} = f_{SYNC} / 32 \quad (20)$$

The maximum recommended SYNC frequency is 1MHz. This frequency yields a PWM frequency of 31.25KHz and the minimum step time of 32µsec.

MAXIMUM OUTPUT CURRENT, MAXIMUM LED VOLTAGE, MINIMUM INPUT VOLTAGE

The LM2755 can drive 3 LEDs at 30mA each (D1, D2, D3) from an input voltage as low as 3.2V, as long as the LEDs have a forward voltage of 3.6V or less (room temperature).

The statement above is a simple example of the LED drive capability of the LM2755. The statement contains the key application parameters that are required to validate an LED-drive design using the LM2755: LED current (I_{LEDx}), number of active LEDs (N_x), LED forward voltage (V_{LED}), and minimum input voltage (V_{IN-MIN}).

The equation below can be used to estimate the maximum output current capability of the LM2755:

$$I_{LED\_MAX} = [(1.5 \times V_{IN}) - V_{LED} - (I_{ADDITIONAL} \times R_{OUT})] \div [(N_x \times R_{OUT}) + k_{HRx}] \quad (21)$$

$$I_{LED\_MAX} = [(1.5 \times V_{IN}) - V_{LED} - (I_{ADDITIONAL} \times 2.4\Omega)] \div [(N_x \times 2.4\Omega) + k_{HRx}]$$

- $I_{ADDITIONAL}$ is the additional current that could be delivered to the other LED Groups. (22)

R_{OUT}: Output resistance. This parameter models the internal losses of the charge pump that result in voltage droop at the pump output V_{OUT}. Since the magnitude of the voltage droop is proportional to the total output current of the charge pump, the loss parameter is modeled as a resistance. The output resistance of the LM2755 is typically 2.4Ω (V_{IN} = 3.6V, T_A = 25°C). In equation form:

$$V_{VOUT} = (1.5 \times V_{IN}) - [(I_{LED1} + I_{LED2} + I_{LED3}) \times R_{OUT}] \quad (23)$$

k_{HR} – Headroom constant. This parameter models the minimum voltage required to be present across the current sinks for them to regulate properly. This minimum voltage is proportional to the programmed LED current, so the constant has units of mV/mA. The typical k_{HR} of the LM2755 is 3.25mV/mA. In equation form:

$$(V_{VOUT} - V_{LEDx}) > k_{HRx} \times I_{LEDx} \quad (24)$$

Typical Headroom Constant Values $k_{HR1} = k_{HR2} = k_{HR3} = 10$ mV/mA (25)

The "$I_{LED-MAX}$" Equation 21 is obtained from combining the "R_{OUT}" Equation 23 with the "k_{HRx}" Equation 24 and solving for I_{LEDx}. Maximum LED current is highly dependent on minimum input voltage and LED forward voltage. Output current capability can be increased by raising the minimum input voltage of the application, or by selecting an LED with a lower forward voltage. Excessive power dissipation may also limit output current capability of an application.

Total Output Current Capability

The maximum output current that can be drawn from the LM2755 is 90mA. Each driver group has a maximum allotted current per Dx sink that must not be exceeded.

Table 2.

DRIVER TYPE	MAXIMUM Dx CURRENT
Dx	30mA per Dx Pin

The 90mA load can be distributed in many different configurations. Special care must be taken when running the LM2755 at the maximum output current to ensure proper functionality.

POWER EFFICIENCY

Efficiency of LED drivers is commonly taken to be the ratio of power consumed by the LEDs (P_{LED}) to the power drawn at the input of the part (P_{IN}). With a 3/2× - 1× charge pump, the input current is equal to the charge pump gain times the output current (total LED current). The efficiency of the LM2755 can be predicted as follow:

$$P_{LEDTOTAL} = (V_{LEDA} \times N_A \times I_{LEDA}) + (V_{LEDB} \times N_B \times I_{LEDB}) + (V_{LEDC} \times I_{LEDC}) \quad (26)$$

$$P_{IN} = V_{IN} \times I_{IN} \quad (27)$$

$$P_{IN} = V_{IN} \times (GAIN \times I_{LEDTOTAL} + I_Q) \quad (28)$$

$$E = (P_{LEDTOTAL} \div P_{IN}) \quad (29)$$

The LED voltage is the main contributor to the charge-pump gain selection process. Use of low forward-voltage LEDs (3.0V to 3.5V) will allow the LM2755 to stay in the gain of 1× for a higher percentage of the lithium-ion battery voltage range when compared to the use of higher forward voltage LEDs (3.5V to 4.0V). See LED FORWARD VOLTAGE MONITORINGfor a more detailed description of the gain selection and transition process.

For an advanced analysis, it is recommended that power consumed by the circuit (V_{IN} x I_{IN}) for a given load be evaluated rather than power efficiency.

POWER DISSIPATION

The power dissipation (P_{DISS}) and junction temperature (T_J) can be approximated with the equations below. P_{IN} is the power generated by the 3/2× - 1× charge pump, P_{LED} is the power consumed by the LEDs, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance for the DSBGA 18-bump package. V_{IN} is the input voltage to the LM2755, V_{LED} is the nominal LED forward voltage, N is the number of LEDs and I_{LED} is the programmed LED current.

$$P_{DISS} = P_{IN} - P_{LED1} - P_{LED2} - P_{LED3} \quad (30)$$

$$P_{DISS} = (GAIN \times V_{IN} \times I_{D1 + D2 + D3}) - (V_{LED1} \times I_{LED1}) - (V_{LED2} \times I_{LED2}) - (V_{LED3} \times I_{LED3}) \quad (31)$$

$$T_J = T_A + (P_{DISS} \times \theta_{JA}) \quad (32)$$

The junction temperature rating takes precedence over the ambient temperature rating. The LM2755 may be operated outside the ambient temperature rating, as long as the junction temperature of the device does not exceed the maximum operating rating of 105°C. The maximum ambient temperature rating must be derated in applications where high power dissipation and/or poor thermal resistance causes the junction temperature to exceed 105°C.

THERMAL PROTECTION

Internal thermal protection circuitry disables the LM2755 when the junction temperature exceeds 160°C (typ.). This feature protects the device from being damaged by high die temperatures that might otherwise result from excessive power dissipation. The device will recover and operate normally when the junction temperature falls below 155°C (typ.). It is important that the board layout provide good thermal conduction to keep the junction temperature within the specified operating ratings.

CAPACITOR SELECTION

The LM2755 requires 4 external capacitors for proper operation (C_{IN} = C_{OUT} = 1µF, C_1 = C_2 = 0.47µF). Surface-mount multi-layer ceramic capacitors are recommended. These capacitors are small, inexpensive and have very low equivalent series resistance (ESR <20mΩ typ.). Tantalum capacitors, OS-CON capacitors, and aluminum electrolytic capacitors are not recommended for use with the LM2755 due to their high ESR, as compared to ceramic capacitors.

For most applications, ceramic capacitors with X7R or X5R temperature characteristic are preferred for use with the LM2755. These capacitors have tight capacitance tolerance (as good as ±10%) and hold their value over temperature (X7R: ±15% over −55°C to 125°C; X5R: ±15% over −55°C to 85°C).

Capacitors with Y5V or Z5U temperature characteristic are generally not recommended for use with the LM2755. Capacitors with these temperature characteristics typically have wide capacitance tolerance (+80%, −20%) and vary significantly over temperature (Y5V: +22%, −82% over −30°C to +85°C range; Z5U: +22%, −56% over +10°C to +85°C range). Under some conditions, a nominal 1µF Y5V or Z5U capacitor could have a capacitance of only 0.1µF. Such detrimental deviation is likely to cause Y5V and Z5U capacitors to fail to meet the minimum capacitance requirements of the LM2755.

The recommended voltage rating for the capacitors is 10V to account for DC bias capacitance losses.

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2755TM/NOPB	ACTIVE	DSBGA	YFQ	18	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-30 to 85	D32	Samples
LM2755TMX/NOPB	ACTIVE	DSBGA	YFQ	18	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-30 to 85	D32	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

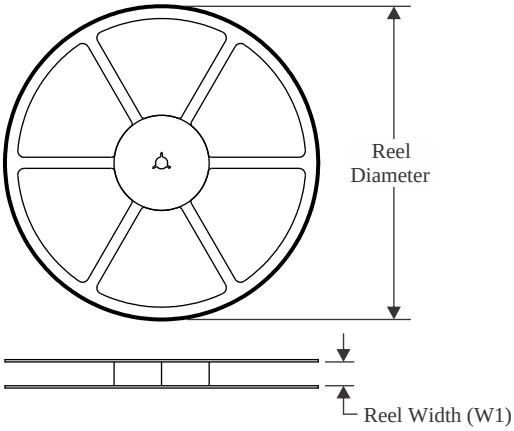
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

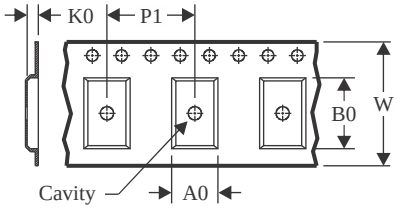
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

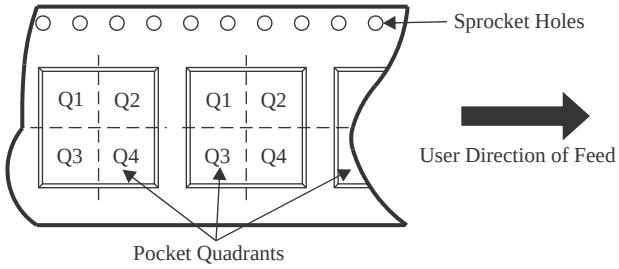


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

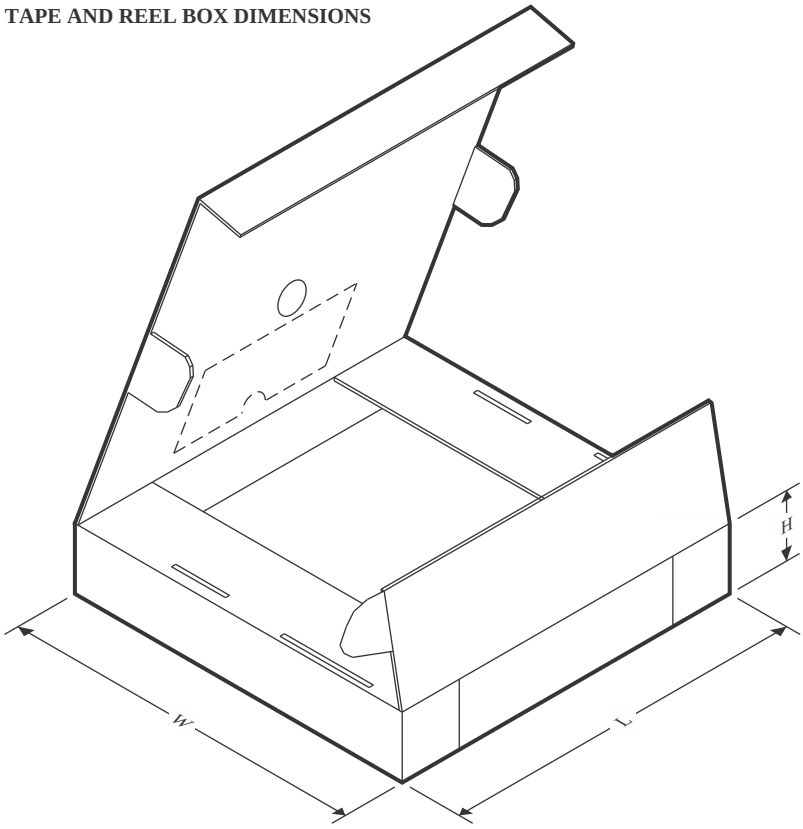
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2755TM/NOPB	DSBGA	YFQ	18	250	178.0	8.4	1.85	2.01	0.76	4.0	8.0	Q1
LM2755TMX/NOPB	DSBGA	YFQ	18	3000	178.0	8.4	1.85	2.01	0.76	4.0	8.0	Q1

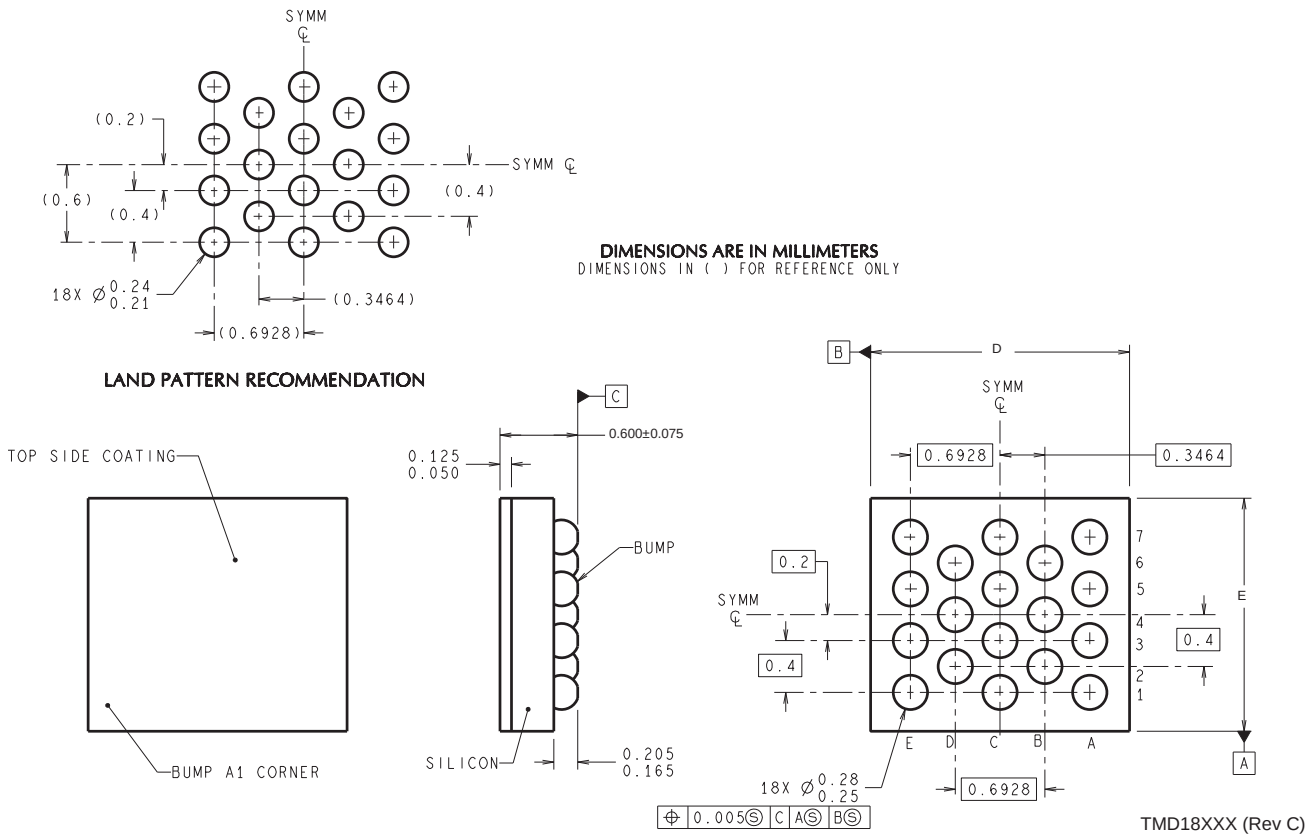
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2755TM/NOPB	DSBGA	YFQ	18	250	210.0	185.0	35.0
LM2755TMX/NOPB	DSBGA	YFQ	18	3000	210.0	185.0	35.0

YFQ0018



D: Max = 1.832 mm, Min =1.771 mm

E: Max = 1.641 mm, Min =1.581 mm

4215082/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265