LM3687 Step-Down DC-DC Converter with Integrated Low Dropout Regulator and Startup Mode

Check for Samples: LM3687

FEATURES

DC-DC Converter:

- **750mA Maximum Load Capability**
- **1.8MHz PWM Fixed Switching Frequency (Typ.)**
- **Automatic PFM/PWM Mode Switching**
- **27µA typ. Quiescent Current**
- **Internal Synchronous Rectification for High Efficiency**
- **Internal Soft Start**

Dual Rail Linear Regulator:

- **Startup Mode**
- **Load Transients < 25mVpeak Typ.**
- **Line Transients < 1mVpeak Typ.**
- **Very Low Dropout Voltage: 82mV Typ. at 350mA Load Current**
- **0.7V ≤ V_{IN_LIN} ≤ 4.5V**
- **10µA Typical I_Q from V_{IN_LIN}**
- **350mA Maximum Load Capability**

Combined Common Features:

- **65µA typical Quiescent Current from V_{BATT} if Both Regulators are Enabled**
- **750mA Maximum Combined Load Capability in Post Regulation Setup (DC-DC 400mA + Linear Regulator 350mA)**
- **1100mA Maximum Total Load Capability in Independent Mode of Operation (DC-DC: 750mA, Linear Regulator: 350mA)**
- **Operates from a Single Li-Ion Cell or 3 Cell NiMH/NiCd Batteries**
- **Only Four Tiny Surface-Mount External Components Required (One Inductor, Three Ceramic Capacitors)**
- **Small 9-Bump DSBGA Package**
- **Over-Temperature, Current Overload and Under-Voltage Protection**

APPLICATIONS

- **Mobile Phones**
- **Hand-Held Radios**
- **Personal Digital Assistants**
- **Palm-top PCs**
- **Portable Instruments**
- **Battery Powered Devices**

DESCRIPTION

The LM3687 is a step-down DC-DC converter with an integrated low dropout Linear Regulator optimized for powering ultra-low voltage circuits from a single Li-Ion cell or 3 cell NiMH/NiCd batteries. It provides a dual output with fixed output voltages and combined load current up to 750mA in post regulation mode or 1100mA in independent mode of operation, over an input voltage range from 2.7V to 5.5V. There are several different fixed output voltage combinations available (refer to Voltage Options).

The Linear Regulator being driven from the fixed output voltage of the buck converter (post regulation) translates to high efficiency.

The device offers superior features and performance for mobile phones and similar portable applications with complex power management systems. Automatic intelligent switching between PWM low-noise and PFM low-current mode offers improved efficiency over the full load current range. During full-power operation, a fixed-frequency 1.8MHz (typ.) PWM mode drives loads from ~80mA to 750mA max. Hysteretic PFM mode extends the battery life through reduction of the quiescent current during light loads and system standby.

The LM3687 also features internal protection against over-temperature, current overload and under-voltage conditions.

DESCRIPTION (CONTINUED)

Two enable pins allow the separate operation of either the DC-DC or the Linear Regulator alone or both. If the power input voltage for the Linear Regulator V_{IN_LIN} is not sufficiently high (e.g. the DC-DC converter is not enabled or starting up) a startup LDO supplies the Linear Regulator Output from V_{BATT} for 50mA rated load current (Startup Mode). If V_{IN_LIN} is at the required voltage level, the startup LDO is deactivated and the main regulator provides 350mA output current. In shutdown mode (Enable pins pulled low) the device turns off and reduces battery consumption to 0.1µA (typ.).

The LM3687 is available in a tiny, lead-free (NO PB) 9-bump DSBGA package. A high switching frequency of 1.8MHz (typ.) allows the use of tiny surface-mount components. Only four external components -one inductor and three ceramic capacitors- are required.

Typical Application Circuit

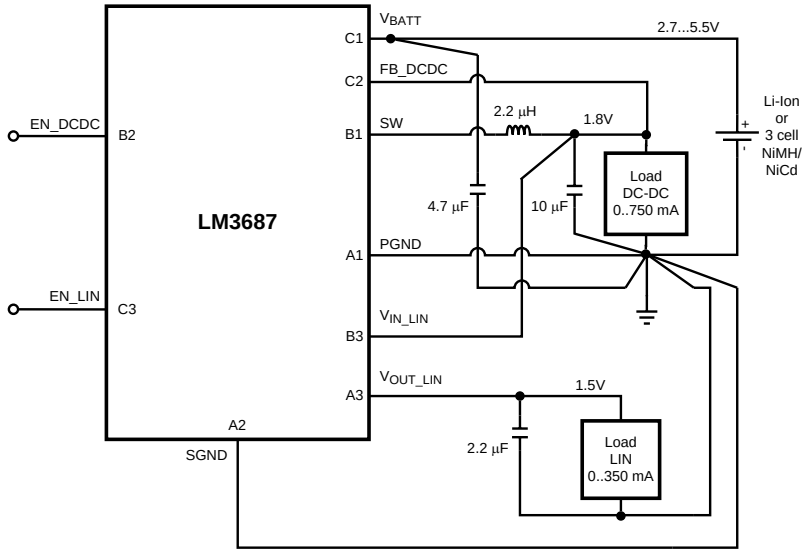

Figure 1. Typical Application Circuit: Linear Regulator as Post Regulator

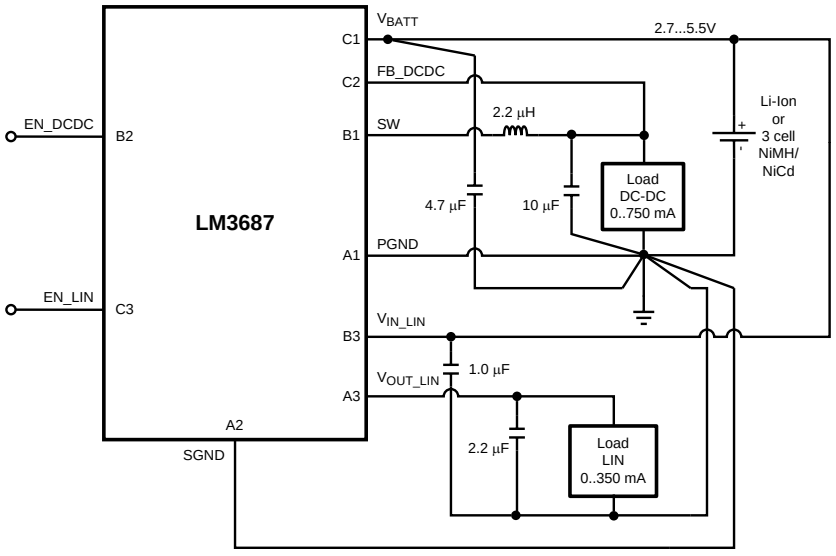

Figure 2. Typical Application Circuit: Independent Mode of Operation

Connection Diagram

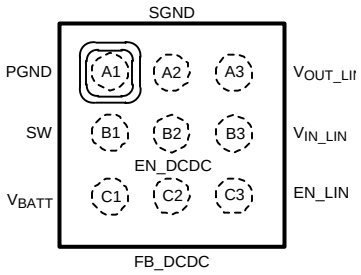

Figure 3. Connection Diagram 9-Bump Thin DSBGA Package
Top View
(See Package Number YZR0009BBA)

PIN DESCRIPTIONS

Pin Number	Pin Name	Description
A1	PGND	Power Ground pin
A2	SGND	Signal Ground pin
A3	V_{OUT_LIN}	Voltage Output of the linear regulator
B1	SW	Switching Node Connection to the internal PFET switch and NFET synchronous rectifier
B2	EN_DCDC	Enable Input for the DC-DC converter. The DC-DC converter is in shutdown mode if voltage at this pin is < 0.4V and enabled if > 1.0V. Do not leave this pin floating. Please see Enable Combinations.
B3	V_{IN_LIN}	Power Supply Input for the linear regulator
C1	V_{BATT}	Power Supply for the DC-DC output stage and internal circuitry. Connect to the input filter capacitor (see Typical Application Circuit).
C2	FB_DCDC	Feedback Analog Input for the DC-DC converter. Connect directly to the output filter capacitor.
C3	EN_LIN	Enable Input for the linear regulator. The linear regulator is in shutdown mode if voltage at this pin is < 0.4V and enabled if > 1.0V. Do not leave this pin floating. Please see Enable Combinations.

Voltage Options

DC-DC Converter Output: V_{OUT_DCDC}	Linear Regulator Output: V_{OUT_LIN}
1.80V	1.50V
1.80V	1.20V
1.80V (1)	1.30V (1)

(1) For availability of these or other output voltage combinations please contact your local Texas Instruments sales office

Enable Combinations

EN_DCDC	EN_LIN	Comments
0	0	No Outputs
0	1	Linear Regulator enabled only (1)
1	0	DC-DC converter enabled only
1	1	DC-DC converter and linear regulator active (1)

(1) Startup Mode

Startup Mode:

V_{IN_LIN} must be higher than $V_{OUT\_LIN(NOM)}$ + 200mV in order to enable the main regulator (I_{MAX} = 350mA).

If V_{IN_LIN} < $V_{OUT\_LIN(NOM)}$ + 100mV (100mV hysteresis), the startup LDO (I_{MAX} = 50mA) is active, supplied from V_{BATT}.

For example in the typical post regulation application the LDO will remain in startup mode until the DC-DC converter has ramped up its output voltage.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)(3)

V_{IN_LIN}, V_{BATT} pins: Voltage to GND, $V_{IN\_LIN} \leq V_{BATT}$	-0.2V to 6.0V
V_{IN_LIN} pin to V_{BATT} pin	0.2V
Enable pins, Feedback pin, SW pin	(GND-0.2V) to (V_{BATT}+0.2V) with 6.0V max
Continuous Power Dissipation (4)	Internally Limited
Junction Temperature (T_{J-MAX})	150°C
Storage Temperature Range	-65°C to + 150°C
Package Peak Reflow Temperature (Pb-free, 10-20 sec.) (5)	260°C
ESD Rating (6)	
Human Body Model:	2.0kV
Machine Model	200V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the SGND pin.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 160°C (typ.) and disengages at T_J = 140°C (typ.).
(5) For detailed soldering specifications and information, please refer to Application Note 1112: DSBGA Wafer Level Chip Scale Package SNVA009.
(6) The Human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin. (MIL-STD-883 3015.7)

Operating Ratings (1)(2)

Input Voltage Range V_{BATT} (3)	2.7V to 5.5V ($\geq V_{OUT\_LIN(NOM)}$ + 1.5V and $\geq V_{OUT\_DCDC(NOM)}$ + 1.0V)
Input Voltage Range V_{IN_LIN}	($V_{OUT\_LIN(NOM)}$ + 0.25V) to 4.5V
Junction Temperature (T_J) Range	-30°C to + 125°C
Ambient Temperature (T_A) Range (4)	-30°C to + 125°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the SGND pin.
(3) The battery input voltage range recommended for ideal applications performance for the specified output voltages is given as follows: V_{BATT} = 2.7V to 5.5V for 1.0V < V_{OUT_DCDC} < 1.8V; V_{BATT} = (V_{OUT_DCDC} +1V) to 5.5V for 1.8V ≤ V_{OUT_DCDC} ≤ 1.875V
(4) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$.

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA}), for 4 layer board (1)	
DSBGA 9	70°C/W

(1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special attention must be paid to thermal dissipation issues in board design.

Electrical Characteristics: DC-DC Converter (1)(2)(3)

Typical values and limits appearing in standard typeface are for T_A = 25°C. Limits appearing in **boldface** type apply over the full operating temperature range: -30°C ≤ T_J ≤ +125°C. Unless otherwise noted, V_{IN_LIN} = $V_{OUT\_LIN(NOM)}$ + 0.3V, V_{BATT} = 3.6V, I_{OUT_LIN} = 1mA, V_{EN_DCDC} = V_{EN_LIN} = V_{BATT}, C_{VBATT} = 4.7µF, C_{VOUT_DCDC} = 10µF, C_{VOUT_LIN} = 2.2µF, C_{VIN_LIN} = 1.0µF, L = 2.2µH.

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
V_{FB_DCDC}	Feedback Voltage Accuracy	PWM Mode		**-2.5**	**+2.5**	%
	Line Regulation	V_{OUT_DCDC} + 1.0V ≤ V_{BATT} ≤ 5.5V, I_{OUT_DCDC} = 150mA	0.06			%/V
	Load Regulation	100mA ≤ I_{OUT_DCDC} ≤ 750mA	0.0005			%/mA
$R_{DSON(P)}$	Pin-Pin Resistance for PFET		280		500	mΩ
$R_{DSON(N)}$	Pin-Pin Resistance for NFET		200		400	mΩ
I_{LIM_DCDC}	Switch Peak Current Limit	Open loop (4)	1172	**994**	**1380**	mA
F_{OSC}	Internal Oscillator Frequency	PWM Mode	1.8	**1.3**	**2.3**	MHz

(1) All voltages are with respect to the potential at the SGND pin.
(2) Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm. Unless otherwise specified, conditions for typ. specifications are: V_{BATT} = 3.6V and T_A = 25°C.
(3) The parameters in the electrical characteristic table are tested at V_{BATT} = 3.6V unless otherwise specified. For performance over the input voltage range refer to datasheet curves.
(4) Refer to datasheet curves for closed loop data and its variation with regards to supply voltage and temperature. Electrical Characteristic table reflects open loop data (FB=0V and current drawn from SW pin ramped up until cycle by cycle current limit is activated). Closed loop current limit is the peak inductor current measured in the application circuit by increasing output current until output voltage drops by 10%.

Electrical Characteristics: Linear Regulator, Normal Mode[1][2]

Symbol	Parameter	Condition	Typ	Limit		Units
				Min	Max	
ΔV_{OUT_LIN} / $V_{OUT\_LIN(NOM)}$	Output Voltage Accuracy	In startup and normal mode		-1.5 **-2.0**	1.5 **2.0**	% %
ΔV_{OUT_LIN} / ΔV_{IN_LIN}	Line Regulation Error	V_{IN_LIN} = $V_{OUT\_LIN(NOM)}$ + 0.3V to 4.5V, V_{BATT} = 4.5V	0.3		**1**	mV/V
ΔV_{OUT_LIN} / ΔV_{BATT}		V_{BATT} = $V_{OUT\_LIN(NOM)}$ + 1.5V (≥2.7V) to 5.5V	0.5		**3.1**	
ΔV_{OUT_LIN} / ΔmA	Load Regulation Error	I_{OUT_LIN} = 1mA to 350mA	10		**60**	µV/mA
$V_{DO\_VIN\_LIN}$	Output Voltage Dropout [3][4]	I_{OUT_LIN} = 350mA , V_{BATT} = $V_{OUT\_LIN(NOM)}$ + 1.5V (≥2.7V)	85		**200**	mV
		I_{OUT_LIN} = 150mA , V_{BATT} = $V_{OUT\_LIN(NOM)}$ + 1.3V (≥2.7V)	42		**100**	mV
$I_{Q\_VIN\_LIN}$	Quiescent Current into V_{IN_LIN}	I_{OUT_LIN} = 0mA	10		**28**	µA
	Shutdown Current into V_{IN_LIN}	V_{EN_LIN} = 0V	0.1		**1**	µA
I_{SC_LIN}	Output Current (short circuit)	V_{OUT_LIN} = 0V	500	**350**		mA
PSRR	Power Supply Rejection Ratio	Sine modulated V_{BATT}, f = 10Hz f = 100Hz f = 1kHz	 70 65 45			dB
		Sine modulated V_{IN} f = 10Hz f = 100Hz f = 1kHz f = 10kHz	 80 90 95 85			dB
E_N	Output Noise linear regulator	10Hz - 100kHz	100			μV_{RMS}
ΔV_{OUT_LIN}	Dynamic line transient response V_{IN_LIN}	V_{IN_LIN} = $V_{OUT\_LIN(NOM)}$ + 0.3V to $V_{OUT\_LIN(NOM)}$ + 0.9V tr, tf = 10µs	±1			mVp
	Dynamic line transient response V_{BATT}	V_{BATT} = $V_{OUT\_LIN(NOM)}$ + 1.5V to $V_{OUT\_LIN(NOM)}$ + 2.1V tr, tf = 10µs	±15			mVp
ΔV_{OUT_LIN}	Dynamic load transient response	Pulsed load 0 ... 350mA di/dt = 350mA/1µs	±30			mVp

(1) All voltages are with respect to the potential at the SGND pin.
(2) Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm. Unless otherwise specified, conditions for typ. specifications are: V_{BATT} = 3.6V and T_A = 25°C.
(3) Dropout voltage is defined as the input to output voltage differential at which the output voltage falls to 100mV below the nominal output voltage.
(4) This specification does not apply if the battery voltage V_{BATT} needs to be decreased below the minimum operating limit of 2.7V.

Electrical Characteristics: Startup LDO[1][2]

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
I_{OUT}	Rated output current		50			mA
I_{SC_LIN}	Output Current (short circuit)	V_{OUT_LIN} = 0V	100	**50**		mA

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(2) Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm. Unless otherwise specified, conditions for typ. specifications are: V_{BATT} = 3.6V and T_A = 25°C.

Electrical Characteristics: System Parameters Supply[1][2]

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
I_{Q_VBATT}	Quiescent current into V_{BATT}	EN_LIN = low, EN_DCDC = high, I_{OUT_DCDC} = I_{OUT_LIN} = 0mA, DC-DC is not switching (FB_DCDC forced higher than V_{OUT_DCDC})	27		**60**	µA
		EN_LIN = high, EN_DCDC = low	55			µA
		EN_LIN = EN_DCDC = high	65			µA
	Shutdown current into V_{BATT}	V_{EN_DCDC} = V_{EN_LIN} = 0V -30°C ≤ T_J ≤ +85°C	0.1		**5**	µA

(1) All voltages are with respect to the potential at the SGND pin.
(2) Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm. Unless otherwise specified, conditions for typ. specifications are: V_{BATT} = 3.6V and T_A = 25°C.

Electrical Characteristics: Under-Voltage Protection[1][2]

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
V_{BATT_UVP}	Under-Voltage Lockout		2.41			V
V_{BATT_EN}	System Enable Voltage		2.65			V

(1) All voltages are with respect to the potential at the SGND pin.
(2) Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm. Unless otherwise specified, conditions for typ. specifications are: V_{BATT} = 3.6V and T_A = 25°C.

Electrical Characteristics: Enable Pins (EN_DCDC, EN_LIN)[1][2]

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
I_{EN}	Enable pin input current		0.01		**1**	µA
V_{IH}	Logic High voltage level			**1.0**		V
V_{IL}	Logic Low voltage level				**0.4**	V

(1) All voltages are with respect to the potential at the SGND pin.
(2) Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm. Unless otherwise specified, conditions for typ. specifications are: V_{BATT} = 3.6V and T_A = 25°C.

Electrical Characteristics: Thermal Protection[1][2]

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
T_{SHDN}[3]	Thermal-Shutdown Temperature		160			°C
ΔT_{SHDN}	Thermal-Shutdown Hysteresis		20			°C

(1) All voltages are with respect to the potential at the SGND pin.
(2) Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm. Unless otherwise specified, conditions for typ. specifications are: V_{BATT} = 3.6V and T_A = 25°C.
(3) The DC-DC converter will only enter thermal shutdown from PWM mode. At light loads -present for PFM mode- no significant contribution to the power dissipation is added by the DC-DC converter.

Electrical Characteristics: External Components, Recommended Specification (1)(2)(3)

Symbol	Parameter	Conditions	Value	Limit		Units
				Min	Max	
C_{VOUT_LIN}	Output Capacitance for linear regulator		2.2	1.5	10	µF
C_{VIN_LIN}	Input Capacitance for linear regulator	V_{IN_LIN} is biased separately, not by V_{OUT_DCDC} (no C_{VIN_LIN} needed for post regulation application)	1.0	0.47		µF
C_{VBATT}	Input Capacitance for DC-DC converter		4.7			µF
C_{VOUT_DCDC}	DC-DC converter output filter capacitor		10			µF
C_{ESR}	ESR of all capacitors			0.003	0.300	Ω
L	Inductance		2.2			µH
	I_{SAT}		1.6			A
	DCR				200	mΩ

(1) All voltages are with respect to the potential at the SGND pin.
(2) Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm. Unless otherwise specified, conditions for typ. specifications are: V_{BATT} = 3.6V and T_A = 25°C.
(3) The capacitor tolerance should be 30% or better over temperature. The full operating conditions for the application should be considered when selecting a suitable capacitor to ensure that the minimum value of capacitance is always met. Recommended capacitor type is X7R. However, dependent on application, X5R, Y5V, and Z5U can also be used. The shown minimum limit represents real minimum capacitance, including all tolerances and must be maintained over temperature and dc bias voltage (See CAPACITOR CHARACTERISTICS)

BLOCK DIAGRAM

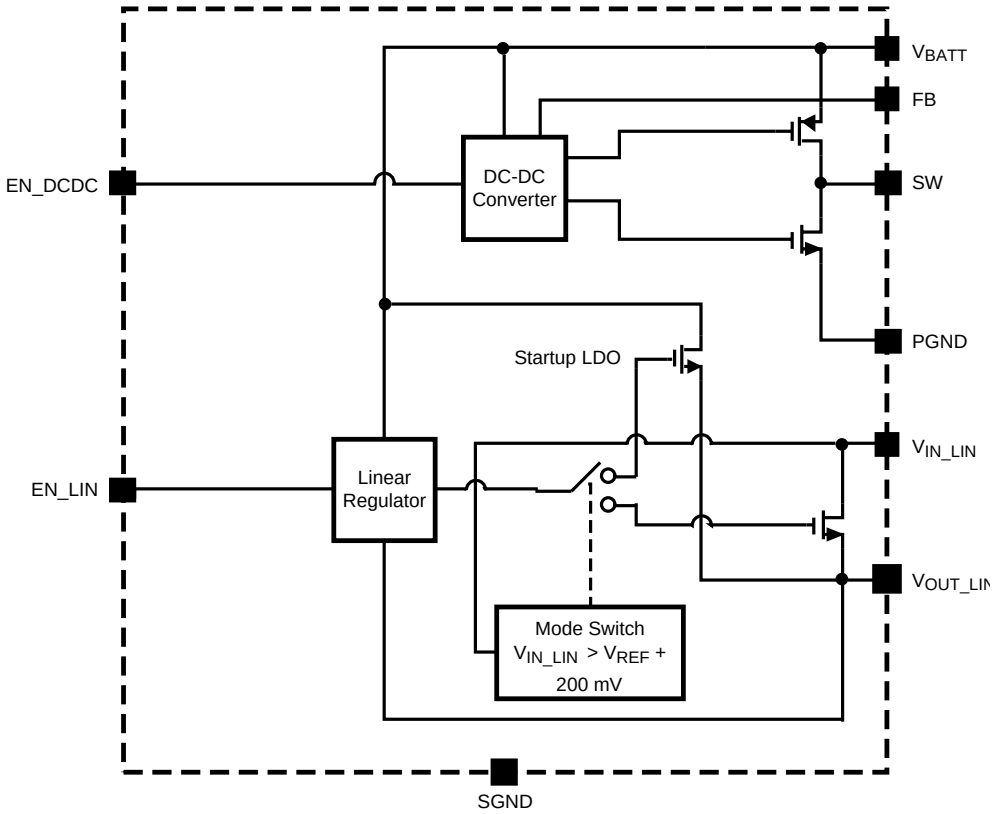


Figure 4. Simplified Block Diagram

Typical Performance Characteristics

Unless otherwise specified, typical application (post regulation), V_{BATT} = 3.6V, T_A = 25°C, enable pins tied to V_{BATT}, V_{OUT_DCDC} = 1.8V, V_{OUT_LIN} = 1.2V

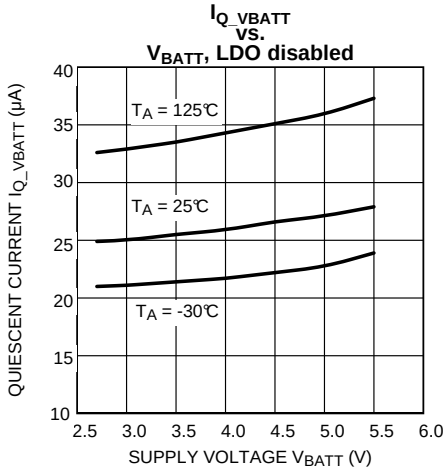


Figure 5.

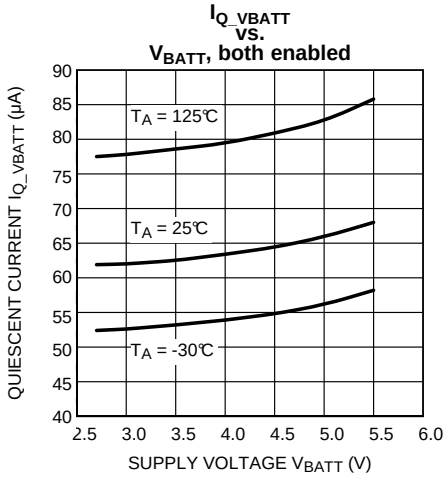


Figure 6.

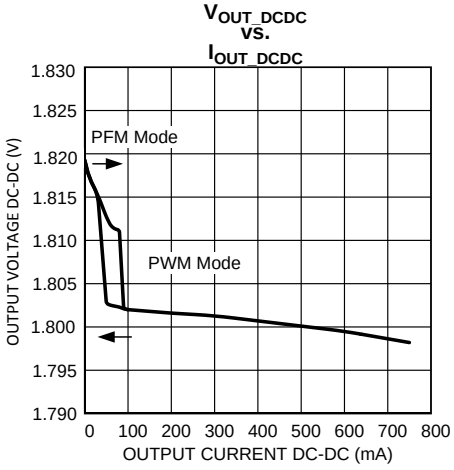


Figure 7.

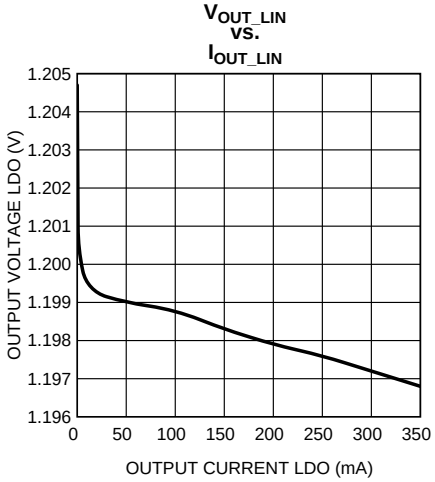


Figure 8.

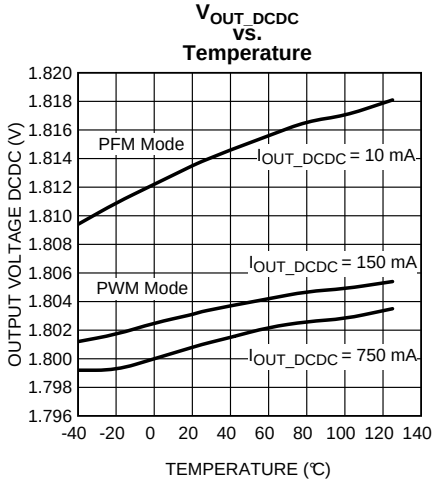


Figure 9.

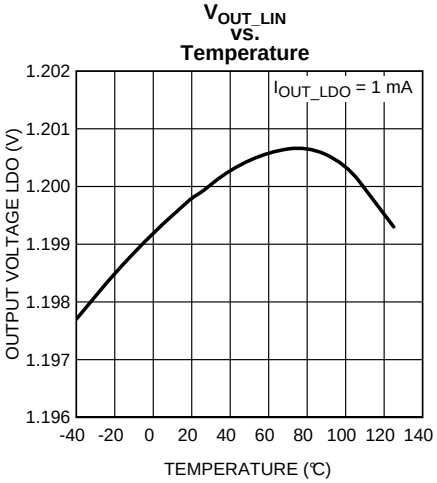


Figure 10.

Typical Performance Characteristics (continued)

Unless otherwise specified, typical application (post regulation), V_{BATT} = 3.6V, T_A = 25°C, enable pins tied to V_{BATT}, V_{OUT_DCDC} = 1.8V, V_{OUT_LIN} = 1.2V

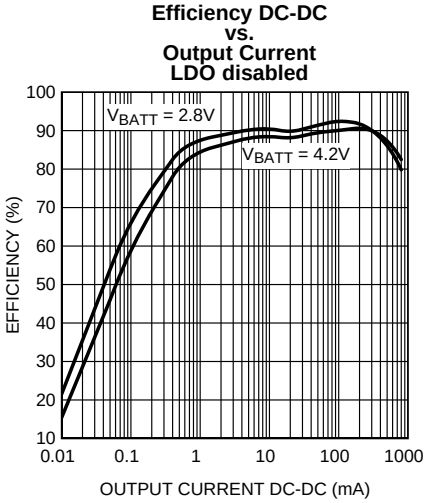


Figure 11.

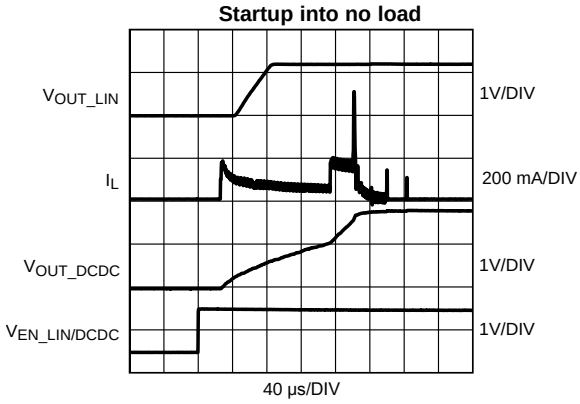


Figure 12.

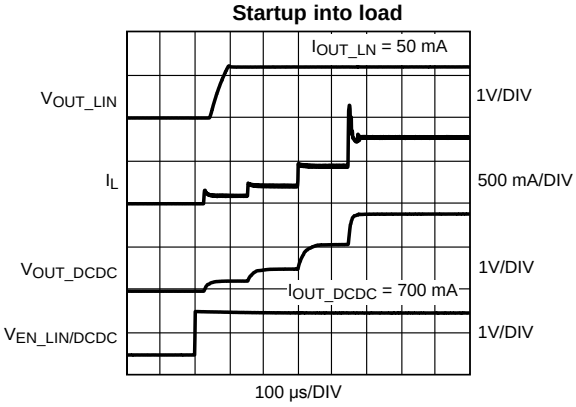


Figure 13.

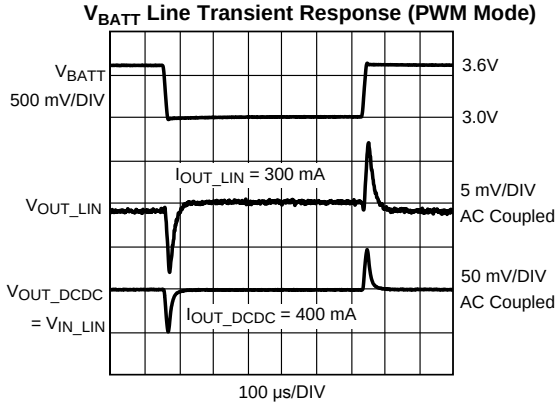


Figure 14.

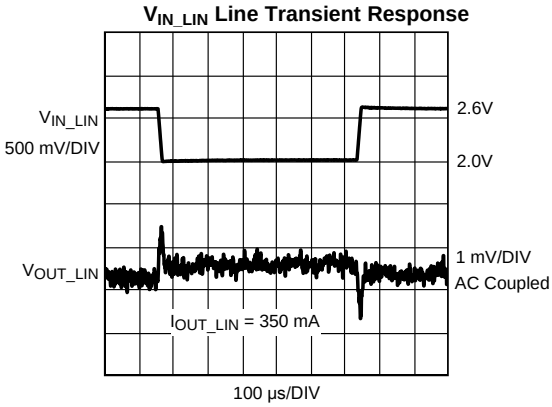


Figure 15.

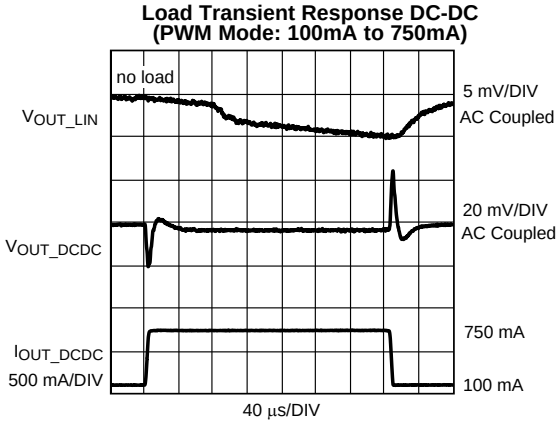


Figure 16.

Typical Performance Characteristics (continued)

Unless otherwise specified, typical application (post regulation), V_{BATT} = 3.6V, T_A = 25°C, enable pins tied to V_{BATT}, V_{OUT_DCDC} = 1.8V, V_{OUT_LIN} = 1.2V

Load Transient Response DC-DC (PFM Mode: 1mA to 50mA)

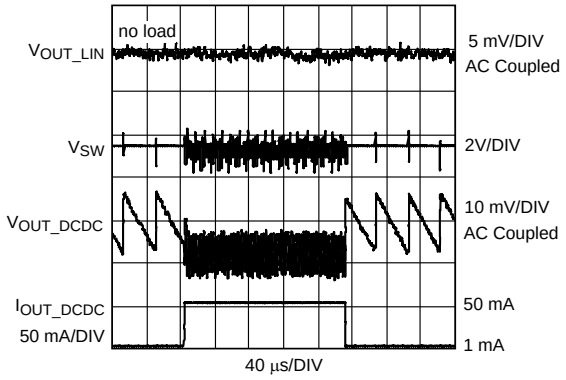


Figure 17.

Load Transient Response Linear Regulator 0mA to 350mA

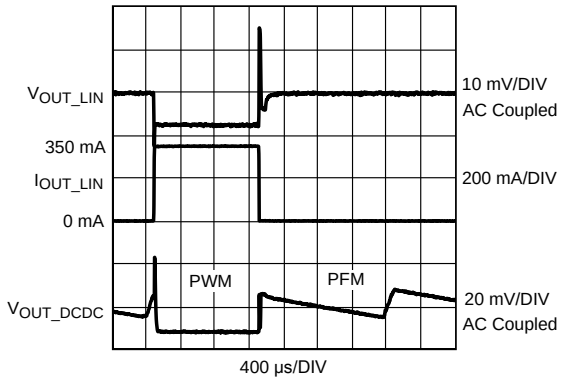


Figure 18.

Mode Change by Load Transients (PFM to PWM)

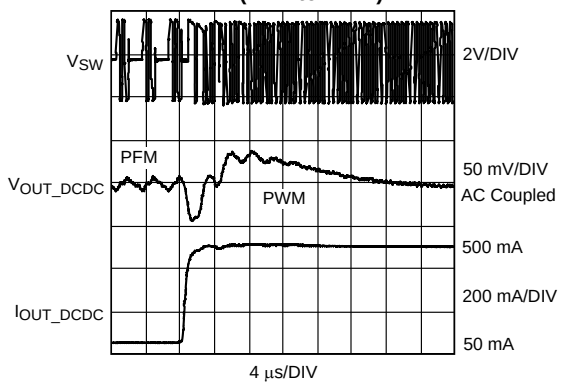


Figure 19.

Mode Change by Load Transients (PWM to PFM)

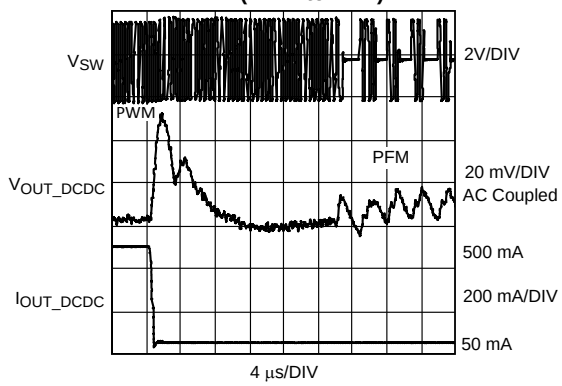


Figure 20.

Output Ripple PFM Mode

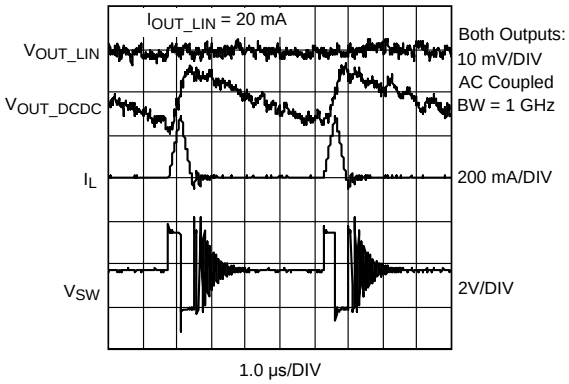


Figure 21.

Output Ripple PWM Mode

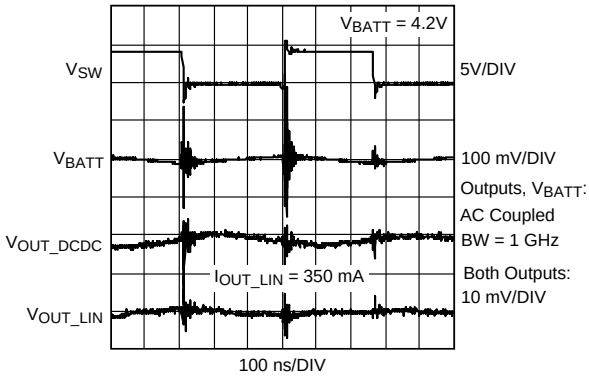


Figure 22.

OPERATION DESCRIPTION

DEVICE INFORMATION

The LM3687 incorporates a high efficiency synchronous switching step-down DC-DC converter and a very low dropout linear regulator.

The DC-DC converter delivers a constant voltage from a single Li- Ion battery and input voltage rails from 2.7V to 5.5V to portable devices such as cell phones and PDAs. Using a voltage mode architecture with synchronous rectification, it has the ability to deliver up to 750mA load current depending on the input voltage, output voltage, ambient temperature and the inductor chosen.

The linear regulator delivers a constant voltage biased from V_{IN_LIN} power input - typically the output voltage of the DC-DC converter is used (post regulation) - with a maximum load current of 350mA.

Two enable pins allow the independent control of the two outputs. Shutdown mode turns off the device, offering the lowest current consumption ($I_{SHUTDOWN}$ = 0.1 µA typ).

Besides the shutdown feature, for the DC-DC converter there are two more modes of operation depending on the current required:

- PWM Operation, and
- PFM Operation.

The device operates in PWM mode at load current of approximately 80 mA or higher. Lighter load currents cause the device to automatically switch into PFM for reduced current consumption (I_{Q_VBATT} = 27 µA typ) and a longer battery life.

Additional features include soft-start, startup mode of the linear regulator, under-voltage protection, current overload protection, and over-temperature protection.

As shown in Typical Application Circuit, only four external surface-mount components are required for implementation -one inductor and three ceramic capacitors.

An internal reference generates 1.8V biasing an internal resistive divider to create a reference voltage range from 0.45V to 1.8V (in 50mV steps) for the linear regulator (depending on the output voltage setting defined in the fab) and the 0.5V reference used for the DC-DC converter.

The Under-voltage lockout feature enables the device to startup once V_{BATT} has reached 2.65V typically and turns the device off if V_{BATT} drops below 2.41V typically.

NOTE

In the case that the DC-DC converter is switched off while the Linear Regulator is still enabled, an overshoot of up to 150mV might appear at V_{OUT_LIN}, if all of the following conditions are present:

- high V_{BATT}
- down ramp on V_{IN_LIN} of greater than 100mV/16us taking the Linear Regulator into dropout
- light load on Linear Regulator

DC-DC CONVERTER OPERATION

During the first part of each switching cycle, the control block in the LM3687 turns on the internal PFET switch. This allows current to flow from the input V_{BATT} through the switch pin SW and the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of (V_{BATT} - V_{OUT_DCDC}) / L, by storing energy in the magnetic field.

During the second part of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of (- V_{OUT_DCDC} / L).

The output filter stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load.

The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at the SW pin to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

PWM Operation

During PWM (Pulse Width Modulation) operation the converter operates as a voltage-mode controller with input voltage feed forward. This allows the converter to achieve good load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependency, feed forward inversely proportional to the input voltage is introduced.

While in PWM mode, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. At the beginning of each clock cycle the PFET switch is turned on and the inductor current ramps up until the duty-cycle-comparator trips and the control logic turns off the switch. The current limit comparator can also turn off the switch in case the current limit of the PFET is exceeded. Then the NFET switch is turned on and the inductor current ramps down. The next cycle is initiated by the clock turning off the NFET and turning on the PFET.

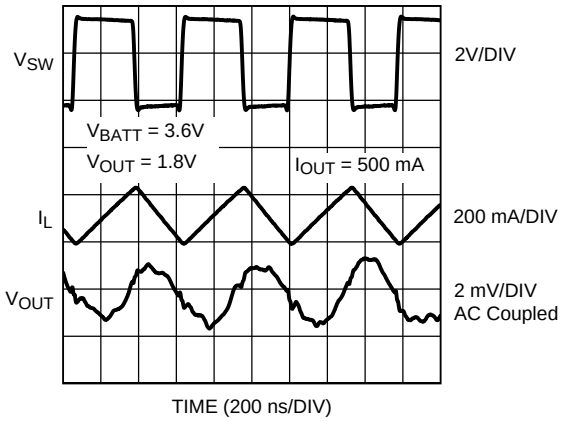


Figure 23. Typical PWM Operation

Internal Synchronous Rectification

While in PWM mode, the DC-DC converter uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

Current Limiting

A current limit feature allows the LM3687 to protect itself and external components during overload conditions. PWM mode implements current limiting using an internal comparator that trips at 1172 mA (typ). If the output is shorted to ground the device enters a timed current limit mode where the NFET is turned on for a longer duration until the inductor current falls below a low threshold. This allows the inductor current more time to decay, thereby preventing runaway.

PFM Operation

At very light load, the DC-DC converter enters PFM mode and operates with reduced switching frequency and supply current to maintain high efficiency. The part automatically transitions into PFM mode when either of two conditions occurs for a duration of 32 or more clock cycles:

- The NFET current reaches zero.
- The peak PMOS switch current drops below the I_{MODE} level, (typically $I_{MODE} < 36mA + V_{BATT} / 35\Omega$).

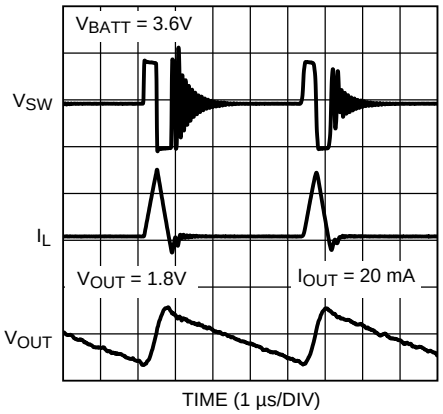


Figure 24. Typical PFM Operation

During PFM operation, the DC-DC converter positions the output voltage slightly higher than the nominal output voltage during PWM operation, allowing additional headroom for voltage drop during a load transient from light to heavy load. The PFM comparators sense the output voltage via the feedback pin and control the switching of the output FETs such that the output voltage ramps between ~0.6% and ~1.7% above the nominal PWM output voltage. If the output voltage is below the 'high' PFM comparator threshold, the PMOS power switch is turned on. It remains on until the output voltage reaches the 'high' PFM threshold or the peak current exceeds the I_{PFM} level set for PFM mode. The typical peak current in PFM mode is: I_{PFM} = 134mA + V_{BATT} / 23Ω.

Once the PMOS power switch is turned off, the NMOS power switch is turned on until the inductor current ramps to zero. When the NMOS zero-current condition is detected, the NMOS power switch is turned off. If the output voltage is below the 'high' PFM comparator threshold (see Figure 25), the PMOS switch is again turned on and the cycle is repeated until the output reaches the desired level. Once the output reaches the 'high' PFM threshold, the NMOS switch is turned on briefly to ramp the inductor current to zero and then both output switches are turned off and the part enters an extremely low power mode. Quiescent supply current during this 'sleep' mode is 27µA (typ), which allows the part to achieve high efficiency under extremely light load conditions.

If the load current should increase during PFM mode (see Figure 25) causing the output voltage to fall below the 'low2' PFM threshold, the part will automatically transition into fixed-frequency PWM mode.

When V_{BATT} =2.7V the part transitions from PWM to PFM mode at ~30mA output current and from PFM to PWM mode at ~80mA , when V_{BATT}=3.6V, PWM to PFM transition happens at ~60mA and PFM to PWM transition happens at ~90mA, when V_{BATT} =5.5V, PWM to PFM transition happens at ~100mA and PFM to PWM transition happens at ~125mA.

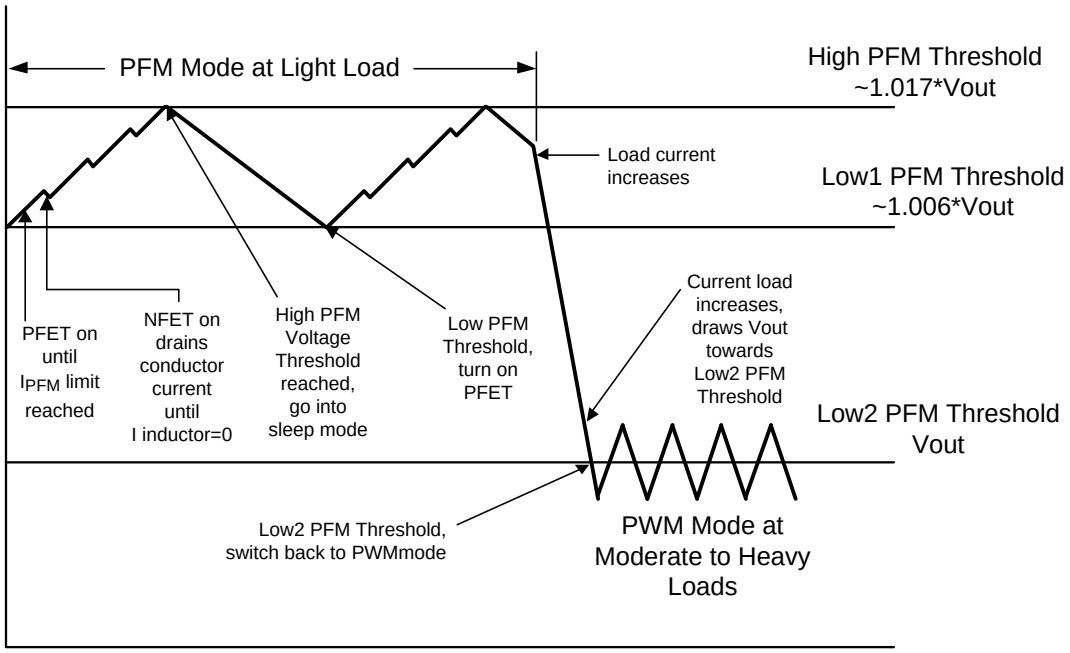


Figure 25. Operation in PFM Mode and Transfer to PWM Mode

Soft Start

The DC-DC converter has a soft-start circuit that limits in-rush current during start-up. During start-up the switch current limit is increased in steps. Soft start is activated only if EN_DCDC goes from logic low to logic high after V_{BATT} reaches 2.7V. Soft start is implemented by increasing switch current limit in steps of 85mA, 170mA, 340mA and 1120mA (typical switch current limit). The start-up time thereby depends on the output capacitor and load current demanded at start-up. Typical start-up times with a 10µF output capacitor and 750mA load is 455 µs and with 1mA load is 180µs.

LINEAR REGULATOR OPERATION

In the typical post regulation application the power input voltage V_{IN_LIN} for the linear regulator is generated by the DC-DC converter. Using a buck converter to reduce the battery voltage to a lower input voltage for the linear regulator translates to higher efficiency and lower power dissipation.

It's also possible to operate the linear regulator independent of the DC-DC converter output voltage either from V_{BATT} or a different source. In this case it's important that **V_{IN_LIN} does not exceed V_{BATT} at any time**. V_{BATT} is needed for the linear regulator as well, it supplies internal circuitry.

An input capacitor of 1µF at V_{IN_LIN} needs to be added if no other filter or bypass capacitor is present in the V_{IN_LIN} path.

Startup Mode

If the linear regulator is enabled (logic high at EN_LIN), the power input voltage V_{IN_LIN} is continuously compared to the nominal output voltage of the linear regulator V_{OUT_LIN}.

If $V_{IN\_LIN} > V_{OUT\_LIN(NOM)}$ + 200mV the main regulator is active, offering a rated output current of 350mA and supplied by V_{IN_LIN}.

If $V_{IN\_LIN} < V_{OUT\_LIN(NOM)}$ + 100mV the startup LDO is active, providing a reduced rated output current of 50mA typical, supplied by V_{BATT}. Between these two levels a hystersis of 100mV is established. This feature is intended to enable the supply of loads at the output of the linear regulator while the output of the DC-DC converter is still ramping up.

In the typical post regulation application with both enable pins connected to V_{BATT} and V_{IN_LIN} supplied by V_{OUT_DCDC} as an example, the linear regulator turns on in startup mode (I_{MAX} = 50mA) supplied out of V_{BATT}. At the same time the DC-DC converter turns on, but V_{OUT_DCDC} startup time is longer. The internal signal 'Mode Switch' monitors the voltage level of V_{IN_LIN}. Once V_{IN_LIN} > $V_{OUT\_LIN(NOM)}$ + 200mV, the linear regulator changes to normal mode (I_{MAX} = 350mA) supplied out of V_{IN_LIN}. If V_{IN_LIN} drops below $V_{OUT\_LIN(NOM)}$ + 100mV the linear regulator switches back to startup mode.

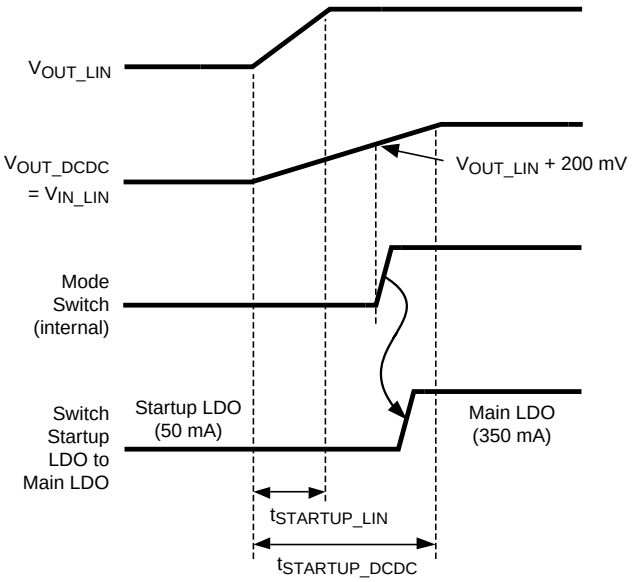


Figure 26. Startup Sequence, V_{EN_DCDC} = V_{EN_LIN} = V_{BATT}

Current Limiting

The LM3687 incorporates also a current limit feature for the linear regulator to protect itself and external components during overload conditions at V_{OUT_LIN}. In the event of a peak over-current condition at V_{OUT_LIN} the output current through the NFET pass device will be limited.

Application Hints

INDUCTOR SELECTION

There are two main considerations when choosing an inductor; the inductor should not saturate, and the inductor current ripple should be small enough to achieve the desired output voltage ripple. Different saturation current rating specifications are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25°C. However, ratings at the maximum ambient temperature of application should be requested from the manufacturer. **The minimum value of inductance to guarantee good performance is 1.76µH at I_{LIM} (typ) dc current over the ambient temperature range.** Shielded inductors radiate less noise and should be preferred. There are two methods to choose the inductor saturation current rating.

Method 1

The saturation current should be greater than the sum of the maximum load current and the worst case average to peak inductor current. This can be written as:

$I_{SAT} > I_{OUT\_DCDC\_MAX} + I_{RIPPLE}$ (1)

where

$I_{SAT} > I_{OUTMAX} + I_{RIPPLE}$

where $I_{RIPPLE} = \left(\frac{V_{BATT} - V_{OUT}}{2 \times L}\right) x \left(\frac{V_{OUT}}{V_{BATT}}\right) x \left(\frac{1}{f}\right)$

where

- I_{RIPPLE}: average to peak inductor current
- $I_{OUT\_DCDCMAX}$: maximum load current (750mA)
- V_{BATT}: maximum input voltage in application
- L: minimum inductor value including worst case tolerances (30% drop can be considered for method 1)
- f: minimum switching frequency (1.3MHz) (2)

Method 2

A more conservative and recommended approach is to choose an inductor that has a saturation current rating greater than the maximum current limit of 1380mA.

A 2.2 µH inductor with a saturation current rating of at least 1380mA is recommended for most applications. The inductor's resistance should be less than 0.3Ω for good efficiency. Table 1 lists suggested inductors and suppliers. For low-cost applications, an unshielded bobbin inductor could be considered. For noise critical applications, a toroidal or shielded- bobbin inductor should be used. A good practice is to lay out the board with overlapping footprints of both types for design flexibility. This allows substitution of a low-noise shielded inductor, in the event that noise from low-cost bobbin models is unacceptable.

Table 1. Suggested Inductors and their Suppliers

Model	Vendor	Dimensions LxWxH (mm)	DCR (max)
NR3015T2R2M	Taiyo Yuden	3.0 x 3.0 x 1.5	72mΩ
LPS3015-222ML	Coilcraft	3.0 x 3.0 x 1.5	110mΩ
DO3314-222MX	Coilcraft	3.3 x 3.3 x 1.4	200mΩ

EXTERNAL CAPACITORS

As is common with most regulators, the LM3687 requires external capacitors to ensure stable operation. The LM3687 is specifically designed for portable applications requiring minimum board space and the smallest size components. These capacitors must be correctly selected for good performance.

INPUT CAPACITOR SELECTION

V_{BATT}

A ceramic input capacitor of 4.7 µF, 6.3V is sufficient for most applications. Place the input capacitor as close as possible to the V_{BATT} pin of the device. A larger value may be used for improved input voltage filtering. Use X7R or X5R types; do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. The minimum input capacitance to guarantee good performance is 2.2µF at 3V dc bias; 1.5µF at 5V dc bias including tolerances and over ambient temperature range. The input filter capacitor supplies current to the PFET switch of the LM3687 DC-DC converter in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low ESR provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select a capacitor with sufficient ripple current rating. The input current ripple can be calculated as:

$$I_{RMS} = I_{OUTMAX} \times \sqrt{\frac{V_{OUT}}{V_{BATT}} \times \left(1 - \frac{V_{OUT}}{V_{BATT}} + \frac{r^2}{12}\right)}$$

$$r = \frac{(V_{BATT} - V_{OUT}) \times V_{OUT}}{L \times f \times I_{OUTMAX} \times V_{BATT}}$$

The worst case is when $V_{BATT} = 2 \times V_{OUT}$ (3)

V_{IN_LIN}

If the linear regulator is used as post regulation no additional capacitor is needed at V_{IN_LIN} as the output filter capacitor of the DC-DC converter is close by and therefore sufficient.

In case of independent use, a 1.0µF ceramic capacitor is recommended at V_{IN_LIN} if no other filter capacitor is present in the V_{IN_LIN} supply path. This capacitor must be located a distance of not more than 1 cm from the V_{IN_LIN} input pin and returned to a clean analogue ground. Any good quality ceramic, tantalum, or film capacitor may be used at this input.

Important

Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at this input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application.

The ESR (Equivalent Series Resistance) of this input capacitor should be in the range of 3mΩ to 300mΩ. The tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain ≥ 470nF over the entire operating temperature range.

OUTPUT CAPACITOR

V_{OUT_DCDC}

A ceramic output capacitor of 10 µF, 6.3V is sufficient for most applications. Use X7R or X5R types; do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. DC bias characteristics vary from manufacturer to manufacturer and dc bias curves should be requested from them as part of the capacitor selection process.

The minimum output capacitance to guarantee good performance is 5.75µF at 1.8V DC bias including tolerances and over ambient temperature range. The output filter capacitor smoothes out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions.

The output voltage ripple is caused by the charging and discharging of the output capacitor and by the R_{ESR} and can be calculated as:

Voltage peak-to-peak ripple due to capacitance can be expressed as follow:

$$V_{PP\text{-}C} = \frac{I_{RIPPLE}}{4 \times f \times C}$$ (4)

Voltage peak-to-peak ripple due to ESR can be expressed as follow:

$V_{PP\text{-}ESR} = (2 * I_{RIPPLE}) * R_{ESR}$

Because these two components are out of phase, the rms (root mean squared) value can be used to get an approximate value of peak-to-peak ripple. The peak-to-peak ripple voltage, rms value can be expressed as follow:

$$V_{PP\text{-}RMS} = \sqrt{V_{PP\text{-}C}^2 + V_{PP\text{-}ESR}^2}$$ (5)

Note that the output voltage ripple is dependent on the inductor current ripple and the equivalent series resistance of the output capacitor (R_{ESR}). The R_{ESR} is frequency dependent (as well as temperature dependent); make sure the value used for calculations is at the switching frequency of the part.

V_{OUT_LIN}

The linear regulator is designed specifically to work with very small ceramic output capacitors. A ceramic capacitor (dielectric types X7R, Z5U, or Y5V) in the 2.2µF range (up to 10µF) and with an ESR between 3mΩ to 300mΩ is suitable as C_{OUT_LIN} in the LM3687 application circuit.

This capacitor must be located a distance of not more than 1cm from the V_{OUT_LIN} pin and returned to a clean analogue ground. It is also possible to use tantalum or film capacitors at the device output, V_{OUT_LIN}, but these are not as attractive for reasons of size and cost (see CAPACITOR CHARACTERISTICS).

CAPACITOR CHARACTERISTICS

The LM3687 is designed to work with ceramic capacitors on the outputs to take advantage of the benefits they offer. For capacitance values in the range of 1µF to 4.7µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1µF ceramic capacitor is in the range of 3mΩ to 40mΩ, which easily meets the ESR requirement for stability for the LM3687.

For both input and output capacitors, careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly, depending on the operating conditions and capacitor type.

In particular, the output capacitor selection should take account of all the capacitor parameters, to ensure that the specification is met within the application. The capacitance can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size, with smaller sizes giving poorer performance figures in general. As an example, the graph below shows a comparison of different capacitor case sizes in a Capacitance vs. DC Bias plot. As shown in the graph, increasing the DC Bias condition can result in the capacitance value falling below the minimum recommended value. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions, as some capacitor sizes (e.g. 0402) may not be suitable in the actual application.

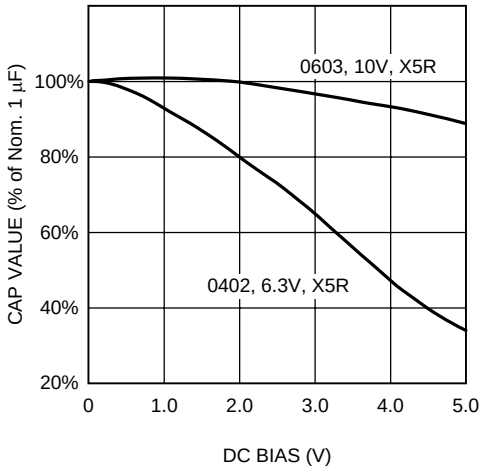


Figure 27. Graph Showing a Typical Variation In Capacitance vs. DC Bias

The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of -55°C to +125°C, will only vary the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of -55°C to +85°C. Many large value ceramic capacitors, larger than 1µF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C. Therefore X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1µF to 4.7µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to -40°C, so some guard band must be allowed. For the output capacitor of the DC-DC converter, please note that the output voltage ripple is dependent on the ESR of the output capacitor.

Table 2. Suggested Capacitors and their Suppliers

Capacitance / µF	Model	Voltage Rating	Vendor	Type	Case Size / Inch (mm)
10.0	C1608X5R0J106K	6.3V	TDK	Ceramic, X5R	0603 (1608)
4.7	C1608X5R1A475K	10V	TDK	Ceramic, X5R	0603 (1608)
2.2	C1608X5R1A225K	10V	TDK	Ceramic, X5R	0603 (1608)
1.0	C1005X5R1A105K	10V	TDK	Ceramic, X5R	0402 (1005)

POWER DISSIPATION AND DEVICE OPERATION

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die and ambient air.

As stated in Operating Ratings, the allowable power dissipation for the device in a given package can be calculated using the equation:

$$P_{D\_SYS} = (T_{J(MAX)} - T_A) / \theta_{JA} \quad (6)$$

For the LM3687 there are two different main sources contributing to the systems power dissipation (P_{D_SYS}): the DC-DC converter (P_{D_DCDC}) and the linear regulator (P_{D_LIN}). Neglecting switching losses and quiescent currents these two main contributors can be estimated by the following equations:

$$P_{D\_LIN} = (V_{IN\_LIN} - V_{OUT\_LIN}) * I_{OUT\_LIN} \quad (7)$$

$$P_{D\_DCDC} = I_{OUT\_DCDC}^2 * [(R_{DSON(P)} * D) + (R_{DSON(N)} * (1-D))]$$

where

- duty cycle $D = V_{OUT\_DCDC} / V_{BATT}$. (8)

As an example, assuming the typical post regulation application, the conversion from V_{BATT} = 3.6V to V_{OUT_DCDC} = 1.8V and further to V_{OUT_LIN} = 1.5V, at maximum load currents, results in following power dissipations:

$P_{D\_DCDC} = (0.75A)^2 * (0.38\Omega * 1.8V / 3.6V + 0.25\Omega * (1 - 1.8V / 3.6V)) = 177mW$ and

$P_{D\_LIN} = (1.8V - 1.5V) * 0.35A = 105mW$.

$P_{D\_SYS} = 282mW$.

With a θ_{JA} = 70°C/W for the DSBGA 9 package this P_{D_SYS} will cause a rise of the junction temperature T_J of:

$\Delta T_J = P_{D\_SYS} * \theta_{JA} = 20K$.

For the same conditions but the linear regulator biased from V_{BATT}, this results in a P_{D_LIN} of 735mW, P_{D_DCDC} = 50mW (because I_{OUT_DCDC} = 400mA) and therefore an increase of T_J of 55K.

As lower total power dissipation translates to higher efficiency this example highlights the advantage of the post regulation setup.

NO-LOAD STABILITY

Both outputs of the LM3687 will remain stable and in regulation with no external load. This is an important consideration in some circuits, for example CMOS RAM keep-alive applications.

ENABLE OPERATION

The outputs of LM3687 may be switched ON or OFF by a logic input at the Enable pins, V_{EN_DCDC} and V_{EN_LIN}. A logic high (related to V_{BATT}) at these pins will turn the outputs on (for information on startup sequence please refer to Operation Description).

When both enable pins are low, the outputs are off (pins SW and V_{OUT_LIN} are high impedance) and the device typically consumes 0.1µA.

If the application does not require the Enable switching feature, the enable pins should be tied to V_{BATT} to keep the outputs permanently on.

To ensure proper operation, the signal source used to drive the enable inputs must be able to swing above and below the specified turn-on/off voltage thresholds listed in Electrical Characteristics: Enable Pins (EN_DCDC, EN_LIN), V_{IL} and V_{IH}.

FAST TURN ON

For V_{OUT_LIN} fast turn-on is guaranteed by an optimized architecture allowing a fast ramp of the output voltage to reach the target voltage while the inrush current is controlled low at 120mA typical (for a C_{OUT} of 2.2µF; assuming V_{IN_LIN} is settled before enable happens).

SHORT-CIRCUIT PROTECTION

Both outputs of the LM3687 are short circuit protected and in the event of a peak over-current condition, the output current through the MOS transistors will be limited.

If the over-current condition exists for a longer time, the average power dissipation will increase depending on the input to output voltage differences until the thermal shutdown circuitry will turn off the MOS transistors.

Please refer to POWER DISSIPATION AND DEVICE OPERATION for calculations.

THERMAL-OVERLOAD PROTECTION

Thermal-Overload Protection limits the total power dissipation in the LM3687. When the junction temperature exceeds T_J = 160°C typ., the shutdown logic is triggered and the output MOS transistors are turned off, allowing the device to cool down. After the junction temperature dropped by 20°C (temperature hysteresis), the output MOS transistors are activated again. This results in a pulsed output voltage during continuous thermal-overload conditions.

As the DC-DC converter in PFM mode (low load current) does not contribute significantly to an increase of T_J, it is not turned off in case a thermal shutdown is initiated. If the DC-DC converter operates in PWM mode, the PMOS is turned off in case of a thermal shutdown.

The Thermal-Overload Protection is designed to protect the LM3687 in the event of a fault condition. For normal, continuous operation, do not exceed the absolute maximum junction temperature rating of T_J = +150°C (see Absolute Maximum Ratings).

REVERSE CURRENT PATH

There are two body diodes at the switch pin of the DC-DC converter. It is not allowed to pull the switch pin above V_{BATT} or below PGND by more than 200mV.

On the main linear regulator there is a bulk switching feature in place preventing the parasitic diode structures from conducting current. This feature is only active as long as any of the regulators is enabled.

For the startup LDO, V_{OUT_LIN} must not exceed V_{BATT}.

EVALUATION BOARDS

For availability of evaluation boards please refer to the Product Folder of LM3687 at www.ti.com. For information regarding evaluation boards, please refer to Application Note: AN-1647 SNVA249.

DSBGA PACKAGE ASSEMBLY AND USE

Use of the DSBGA package requires specialized board layout, precision mounting and careful re-flow techniques, as detailed in Application Note 1112 SNVA009. Refer to the section "Surface Mount Assembly Considerations". For best results in assembly, alignment ordinals on the PC board should be used to facilitate placement of the device. The pad style used with DSBGA package must be the NSMD (non-solder mask defined) type. This means that the solder-mask opening is larger than the pad size. This prevents a lip that otherwise forms if the soldermask and pad overlap, from holding the device off the surface of the board and interfering with mounting. See Application Note 1112 SNVA009 for specific instructions how to do this. The 9-Bump package used for LM3687 has 300 micron solder balls and requires 275 micron pads for mounting on the circuit board. The trace to each pad should enter the pad with a 90° entry angle to prevent debris from being caught in deep corners. Initially, the trace to each pad should not exceed 183 micron, for a section approximately 183 micron long or longer, as a thermal relief. Then each trace should neck up or down to its optimal width. The important criteria is symmetry. This ensures the solder bumps on the LM3687 re-flow evenly and that the device solders level to the board. In particular, special attention must be paid to the pads for bumps A1, A2, C1 and B3, because PGND, SGND, V_{BATT} and V_{IN_LIN} are typically connected to large copper planes, inadequate thermal relief can result in late or inadequate re-flow of these bumps. The DSBGA package is optimized for the smallest possible size in applications with red or infrared opaque cases. Because the DSBGA package lacks the plastic encapsulation characteristic of larger devices, it is vulnerable to light. Backside metallization and/or epoxy coating, along with frontside shading by the printed circuit board, reduce this sensitivity. However, the package has exposed die edges. In particular, DSBGA devices are sensitive to light, in the red and infrared range, shining on the package's exposed die edges.

BOARD LAYOUT CONSIDERATIONS

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter IC, resulting in poor regulation or instability. Good layout for the LM3687 can be implemented by following a few simple design rules below. Refer to Figure 28 for top layer board layout.

1. Place the LM3687, inductor and filter capacitor close together and make the traces short. The traces between these components carry relatively high switching currents and act as antennas. Following this rule reduces radiated noise. Special care must be given to place the input filter capacitor very close to the V_{BATT} and PGND pin. Place the output capacitor of the linear regulator close to the output pin.
2. Arrange the components so that the switching current loops curl in the same direction. During the first half of each cycle, current flows from the input filter capacitor through the LM3687 and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground through the LM3687 by the inductor to the output filter capacitor and then back through ground forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
3. Connect the ground pins of the LM3687 and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then, connect this to the ground-plane (if one is used) with several vias. This reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the LM3687 by giving it a low impedance ground connection. Route SGND to the ground-plane by a separate trace.
4. Use wide traces between the power components and for power connections to the DC-DC converter circuit. This reduces voltage errors caused by resistive losses across the traces.
5. Route noise sensitive traces, such as the voltage feedback path (FB_DCDC), away from noisy traces between the power components. The voltage feedback trace must remain close to the LM3687 circuit and should be direct but should be routed opposite to noisy components. This reduces EMI radiated onto the DC-DC converter's own voltage feedback trace. A good approach is to route the feedback trace on another layer and to have a ground plane between the top layer and layer on which the feedback trace is routed.
6. Place noise sensitive circuitry, such as radio IF blocks, away from the DC-DC converter, CMOS digital blocks and other noisy circuitry. Interference with noise sensitive circuitry in the system can be reduced through distance.

In mobile phones, for example, a common practice is to place the DC-DC converter on one corner of the board, arrange the CMOS digital circuitry around it (since this also generates noise), and then place sensitive preamplifiers and IF stages on the diagonally opposing corner. Often, the sensitive circuitry is shielded with a metal pan and power to it is postregulated to reduce conducted noise, a good field of application for the on-chip low-dropout linear regulator.

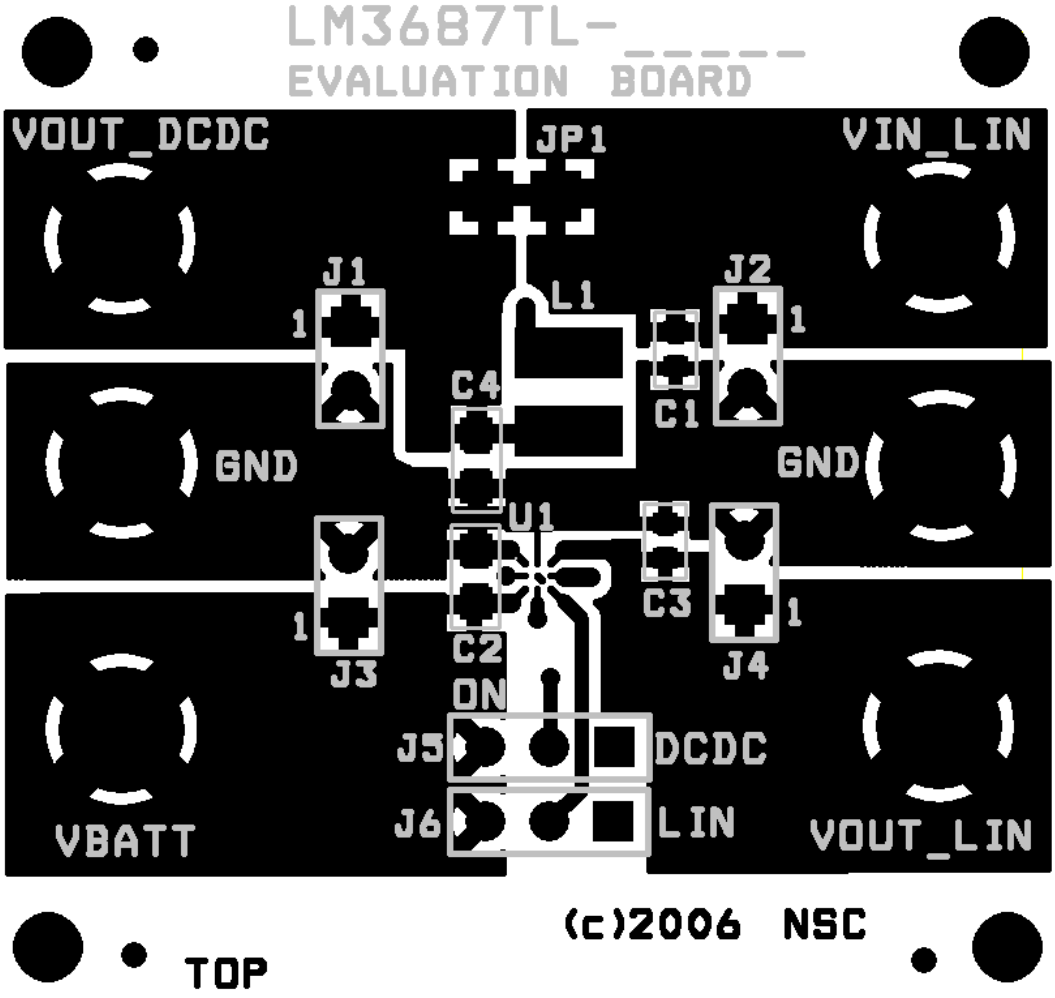


Figure 28. Top Layer Board Layout

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	23

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3687TL-1812/NOPB	ACTIVE	DSBGA	YZR	9	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM		SB	Samples
LM3687TL-1815/NOPB	ACTIVE	DSBGA	YZR	9	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-30 to 125	S9	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

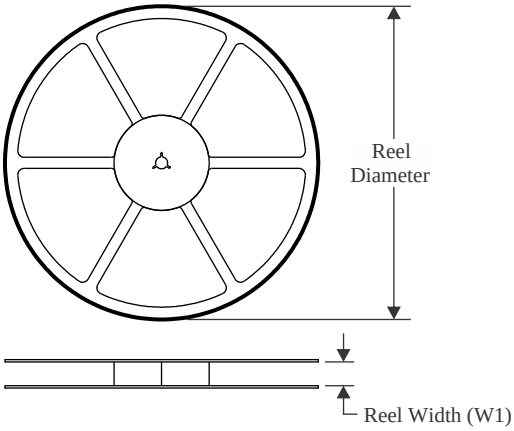
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

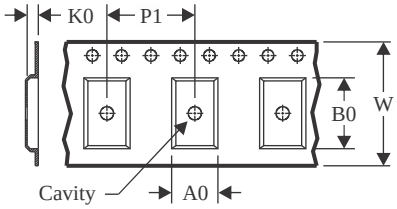
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

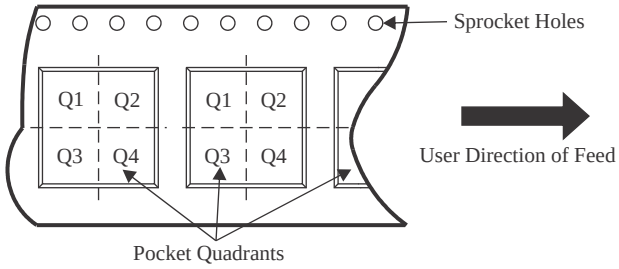


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

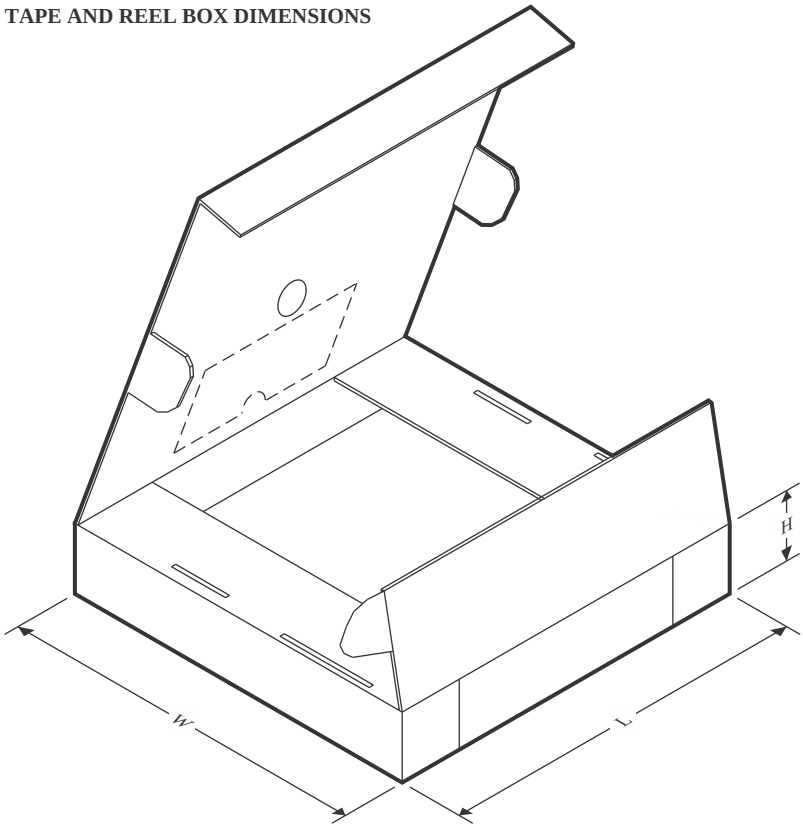
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3687TL-1812/NOPB	DSBGA	YZR	9	250	178.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1
LM3687TL-1815/NOPB	DSBGA	YZR	9	250	178.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1

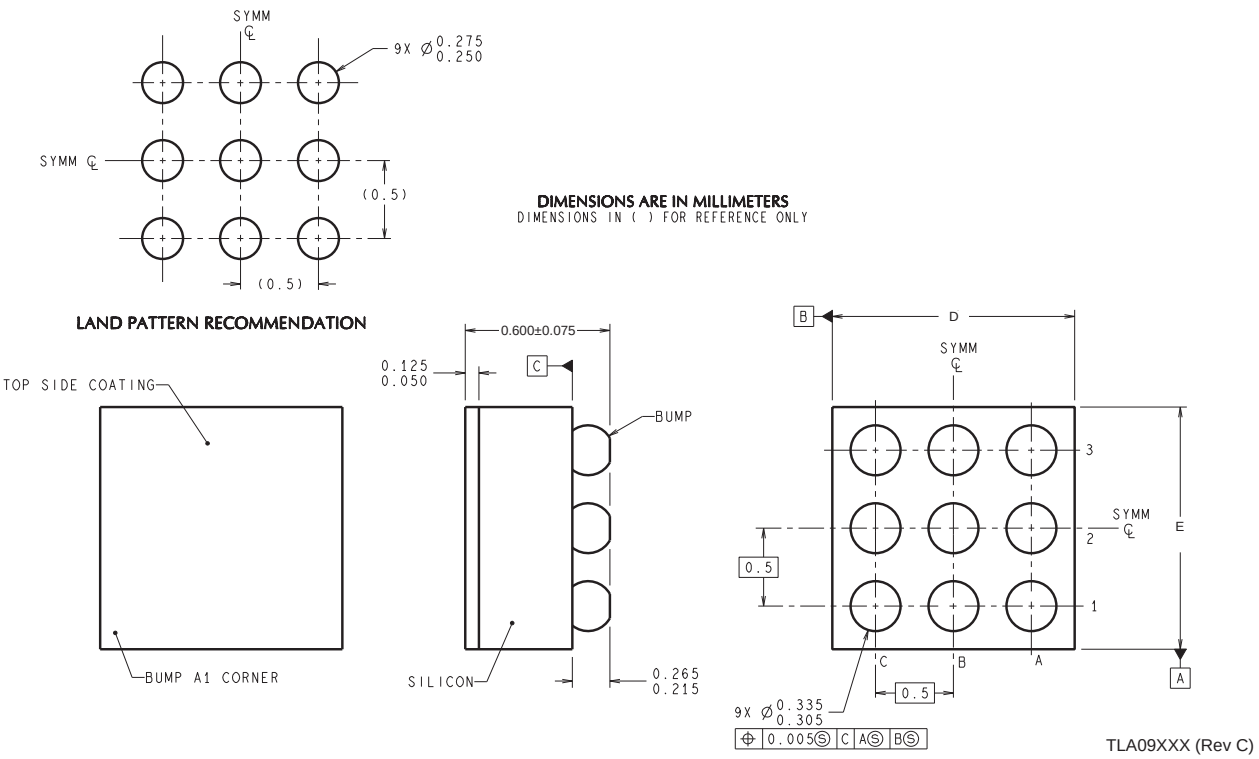
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3687TL-1812/NOPB	DSBGA	YZR	9	250	208.0	191.0	35.0
LM3687TL-1815/NOPB	DSBGA	YZR	9	250	208.0	191.0	35.0

YZR0009



D: Max = 1.574 mm, Min =1.514 mm

E: Max = 1.574 mm, Min =1.514 mm

4215046/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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