LM7332 Dual Rail-to-Rail Input and Output 30-V, Wide Voltage Range, High Output, Operational Amplifier

1 Features

- V_S = ±15 V, T_A = 25°C, Typical Values Unless Specified
- Wide Supply Voltage Range 2.5 V to 32 V
- Wide Input Common Mode Voltage 0.3 V Beyond Rails
- Output Short Circuit Current > 100 mA
- High Output Current (1 V from Rails) ±70 mA
- GBWP 21 MHz
- Slew Rate 15.2 V/µs
- Capacitive Load Tolerance Unlimited
- Total Supply Current 2 mA
- Temperature Range −40°C to +125°C
- Tested at −40°C, +125°C, and +25°C at 5 V, ±5 V, ±15 V

2 Applications

- MOSFET and Power Transistor Driver
- Replaces Discrete Transistors in High Current Output Circuits
- Instrumentation 4–20 mA Current Loops
- Analog Data Transmission
- Multiple Voltage Power Supplies and Battery Chargers
- High-Side and Low-Side Current Sensing
- Bridge and Sensor Driving
- Digital-to-Analog Converter Output

3 Description

The LM7332 device is a dual rail-to-rail input and output amplifier with a wide operating temperature range (−40°C to +125°C) that meets the needs of automotive, industrial, and power supply applications. The LM7332 has an output current of 100 mA, which is higher than that of most monolithic operational amplifiers. Circuit designs with high output current requirements often require discrete transistors because many operational amplifiers have low current output. The LM7332 has enough current output to drive many loads directly, saving the cost and space of the discrete transistors.

The exceptionally wide operating supply voltage range of 2.5 V to 32 V alleviates any concerns over functionality under extreme conditions and offers flexibility of use in a multitude of applications. Most parameters of this device are insensitive to power supply variations; this design enhancement is another step in simplifying usage. Greater than rail-to-rail input common mode voltage range allows operation in many applications, including high-side and low-side sensing, without exceeding the input range.

The LM7332 can drive unlimited capacitive loads without oscillations.

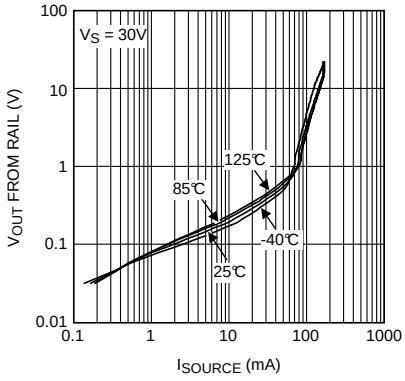
The LM7332 is offered in the 8-pin VSSOP and SOIC packages.

Device Information(1)

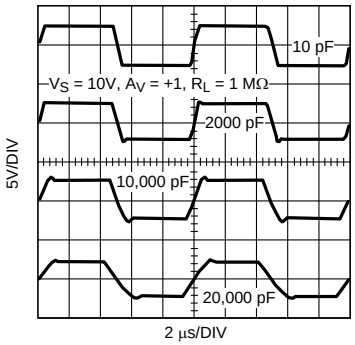
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM7332	VSSOP (8)	3.00 mm × 3.00 mm
	SOIC (8)	3.91 mm × 4.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Output Swing vs Sourcing Current



Large Signal Step Response for Various Capacitive Loads



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2013) to Revision B **Page**

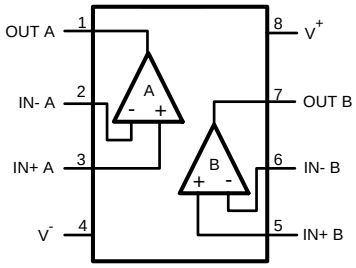
- Added *Device Information, ESD Ratings* and *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1

Changes from Original (March 2013) to Revision A **Page**

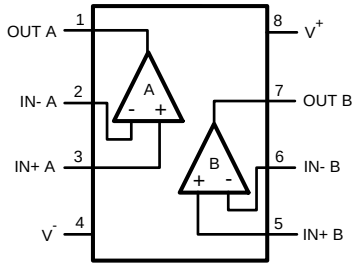
- Changed layout of National Data Sheet to TI format 20

5 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View



D Package
8-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN+ A	3	I	Noninverting Input for Amplifier A
IN– A	2	I	Inverting Input for Amplifier A
IN+ B	5	I	Noninverting Input for Amplifier B
IN– B	6	I	Inverting Input for Amplifier AB
OUT A	1	O	Output for Amplifier A
OUT B	7	O	Output for Amplifier B
V^+	8	P	Positive Supply
V^-	4	P	Negative Supply

6 Specifications

6.1 Absolute Maximum Ratings

See (1)(2)

		MIN	MAX	UNIT
V_{IN} differential			±10	V
Output short-circuit duration		See (3)(4)		
Supply voltage ($V_S = V^+ – V^–$)			35	V
Voltage at input/output pins		$V^+ + 0.3$	$V^– – 0.3$	V
Junction temperature(5)			150	°C
Soldering information	Infrared or convection (20 sec.)		235	°C
	Wave soldering (10 sec.)		260	°C
Storage temperature, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the TI Sales Office/Distributors for availability and specifications.
(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(4) Short-circuit test is a momentary test. Output short circuit duration is infinite for $V_S \leq 6$ V at room temperature and below. For $V_S > 6$ V, allowable short circuit duration is 1.5 ms.
(5) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)(2)	±2000	V
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Supply voltage ($V_S = V^+ – V^–$)	2.5	32	V
Temperature range(1)	−40	125	°C

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

6.4 Thermal Information

THERMAL METRIC(1)		LM7332		UNIT
		DGK (VSSOP)	D (SOIC)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	161.1	109.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55	55.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	80.5	49.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.5	10.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	79.2	48.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

6.5 5-V Electrical Characteristics

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = 0.5 V, V_O = 2.5 V, and R_L > 1 MΩ to 2.5 V.(1)

PARAMETER		TEST CONDITIONS	MIN (2)	TYP (3)	MAX (2)	UNIT
V_{OS}	Input offset voltage	V_{CM} = 0.5 V and V_{CM} = 4.5 V	−4	±1.6	4	mV
		At the temperature extremes	–5		5	
TC V_{OS}	Input offset voltage temperature drift	V_{CM} = 0.5 V and V_{CM} = 4.5 V (4)		±2		µV/°C
I_B	Input bias current	See (5)	−2	±1	2	µA
		At the temperature extremes	−2.5		2.5	
I_{OS}	Input offset current			20	250	nA
		At the temperature extremes			300	
CMRR	Common-mode Rejection Ratio	0 V ≤ V_{CM} ≤ 3 V	67	80		dB
		At the temperature extremes	65			
		0 V ≤ V_{CM} ≤ 5 V	62	70		
		At the temperature extremes	60			
PSRR	Power supply Rejection Ratio	5 V ≤ V^+ ≤ 30 V	78	100		dB
		At the temperature extremes	74			
CMVR	Input common-mode Voltage Range	CMRR > 50 dB	5.1	−0.3	−0.1	V
		At the temperature extremes	5	5.3	0	
A_{VOL}	Large signal Voltage Gain	0.5 V ≤ V_O ≤ 4.5 V R_L = 10 kΩ to 2.5 V	70	77		dB
		At the temperature extremes	65			
V_O	Output swing high	R_L = 10 kΩ to 2.5 V V_{ID} = 100 mV		60	150	mV from either rail
		At the temperature extremes			200	
		R_L = 2 kΩ to 2.5 V V_{ID} = 100 mV		100	300	
		At the temperature extremes			350	
	Output swing low	R_L = 10 kΩ to 2.5 V V_{ID} = −100 mV		5	150	
		At the temperature extremes			200	
		R_L = 2 kΩ to 2.5 V V_{ID} = −100 mV		20	300	
		At the temperature extremes			350	
I_{SC}	Output short circuit current	Sourcing from V^+, V_{ID} = 200 mV(6)	60	90		mA
		Sinking to V^-, V_{ID} = –200 mV(6)	60	90		
I_{OUT}	Output current	V_{ID} = ±200 mV, V_O = 1 V from rails		±55		mA
I_S	Total supply current	No Load, V_{CM} = 0.5 V		1.5	2.3	mA
		At the temperature extremes			2.6	
SR	Slew rate(7)	A_V = +1, V_I = 5-V Step, R_L = 1 MΩ, C_L = 10 pF		12		V/µs
f_u	Unity-gain frequency	R_L = 10 MΩ, C_L = 20 pF		7.5		MHz

(1) *Electrical Characteristics* values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) All limits are ensured by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Offset voltage temperature drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(5) Positive current corresponds to current flowing in the device.
(6) Short-circuit test is a momentary test. Output short circuit duration is infinite for V_S ≤ 6 V at room temperature and below. For V_S > 6 V, allowable short circuit duration is 1.5 ms.
(7) Slew rate is the slower of the rising and falling slew rates. Connected as a voltage follower.

5-V Electrical Characteristics (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = 0.5 V, V_O = 2.5 V, and R_L > 1 MΩ to 2.5 V.(1)

PARAMETER		TEST CONDITIONS	MIN (2)	TYP (3)	MAX (2)	UNIT
GBWP	Gain bandwidth product	f = 50 kHz		19.3		MHz
e_n	Input-referred voltage noise	f = 2 kHz		14.8		nV/√HZ
i_n	Input-referred current noise	f = 2 kHz		1.35		pA/√HZ
THD+N	Total harmonic distortion + noise	A_V = +2, R_L = 100 kΩ, f = 1 kHz, V_O = 4 V_{PP}		−84		dB
CT Rej.	Crosstalk rejection	f = 3 MHz, Driver R_L = 10 kΩ		68		dB

6.6 ±5-V Electrical Characteristics

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = +5 V, V^- = −5 V, V_{CM} = 0 V, V_O = 0 V, and R_L > 1 MΩ to 0 V.(1)

PARAMETER		TEST CONDITIONS	MIN (2)	TYP (3)	MAX (2)	UNIT
V_{OS}	Input offset voltage	V_{CM} = −4.5 V and V_{CM} = 4.5 V	−4	±1.6	4	mV
		At the temperature extremes	−5		5	
TC V_{OS}	Input offset voltage temperature drift	V_{CM} = −4.5 V and V_{CM} = 4.5 V (4)		±2		µV/°C
I_B	Input bias current	See (5)	−2	±1	2	µA
		At the temperature extremes	−2.5		2.5	
I_{OS}	Input offset current			20	250	nA
		At the temperature extremes			300	
CMRR	Common-mode rejection ratio	−5 V ≤ V_{CM} ≤ 3 V	74	88		dB
		At the temperature extremes	75			
		−5 V ≤ V_{CM} ≤ 5 V	70	74		
		At the temperature extremes	65			
PSRR	Power supply rejection ration	5 V ≤ V^+ ≤ 30 V, V_{CM} = −4.5 V	78	100		dB
		At the temperature extremes	74			
CMVR	Input common-mode voltage range	CMRR > 50 dB	5.1	–5.3	–5.1	V
		At the temperature extremes	5	5.3	–5.1	
A_{VOL}	Large signal voltage gain	−4 V ≤ V_O ≤ 4 V, R_L = 10 kΩ to 0 V	72	80		dB
		At the temperature extremes	70			

(1) *Electrical Characteristics* values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) All limits are ensured by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Offset voltage temperature drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(5) Positive current corresponds to current flowing in the device.

±5-V Electrical Characteristics (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = +5 V, V^- = −5 V, V_{CM} = 0 V, V_O = 0 V, and R_L > 1 MΩ to 0 V.(1)

PARAMETER		TEST CONDITIONS	MIN (2)	TYP (3)	MAX (2)	UNIT
V_O	Output swing high	R_L = 10 kΩ to 0 V V_{ID} = 100 mV		75	250	mV from either rail
		At the temperature extremes			300	
		R_L = 2 kΩ to 0 V V_{ID} = 100 mV		125	350	
		At the temperature extremes			400	
	Output swing low	R_L = 10 kΩ to 0 V V_{ID} = −100 mV		10	250	
		At the temperature extremes			300	
		R_L = 2 kΩ to 0V V_{ID} = −100 mV		30	350	
		At the temperature extremes			400	
I_{SC}	Output short circuit current	Sourcing from V^+, V_{ID} = 200 mV (6)	90	120		mA
		Sinking to V^-, V_{ID} = −200 mV (6)	90	100		
I_{OUT}	Output current	V_{ID} = ±200 mV, V_O = 1 V from rails		±65		mA
I_S	Total supply current	No Load, V_{CM} = −4.5 V		1.5	2.4	mA
		At the temperature extremes			2.6	
SR	Slew rate(7)	A_V = +1, V_I = 8-V step, R_L = 1 MΩ, C_L = 10 pF		13.2		V/µs
R_{OUT}	Close-loop output resistance	A_V = +1, f = 100 kHz		3		Ω
f_u	Unity-gain frequency	R_L = 10 MΩ, C_L = 20 pF		7.9		MHz
GBWP	Gain bandwidth product	f = 50 kHz		19.9		MHz
e_n	Input-referred voltage noise	f = 2 kHz		14.7		nV/√HZ
i_n	Input-referred current noise	f = 2 kHz		1.3		pA/√HZ
THD+N	Total harmonic distortion + noise	A_V = +2, R_L = 100 kΩ, f = 1 kHz V_O = 8 V_{PP}		−87		dB
CT Rej.	Crosstalk rejection	f = 3 MHz, driver R_L = 10 kΩ		68		dB

(6) Short-circuit test is a momentary test. Output short circuit duration is infinite for V_S ≤ 6 V at room temperature and below. For V_S > 6 V, allowable short circuit duration is 1.5 ms.
(7) Slew rate is the slower of the rising and falling slew rates. Connected as a voltage follower.

6.7 ±15-V Electrical Characteristics

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = +15 V, V^- = −15 V, V_{CM} = 0 V, V_O = 0 V, and R_L > 1 MΩ to 0 V.(1)

PARAMETER		TEST CONDITIONS	MIN (2)	TYP (3)	MAX (2)	UNIT
V_{OS}	Input offset voltage	V_{CM} = −14.5 V and V_{CM} = 14.5 V	−5	±2	5	mV
		At the temperature extremes	−6		6	
TC V_{OS}	Input offset voltage temperature drift	V_{CM} = −14.5 V and V_{CM} = 14.5 V (4)		±2		µV/°C
I_B	Input bias current	See (5)	−2	±1	2	µA
		At the temperature extremes	−2.5		2.5	

(1) *Electrical Characteristics* values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) All limits are ensured by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Offset voltage temperature drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(5) Positive current corresponds to current flowing in the device.

±15-V Electrical Characteristics (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = +15 V, V^- = −15 V, V_{CM} = 0 V, V_O = 0 V, and R_L > 1 MΩ to 0 V.(1)

PARAMETER		TEST CONDITIONS	MIN (2)	TYP (3)	MAX (2)	UNIT
I_{OS}	Input offset current			20	250	nA
		At the temperature extremes			300	
CMRR	Common-mode rejection ratio	−15 V ≤ V_{CM} ≤ 12 V	74	88		dB
		At the temperature extremes	74			
		−15 V ≤ V_{CM} ≤ 15 V	72	80		
		At the temperature extremes	72			
PSRR	Power supply rejection ratio	−10 V ≤ V^+ ≤ 15 V, V_{CM} = −14.5 V	78	100		dB
		At the temperature extremes	74			
CMVR	Input common-mode voltage range	CMRR > 50 dB	15.1	−15.3	−15.1	V
		At the temperature extremes	15	15.3	−15	
A_{VOL}	Large signal voltage gain	−14 V ≤ V_O ≤ 14 V R_L = 10 kΩ to 0 V	72	80		dB
		At the temperature extremes	70			
V_O	Output swing high	R_L = 10 kΩ to 0 V V_{ID} = 100 mV		100	350	mV from either rail
		At the temperature extremes			400	
		R_L = 2 kΩ to 0 V V_{ID} = 100 mV		200	550	
		At the temperature extremes			600	
	Output swing low	R_L = 10 kΩ to 0 V V_{ID} = −100 mV		20	450	
		At the temperature extremes			500	
		R_L = 2 kΩ to 0 V V_{ID} = −100 mV		25	550	
		At the temperature extremes			600	
I_{SC}	Output short circuit current	Sourcing from V^+, V_{ID} = 200 mV(6)		140		mA
		Sinking to V^-, V_{ID} = −200 mV (6)		140		
I_{OUT}	Output current	V_{ID} = ±200 mV, V_O = 1 V from rails		±70		mA
I_S	Total supply current	No Load, V_{CM} = −14.5 V		2	2.5	mA
		At the temperature extremes			3	
SR	Slew rate(7)	A_V = +1, V_I = 20-V Step, R_L = 1 MΩ, C_L = 10 pF		15.2		V/µs
f_u	Unity-gain frequency	R_L = 10 MΩ, C_L = 20 pF		9		MHz
GBWP	Gain bandwidth product	f = 50 kHz		21		MHz
e_n	Input-referred voltage noise	f = 2 kHz		15.5		nV/√HZ
i_n	Input-referred current noise	f = 2 kHz		1		pA/√HZ
THD+N	Total harmonic distortion plus noise	A_V = +2, R_L = 100 kΩ, f = 1 kHz V_O = 25 V_{PP}		−93		dB
CT Rej.	Crosstalk rejection	f = 3 MHz, Driver R_L = 10 kΩ		68		dB

(6) Short-circuit test is a momentary test. Output short circuit duration is infinite for V_S ≤ 6 V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5 ms.
(7) Slew rate is the slower of the rising and falling slew rates. Connected as a voltage follower.

6.8 Typical Characteristics

Unless otherwise specified, T_A = 25°C.

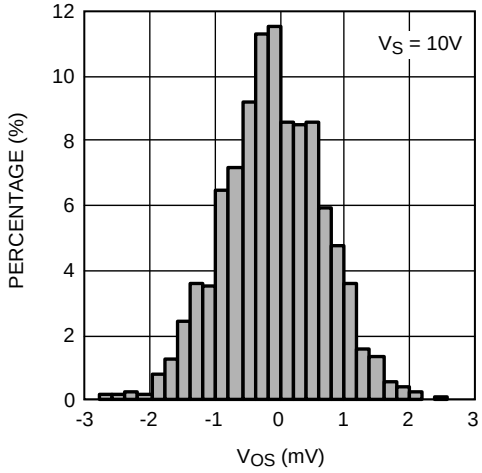


Figure 1. V_{OS} Distribution

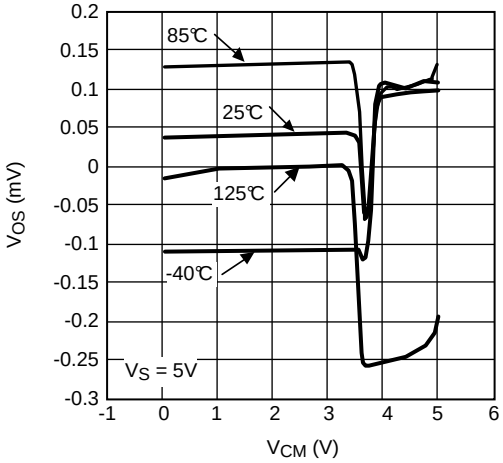


Figure 2. V_{OS} vs V_{CM} (Unit 1)

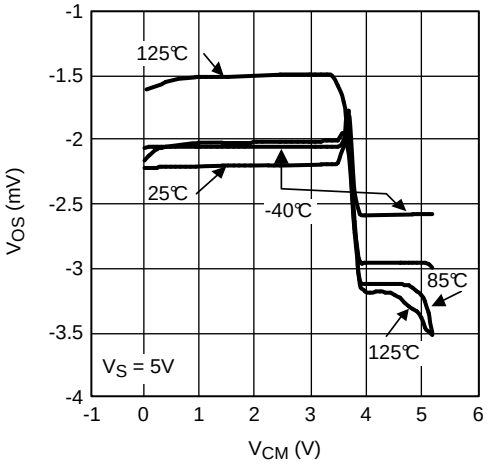


Figure 3. V_{OS} vs V_{CM} (Unit 2)

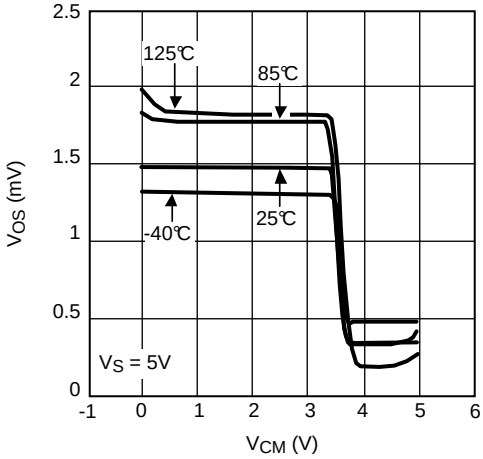


Figure 4. V_{OS} vs V_{CM} (Unit 3)

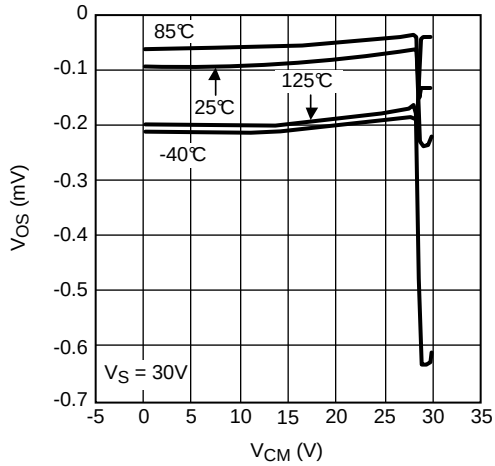


Figure 5. V_{OS} vs V_{CM} (Unit 1)

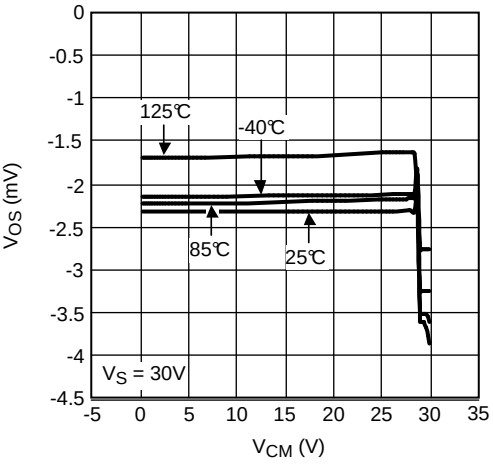


Figure 6. V_{OS} vs V_{CM} (Unit 2)

Typical Characteristics (continued)

Unless otherwise specified, T_A = 25°C.

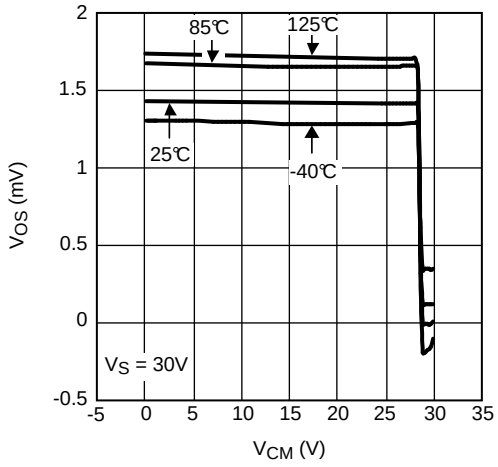


Figure 7. V_{OS} vs V_{CM} (Unit 3)

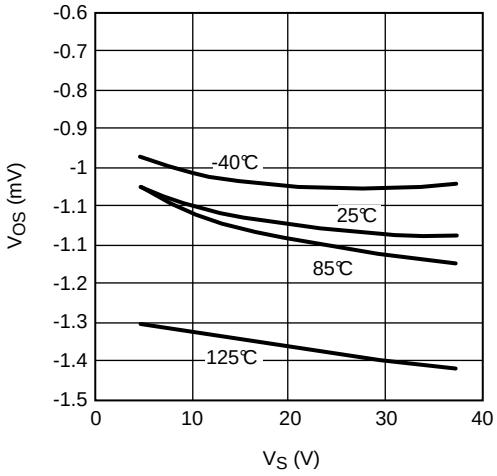


Figure 8. V_{OS} vs V_S (Unit 1)

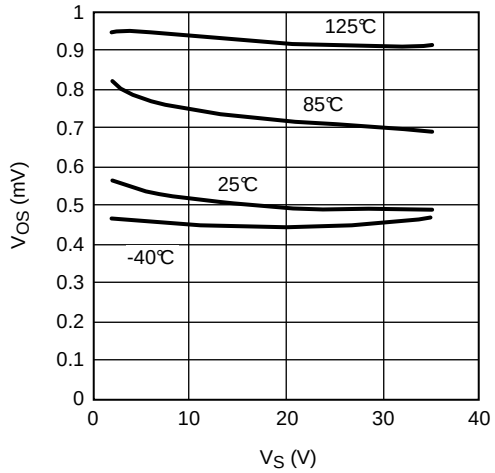


Figure 9. V_{OS} vs V_S (Unit 2)

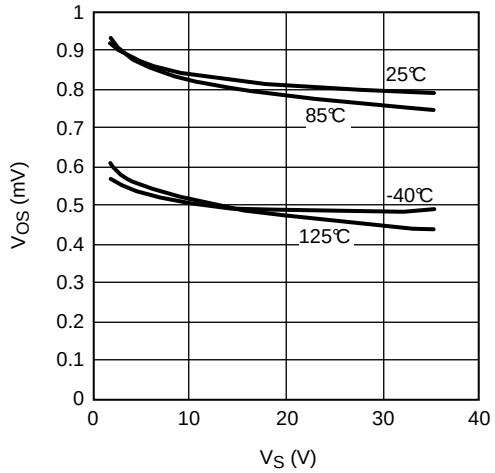


Figure 10. V_{OS} vs V_S (Unit 3)

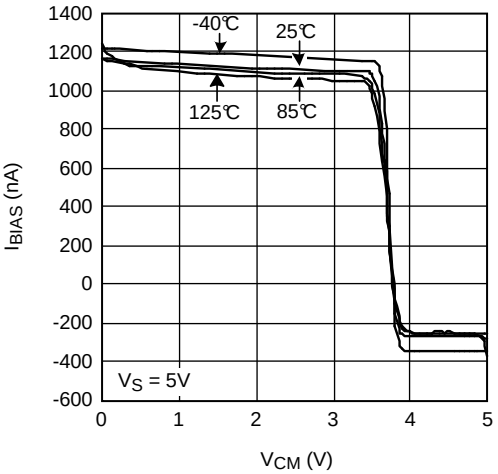


Figure 11. I_{BIAS} vs V_{CM}

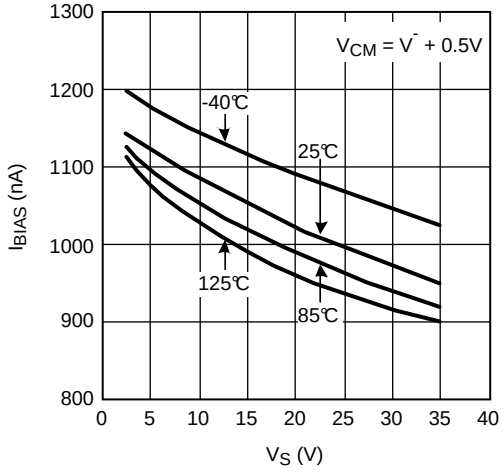


Figure 12. I_{BIAS} vs Supply Voltage

Typical Characteristics (continued)

Unless otherwise specified, T_A = 25°C.

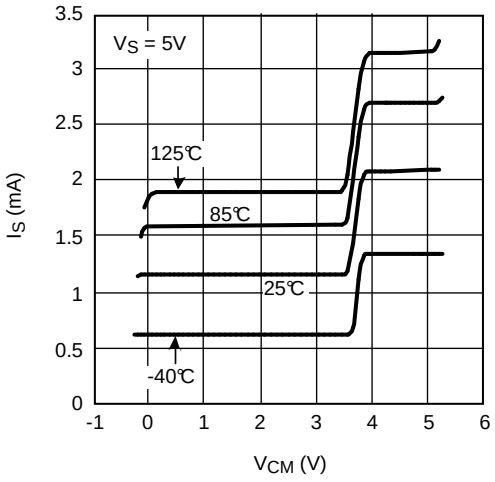


Figure 13. I_S vs V_{CM}

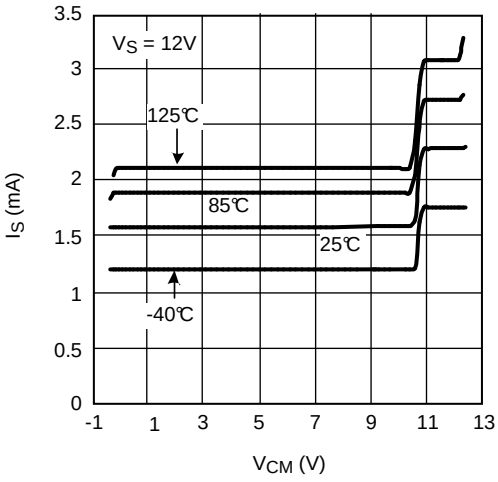


Figure 14. I_S vs V_{CM}

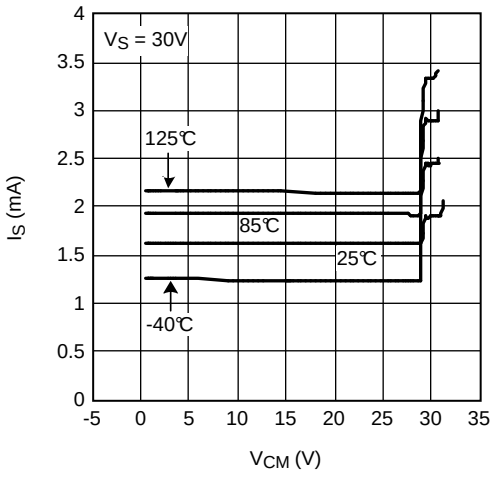


Figure 15. I_S vs V_{CM}

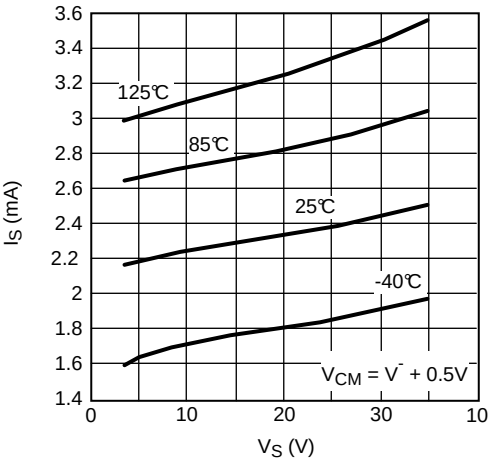


Figure 16. I_S vs Supply Voltage

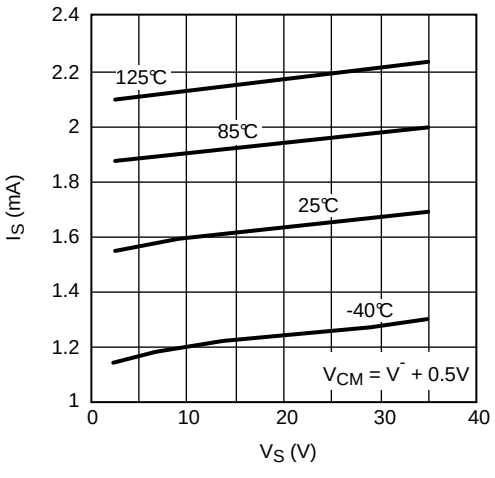


Figure 17. I_S vs Supply Voltage

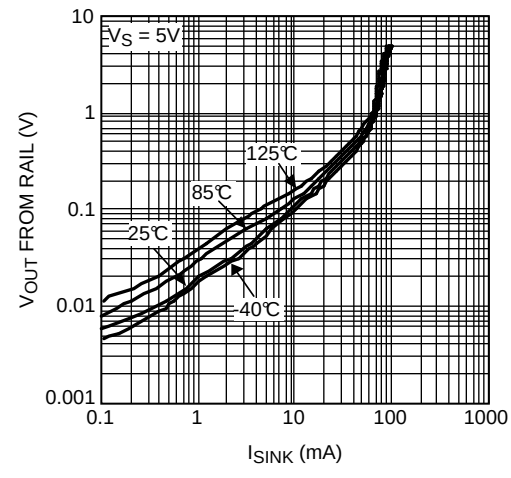


Figure 18. Output Swing vs Sinking Current

Typical Characteristics (continued)

Unless otherwise specified, T_A = 25°C.

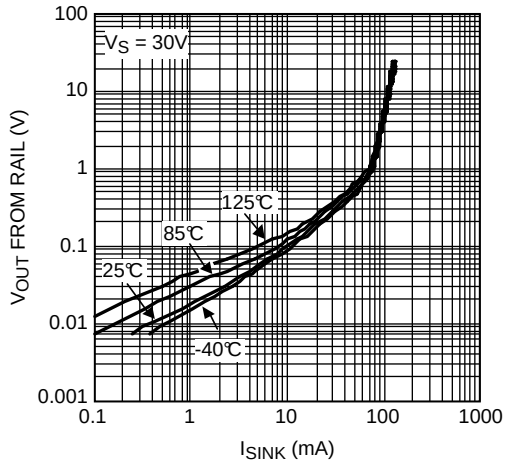


Figure 19. Output Swing vs Sinking Current

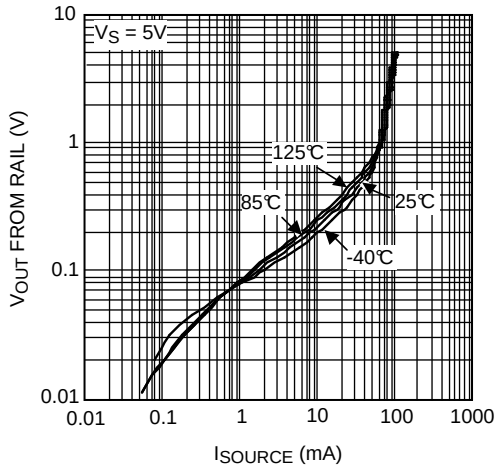


Figure 20. Output Swing vs Sourcing Current

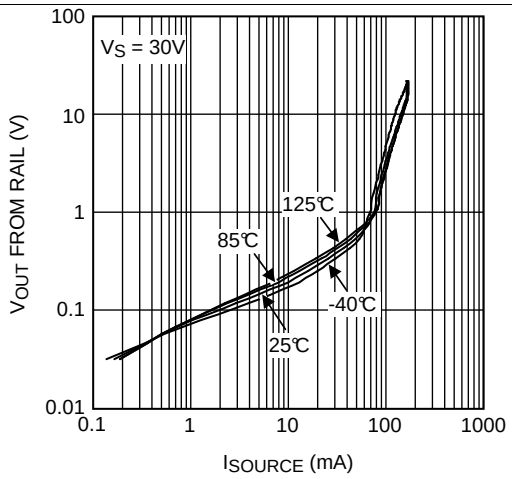


Figure 21. Output Swing vs Sourcing Current

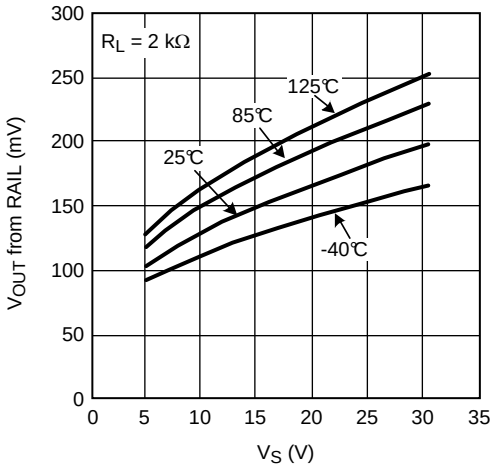


Figure 22. Positive Output Swing vs Supply Voltage

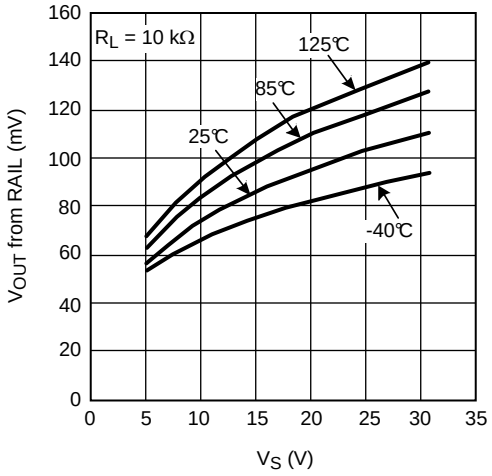


Figure 23. Positive Output Swing vs Supply Voltage

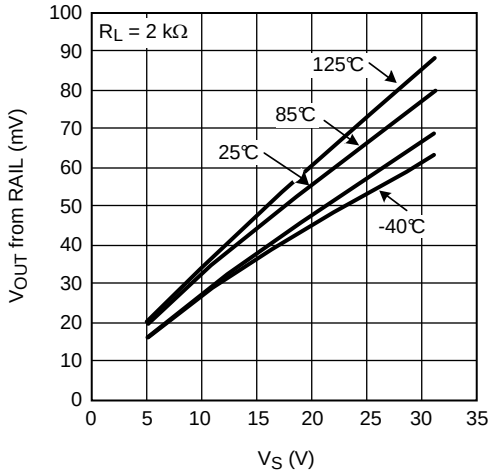


Figure 24. Negative Output Swing vs Supply Voltage

Typical Characteristics (continued)

Unless otherwise specified, T_A = 25°C.

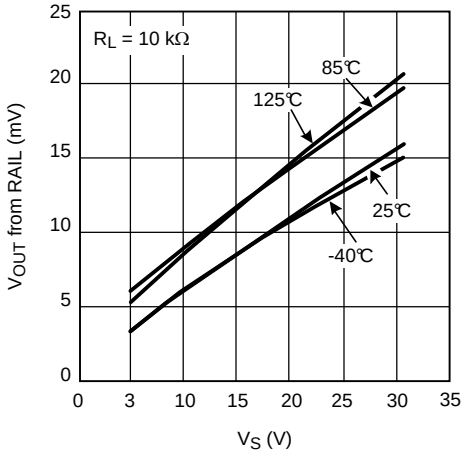


Figure 25. Negative Output Swing vs Supply Voltage

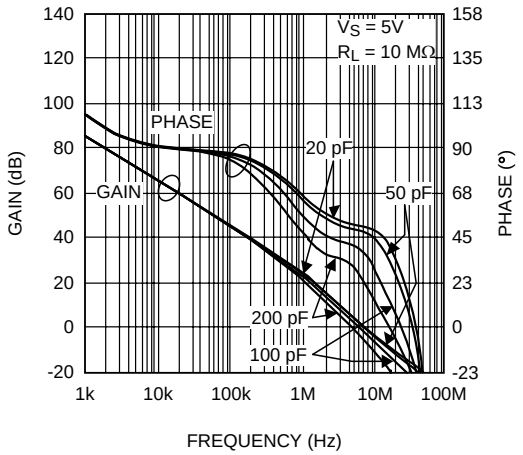


Figure 26. Open-Loop Frequency Response With Various Capacitive Loads

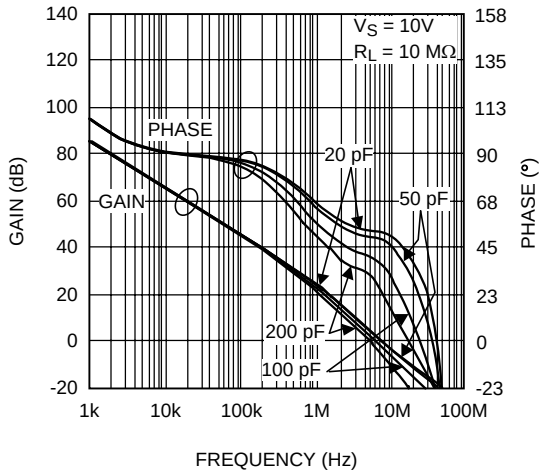


Figure 27. Open-Loop Frequency Response With Various Capacitive Loads

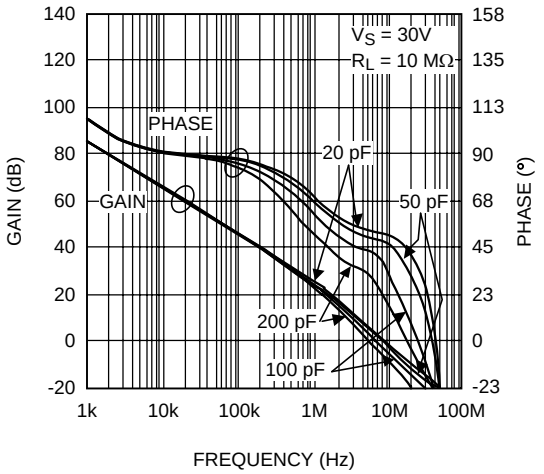


Figure 28. Open-Loop Frequency Response With Various Capacitive Loads

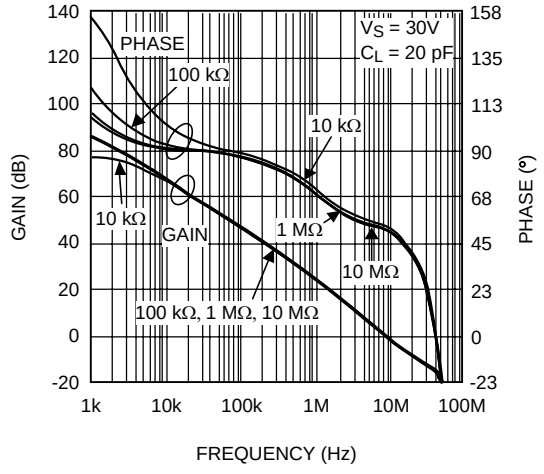


Figure 29. Open-Loop Frequency Response vs With Various Resistive Loads

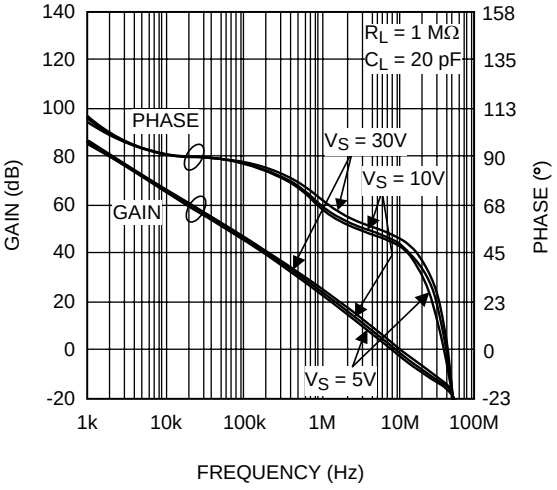


Figure 30. Open-Loop Frequency Response vs With Various Supply Voltages

Typical Characteristics (continued)

Unless otherwise specified, T_A = 25°C.

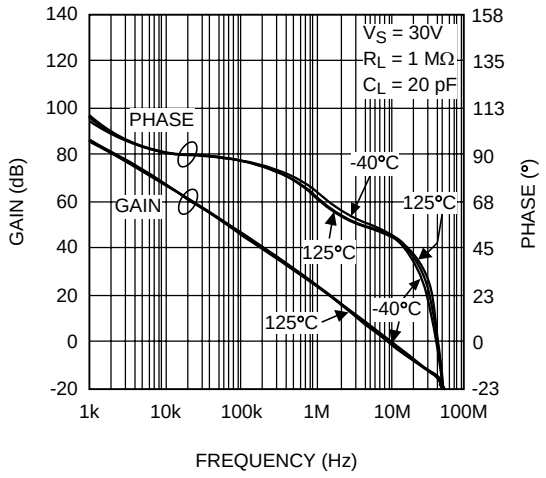


Figure 31. Open-Loop Frequency Response at Various Temperatures

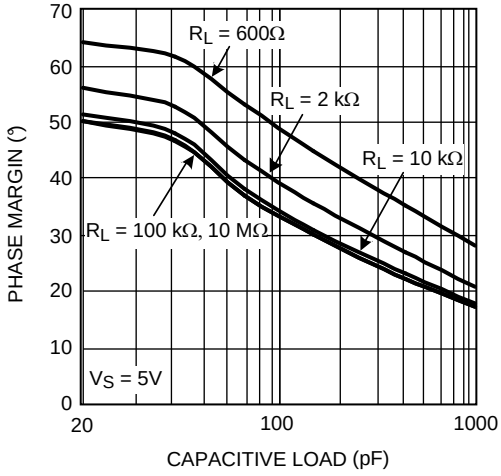


Figure 32. Phase Margin vs Capacitive Load

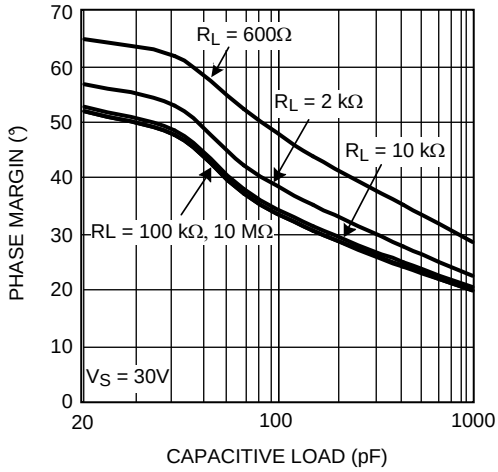


Figure 33. Phase Margin vs Capacitive Load

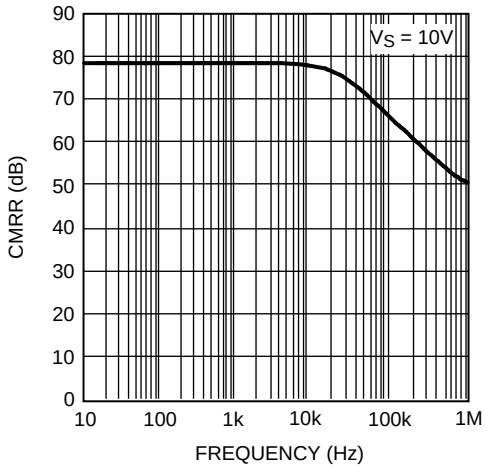


Figure 34. CMRR vs Frequency

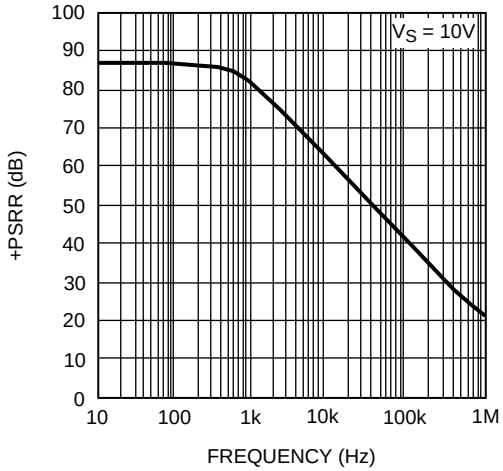


Figure 35. +PSRR vs Frequency

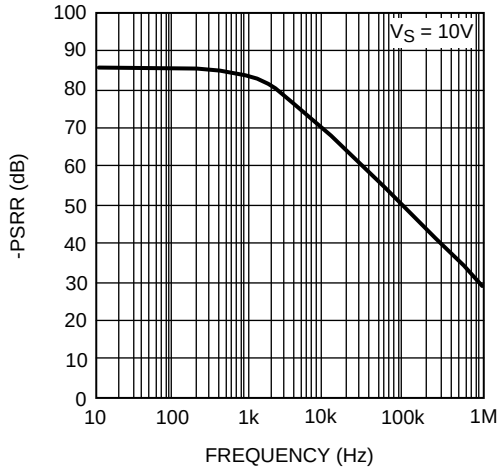


Figure 36. −PSRR vs Frequency

Typical Characteristics (continued)

Unless otherwise specified, T_A = 25°C.

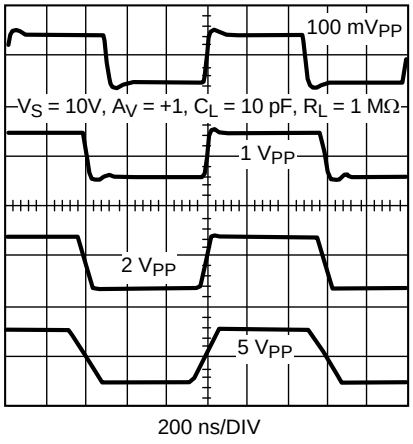


Figure 37. Step Response for Various Amplitudes

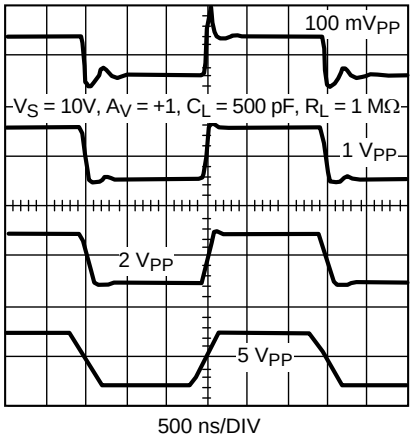


Figure 38. Step Response for Various Amplitudes

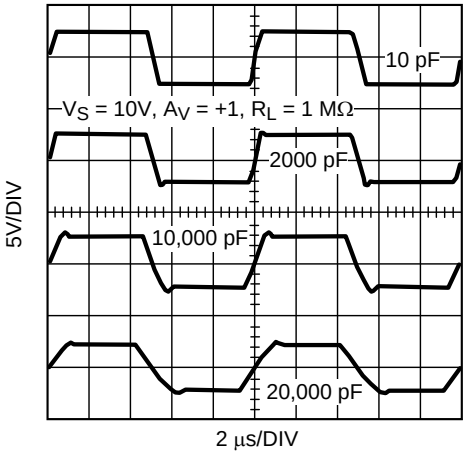


Figure 39. Large Signal Step Response for Various Capacitive Loads

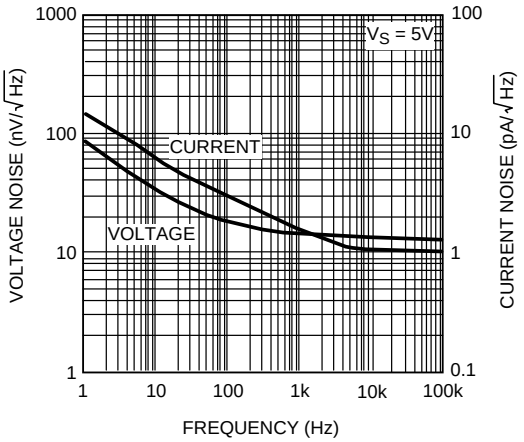


Figure 40. Input-Referred Noise Density vs Frequency

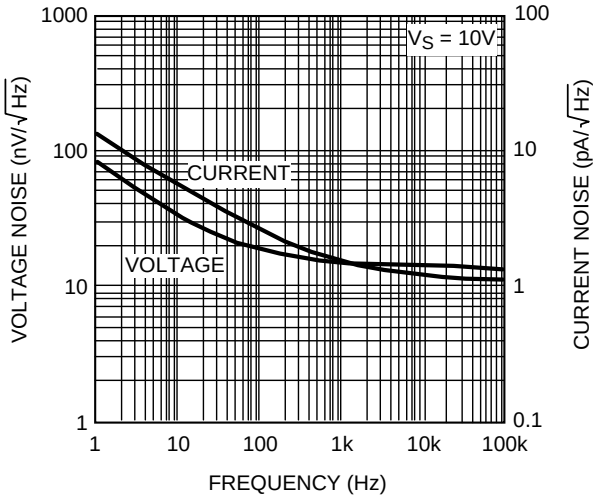


Figure 41. Input-Referred Noise Density vs Frequency

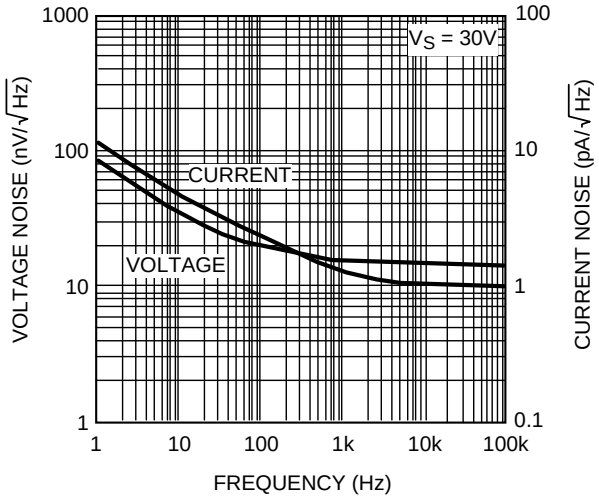


Figure 42. Input-Referred Noise Density vs Frequency

Typical Characteristics (continued)

Unless otherwise specified, T_A = 25°C.

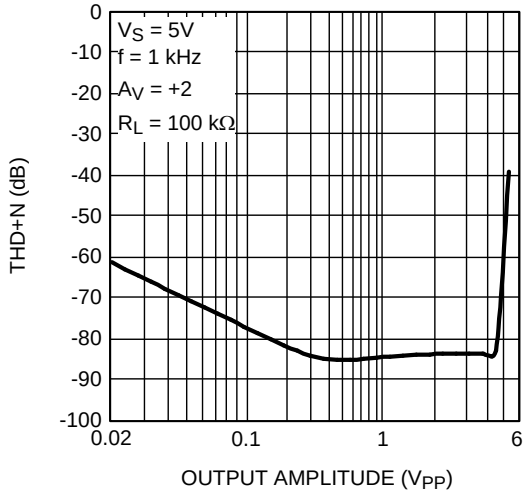


Figure 43. THD+N vs Output Amplitude (V_{PP})

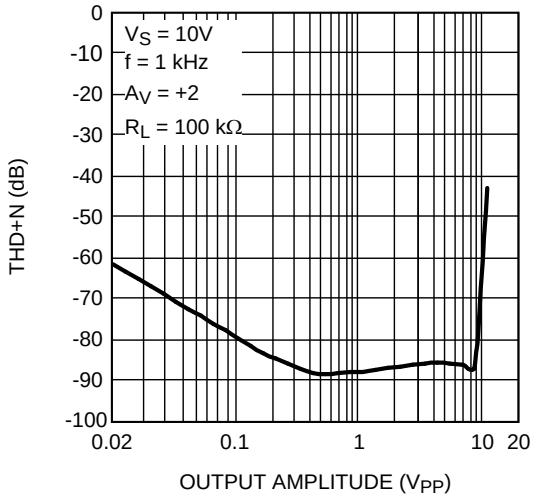


Figure 44. THD+N vs Output Amplitude (V_{PP})

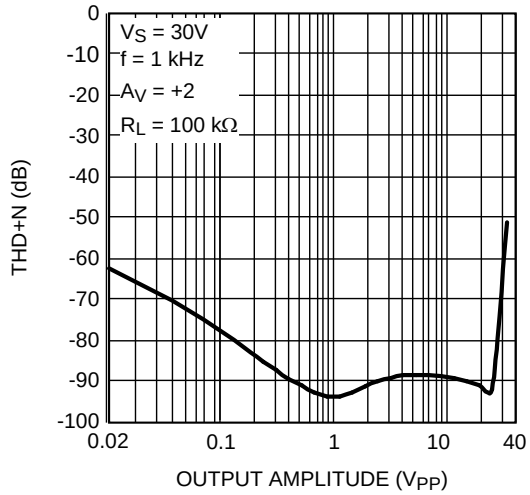


Figure 45. THD+N vs Output Amplitude (V_{PP})

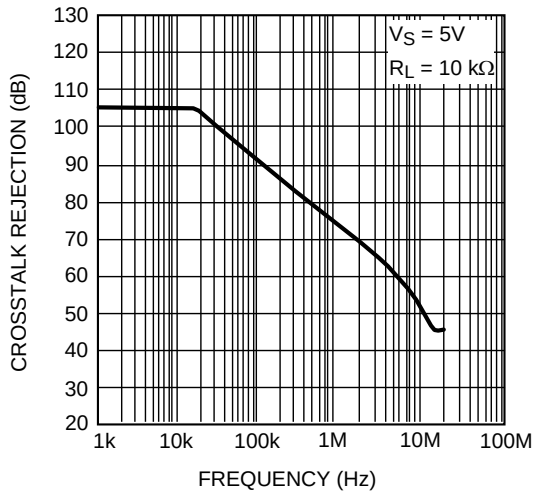


Figure 46. Crosstalk vs Frequency

7 Detailed Description

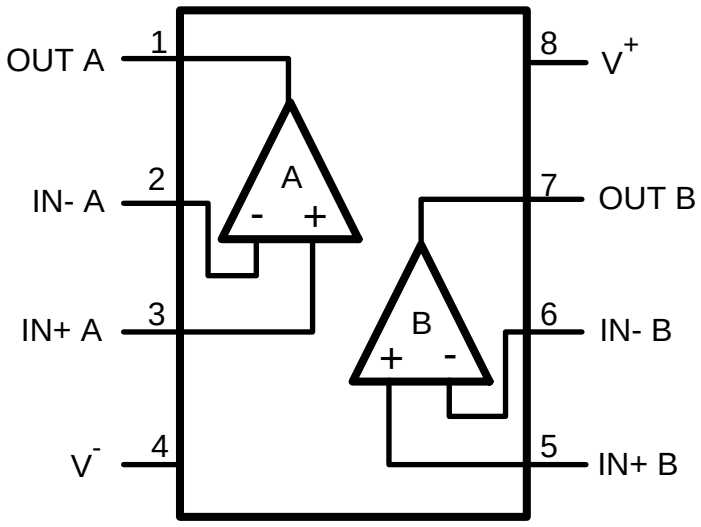
7.1 Overview

The LM7332 device is a rail-to-rail input and output amplifier with wide operating voltages and high-output currents. The LM7322 is efficient, achieving 15.2-V/µs slew rate and 21-MHz unity gain bandwidth while requiring only 2 mA of total supply current. The LM7332 device performance is fully specified for operation at 5 V, ±5 V and ±15 V.

The LM7332 device is designed to drive unlimited capacitive loads without oscillations. The LM7332 is fully tested at −40°C, 125°C, and 25°C, with modern automatic test equipment. High performance from −40°C to +125°C, detailed specifications, and extensive testing makes them suitable for industrial, automotive, and communications applications.

Most device parameters are insensitive to power supply voltage, and this makes the parts easier to use where supply voltage may vary, such as automotive electrical systems and battery-powered equipment. The LM7332 has a true rail-to-rail output and can supply a respectable amount of current (±70 mA) with minimal head room from either rail (1 V).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Estimating the Output Voltage Swing

It is important to keep in mind that the steady-state output current will be less than the current available when there is an input overdrive present. For steady-state conditions, Figure 47 and Figure 48 plots can be used to predict the output swing. These plots also show several load lines corresponding to loads tied between the output and ground. In each case, the intersection of the device plot at the appropriate temperature with the load line would be the typical output swing possible for that load. For example, a 600-Ω load can accommodate an output swing to within 100 mV of V^- and to 250 mV of V^+ (V_S = ±5 V) corresponding to a typical 9.65-V_{PP} unclipped swing.

Feature Description (continued)

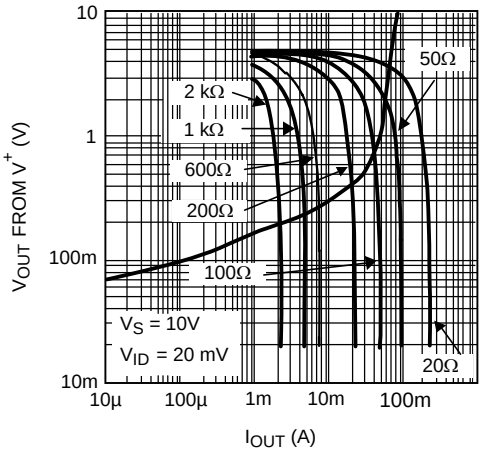


Figure 47. Steady-State Output Sourcing Characteristics With Load Lines

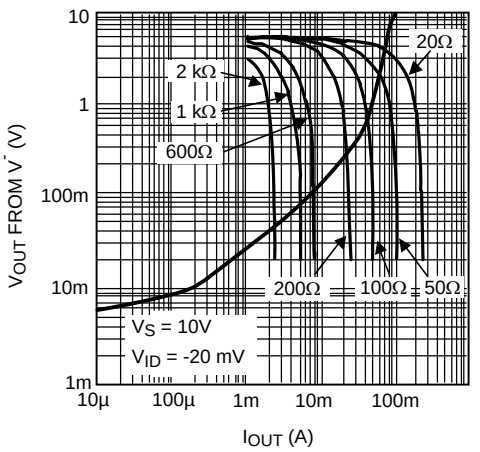


Figure 48. Steady-State Output Sinking Characteristics With Load Lines

7.4 Device Functional Modes

7.4.1 Driving Capacitive Loads

The LM7332 is specifically designed to drive unlimited capacitive loads without oscillations as shown in Figure 49.

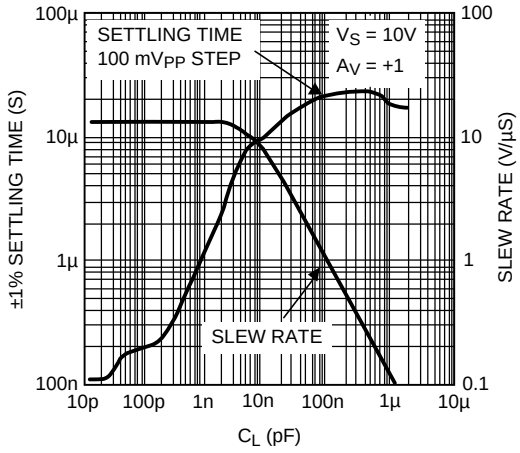


Figure 49. Settling Time and Slew Rate vs Capacitive Load

In addition, the output current handling capability of the device allows for good slewing characteristics even with large capacitive loads as shown in Figure 49. The combination of these features is ideal for applications such as TFT flat panel buffers, A/D converter input amplifiers and power transistor driver.

However, as in most operational amplifiers, addition of a series isolation resistor between the operational amplifier and the capacitive load improves the settling and overshoot performance.

Output current drive is an important parameter when driving capacitive loads. This parameter will determine how fast the output voltage can change. Referring to Figure 49, two distinct regions can be identified. Below about 10,000 pF, the output slew rate is solely determined by the compensation capacitor value of the operational amplifier and available current into that capacitor. Beyond 10 nF, the slew rate is determined by the available output current of the operational amplifier. An estimate of positive and negative slew rates for loads larger than 100 nF can be made by dividing the short circuit current value by the capacitor.

Device Functional Modes (continued)

7.4.2 Output Voltage Swing Close to V^-

The output stage design of the LM7332 allows voltage swings to within millivolts of either supply rail for maximum flexibility and improved useful range. Because of this design architecture, with output approaching either supply rail, the output transistor collector-base junction reverse bias decreases. With output less than a V_{be} from either rail, the corresponding output transistor operates near saturation. In this mode of operation, the transistor exhibits higher junction capacitance and lower f_t which reduces phase margin. With the Noise Gain ($NG = 1 + R_F/R_G$, R_F and R_G are external gain setting resistors) of 2 or higher, there is sufficient phase margin that this reduction in phase margin is of no consequence. However, with lower Noise Gain (<2) and with less than 150 mV to the supply rail, if the output loading is light, the phase margin reduction could result in unwanted oscillations.

In the case of the LM7332, due to inherent architectural specifics, the oscillation occurs only with respect to the output transistor at V^- when output swings to within 150 mV of V^-. However, if this output transistor's collector current is larger than its idle value of a few microamps, the phase margin loss becomes insignificant. In this case, 300 µA is the required collector current of the output transistor to remedy this situation. Therefore, when all the aforementioned critical conditions are present at the same time ($NG < 2$, $V_{OUT} < 150$ mV from supply rails and output load is light) it is possible to ensure stability by adding a load resistor to the output to provide the output transistor the necessary minimum collector current (300 µA).

For 12-V (or ±6-V) operation, for example, add a 39-kΩ resistor from the output to V^+ to cause 300-µA output sinking current and ensure stability. This is equivalent to about 15% increase in total quiescent power dissipation.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM7332 is a rail-to-rail input and output part with a slightly higher GBW of 20 MHz. It has current capability of 40-mA sourcing and 65-mA sinking, and can drive unlimited capacitive loads. The LM7332 is available in both VSSOP and SOIC packages.

8.1.1 Similar High Current Output Devices

The LM6172 has a higher GBW of 100 MHz and over 80 mA of current output. There is also a single version, the LM6171. The LM7372 has 120 MHz of GBW and 150 mA of current output. The LM7372 is available in an 8-pin SO PowerPAD™, and 16-pin SOIC packages with higher power dissipation.

The LME49600 buffer has 250 mA of current out and a 110-MHz bandwidth. The LME49600 is available in a DDPAK/TO-263 package for higher power dissipation.

Detailed information on these parts can be found at www.ti.com.

8.2 Typical Application

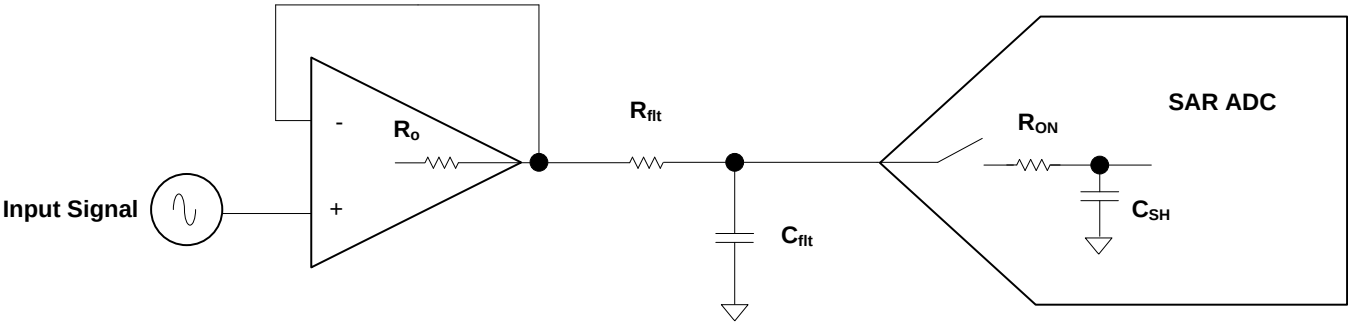


Figure 50. Drive Amplifier for SAR ADC Schematic

8.2.1 Design Requirements

Assume a portable application requires the use of a 12-bit SAR ADC with acquisition time (t_{AQ}) of 1 µs and sample and hold capacitance (C_{SH}) of 80 pF.

The ADC runs on a single supply voltage of 5 V and has a full scale input of 2.5 V_{PP}. A total harmonic distortion plus noise (THD+N) of less than –80 dB is required to maintain signal fidelity. Determine if the LM7332 is a suitable drive amplifier and find the values of R_{flt} and C_{flt}.

Typical Application (continued)

8.2.2 Detailed Design Procedure

The LM7332 can be used as a drive amplifier for SAR ADCs as shown in Figure 50.

The values of R_{flt} and C_{flt} depend on the ADC specifications as well as amplifier gain bandwidth product (GBWP) and output resistance (R_O). It is also common to have a single ground-referenced supply voltage and sample signals up to half of the supply voltage with low distortion.

To determine whether or not the LM7332 is a suitable driver for this application, one must compare the settling time of the amplifier to the acquisition time of the ADC with Equation 1:

$$GBWP_{min} \geq 4 \times (N+1) \times \ln(2) / (2\pi \times t_{AQ}) \quad (1)$$

where

- $GBWP_{min}$: The minimum required gain bandwidth product of the drive amplifier
- N: Number of bits in ADC
- t_{AQ}: The acquisition time of the ADC

Using a value of 12 bits for N and 1µs for t_{AQ}, the $GBWP_{min}$ must be greater than 5.7 MHz. The LM7332 has a GBWP of 21 MHz so it is indeed a suitable driver for this application.

Next, determine the value of C_{flt} with Equation 2:

$$20 \times C_{SH} \leq C_{flt} \leq 60 \times C_{SH} \quad (2)$$

where

- C_{SH}: The ADC sample and hold capacitance
- C_{flt}: The external filter capacitance

Using a value of 80 pF for C_{SH}, the value of C_{flt} must be between 1600 pF and 4800 pF. According to Figure 39, the LM7332 can drive a capacitive load of 2000 pF with 5 V_{PP} and settle within 1 µs, therefore select 1800 pF as the nearest common capacitor value within the range.

Next determine the value of R_{flt} with Equation 3:

$$R_{flt} = 40 / (2\pi \times C_{flt} \times GBWP_{min}) - R_O \quad (3)$$

where

- R_{flt}: The external filter resistance
- C_{flt}: The external filter capacitance determined above
- $GBWP_{min}$: The minimum required gain bandwidth product of the drive amplifier determined above
- R_O: The closed loop output impedance of the drive amplifier typically specified in the electrical characteristics table

Using a value of 1800 pF for C_{flt}, 5.7 MHz for $GBWP_{min}$, and a value of 3 Ω for R_O the value of R_{flt} is determined to be 617.5 Ω. Use closest value of 620 Ω for a filter frequency (f_{flt}) of 142 kHz given Equation 4:

$$f_{flt} = 1 / (2\pi \times (R_O + R_{flt}) \times C_{flt}) \quad (4)$$

The last requirement is to drive input signals of 2.5 V_{PP} on a single 5-V supply with THD+N less than –80 dB.

Figure 51 shows the THD+N response of the LM7332 with a single supply voltage of 5 V. The LM7332 can maintain THD+N levels as low as –83 dB for output levels up to 4 V_{PP}. Therefore the final requirement has been met, and the LM7332 is a suitable drive amplifier for the 12-bit SAR ADC in this design example.

Driving two independent channels of the SAR ADC within minimal crosstalk between the channels may also be required. Figure 52 shows the crosstalk rejection over frequency. The LM7332 achieves 105 dB of crosstalk rejection up to 20 kHz and greater than 75 dB up to 1MHz which demonstrates the suitability of measuring very large input signals without interfering with adjacent channels.

Typical Application (continued)

8.2.3 Application Curves

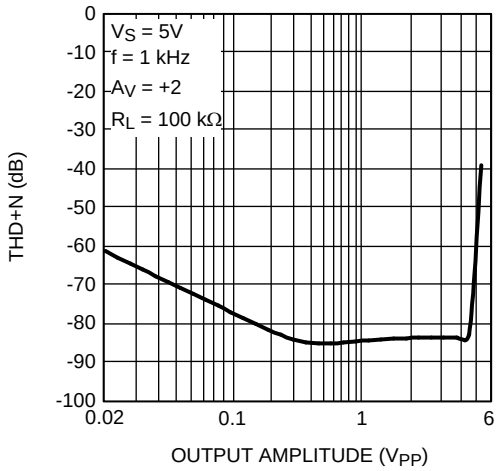


Figure 51. THD+N vs Output Amplitude

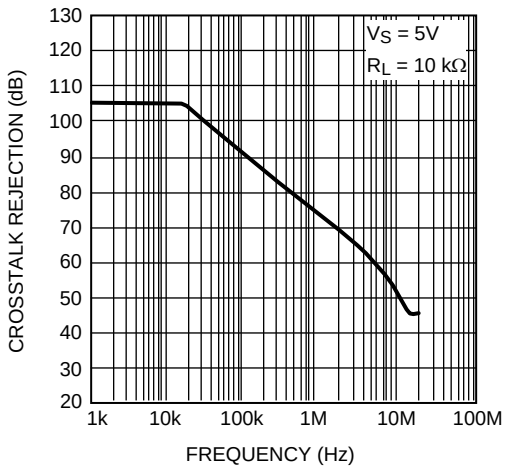


Figure 52. Crosstalk Rejection vs. Frequency

9 Power Supply Recommendations

The use of supply decoupling is mandatory in most applications. As with most relatively high-speed or high output current operational amplifiers, best results are achieved when each supply line is decoupled with two capacitors: a small value ceramic capacitor (approximately 0.01 µF) placed very close to the supply lead in addition to a large value tantalum or aluminum capacitor (> 4.7 µF). The large capacitor can be shared by more than one device if necessary. The small ceramic capacitor maintains low supply impedance at high frequencies while the large capacitor acts as the charge *bucket* for fast load current spikes at the operational amplifier output. The combination of these capacitors provides supply decoupling and helps keep the operational amplifier oscillation free under any load.

10 Layout

10.1 Layout Guidelines

Take care to minimize the loop area formed by the bypass capacitor connection between supply pins and ground. A ground plane underneath the device is recommended; any bypass components to ground must have a nearby via to the ground plane. The optimum bypass capacitor placement is closest to the corresponding supply pin. Use of thicker traces from the bypass capacitors to the corresponding supply pins lowers the power supply inductance and provide a more stable power supply.

The feedback components must be placed as close to the device as possible to minimize stray parasitics.

10.2 Layout Example

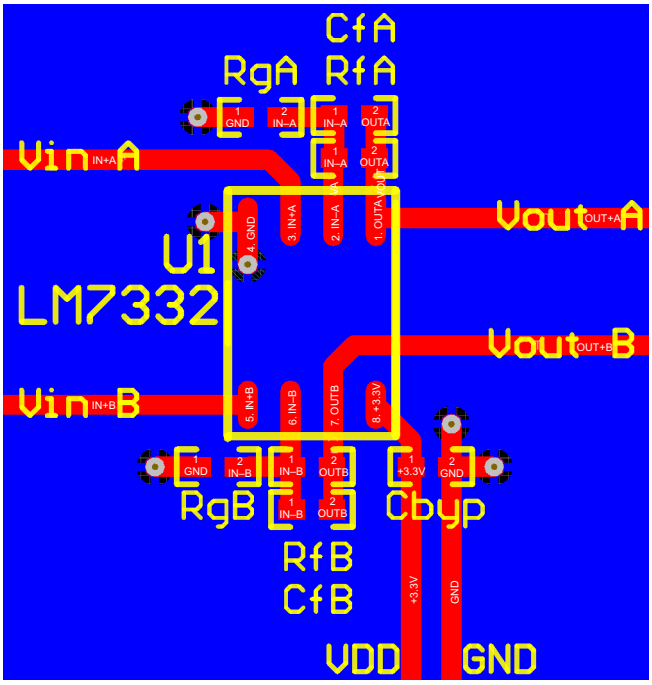


Figure 53. LM7332 Layout Example

10.3 Output Short Circuit Current and Dissipation Issues

The LM7332 output stage is designed for maximum output current capability. Even though momentary output shorts to ground and either supply can be tolerated at all operating voltages, longer-lasting short conditions can cause the junction temperature to rise beyond the absolute maximum rating of the device, especially at higher supply voltage conditions. Below a supply voltage of 6 V, the output short circuit condition can be tolerated indefinitely.

With the operational amplifier tied to a load, the device power dissipation consists of the quiescent power due to the supply current flow into the device, in addition to power dissipation due to the load current. The load portion of the power itself could include an average value (due to a DC load current) and an AC component. DC load current would flow if there is an output voltage offset, or the output AC average current is non-zero, or if the operational amplifier operates in a single-supply application where the output is maintained somewhere in the range of linear operation.

Therefore,

$$P_{TOTAL} = P_Q + P_{DC} + P_{AC} \quad (5)$$

Output Short Circuit Current and Dissipation Issues (continued)

The operational amplifier quiescent power dissipation is calculated by Equation 6:

$$P_Q = I_S \times V_S \quad (6)$$

where

- I_S: Supply Current
- V_S: Total Supply Voltage ($V^+ - V^-$)

The DC load power is calculated by Equation 7:

$$P_{DC} = I_O \times (V_r - V_o) \quad (7)$$

where

- V_O: Average Output Voltage
- V_r: V^+ for sourcing and V^- for sinking current

The AC load power is calculated as P_{AC} = the value shown in Table 1.

Table 1 shows the maximum AC component of the load power dissipated by the operational amplifier for standard sinusoidal, triangular, and square waveforms:

Table 1. Normalized AC Power Dissipated in the Output Stage for Standard Waveforms

P_{AC} (W.Ω/V^2)		
SINUSOIDAL	TRIANGULAR	SQUARE
50.7 x 10^{-3}	46.9 x 10^{-3}	62.5 x 10^{-3}

The table entries are normalized to V_S^2/R_L. To figure out the AC load current component of power dissipation, simply multiply the table entry corresponding to the output waveform by the factor V_S^2/R_L. For example, with ±12-V supplies, a 600-Ω load, and triangular waveform power dissipation in the output stage is calculated as:

$$P_{AC} = (46.9 \times 10^{-3}) \times [24^2/600] = 45.0 \text{ mW} \quad (8)$$

The maximum power dissipation allowed at a certain temperature is a function of maximum die junction temperature ($T_{J(MAX)}$) allowed, ambient temperature T_A, and package thermal resistance from junction to ambient, $R_{\theta JA}$.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} \quad (9)$$

For the LM7332, the maximum junction temperature allowed is 150°C at which no power dissipation is allowed. The power capability at 25°C is given by Equation 10 and Equation 11.

For VSSOP package:

$$P_{D(MAX)} = \frac{150℃ - 25℃}{161.1℃/W} = 0.78W \quad (10)$$

For SOIC package:

$$P_{D(MAX)} = \frac{150℃ - 25℃}{109.1℃/W} = 1.15W \quad (11)$$

Similarly, the power capability at 125°C is given by Equation 12 and Equation 13.

For VSSOP package:

$$P_{D(MAX)} = \frac{150℃ - 125℃}{161.1℃/W} = 0.16W \quad (12)$$

For SOIC package:

$$P_{D(MAX)} = \frac{150℃ - 125℃}{109.1℃/W} = 0.23W \quad (13)$$

Figure 54 shows the power capability vs temperature for VSSOP and SOIC packages. The area under the maximum thermal capability line is the operating area for the device. When the device works in the operating area where P_{TOTAL} is less than $P_{D(MAX)}$, the device junction temperature will remain below 150°C. If the intersection of ambient temperature and package power is above the maximum thermal capability line, the junction temperature will exceed 150°C, and this must be strictly prohibited.

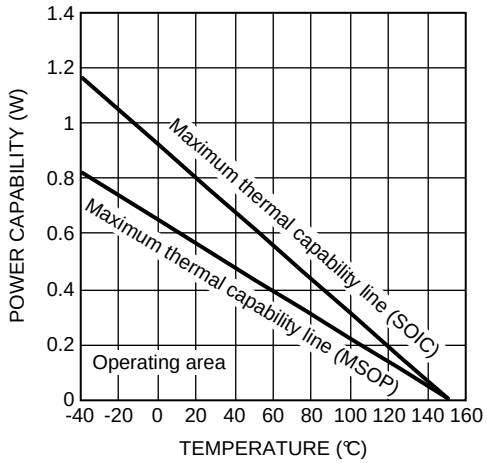


Figure 54. Power Capability vs Temperature

When high power is required and ambient temperature cannot be reduced, providing air flow is an effective approach to reduce thermal resistance therefore to improve power capability.

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM7332MA/NOPB	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125	LM733 2MA	
LM7332MAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LM733 2MA	Samples
LM7332MM/NOPB	OBSOLETE	VSSOP	DGK	8		TBD	Call TI	Call TI	-40 to 125	AA5A	
LM7332MME/NOPB	OBSOLETE	VSSOP	DGK	8		TBD	Call TI	Call TI	-40 to 125	AA5A	
LM7332MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AA5A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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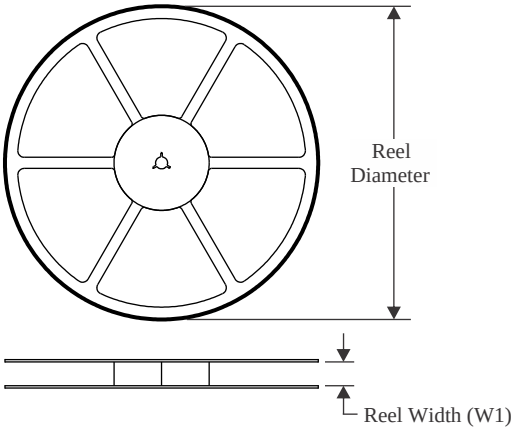
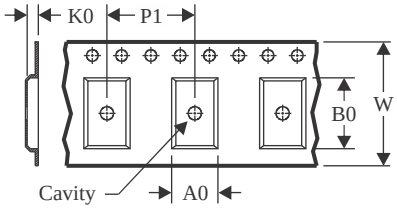
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

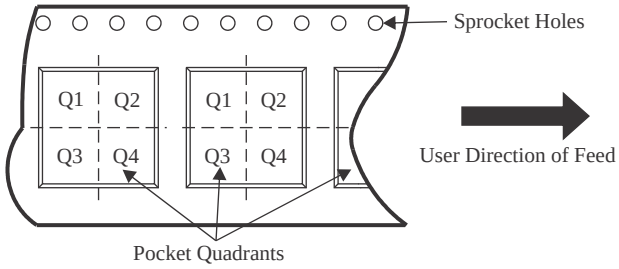


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

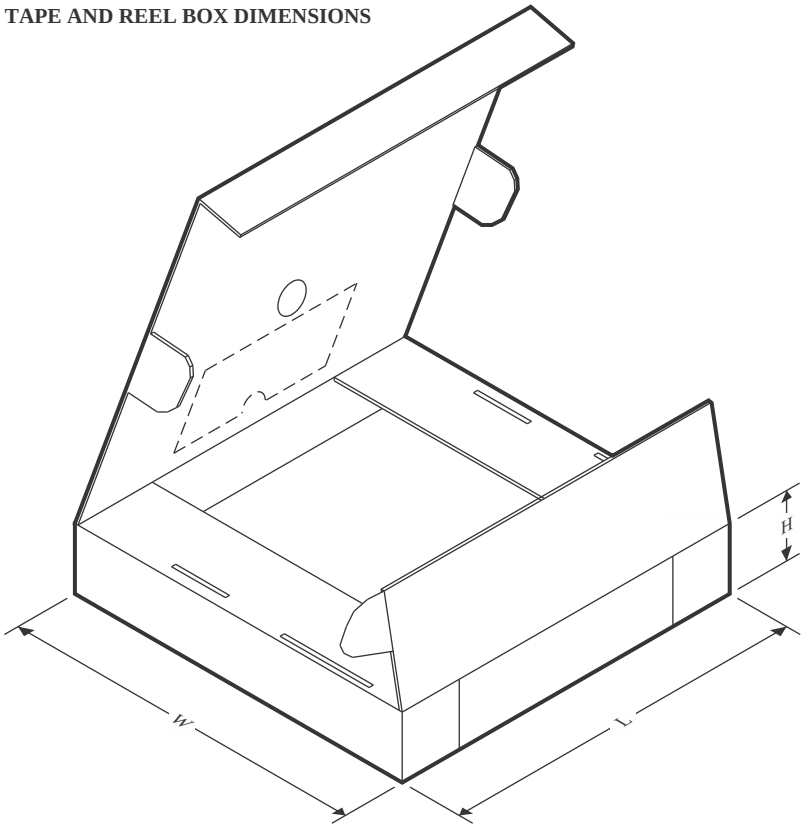
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM7332MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM7332MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM7332MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM7332MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

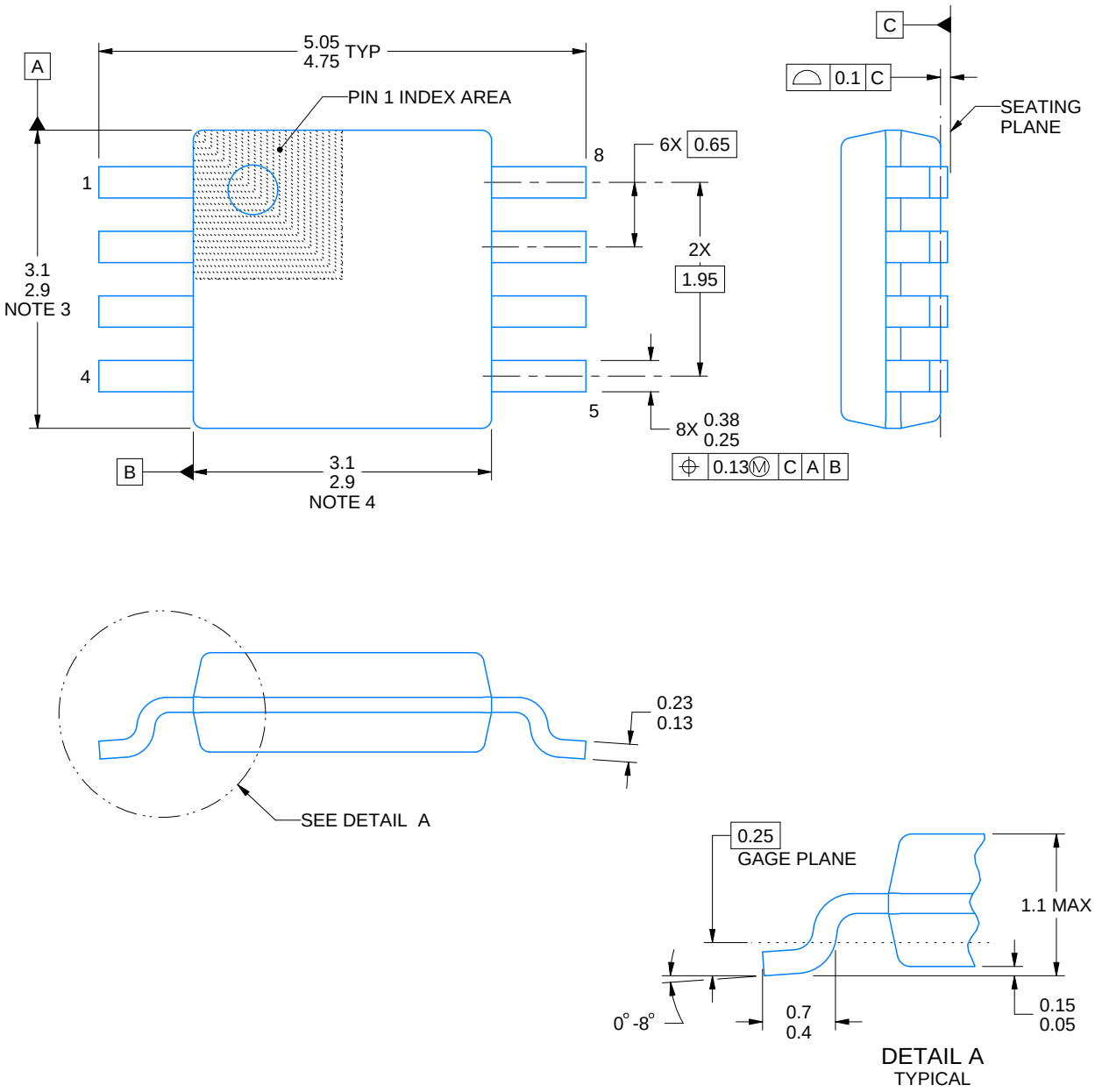
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM7332MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM7332MAX/NOPB	SOIC	D	8	2500	353.0	353.0	32.0
LM7332MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM7332MMX/NOPB	VSSOP	DGK	8	3500	366.0	364.0	50.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

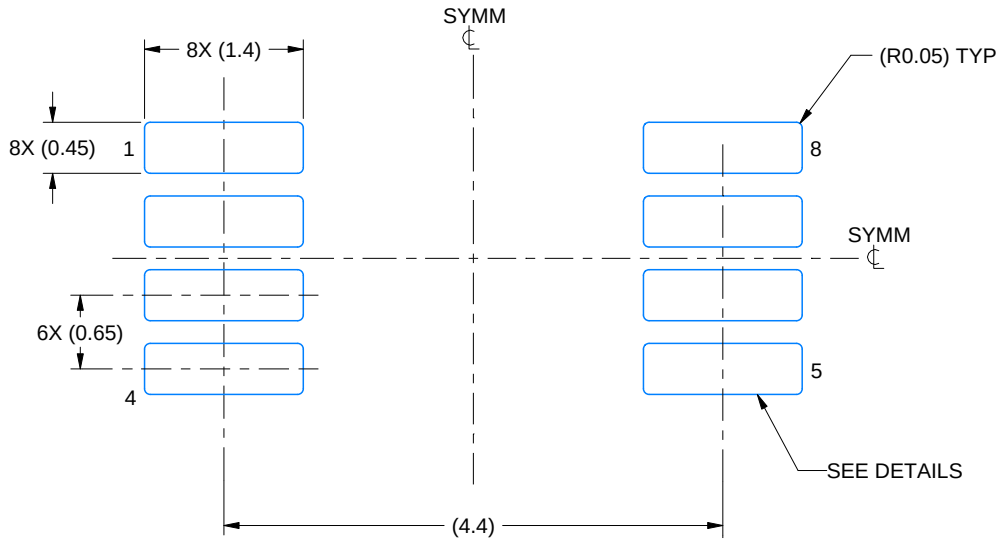
SMALL OUTLINE PACKAGE



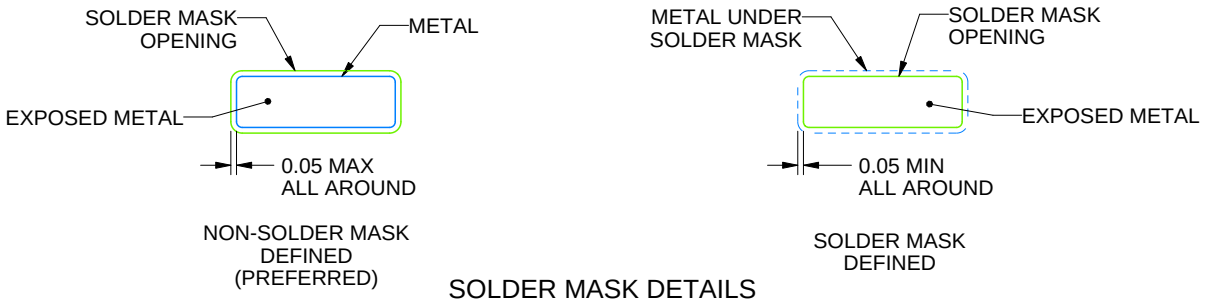
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

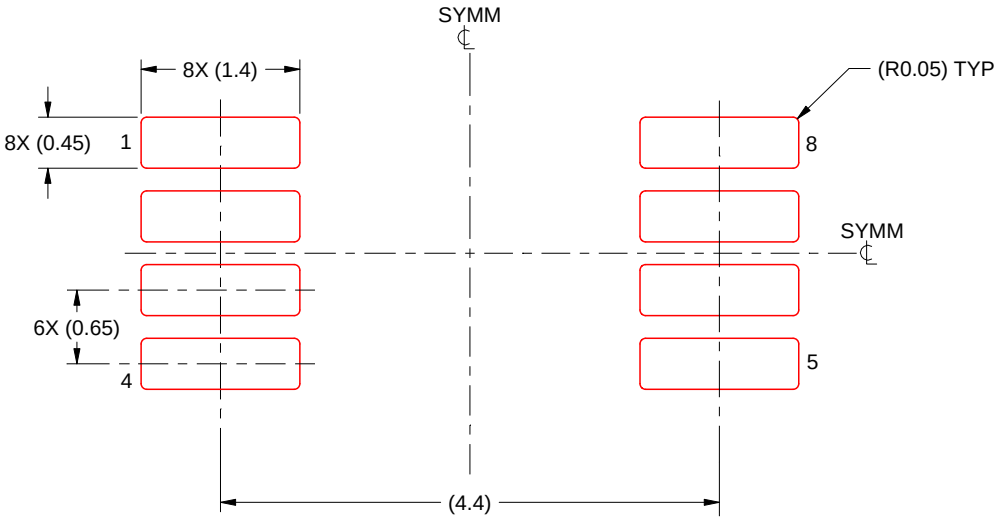


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

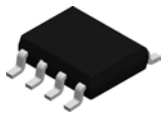


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

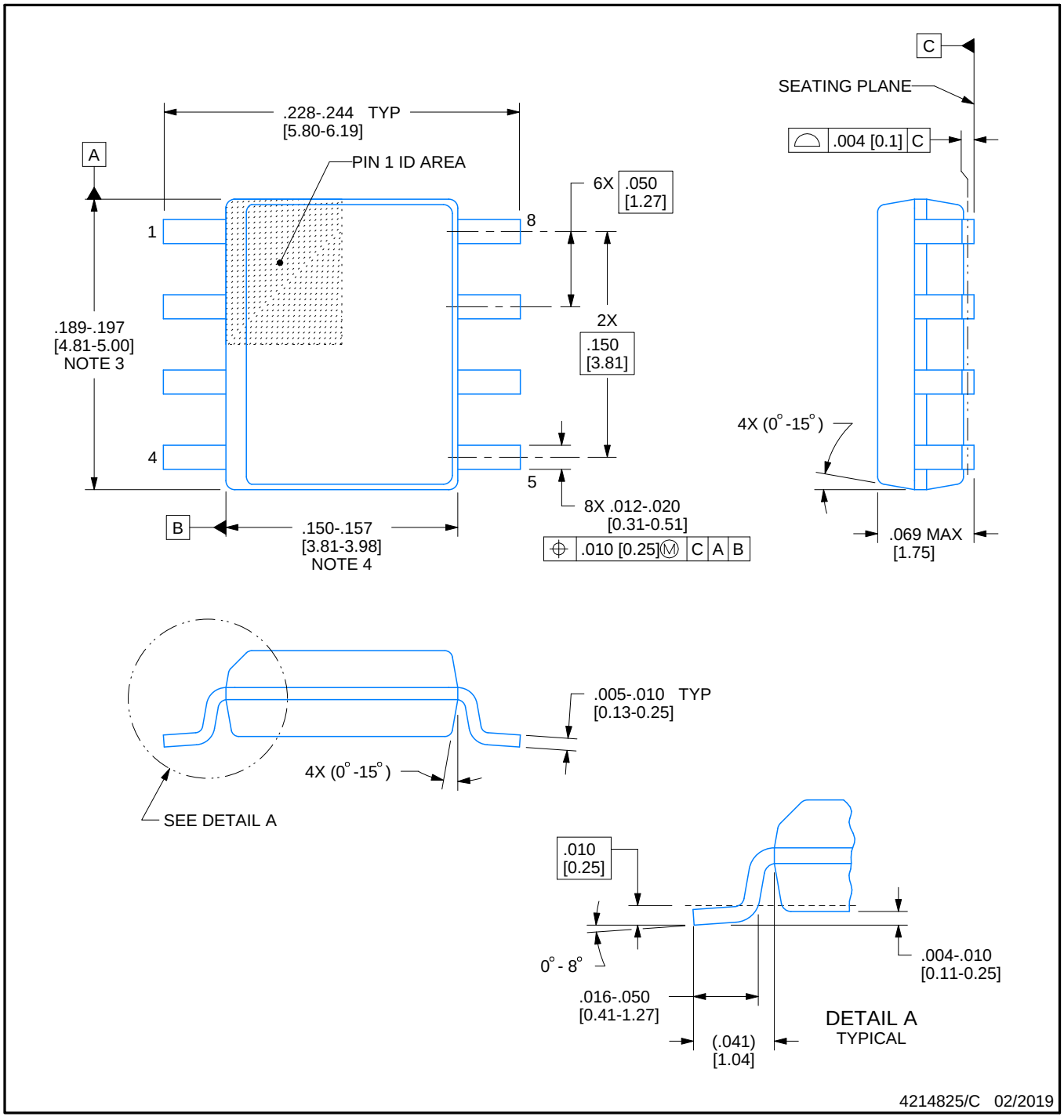


PACKAGE OUTLINE

D0008A

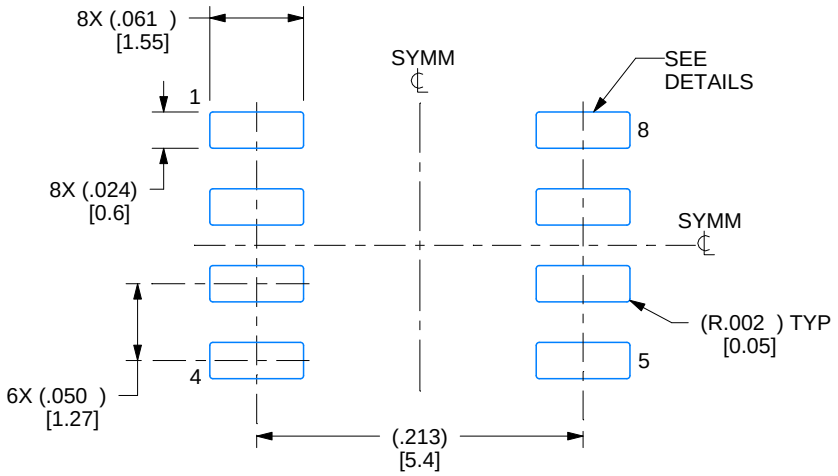
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

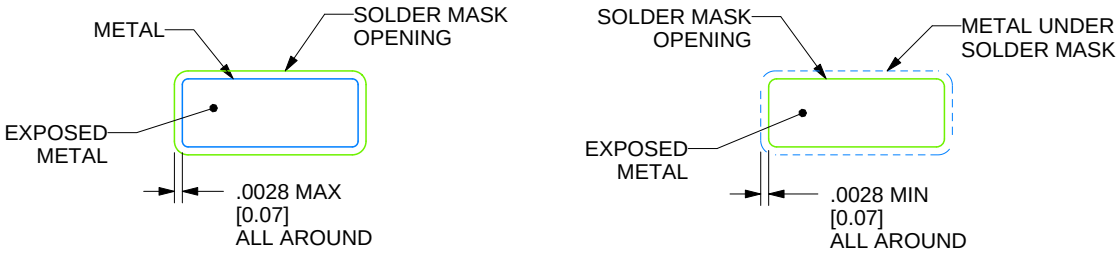


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

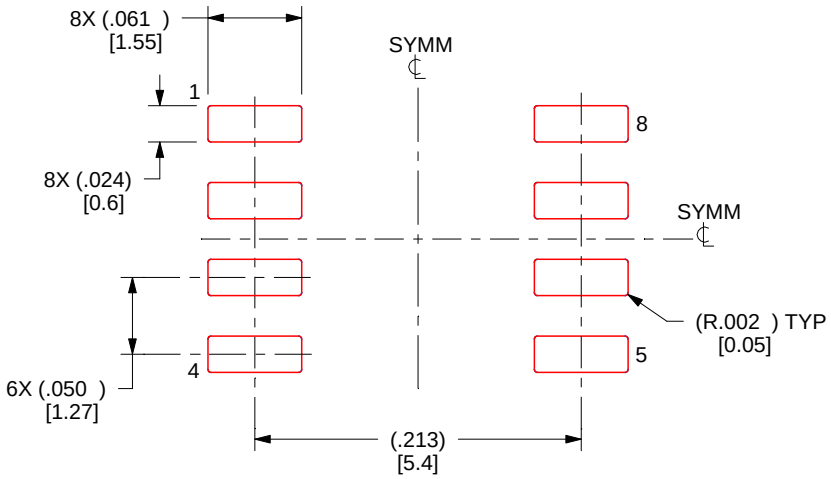
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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