LMC6035-Q1 Automotive, 2.7V, Low-Power, Single-Supply, CMOS Operational Amplifier

1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 3: –40°C to +85°C, T_A
- Typical unless otherwise noted
- Specified 2.7V, 3V, 5V, and 15V performance
- Specified for 2kΩ and 600Ω loads
- Wide operating range: 2.0V to 15.5V
- Ultra-low input current: 20fA
- Rail-to-rail output swing
  - At 600Ω: 200mV from either rail at 2.7V
  - At 100kΩ: 5mV from either rail at 2.7V
- High voltage gain: 126dB
- Wide input common-mode voltage range
  - –0.1V to +2.3V at V_S = 2.7V
- Low distortion: 0.01% at 10kHz

2 Applications

- Filters
- High impedance buffer or preamplifier
- Battery powered electronics
- Medical instrumentation
- Automotive applications

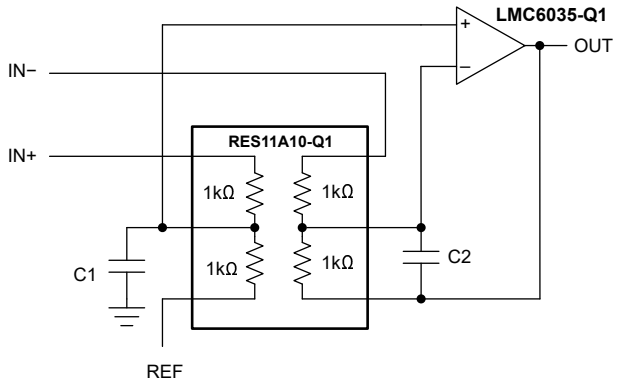
3 Description

The LMC6035-Q1 is an economical, low-voltage op amp capable of rail-to-rail output swing into loads of 600Ω. These devices also feature a well behaved decrease in specifications at supply voltages less than the specified 2.7V operation. This decrease provides a *comfort zone* for adequate operation at voltages significantly less than 2.7V. The ultra low input current (I_B) makes this device and excellent choice for low-power, active-filter applications because a low I_B allows the use of higher resistor values and lower capacitor values. In addition, the drive capability of the LMC6035-Q1 makes this op amp an excellent choice in a broad range of applications for low-voltage systems.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LMC6035-Q1	D (SOIC, 8)	4.9mm × 6mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Difference Amplifier Application With RES11A

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4 Pin Configuration and Functions

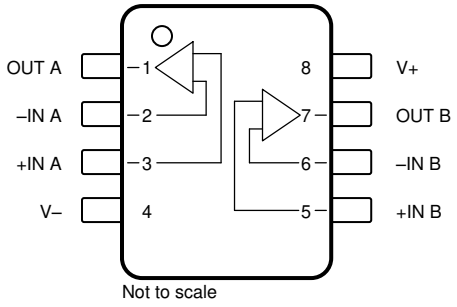


Figure 4-1. D Package, 8-Pin SOIC (Top View)

Table 4-1. Pin Functions: D Package

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN A	2	Input	Inverting input channel A
–IN B	6	Input	Inverting input channel B
+IN A	3	Input	Noninverting input channel A
+IN B	5	Input	Noninverting input channel B
OUT A	1	Output	Output channel A
OUT B	7	Output	Output channel B
V–	4	Power	Negative supply
V+	8	Power	Positive supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1] [2]

			MIN	MAX	UNIT
	Differential input voltage			±Supply voltage	V
V_S	Supply voltage, V_S = (V+) – (V–)		0	16	V
I_{SC}	Output short circuit	To V+		See[3]	mA
		To V–		See[4]	
	Current at input pin			±5	mA
	Current at output pin			±18	mA
	Current at power supply pin			35	mA
T_J	Junction temperature[5]			150	°C
T_{stg}	Storage temperature		–65	150	°C
	Lead temperature (soldering, 10s)			260	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) Do not connect output to V+, when V+ is greater than 13V or reliability is adversely affected.
(4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30mA over long term adversely affect reliability.
(5) The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} – T_A) / \theta_{JA}$.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)[1]	2000	V
		Machine model	300	

(1) Human body model, 1.5kΩ in series with 100pF.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	2		15.5	V
T_J	Junction temperature	–40		85	°C

5.4 Thermal Information

THERMAL METRIC[1]		LMC6035-Q1 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	175	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	N/A	°C/W
ψ_{JT}	Junction-to-top characterization parameter	N/A	°C/W
ψ_{JB}	Junction-to-board characterization parameter	N/A	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

at T_J = +25°C, V+ = 2.7V, V– = 0V, V_{CM} = 1V, V_{OUT} = V+ / 2, and R_L > 1MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				0.5	5	mV
		T_J = –40°C to +85°C				6	
dV_{OS}/dT	Input offset voltage drift	T_J = –40°C to +85°C			2.3		µV/°C
PSRR	Power-supply rejection ratio	Positive, 5V ≤ V+ ≤ 15V		63	93		dB
			T_J = –40°C to +85°C	60			
		Negative, 0V ≤ V– ≤ –10V, V_O = 2.5V, V+ = 5V		74	97		
			T_J = –40°C to +85°C	70			
INPUT BIAS CURRENT							
I_B	Input bias current(3)				20		fA
		T_J = –40°C to +85°C				90	pA
I_{OS}	Input offset current(3)				10		fA
		T_J = –40°C to +85°C				45	pA
NOISE							
e_n	Input voltage noise density	V_{CM} = 1V, f = 1kHz			27		nV/√Hz
i_n	Input current noise density	f = 1kHz			0.2		fA/√Hz
THD	Total harmonic distortion	f= 10kHz, G = –10V/V, R_L = 2kΩ, V_{OUT} = 8V_{pp}, V+ = 10V			0.01		%
INPUT VOLTAGE							
V_{CM}	Common-mode voltage	To positive rail, For CMRR ≥ 40dB		2.0	2.3		V
			T_J = –40°C to +85°C	1.7			
		To negative rail For CMRR ≥ 40dB			–0.1	0.3	
			T_J = –40°C to +85°C			0.5	
		To positive rail, For CMRR ≥ 40dB, V+ = 3V		2.3	2.6		
			T_J = –40°C to +85°C	2.0			
		To negative rail For CMRR ≥ 40dB, V+ = 3V			–0.3	0.1	
			T_J = –40°C to +85°C			0.3	
		To positive rail, For CMRR ≥ 50dB, V+ = 5V		4.2	4.5		
			T_J = –40°C to +85°C	3.9			
		To negative rail For CMRR ≥ 50dB, V+ = 5V			–0.5	–0.2	
			T_J = –40°C to +85°C			0.0	
		To positive rail, For CMRR ≥ 50dB, V+ = 15V		14.0	14.4		
			T_J = –40°C to +85°C	13.7			
		To negative rail For CMRR ≥ 50dB, V+ = 15V			–0.5	–0.2	
			T_J = –40°C to +85°C			0.0	
CMRR	Common-mode rejection ratio	V+ = 15V, 0.7V ≤ V_{CM} ≤ 12.7V		63	96		dB
			T_J = –40°C to +85°C	60			
INPUT IMPEDANCE							
R_{IN}	Input resistance				>10		TΩ

5.5 Electrical Characteristics (continued)

at T_J = +25°C, V+ = 2.7V, V– = 0V, V_{CM} = 1V, V_{OUT} = V+ / 2, and R_L > 1MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
OPEN-LOOP GAIN							
A_V	Large signal voltage gain	Sourcing, V+ = 15V, V_{CM} = 7.5V, 7.5V ≤ V_O ≤ 11.5V	R_L = 2kΩ to 7.5V		2000		V/mV
			R_L = 600Ω to 7.5V	100	1000		
			R_L = 600Ω to 7.5V, T_J = –40°C to +85°C	75			
		Sinking, V+ = 15V, V_{CM} = 7.5V, 3.5V ≤ V_O ≤ 7.5V	R_L = 2kΩ to 7.5V		500		
			R_L = 600Ω to 7.5V	25	250		
			R_L = 600Ω to 7.5V, T_J = –40°C to +85°C	20			
FREQUENCY RESPONSE							
GBW	Gain bandwidth product				1.4		MHz
SR	Slew rate(4)	V_S = 15V, 10V step, g = 1			1.5		V/µs
θ_m	Phase margin				48		°
G_m	Gain margin				17		dB
	Crosstalk	Dual and quad channel, V+ = 15V, R_L = 100kΩ to 7.5V, f = 1kHz, V_{OUT} = 12V_{pp}			130		dB
OUTPUT							
V_O	Voltage output swing	To positive rail, R_L = 2kΩ to 1.35V		2.4	2.62		V
			T_J = –40°C to +85°C	2.2			
		To negative rail, R_L = 2kΩ to 1.35V			0.07	0.2	
			T_J = –40°C to +85°C			0.4	
		To positive rail, R_L = 600Ω to 1.35V		2.0	2.5		
			T_J = –40°C to +85°C	1.8			
		To negative rail, R_L = 600Ω to 1.35V			0.2	0.5	
			T_J = –40°C to +85°C			0.7	
		To positive rail, V+ = 15V, R_L = 2kΩ to 7.5V		14.2	14.8		
			T_J = –40°C to +85°C	13.5			
		To negative rail, V+ = 15V, R_L = 2kΩ to 7.5V			0.12	0.4	
			T_J = –40°C to +85°C			0.5	
		To positive rail, V+ = 15V, R_L = 600Ω to 7.5V		13.5	14.5		
			T_J = –40°C to +85°C	13.0			
		To negative rail, V+ = 15V, R_L = 600Ω to 7.5V			0.36	1.25	
			T_J = –40°C to +85°C			1.50	
I_O	Output current	Sourcing, V_{OUT} = 0V		4	8		mA
			T_J = –40°C to +85°C	3			
		Sinking, V_{OUT} = 2.7V		3	5		
			T_J = –40°C to +85°C	2			
POWER SUPPLY							
I_S	Supply current	V_{OUT} = 1.5V			0.65	1.6	mA
			T_J = –40°C to +85°C			1.9	

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm or one sigma value.
(3) Specified by design.
(4) Number specified is the slower of the positive and negative slew rates.

5.6 Typical Characteristics

at V_S = 2.7V, single supply, and T_A = 25°C (unless otherwise noted)

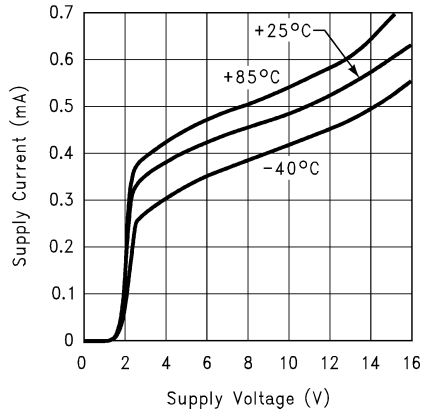


Figure 5-1. Supply Current vs Supply Voltage (Per Amplifier)

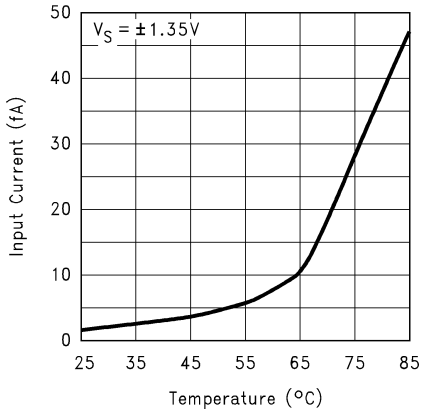


Figure 5-2. Input Bias Current vs Temperature

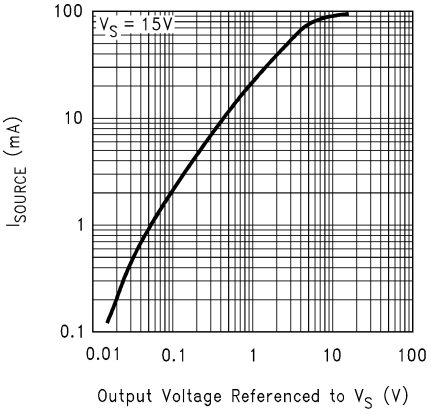


Figure 5-3. Sourcing Current vs Output Voltage

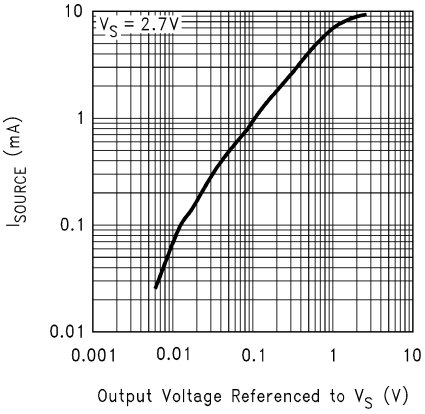


Figure 5-4. Sourcing Current vs Output Voltage

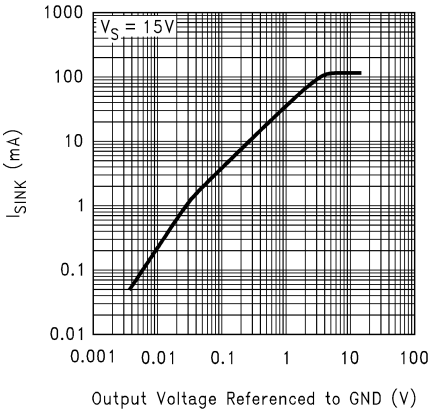


Figure 5-5. Sinking Current vs Output Voltage

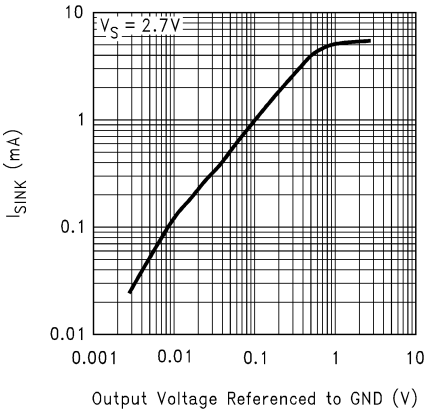


Figure 5-6. Sinking Current vs Output Voltage

5.6 Typical Characteristics (continued)

at V_S = 2.7V, single supply, and T_A = 25°C (unless otherwise noted)

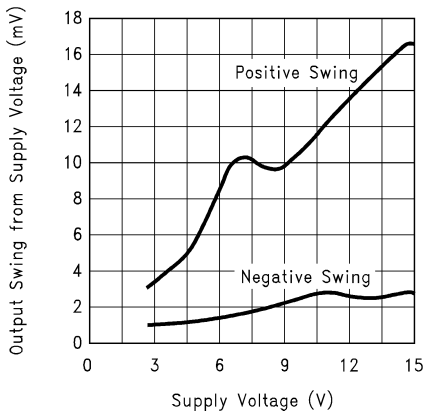


Figure 5-7. Output Voltage Swing vs Supply Voltage

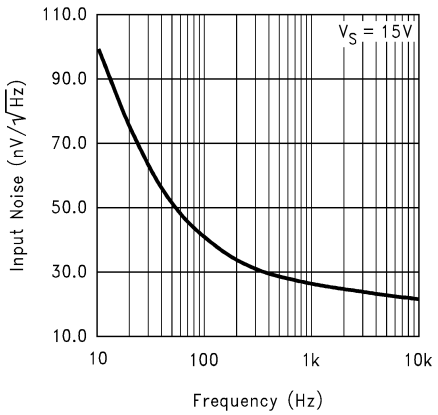


Figure 5-8. Input Noise vs Frequency

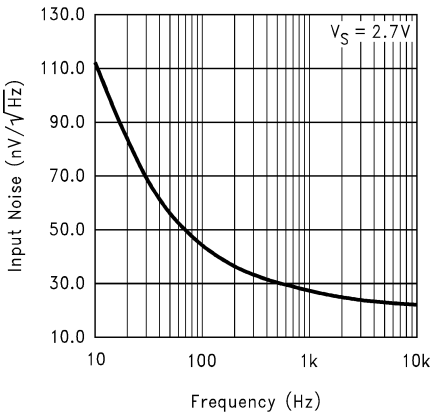


Figure 5-9. Input Noise vs Frequency

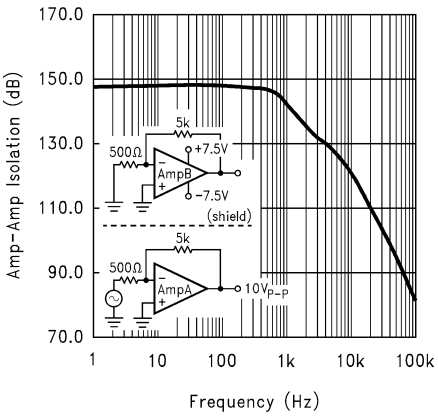


Figure 5-10. Amp to Amp Isolation vs Frequency

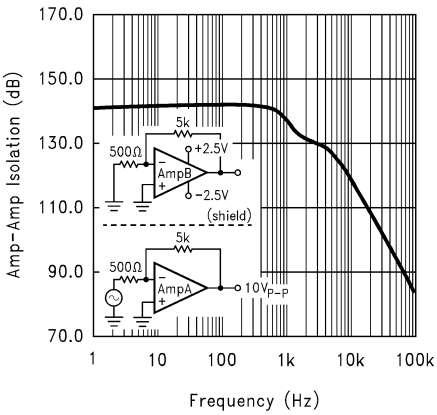


Figure 5-11. Amp to Amp Isolation vs Frequency

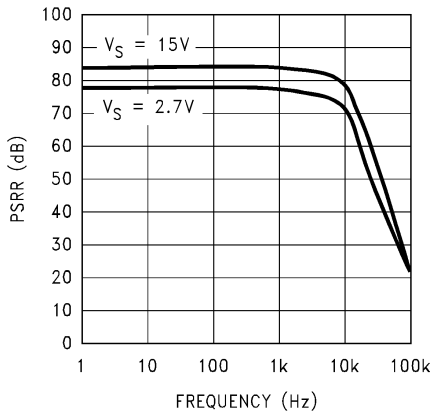


Figure 5-12. +PSRR vs Frequency

5.6 Typical Characteristics (continued)

at V_S = 2.7V, single supply, and T_A = 25°C (unless otherwise noted)

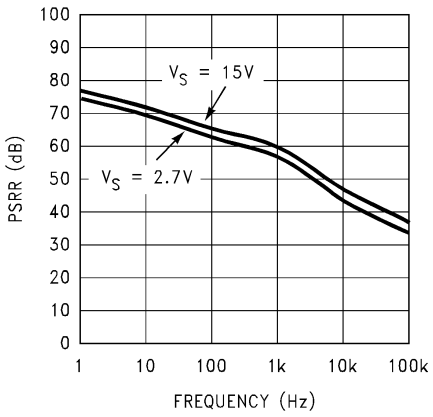


Figure 5-13. −PSRR vs Frequency

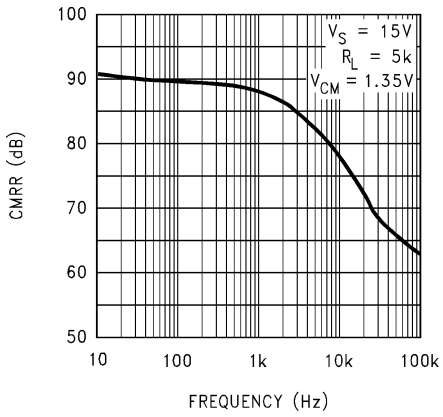


Figure 5-14. CMRR vs Frequency

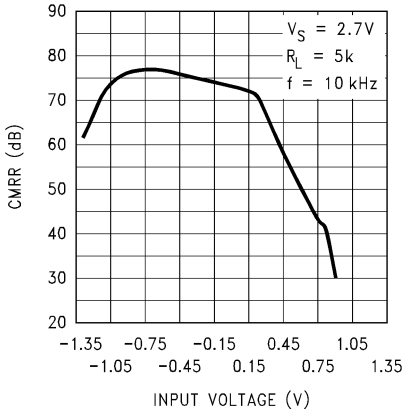


Figure 5-15. CMRR vs Input Voltage

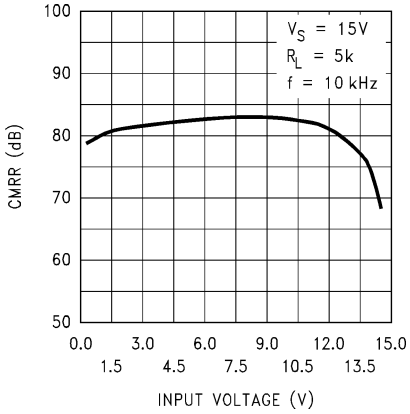


Figure 5-16. CMRR vs Input Voltage

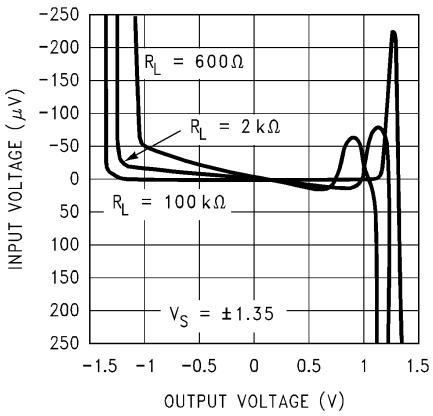


Figure 5-17. Input Voltage vs Output Voltage

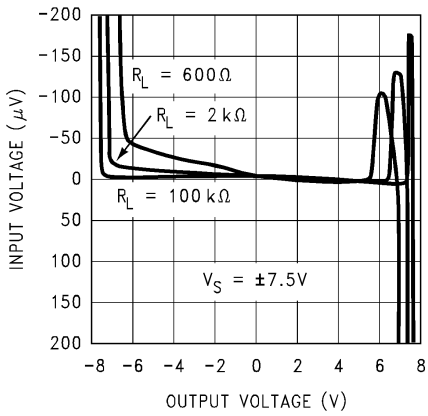


Figure 5-18. Input Voltage vs Output Voltage

5.6 Typical Characteristics (continued)

at V_S = 2.7V, single supply, and T_A = 25°C (unless otherwise noted)

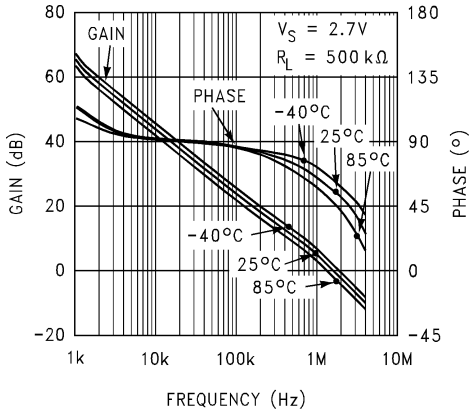


Figure 5-19. Frequency Response vs Temperature

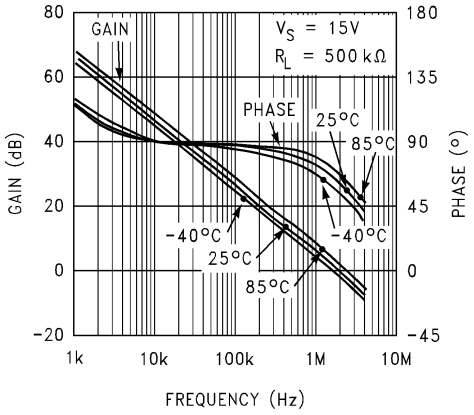


Figure 5-20. Frequency Response vs Temperature

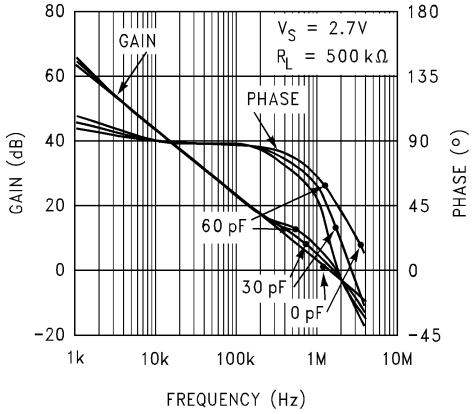


Figure 5-21. Gain and Phase vs Capacitive Load

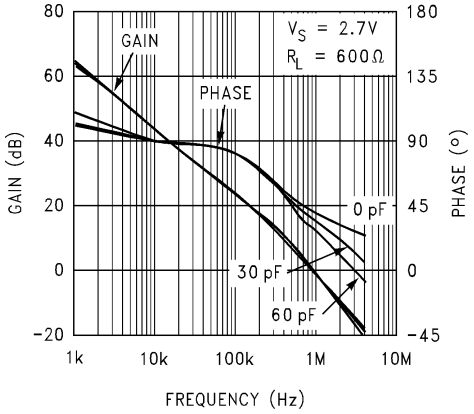


Figure 5-22. Gain and Phase vs Capacitive Load

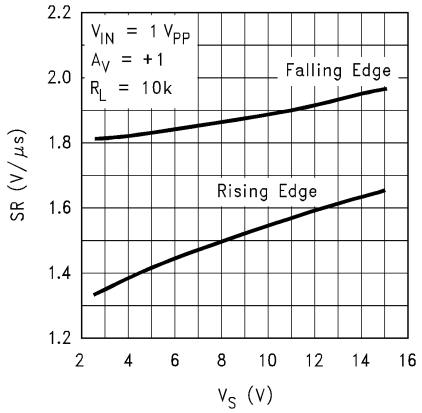


Figure 5-23. Slew Rate vs Supply Voltage

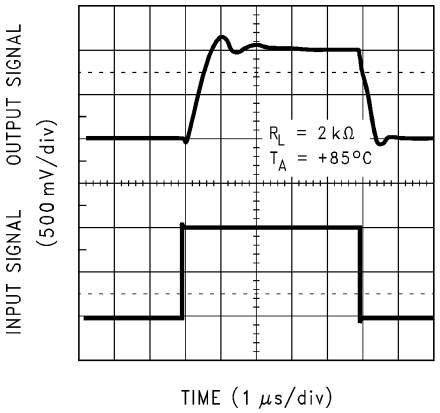


Figure 5-24. Non-Inverting Large Signal Response

5.6 Typical Characteristics (continued)

at V_S = 2.7V, single supply, and T_A = 25°C (unless otherwise noted)

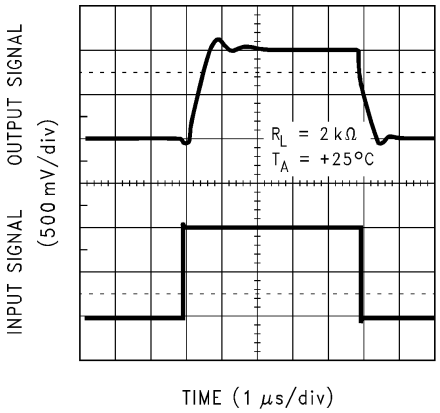


Figure 5-25. Non-Inverting Large Signal Response

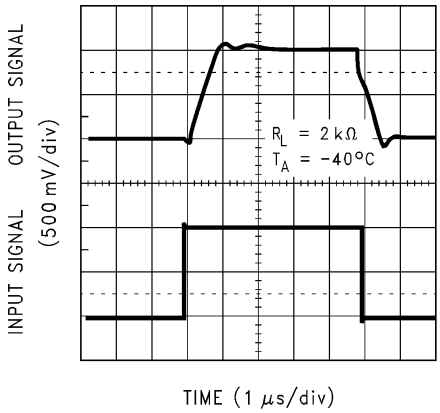


Figure 5-26. Non-Inverting Large Signal Response

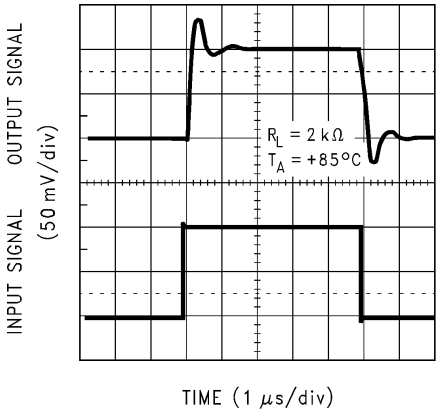


Figure 5-27. Non-Inverting Small Signal Response

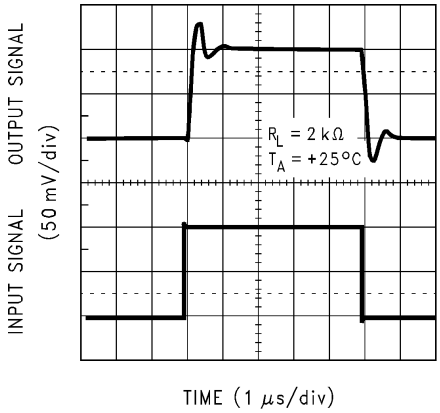


Figure 5-28. Non-Inverting Small Signal Response

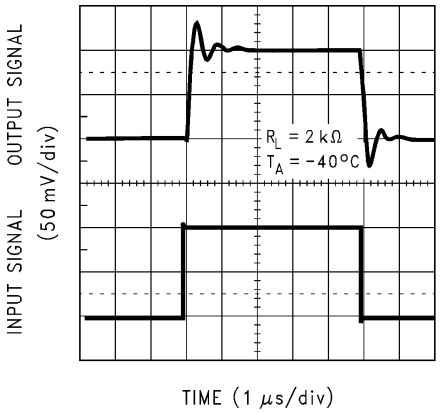


Figure 5-29. Non-Inverting Large Signal Response

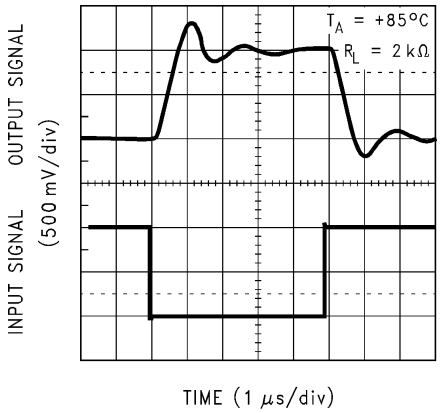


Figure 5-30. Inverting Large Signal Response

5.6 Typical Characteristics (continued)

at V_S = 2.7V, single supply, and T_A = 25°C (unless otherwise noted)

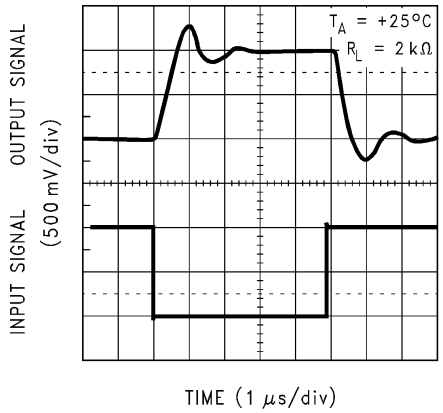


Figure 5-31. Inverting Large Signal Response

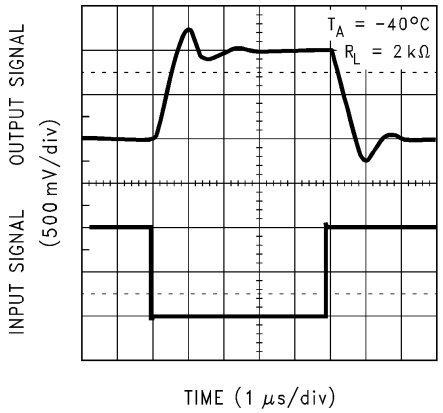


Figure 5-32. Inverting Large Signal Response

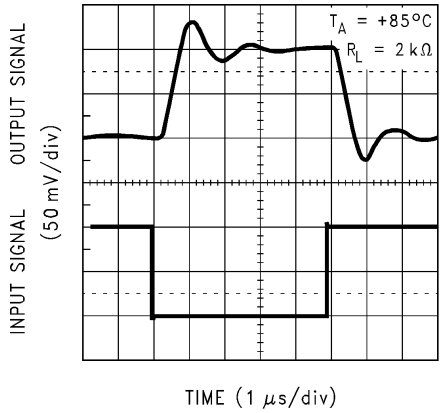


Figure 5-33. Inverting Small Signal Response

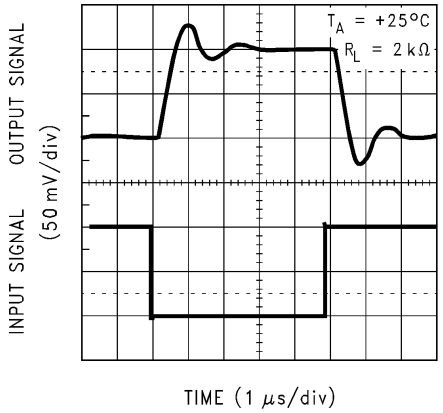


Figure 5-34. Inverting Small Signal Response

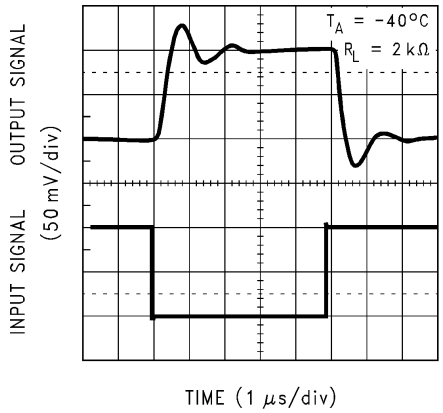


Figure 5-35. Inverting Small Signal Response

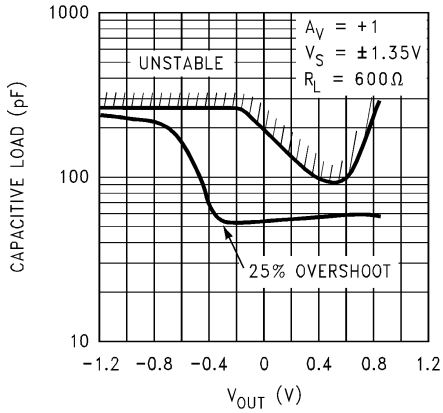


Figure 5-36. Stability vs Capacitive Load

5.6 Typical Characteristics (continued)

at V_S = 2.7V, single supply, and T_A = 25°C (unless otherwise noted)

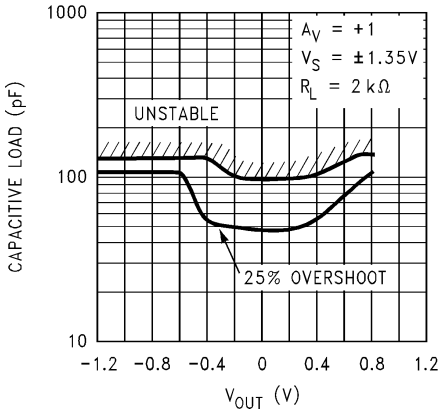


Figure 5-37. Stability vs Capacitive Load

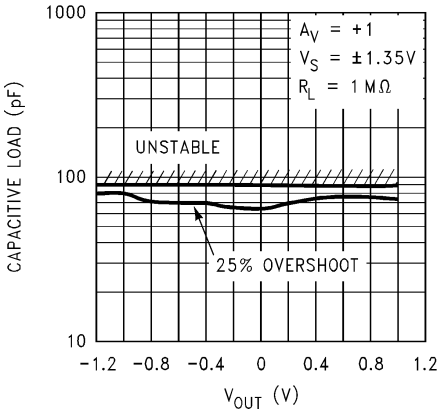


Figure 5-38. Stability vs Capacitive Load

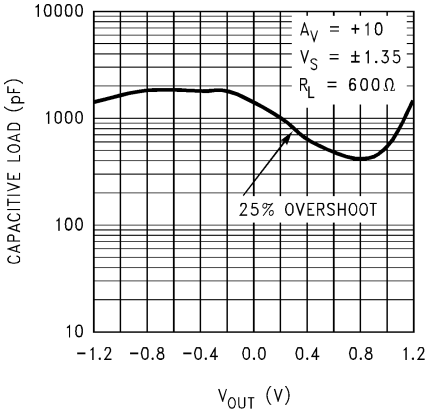


Figure 5-39. Stability vs Capacitive Load

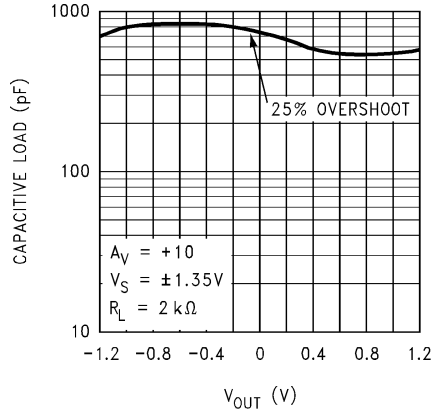


Figure 5-40. Stability vs Capacitive Load

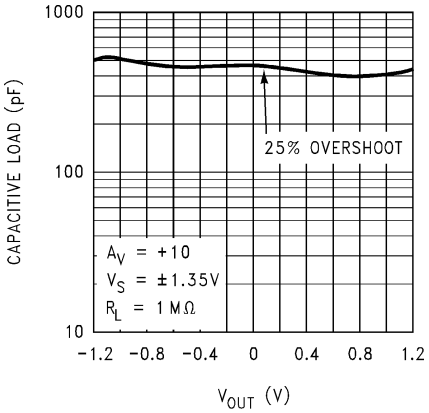


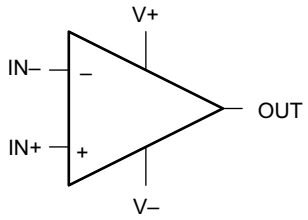
Figure 5-41. Stability vs Capacitive Load

6 Detailed Description

6.1 Overview

The LMC6035-Q1 operational amplifiers are designed to provide very low leakage current. The femtoampere leakage current level makes these op amps an excellent choice for buffering very high impedance sources. The LMC6035-Q1 is capable of operating over a wide supply voltage range and as low as 2V. The low supply operation and AEC-Q100 Grade 3 qualification make the LMC6035-Q1 an excellent choice for a wide range of automotive applications.

6.2 Functional Block Diagram



7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Capacitive Load Tolerance

Like many other op amps, the LMC6035-Q1 can oscillate when the applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See also Section 5.6.

The load capacitance interacts with the op amp output resistance to create an additional pole. If this pole frequency is sufficiently low, the pole degrades the op amp phase margin so that the amplifier is no longer stable at low gains. Figure 7-1 shows that the addition of a small resistor (50Ω to 100Ω) in series with the op amp output, and a capacitor (5pF to 10pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus, larger values of capacitance can be tolerated without oscillation. In all cases, the output rings heavily when the load capacitance is near the threshold for oscillation.

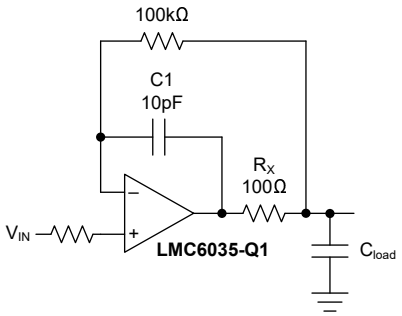


Figure 7-1. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pullup resistor to V+ (shown in Figure 7-2). Typically a pullup resistor conducting 500µA or greater significantly improves capacitive-load responses. The value of the pullup resistor is determined based on the current sinking capability of the amplifier with respect to the desired output swing. The open-loop gain of the amplifier can also be affected by the pullup resistor (see the *Electrical Characteristics*).

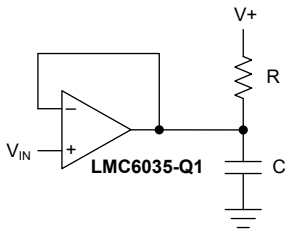


Figure 7-2. Compensating for Large Capacitive Loads With a Pullup Resistor

7.2 Typical Applications

7.2.1 Differential Driver

The LMC6035-Q1 is an excellent choice for low-voltage applications. A desirable feature that the LMC6035-Q1 brings to low-voltage applications is the output drive capability—a hallmark for TI's CMOS amplifiers. The circuit of Figure 7-3 illustrates the drive capability of the LMC6035-Q1 at 3V of supply. These devices are used as a differential output driver for a one-to-one audio transformer, like those used for isolating ground from the telephone lines. The transformer (T1) loads the op amps with about 600Ω of ac load, at 1kHz. Capacitor C1 functions to block dc from the low winding resistance of T1. Although the value of C1 is relatively high, the capacitive load reactance (X_C) is negligible compared to inductive reactance (X_I) of T1.

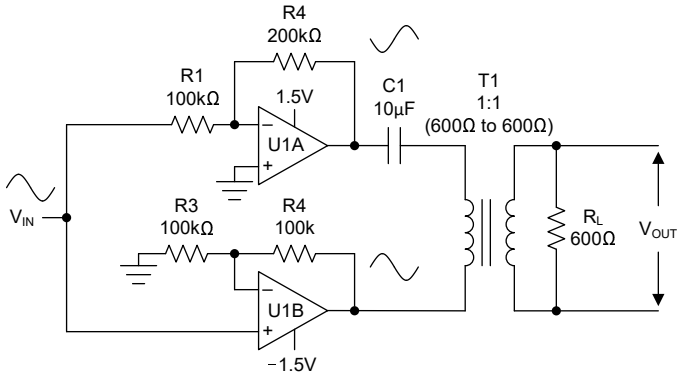


Figure 7-3. Differential Driver

The circuit in Figure 7-3 consists of one input signal and two output signals. U1A amplifies the input with an inverting gain of −2, while the U1B amplifies the input with a non-inverting gain of +2. The two outputs are 180° out of phase with each other; therefore, the gain across the differential output is 4. As the differential output swings between the supply rails, one of the op amps sources the current to the load, while the other op amp sinks the current.

How good a CMOS op amp can sink or source a current is an important factor in determining output swing capability. The output stage of the LMC6035-Q1—like many op amps—sources and sinks output current through two complementary transistors in series. This *totem pole* arrangement translates to a channel resistance (R_{dson}) at each supply rail that acts to limit the output swing. Most CMOS op amps are able to swing the outputs very close to the rails; except, however, under the difficult conditions of low supply voltage and heavy load. The LMC6035-Q1 exhibits exceptional output swing capability under these conditions.

The scope photos of Figure 7-4 and Figure 7-5 represent measurements taken directly at the output (relative to GND) of U1A, in Figure 7-3. Figure 7-4 illustrates the output swing capability of the LMC6035-Q1, while Figure 7-5 provides a benchmark comparison. (The benchmark op amp is another low-voltage (3V) op amp manufactured by one of our reputable competitors.)

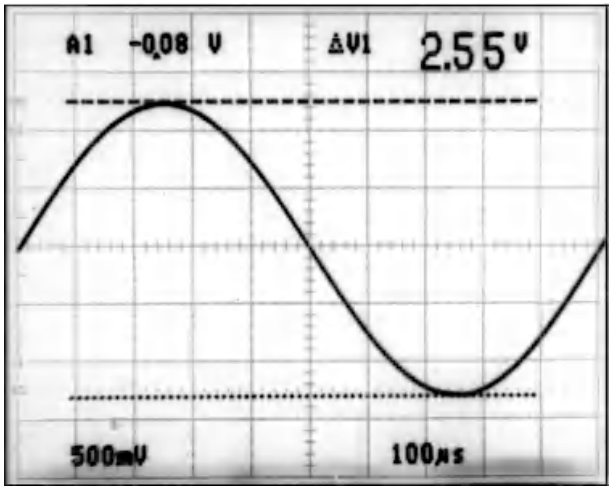


Figure 7-4. Output Swing Performance of the LMC6035-Q1 per the Circuit of Figure 7-3

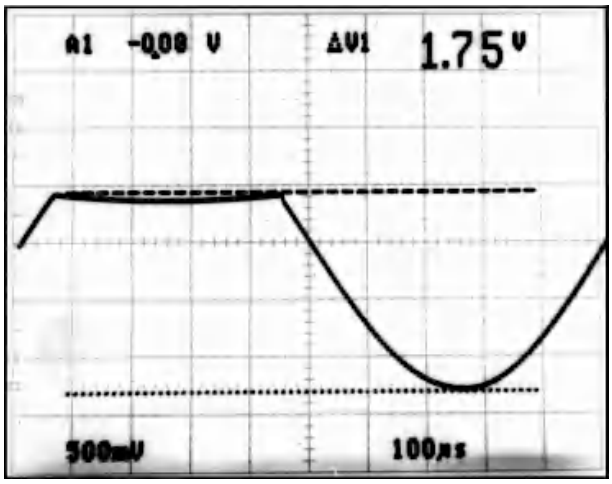


Figure 7-5. Output Swing Performance of Benchmark Op Amp per the Circuit of Figure 7-3

Notice the excellent drive capability of LMC6035-Q1 when compared with the benchmark measurement—even though the benchmark op amp uses twice the supply current.

Not only does the LMC6035-Q1 provide excellent output swing capability at low supply voltages, but these devices also maintain high open-loop gain (A_{OL}) with heavy loads. To illustrate this, the LMC6035-Q1 and the benchmark op amp were compared for distortion performance in the circuit of Figure 7-3. Figure 7-6 shows this comparison. The y-axis represents percent total harmonic distortion (THD + noise) across the loaded secondary of T1. The x-axis represents the input amplitude of a 1kHz sine wave. (Notice that T1 loses about 20% of the voltage to the voltage divider of R_L (600Ω) and T1 winding resistances—a performance deficiency of the transformer.)

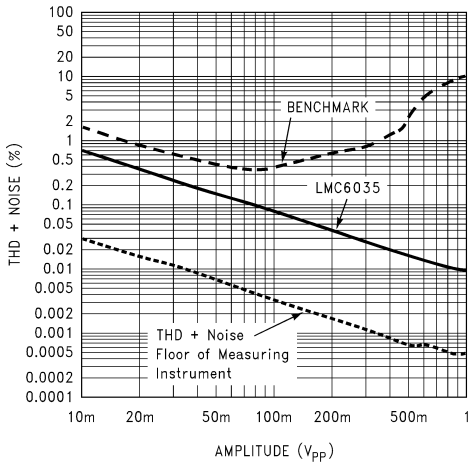


Figure 7-6. THD+Noise Performance of LMC6035-Q1 and *Benchmark* per Circuit of Figure 7-3

Figure 7-6 shows the excellent distortion performance of the LMC6035-Q1 over that of the benchmark op amp. The heavy loading of the circuit causes the A_{OL} of the benchmark part to drop significantly, which causes increased distortion.

7.2.2 Low-Pass Active Filter

A common application for low voltage systems is active filters, in cordless and cellular phones for example. The ultra low input bias currents (I_B) of the LMC6035-Q1 makes this op amp an excellent for low power active filter applications, because the low input bias current allows the use of higher resistor values and lower capacitor values. This reduces power consumption and space.

Figure 7-7 shows a low pass, active filter with a Butterworth (maximally flat) frequency response. The topology is a Sallen and Key filter with unity gain. Note the normalized component values in parenthesis which are obtainable from standard filter design handbooks. These values provide a 1Hz cutoff frequency, but can be easily scaled for a desired cutoff frequency (f_c). The bold component values of Figure 7-7 provide a cutoff frequency of 3kHz. An example of the scaling procedure follows Figure 7-7.

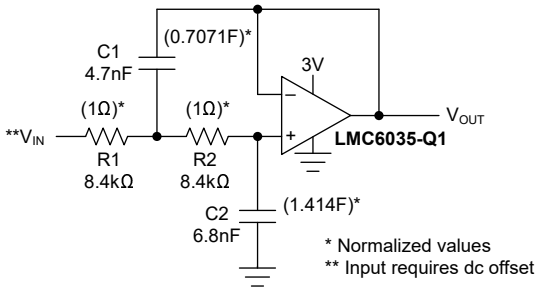


Figure 7-7. 2-Pole, 3kHz, Active, Sallen and Key, Low-Pass Filter With Butterworth Response

7.2.2.1 Low-Pass Frequency Scaling Procedure

The actual component values represented in bold of Figure 7-7 were obtained with the following scaling procedure:

1. First determine the frequency scaling factor (FSF) for the desired cutoff frequency. Choosing f_c at 3kHz, provides the following FSF computation:

$$\mathrm{FSF} = 2\pi \times 300\mathrm{kHz} = 18.84\mathrm{k} \tag{1}$$

2. Then divide all of the normalized capacitor values by the FSF as follows (C1' and C2': prior to impedance scaling):

$$\mathrm{C1}' = \frac{\mathrm{C1_{normalized}}}{\mathrm{FSF}} = \frac{0.707}{18.84\mathrm{k}} = 37.93 \times 10^{-6}\mathrm{F} \tag{2}$$

$$\mathrm{C2}' = \frac{\mathrm{C1_{normalized}}}{\mathrm{FSF}} = \frac{1.414}{18.84\mathrm{k}} = 75.05 \times 10^{-6}\mathrm{F} \tag{3}$$

3. Last, choose an impedance scaling factor (Z). This Z factor can be calculated from a standard value for C2. Then Z can be used to determine the remaining component values as follows:

$$\mathrm{Z} = \frac{\mathrm{C2}'}{\mathrm{C2_{chosen}}} = \frac{75.05 \times 10^{-6}\mathrm{F}}{6.8\mathrm{nF}} = 8.4\mathrm{k} \tag{4}$$

$$\mathrm{C1} = \frac{\mathrm{C1}'}{\mathrm{Z}} = \frac{37.93 \times 10^{-6}\mathrm{F}}{8.4\mathrm{k}} = 4.52\mathrm{nF} \tag{5}$$

$$\mathrm{R1} = \mathrm{R1_{normalized}} \times \mathrm{Z} = 1\Omega \times 8.4\mathrm{k} = 8.4\mathrm{k}\Omega \tag{6}$$

$$\mathrm{R2} = \mathrm{R2_{normalized}} \times \mathrm{Z} = 1\Omega \times 8.4\mathrm{k} = 8.4\mathrm{k}\Omega \tag{7}$$

4. A standard value of 8.45kΩ is chosen for R1 and R2.

7.2.3 High-Pass Active Filter

The previous low-pass filter circuit of Figure 7-7 converts to a high-pass active filter per Figure 7-8.

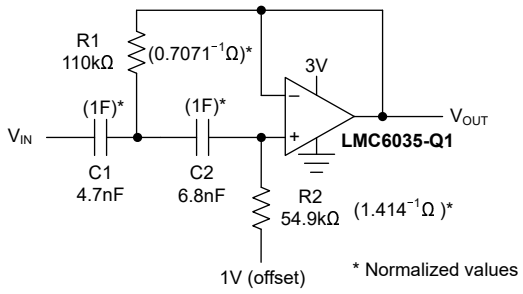


Figure 7-8. 2-Pole, 300Hz, Sallen and Key, High-Pass Filter

7.2.3.1 High-Pass Frequency Scaling Procedure

Choose a standard capacitor value and scale the impedances in the circuit according to the desired cutoff frequency (300Hz) as follows:

$$C = C1 = C2 \tag{8}$$

$$Z = \frac{1}{2\pi f_c C} = \frac{1}{2\pi \times 300\text{Hz} \times 6.8\text{nF}} = 78.05\text{k}\Omega \tag{9}$$

$$R1 = Z \times R1_{\text{normalized}} = 78.05\text{k}\Omega \times \frac{1}{0.707} = 110.4\text{k}\Omega \tag{10}$$

A standard value of 110kΩ is chosen for R1.

$$R2 = Z \times R2_{\text{normalized}} = 78.05\text{k}\Omega \times \frac{1}{1.414} = 55.2\text{k}\Omega \tag{11}$$

A standard value of 54.9kΩ is chosen for R2.

7.2.4 Dual-Amplifier Bandpass Filter

The dual-amplifier bandpass (DABP) filter features the ability to independently adjust f_c and Q. In most other bandpass topologies, the f_c and Q adjustments interact with each other. The DABP filter also offers both low sensitivity to component values and a high Q. The following application of Figure 7-9, provides a 1kHz center frequency and a Q of 100.

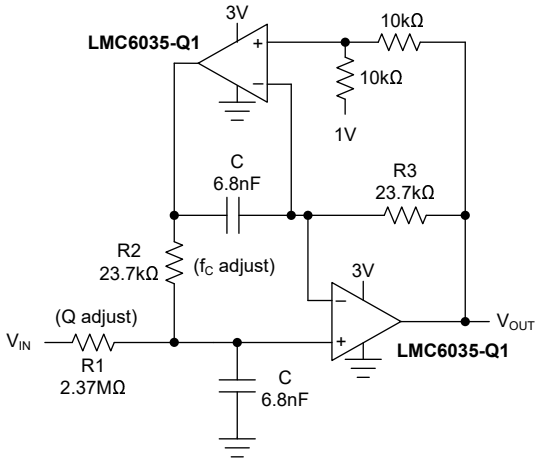


Figure 7-9. Active 2-Pole Bandpass Filter (1kHz)

7.2.4.1 DABP Component Selection Procedure

Component selection for the DABP filter is performed as follows:

1. First choose a center frequency (f_c). Figure 7-9 represents component values that were obtained from the following computation for a center frequency of 1kHz.

$$R2 = R3 = \frac{1}{2\pi f_C C} \tag{12}$$

Given that f_c = 1kHz and $C_{(chosen)}$ = **6.8nF**:

$$R2 = R3 = \frac{1}{2\pi \times 1\text{kHz} \times 6.8\text{nF}} = 23.4\text{k}\Omega \tag{13}$$

A standard value resistor, 23.7kΩ is chosen.

2. Then compute R1 for a desired Q (f_c / BW) as follows:

$$R1 = Q \times R2 \tag{14}$$

Choosing a Q of 100, the resistor R1 can be computed as follows: $R1 = 100 \times 23.7\text{k}\Omega = 2.37\text{M}\Omega$ (15)

7.3 Layout

7.3.1 Layout Guidelines

7.3.1.1 Printed Circuit Board (PCB) Layout for High-Impedance Work

Any circuit that must operate with < 1000pA of leakage current requires special layout of the PCB. To take advantage of the ultra-low bias current of the LMC6035-Q1 (typically < 0.04pA), an excellent layout is essential. Fortunately, the techniques for obtaining low leakages are quite simple. First, do not ignore the surface leakage of the PCB, even though at times the surface leakage can appear acceptably low. Under conditions of high humidity, dust, or contamination, the surface leakage can be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6035-Q1 inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, and so on, connected to the op-amp inputs. See also Figure 7-14. To have a significant effect, place guard rings on both the top and bottom of the PCB. This PCB foil must then be connected to a voltage that is at the same voltage as the amplifier inputs (because no leakage current can flow between two points at the same potential). For example, a PCB trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, can leak 5pA if the trace is a 5V bus adjacent to the pad of an input. This configuration can cause a 100 times degradation from the actual performance of the amplifier. However, if a guard ring is held within 5mV of the inputs, then even a resistance of $10^{11}\Omega$ causes only 0.05pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier performance. See Figure 7-10 through Figure 7-12 for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see also Figure 7-13.

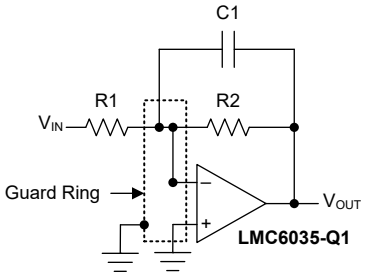


Figure 7-10. Guard Ring Connections: Inverting Amplifier

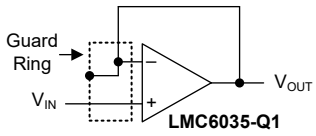


Figure 7-12. Guard Ring Connections: Follower

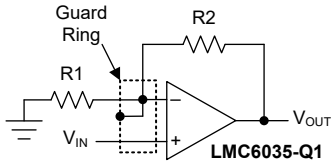


Figure 7-11. Guard Ring Connections: Noninverting Amplifier

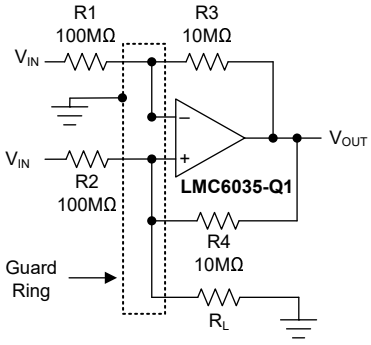


Figure 7-13. Howland Current Pump

A more comprehensive discussion on high impedance circuit design and considerations, see also *Measurement and Calibration Techniques for Ultra-low Current Measurement Systems* application note.

7.3.2 Layout Example

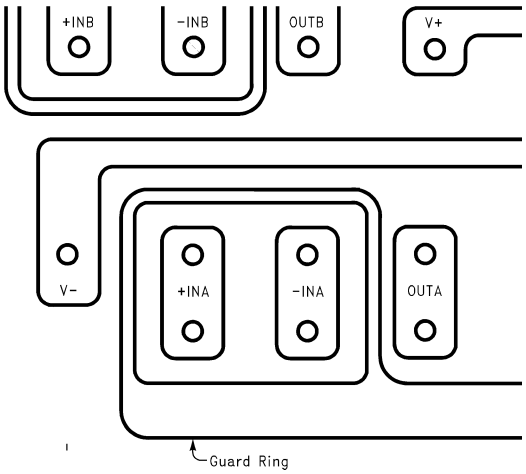


Figure 7-14. Layout Example: Using the LMC6035-Q1 Guard Ring in PCB Layout

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.4 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision SNOS875G (April 2013) to Revision * (December 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added the *Pin Configuration and Functions, Specifications, ESD Ratings, Recommended Operating Conditions, Thermal Information, Detailed Description, Overview, Functional Block Diagram, Application and Implementation, Application Information, Typical Applications, Power Supply Recommendations, Layout, Layout Guidelines, Layout Example, Device and Documentation Support, and Mechanical, Packaging, and Orderable Information* sections	1
• Moved LMC6035-Q1 from SBOS875G to SBOSAM6	1
• Updated *Features*	1
• Updated *Description*	1
• Deleted Figure 1, *8-Bump DSBGA Package*	1
• Added difference amplifier application with RES11 image	1
• Updated figures and tables in *Pin Configuration and Functions*	3
• Updated parameter names and symbols	5
• Moved previous table note 4 into open-loop gain test conditions	5
• Updated previous table note 2 from *AC Electrical Characteristics* and moved conditions to slew rate test conditions	5
• Moved previous table note 3 from *AC Electrical Characteristics* to crosstalk test conditions	5
• Changed A_{VOL} to A_{OL}	16
• Updated Figure 7-7	18

- Updated Figure 7-8 19
- Updated Figure 7-9 20
- Added reference to *Measurement and Calibration Techniques for Ultra-low Current Measurement Systems* application note in *Printed Circuit Board (PCB) Layout for High-Impedance Work* 21

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMC6035IMXQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC60 35IMQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LMC6035-Q1 :

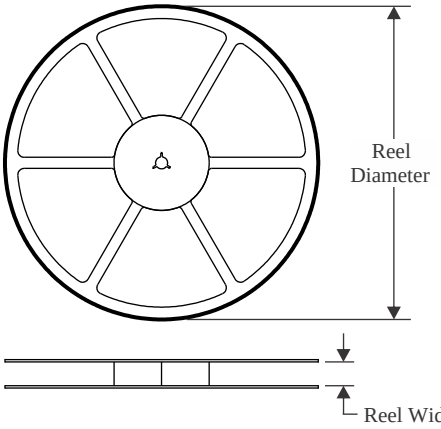
- Catalog : LMC6035

NOTE: Qualified Version Definitions:

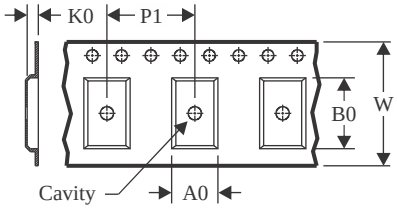
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

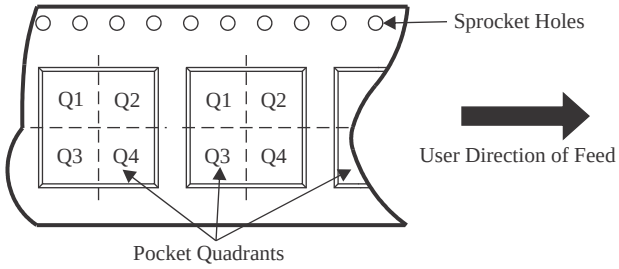


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

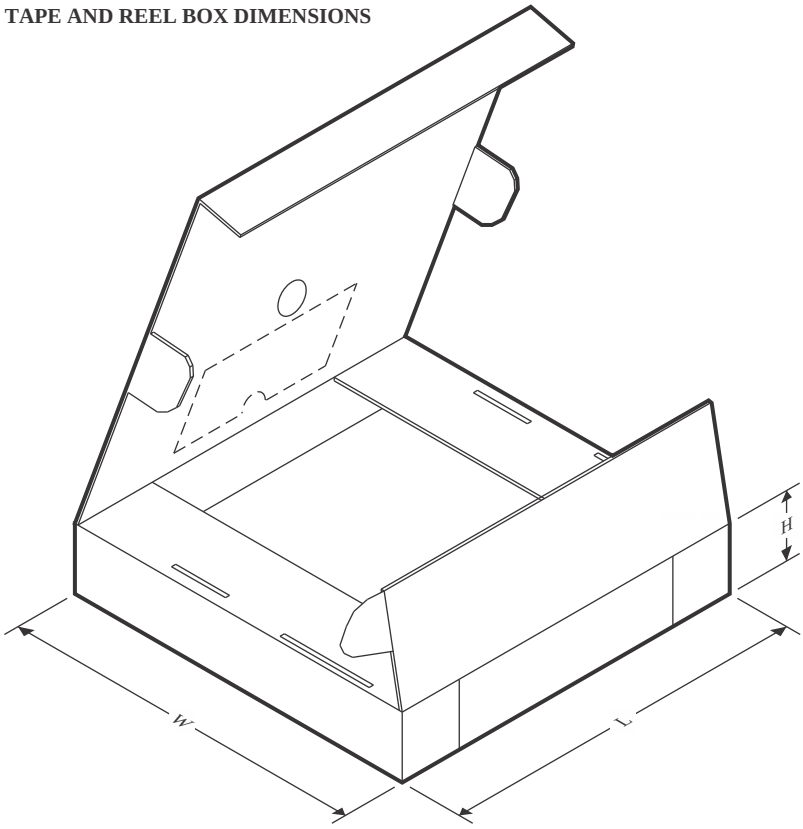
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

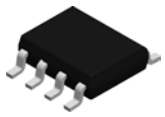
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC6035IMXQ1	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC6035IMXQ1	SOIC	D	8	2500	367.0	367.0	35.0

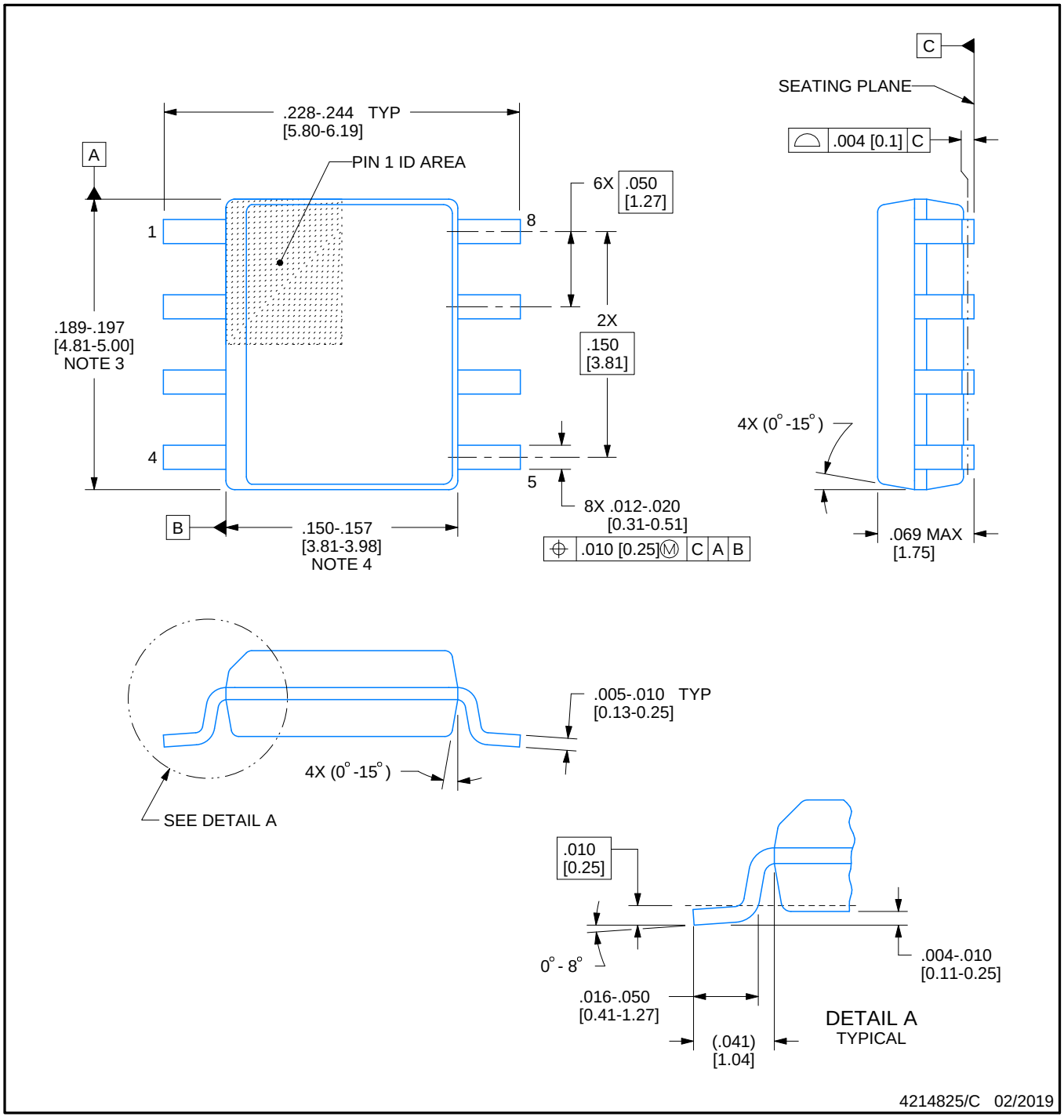


PACKAGE OUTLINE

D0008A

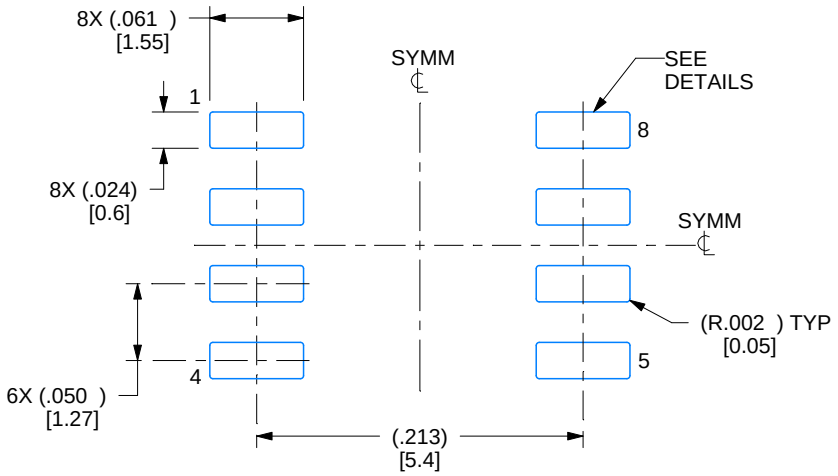
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

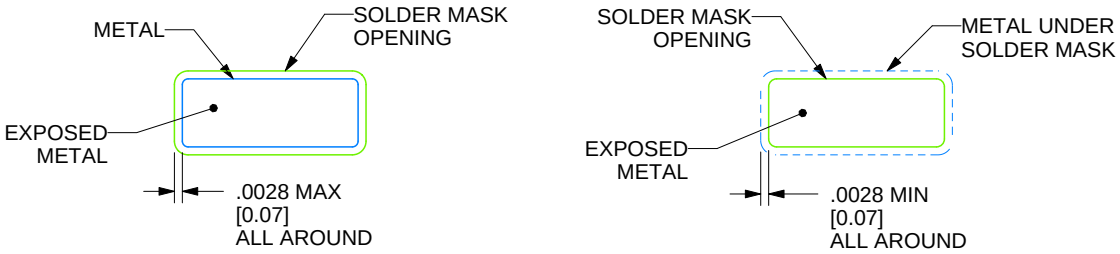


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

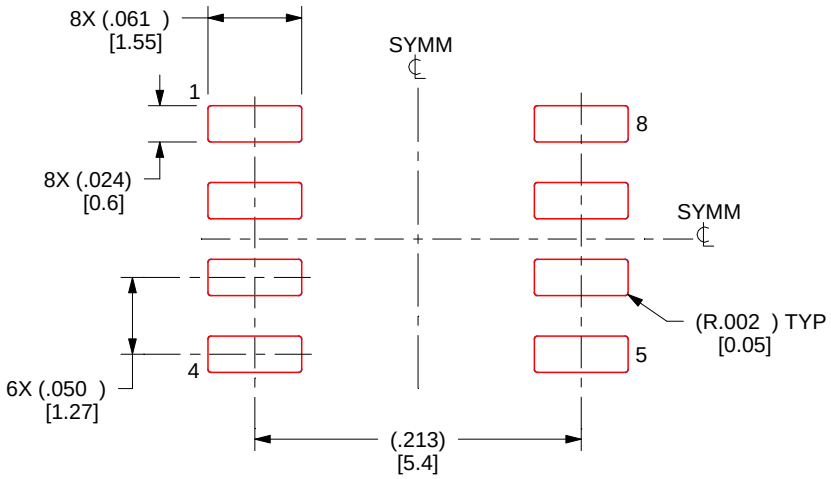
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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