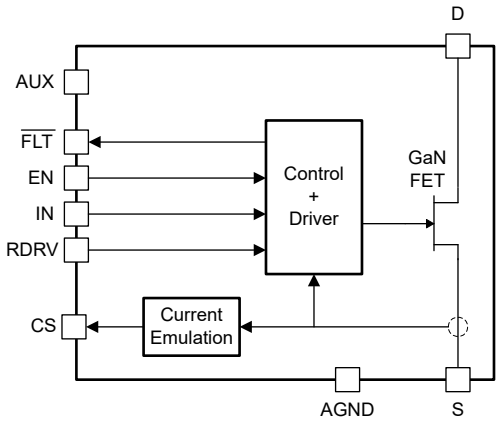
LMG3626 650-V 270-mΩ GaN FET With Integrated Driver and Current-Sense Emulation

1 Features

- 650-V 270-mΩ GaN power FET
- Integrated gate driver with low propagation delays and adjustable turn-on slew-rate control
- Current-sense emulation with high bandwidth and high accuracy
- Cycle-by-cycle overcurrent protection
- Overtemperature protection with $\overline{\text{FLT}}$ pin reporting
- AUX quiescent current: 240 µA
- AUX standby quiescent current: 50 µA
- Maximum supply and input logic pin voltage: 26 V
- 8 mm × 5.3 mm QFN package with thermal pad

2 Applications

- AC/DC adapters and chargers
- AC/DC USB wall outlet power supplies
- AC/DC auxiliary power supplies
- Mobile wall charger design
- USB wall power outlet
- Auxiliary-power supplies



Simplified Block Diagram

3 Description

The LMG3626 is a 650-V 270-mΩ GaN power FET intended for switch-mode power-supply applications. The LMG3626 simplifies design and reduces component count by integrating the GaN FET and gate driver in a 8-mm by 5.3-mm QFN package.

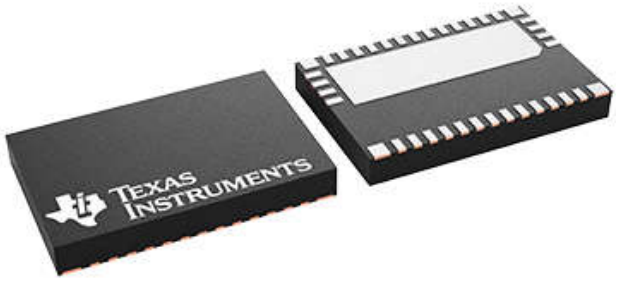
Programmable turn-on slew rates provide EMI and ringing control. The current-sense emulation reduces power dissipation compared to the traditional current-sense resistor and allows the low-side thermal pad to be connected to the cooling PCB power ground.

The LMG3626 supports converter light-load efficiency requirements and burst-mode operation with low quiescent currents and fast start-up times. Protection features include under-voltage lockout (UVLO), cycle-by-cycle current limit, and overtemperature protection. Overtemperature protection is reported with the open-drain $\overline{\text{FLT}}$ pin.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LMG3626	REQ (VQFN, 38)	8 mm × 5.3 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



38-Pin VQFN

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4 Pin Configuration and Functions

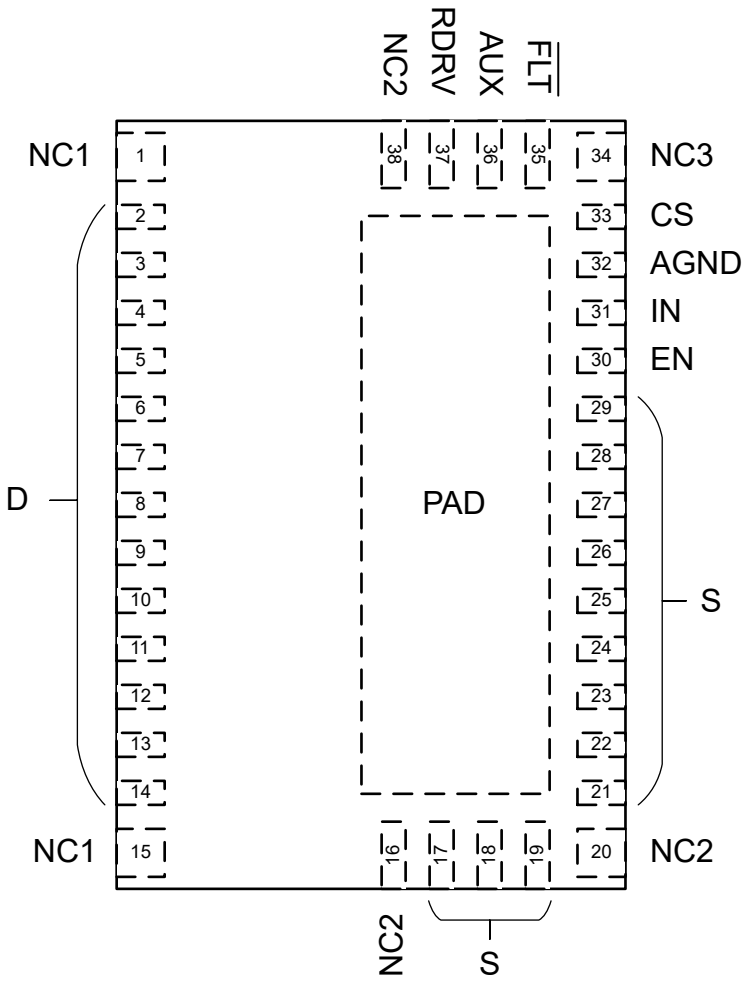


Figure 4-1. REQ Package, 38-Pin VQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
NC1	1, 15	NC	Used to anchor QFN package to PCB. Pins must be soldered to PCB landing pads. The PCB landing pads are non-solder mask defined pads and must not be physically connected to any other metal on the PCB. Internally connected to D.
D	2-14	P	GaN FET drain. Internally connected to NC1.
NC2	16, 20, 38	NC	Used to anchor QFN package to PCB. Pins must be soldered to PCB landing pads. The PCB landing pads are non-solder mask defined pads and must not be physically connected to any other metal on the PCB. Internally connected to AGND, S and, PAD.
S	17-19, 21-29	P	GaN FET source. Internally connected to AGND, PAD, and NC2.
EN	30	I	Enable. Used to toggle between active and standby modes. The standby mode has reduced quiescent current to support converter light load efficiency targets. There is a forward based ESD diode from EN to AUX so avoid driving EN higher than AUX.
IN	31	I	Gate-drive control input. There is a forward based ESD diode from IN to AUX so avoid driving IN higher than AUX.
AGND	32	GND	Analog ground. Internally connected to S, PAD, and NC2.
CS	33	O	Current-sense emulation output. Outputs scaled replica of the GaN FET current. Feed output current into a resistor to create a current sense voltage signal. The resistor should be referenced to the power supply controller IC local ground. This function replaces the external current sense resistor that is used in series with the FET source.
NC3	34	NC	Used to anchor QFN package to PCB. Pin must be soldered to a PCB landing pad. The PCB landing pad is non-solder mask defined pads and must not be physically connected to any other metal on the PCB. Pin not connected internally.
$\overline{\text{FLT}}$	35	O	Active-low fault output. Open-drain output that asserts during overtemperature protection.
AUX	36	P	Auxiliary voltage rail. Device supply voltage. Connect a local bypass capacitor between AUX and AGND.
RDRV	37	I	Drive strength control resistor. Set a resistance between RDRV and AGND to program the GaN FET turn-on slew rate.
PAD	—	—	Thermal pad. Internally connected to S, AGND, and NC2. All the S current may be conducted with PAD (PAD = S).

(1) I = input, O = output, I/O = input or output, GND = ground, P = power, NC = no connect.

5 Specifications

5.1 Absolute Maximum Ratings

Unless otherwise noted: voltages are respect to AGND(1)

			MIN	MAX	UNIT
V_{DS}	Drain-source (D to S) voltage, FET off			650	V
$V_{DS(surge)}$	Drain-source (D to S) voltage, surge condition, FET off(2)			720	V
$V_{DS(tr)(surge)}$	Drain-source (D to S) transient ringing peak voltage, surge condition, FET off(2)			800	V
	Pin voltage	AUX	–0.3	30	V
		EN, IN, $\overline{FLT}$	–0.3	V_{AUX} + 0.3	V
		CS	–0.3	5.5	V
		RDRV	–0.3	4	V
$I_{D(cnts)}$	Drain (D to S) continuous current, FET on		–4	Internally limited	A
$I_{D(pulse)(oc)}$	Drain (D to S) pulsed current during overcurrent response time(3)			10.7	A
$I_{S(cnts)}$	Source (S to D) continuous current, FET off			4	A
	Positive sink current	CS		10	mA
		$\overline{FLT}$ (while asserted)		Internally limited	mA
T_J	Operating junction temperature		–40	150	°C
T_{stg}	Storage temperature		–40	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) See GaN Power FET Switching Capability for more information on the GaN power FET switching capability.
(3) GaN power FET may self-limit below this value if it enters saturation.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Pins 1 through 15	±1000	V
			Pins 16 through 38	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)		±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Unless otherwise noted: voltages are respect to AGND

			MIN	NOM	MAX	UNIT
	Supply voltage	AUX	10		26	V
	Input voltage	EN, IN	0		V_{AUX}	V
	Pull-up voltage on open-drain output	$\overline{FLT}$	0		V_{AUX}	V
V_{IH}	High-level input voltage	EN, IN	2.5			V
V_{IL}	Low-level input voltage				0.6	V
$I_{D(cnts)}$	Drain (D to S) continuous current, FET on		–3.2		3.2	A
C_{AUX}	AUX to AGND capacitance from external bypass capacitor		0.030			µF
R_{RDRV}	RDRV to AGND resistance from external slew-rate control resistor to configure below slew rate settings					
	slew rate setting 0 (slowest)		90	120	open	kΩ
	slew rate setting 1		42.5	47	51.5	kΩ
	slew rate setting 2		20	22	24	kΩ
	slew rate setting 3 (fastest)		0	5.6	11	kΩ

5.4 Thermal Information

THERMAL METRIC(1)		LMG3626 REQ (VQFN) 38 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	27	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.13	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

1) Symbol definitions: I_D = D to S current; I_S = S to D current; $I_{CS(src)}$ = current out of CS; 2) Unless otherwise noted: voltage, resistance, and capacitance are respect to AGND; –40°C ≤ T_J ≤ 125°C; 10 V ≤ V_{AUX} ≤ 26 V; V_{EN} = 5 V; V_{IN} = 0 V; R_{RDRV} = 0 Ω; R_{CS} = 100 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GAN POWER FET						
$R_{DS(on)}$	Drain-source (D to S) on resistance	V_{IN} = 5 V, I_D = 1.9 A, T_J = 25°C		270		mΩ
		V_{IN} = 5 V, I_D = 1.9 A, T_J = 125°C		484		
I_{DSS}	Drain (D to S) leakage current	V_{DS} = 650 V, T_J = 25°C		1.3		µA
		V_{DS} = 650 V, T_J = 125°C		7		
Q_{OSS}	Output (D to S) charge	V_{DS} = 400 V		14		nC
C_{OSS}	Output (D to S) capacitance			22.1		pF
E_{OSS}	Output (D to S) capacitance stored energy			2		µJ
$C_{OSS,er}$	Energy related effective output (D to S) capacitance			24.5		pF
$C_{OSS,tr}$	Time related effective output (D to S) capacitance	V_{DS} = 0 V to 400 V		34.4		pF
Q_{RR}	Reverse recovery charge			0		nC
OVERCURRENT PROTECTION						
$I_{T(OC)}$	Overcurrent fault - threshold current		3.2	3.6	4	A
CS						
	Current sense gain ($I_{CS(src)}$ / I_D)	V_{IN} = 5 V, 0 V ≤ V_{CS} ≤ 2 V, 0 A ≤ I_D < $I_{T(OC)}$		1.633		mA/A
	Current sense input offset current	V_{IN} = 5 V, 0 V ≤ V_{CS} ≤ 2 V, 0 A ≤ I_D < $I_{T(OC)}$	–30		30	mA
	Initial held output after overcurrent fault occurs while IN remains high	V_{IN} = 5 V, 0 V ≤ V_{CS} ≤ 2 V			7	mA
$I_{CS(src)(OC)(final)}$	Final held output after overcurrent fault occurs while IN remains high	V_{IN} = 5 V, 0 V ≤ V_{CS} ≤ 2 V	10	12	15.5	mA
	Output clamp voltage	V_{IN} = 5 V, I_D = 3.1 A, CS sinking 5 mA from external source		2.55		V
EN, IN						
V_{IT+}	Positive-going input threshold voltage		1.7		2.45	V
$V_{IT–}$	Negative-going input threshold voltage		0.7		1.3	V
	Input threshold voltage hysteresis			1		V
	Pull-down input resistance	0 V ≤ V_{PIN} ≤ 3 V	200	400	600	kΩ
	Pull-down input current	10 V ≤ V_{PIN} ≤ 26 V; V_{AUX} = 26 V		10		µA

5.5 Electrical Characteristics (continued)

1) Symbol definitions: I_D = D to S current; I_S = S to D current; $I_{CS(src)}$ = current out of CS; 2) Unless otherwise noted: voltage, resistance, and capacitance are respect to AGND; –40°C ≤ T_J ≤ 125°C; 10 V ≤ V_{AUX} ≤ 26 V; V_{EN} = 5 V; V_{IN} = 0 V; R_{RDRV} = 0 Ω; R_{CS} = 100 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVERTEMPERATURE PROTECTION						
	Temperature fault – postive-going threshold temperature			165		°C
	Temperature fault – negative-going threshold temperature			145		°C
	Temperature fault – threshold temperature hysteresis			20		°C
$\overline{FLT}$						
	Low-level output voltage	$\overline{FLT}$ sinking 1 mA while asserted			200	mV
	Off-state sink current	$V_{\overline{FLT}}$ = V_{AUX} while de-asserted			1	µA
AUX						
$V_{AUX,T+}$ (UVLO)	UVLO – positive-going threshold voltage		8.9	9.3	9.7	V
	UVLO – negative-going threshold voltage		8.6	9.0	9.4	V
	UVLO – threshold voltage hysteresis			250		mV
	Standby quiescent current	V_{EN} = 0 V		50	80	µA
	Quiescent current			240	360	µA
	Operating current	V_{IN} = 0 V or 5 V, V_{DS} = 0 V, I_D = 0 A, f_{IN} = 500 kHz		1.5		mA

5.6 Switching Characteristics

1) Symbol definitions: I_D = D to S current; I_S = S to D current; $I_{CS(src)}$ = current out of CS; 2) Unless otherwise noted: voltage, resistance, and capacitance are respect to AGND; –40°C ≤ T_J ≤ 125°C; 10 V ≤ V_{AUX} ≤ 26 V; V_{EN} = 5 V; V_{IN} = 0 V; R_{RDRV} = 0 Ω; R_{CS} = 100 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GAN POWER FET						
$t_{d(on)}$ (Idrain)	Drain current turn-on delay time	From V_{IN} > $V_{IN,IT+}$ to I_D > 25 mA, V_{BUS} = 400 V, L_{HB} current = 1 A, at following slew rate settings, see GaN Power FET Switching Parameters				
		slew rate setting 0 (slowest)		77		ns
		slew rate setting 1		34		
		slew rate setting 2		28		
		slew rate setting 3 (fastest)		23		
$t_{d(on)}$	Turn-on delay time	From V_{IN} > $V_{IN,IT+}$ to V_{DS} < 320 V, V_{BUS} = 400 V, L_{HB} current = 1 A, at following slew rate settings, see GaN Power FET Switching Parameters				
		slew rate setting 0 (slowest)		97		ns
		slew rate setting 1		44		
		slew rate setting 2		35		
		slew rate setting 3 (fastest)		26		
$t_{d(off)}$	Turn-off delay time	From V_{IN} < $V_{IN,IT-}$ to V_{DS} > 80 V, V_{BUS} = 400 V, L_{HB} current = 1 A, (independent of slew rate setting), see GaN Power FET Switching Parameters		32		ns
$t_{f(off)}$	Turn-off fall time	From V_{DS} > 80 V to V_{DS} > 320 V, V_{BUS} = 400 V, L_{HB} current = 1 A, (independent of slew rate setting), see GaN Power FET Switching Parameters		24		ns
	Turn-on slew rate	From V_{DS} < 250 V to V_{DS} < 150 V, T_J = 25°C, V_{BUS} = 400 V, L_{HB} current = 1 A, at following slew rate settings, see GaN Power FET Switching Parameters				
		slew rate setting 0 (slowest)		20		V/ns
		slew rate setting 1		50		
		slew rate setting 2		75		
		slew rate setting 3 (fastest)		150		
CS						
t_r	Rise time	From $I_{CS(src)}$ > 0.1 × $I_{CS(src)(final)}$ to $I_{CS(src)}$ > 0.9 × $I_{CS(src)(final)}$, 0 V ≤ V_{CS} ≤ 2 V, enabled into a 1-A load			35	ns
EN						
	EN Wake-up time	From V_{EN} > V_{IT+} to $I_{D(ls)}$ > 10 mA, V_{INL} = 5 V		1.5		µs

5.7 Typical Characteristics

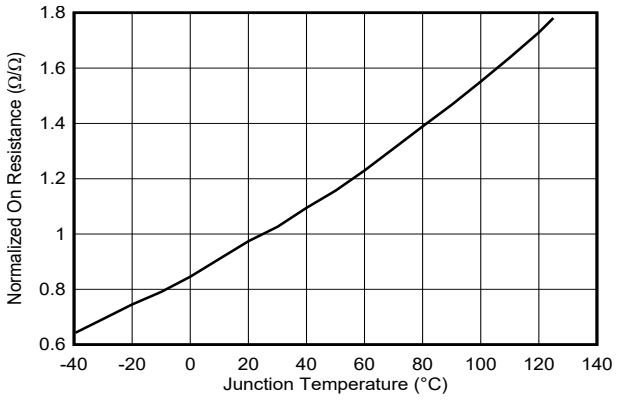


Figure 5-1. Normalized On-Resistance vs Junction Temperature

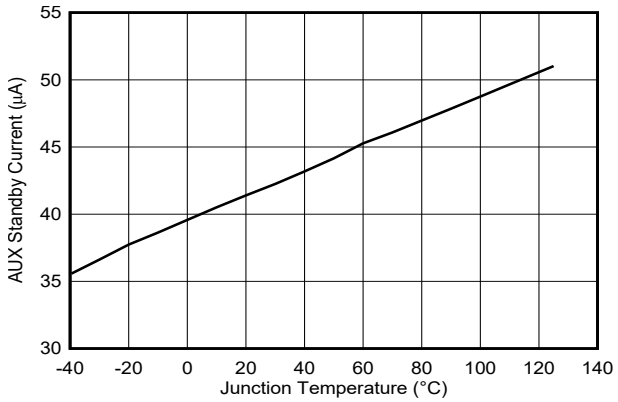


Figure 5-2. AUX Standby Current vs Junction Temperature

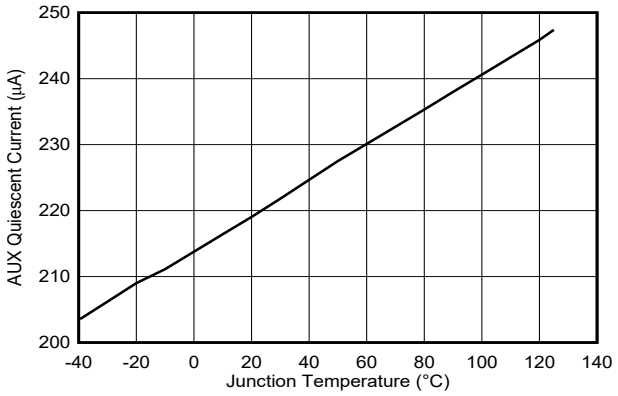


Figure 5-3. AUX Quiescent Current vs Junction Temperature

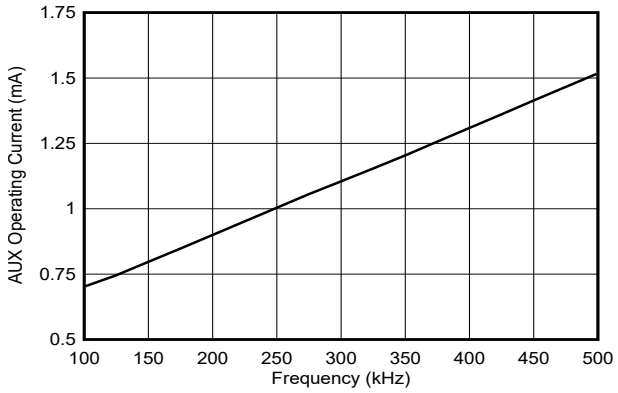


Figure 5-4. AUX Operating Current vs Frequency

6 Parameter Measurement Information

6.1 GaN Power FET Switching Parameters

Figure 6-1 shows the circuit used to measure the GaN power FET switching parameters. The circuit is operated as a double-pulse tester. Consult external references for double-pulse tester details. The circuit operates in the boost configuration with the low-side LMG3626 being the device under test (DUT). The high-side LMG3626 acts as the double-pulse tester diode and circulates the inductor current in the off-state, third-quadrant conduction mode.

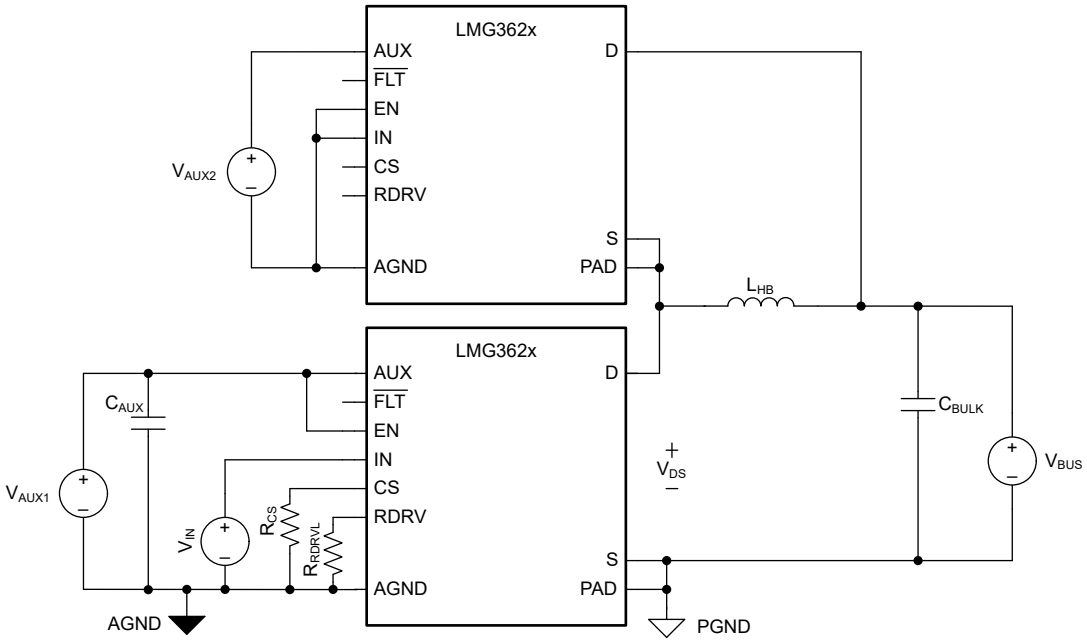


Figure 6-1. GaN Power FET Switching Parameters Test Circuit

Figure 6-2 shows the GaN power FET switching parameters.

The GaN power FET turn-on transition has three timing components: drain-current turn-on delay time, turn-on delay time, and turn-on rise time. Note that the turn-on rise time is the same as the V_{DS} 80% to 20% fall time. All three turn-on timing components are a function of the RDRV pin setting.

The GaN power FET turn-off transition has two timing components: turn-off delay time, and turn-off fall time. Note that the turn-off fall time is the same as the V_{DS} 20% to 80% rise time. The turn-off timing components are independent of the RDRV pin setting, but heavily dependent on the L_{HB} current.

The turn-on slew rate is measured over a smaller voltage delta (100 V) compared to the turn-on rise time voltage delta (240 V) to obtain a faster slew rate which is useful for EMI design. The RDRV pin is used to program the slew rate.

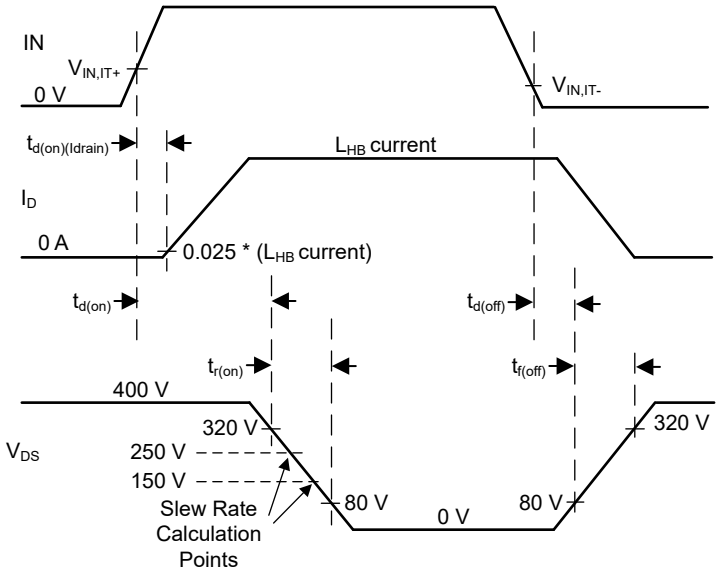


Figure 6-2. GaN Power FET Switching Parameters

7 Detailed Description

7.1 Overview

The LMG3626 is an integrated 650-V 270-mΩ GaN power FET intended for use in switching-power converters. The LMG3626 combines the GaN FET, gate driver, current-sense emulation function, and protection features in a 8-mm by 5.3-mm QFN package.

The 650-V rated GaN FET supports the high voltages encountered in off-line power switching applications. The GaN FET low output-capacitive charge reduces both the time and energy needed for power converter switching and is the key characteristic needed to create small, efficient power converters.

The LMG3626 internal gate driver regulates the drive voltage for optimum GaN FET on-resistance. The internal driver reduces total gate inductance and GaN FET common-source inductance for improved switching performance, including common-mode transient immunity (CMTI). The GaN FET turn-on slew rate can be individually programmed to one of four discrete settings for design flexibility with respect to power loss, switching-induced ringing, and EMI.

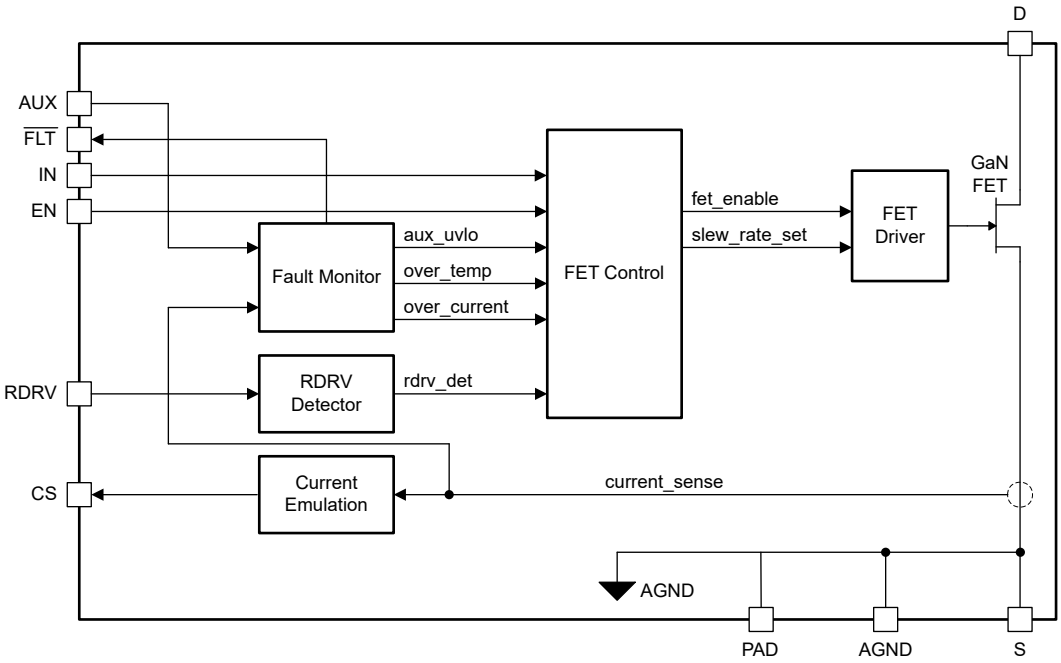
Current-sense emulation places a scaled replica of the GaN FET drain current on the output of the CS pin. The CS pin is terminated with a resistor to AGND to create the current-sense input signal to the external power supply controller. This CS pin resistor replaces the traditional current-sense resistor, placed in series with the GaN FET source, at significant power and space savings. Furthermore, with no current-sense resistor in series with the GaN FET source, the GaN FET thermal pad can be connected directly to the PCB power ground. This thermal pad connection both improves system thermal performance and provides additional device routing flexibility since full device current can be conducted through the thermal pad.

The AUX input supply wide voltage range is compatible with the corresponding wide range supply rail created by power supply controllers. Low AUX quiescent currents support converter burst-mode operation critical for meeting government light-load efficiency mandates. Further AUX quiescent current reduction is obtained by placing the device in standby mode with the EN pin.

The IN and EN control pins have high input impedance, low input threshold voltage and maximum input voltage equal to the AUX voltage. This allows the pins to support both low voltage and high voltage input signals and be driven with low-power outputs.

The LMG3626 protection features are under-voltage lockout (UVLO), cycle-by-cycle current limit, and overtemperature protection. The overtemperature protection is reported on the open drain $\overline{\text{FLT}}$ output.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 GaN Power FET Switching Capability

Due to the silicon FET's long reign as the dominant power-switch technology, many designers are unaware that the nameplate drain-source voltage cannot be used as an equivalent point to compare devices across technologies. The nameplate drain-source voltage of a silicon FET is set by the avalanche breakdown voltage. The nameplate drain-source voltage of a GaN FET is set by the long term compliance to data sheet specifications.

Exceeding the nameplate drain-source voltage of a silicon FET can lead to immediate and permanent damage. Meanwhile, the breakdown voltage of a GaN FET is much higher than the nameplate drain-source voltage. For example, the breakdown drain-source voltage of the LMG3626 GaN power FET is more than 800 V which allows the LMG3626 to operate at conditions beyond an identically nameplate rated silicon FET.

The LMG3626 GaN power FET switching capability is explained with the assistance of Figure 7-1. The figure shows the drain-source voltage versus time for the LMG3626 GaN power FET for four distinct switch cycles in a switching application. No claim is made about the switching frequency or duty cycle. The first two cycles show normal operation and the second two cycles show operation during a rare input voltage surge. The LMG3626 GaN power FETs are intended to be turned on in either zero-voltage switching (ZVS) or discontinuous-conduction mode (DCM) switching conditions.

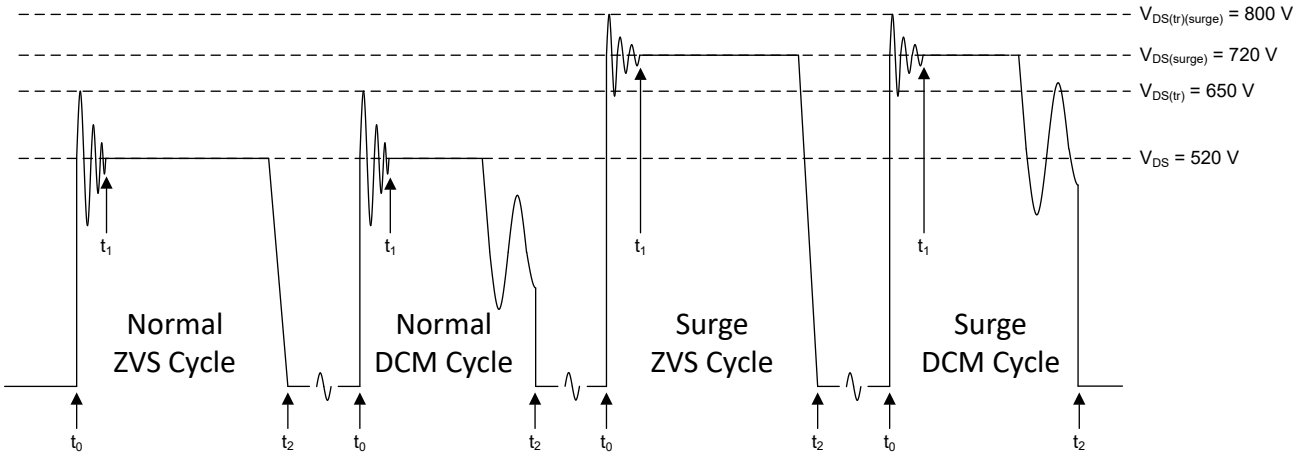


Figure 7-1. GaN Power FET Switching Capability

Each cycle starts before t_0 with the FET in the on state. At t_0 the GaN FET turns off and parasitic elements cause the drain-source voltage to ring at a high frequency. The high frequency ringing has damped out by t_1. Between t_1 and t_2 the FET drain-source voltage is set by the characteristic response of the switching application. The characteristic is shown as a flat line (plateau), but other responses are possible. At t_2 the GaN FET turns on. For normal operation, the transient ring voltage is limited to 650 V and the plateau voltage is limited to 520 V. For rare surge events, the transient ring voltage is limited to 800 V and the plateau voltage is limited to 720 V.

7.3.2 Turn-On Slew-Rate Control

The turn-on slew rate of the GaN power FET is programmed to one of four discrete settings by the resistance between the RDRV and AGND pins. The slew-rate setting is determined one time during AUX power up when the AUX voltage goes above the AUX power-on reset voltage. The slew-rate setting determination time is not specified but is around 0.4 µs.

Table 7-1 shows the recommended typical resistance programming value for the four slew rate settings and the typical turn-on slew rate at each setting. As noted in the table, an open-circuit connection is acceptable for programming slew-rate setting 0 and a short-circuit connection (RDRV shorted to AGND) is acceptable for programming slew-rate setting 3.

Table 7-1. Slew-Rate Setting

TURN-ON SLEW RATE SETTING	RECOMMENDED TYPICAL PROGRAMMING RESISTANCE (kΩ)	TYPICAL TURN-ON SLEW RATE (V/ns)	COMMENT
0 (slowest)	120	20	Open-circuit connection for programming resistance is acceptable.
1	47	50	
2	22	75	
3 (fastest)	5.6	150	Short-circuit connection for programming resistance (RDRV shorted to AGND) is acceptable.

7.3.3 Current-Sense Emulation

The current-sense emulation function creates a scaled replica of the GaN power FET positive drain current at the output of the CS pin. The current-sense emulation gain, G_{CSE}, is 1.633-mA output from the CS pin, I_{CS}, for every 1 A passing into the drain of the low-side GaN power FET, I_D.

$$G_{CSE} = I_{CS} / I_D = 1.633\ mA / 1\ A = 0.001633 \quad (1)$$

The CS pin is terminated with a resistor to AGND, R_{CS}, to create the current-sense voltage input signal to the external power supply controller.

R_{CS} is determined by solving for the traditional current-sense design resistance, $R_{CS(trad)}$, and multiplying by the inverse of G_{CSE}. The traditional current-sense design creates the current-sense voltage, $V_{CS(trad)}$, by passing the GaN power FET drain current, I_D, through $R_{CS(trad)}$. The LMG3626 creates the current-sense voltage, V_{CS}, by passing the CS pin output current, I_{CS}, through R_{CS}. The current-sense voltage must be the same for both designs.

$$V_{CS} = I_{CS} \times R_{CS} = V_{CS(trad)} = I_D \times R_{CS(trad)} \quad (2)$$

$$R_{CS} = I_D / I_{CS} \times R_{CS(trad)} = 1 / G_{CSE} \times R_{CS(trad)} \quad (3)$$

$$R_{CS} = 612 \times R_{CS(trad)} \quad (4)$$

The CS pin is clamped internally to a typical 2.5 V. The clamp protects vulnerable power-supply controller current-sense input pins from over voltage if, for example, the current sense resistor on the CS pin were to become disconnected.

Figure 7-2 shows the current-sense emulation operation. In both cycles, the CS pin current emulates the GaN power FET drain current while the GaN FET is enabled. The first cycle shows normal operation where the controller turns off the GaN power FET when the controller current-sense input threshold is tripped. The second cycle shows a fault situation where the LMG3626 overcurrent protection turns off the GaN power FET before the controller current-sense input threshold is tripped. In this second cycle, the LMG2610 avoids a hung controller IN pulse by generating a fast-ramping artificial current-sense emulation signal to trip the controller current-sense input threshold. The artificial signal persists until the IN pin goes to logic-low which indicates the controller is back in control of switch operation.

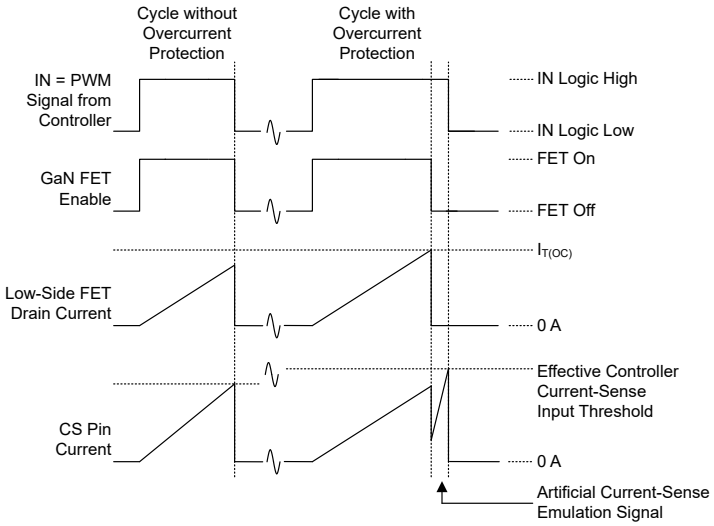


Figure 7-2. Current-Sense Emulation Operation

7.3.4 Input Control Pins (EN, IN)

The EN pin is used to toggle the device between the active and standby modes described in the *Device Functional Modes* section.

The IN pin is used to turn the GaN power FET on and off.

The input control pins have a typical 1-V input-voltage-threshold hysteresis for noise immunity. The pins also have a typical 400-kΩ pull-down resistance to protect against floating inputs. The 400 kΩ saturates for nominal input voltages above 4 V to limit the maximum input pull-down current to a typical 10 µA.

The IN turn-on action is blocked by the following conditions:

- Standby mode (as set by the EN pin above)
- AUX UVLO
- Overcurrent protection
- Overtemperature protection

The standby mode, AUX UVLO, and overtemperature protection are independent of the IN logic state. Figure 7-3 shows the IN independent blocking condition operation.

Meanwhile, overcurrent protection only acts after IN has turned on the GaN power FET. See the *Overcurrent Protection* section for the details.

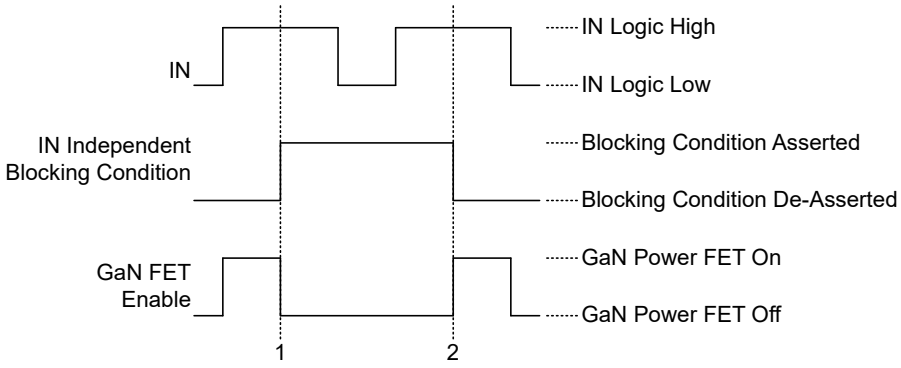


Figure 7-3. IN Independent Blocking Condition Operation

7.3.5 AUX Supply Pin

The AUX pin is the input supply for the internal circuits.

7.3.5.1 AUX Power-On Reset

The AUX power-on reset disables all low-side functionality if the AUX voltage is below the AUX power-on reset voltage. The AUX power-on reset voltage is not specified but is around 5 V. The AUX power-on reset initates the one-time determination of the low-side slew-rate setting programmed on the RDRV pin when the AUX voltage goes above the AUX power-on reset voltage. The AUX power-on reset enables the overtemperature protection function if the AUX voltage is above the AUX power-on reset voltage.

7.3.5.2 AUX Under-Voltage Lockout (UVLO)

The AUX UVLO holds off the GaN power FET if the AUX voltage is below the AUX UVLO voltage. Figure 7-3 shows the AUX UVLO hold-off (blocking) operation. The AUX UVLO voltage hysteresis prevents on-off chatter near the UVLO voltage trip point.

7.3.6 Overcurrent Protection

The LMG3626 implements cycle-by-cycle overcurrent protection for the GaN power FETs. Figure 7-4 shows the cycle-by-cycle overcurrent operation. Every IN logic-high cycle turns on the GaN power FET. If the GaN power FET drain current exceeds the overcurrent threshold current, the overcurrent protection turns off the GaN power FET for the remainder of the IN logic-high duration.

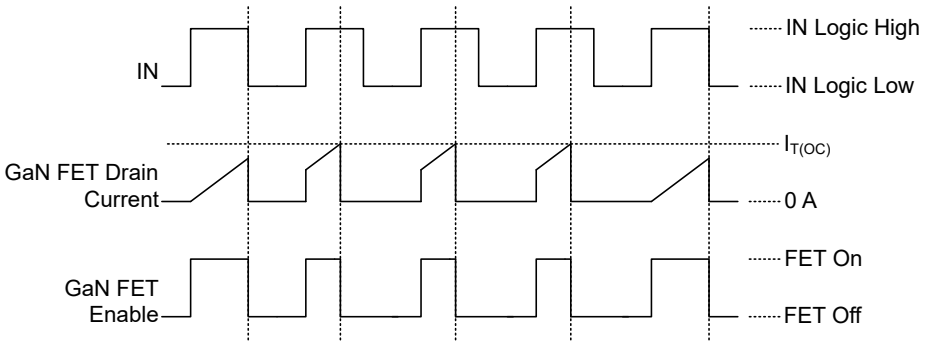


Figure 7-4. Cycle-by-Cycle Overcurrent Protection Operation

An overcurrent protection event is not reported on the $\overline{FLT}$ pin. Cycle-by-cycle overcurrent protection minimizes system disruption because the event is not reported and because the protection allows the GaN power FET to turn on every IN cycle.

As described in the *Current-Sense Emulation* section, an artificial CS pin current is produced after the low-side GaN power FET is turned off by the low-side overcurrent protection, to prevent the controller from entering a hung state.

7.3.7 Overtemperature Protection

The overtemperature protection holds off the GaN power FET if the LMG3626 temperature is above the overtemperature protection temperature. Figure 7-3 shows the overtemperature protection hold-off (blocking) operation. The overtemperature protection hysteresis avoids erratic thermal cycling.

An overtemperature fault is reported on the $\overline{FLT}$ pin when the overtemperature protection is asserted. This is the only fault event reported on the $\overline{FLT}$ pin. The overtemperature protection is enabled when the AUX voltage is above the AUX power-on reset voltage. The low AUX power-on reset voltage helps the overtemperature protection remain operational when the AUX rail droops during the application cool-down phase.

7.3.8 Fault Reporting

The LMG3626 only reports an overtemperature fault. An overtemperature fault is reported on the $\overline{FLT}$ pin when the Overtemperature Protection function is asserted. The $\overline{FLT}$ pin is an active low open-drain output so the pin pulls low when there is an overtemperature fault.

7.4 Device Functional Modes

The LMG3626 has two modes of operation controlled by the EN pin. The device is in active mode when the EN is logic high and in standby mode when the EN pin is logic low. In active mode, the power FET is controlled by the IN pin. In standby mode, the IN pin is ignored, the GaN power FET is held off, and the AUX quiescent current is reduced to the AUX standby quiescent current.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LMG3626 enables the simple adoption of GaN FET technology in switch-mode power-supply applications. The integrated gate driver, low IN input threshold voltage, and wide AUX input-supply voltage allows the LMG3626 to seamlessly pair with common industry power-supply controllers. The current-sense emulation feature saves power and improves thermal conduction.

Using the LMG3626 only requires setting the desired turn-on slew rate with a programming resistor and calculating the current sense resistor.

8.2 Typical Application

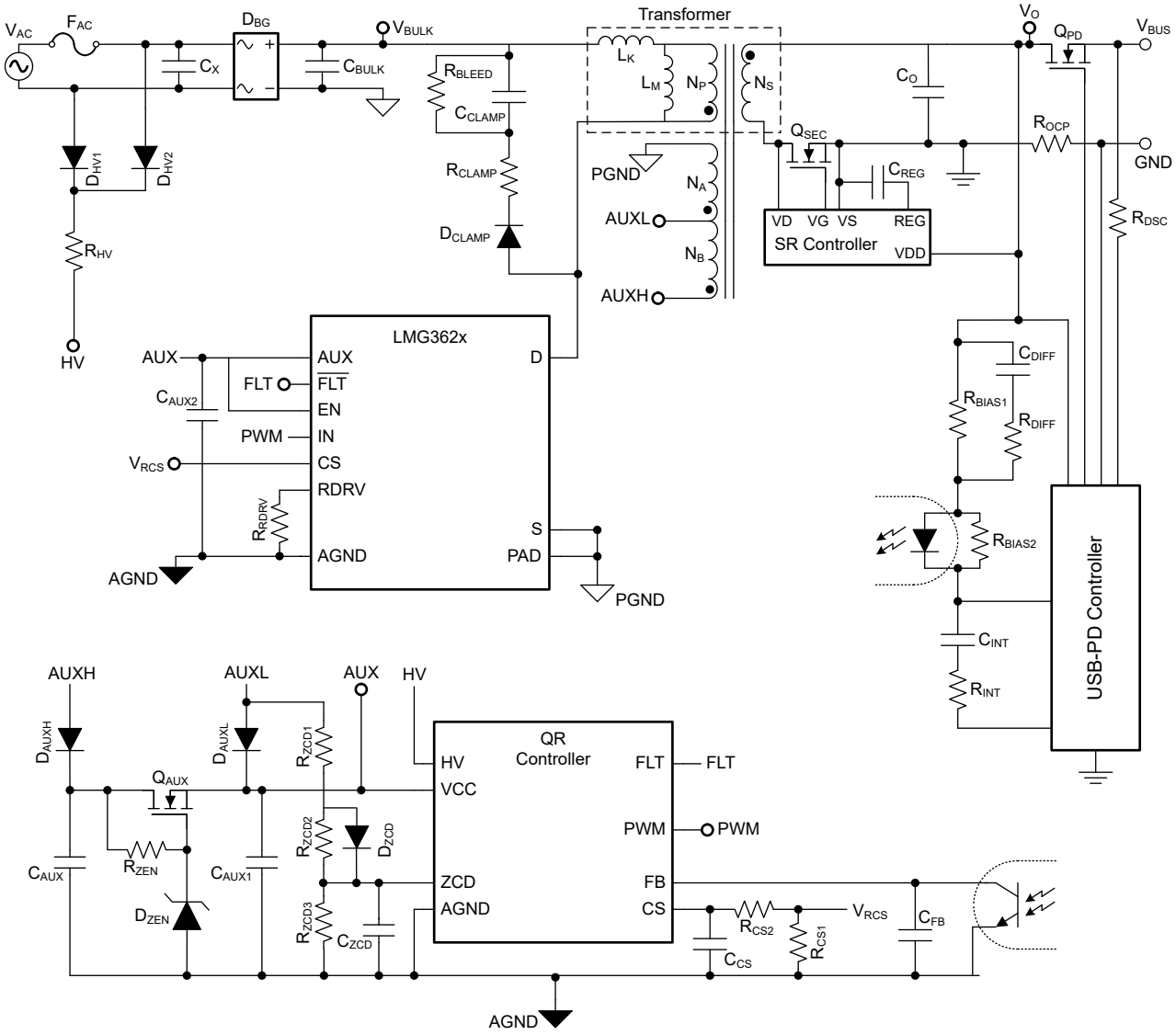


Figure 8-1. 65-W USB PD Charger Quasi-Resonant Flyback Converter Application

8.2.1 Design Requirements

Table 8-1. Design Specification

SPECIFICATION	VALUE
Input AC voltage range	90 VAC to 264 VAC
Input line frequency range	47 Hz to 63 Hz
Output DC voltage settings	5 V, 9 V, 15 V, 20 V
20-V ouput rated current	3.25 A
5-V, 9 -V, and 15-V rated output current	3 A
Maximum AC input power at no output load	70 mW
Minimum efficiency over input AC voltage range at 20-V ouput and full load	93%

8.2.2 Detailed Design Procedure

The 65-W USB-PD charger application is taken from the EVM design found in the *Using the LMG3626EVM-074 65-W USB-C PD High-Density Quasi-Resonant Flyback Converter* user's guide. The entire quasi-resonant flyback converter design is not given here. The *LMG362XX Quasi-Resonant Power-Stage Design Calculator* can be used to create a desired application specific converter design. This detailed design procedure focuses on the specifics of using the LMG3626 in the application.

8.2.2.1 Turn-On Slew-Rate Design

The LMG3626 turn-on slew rates are programmed as discussed in the *Turn-On Slew-Rate Control* section. The design consideration is the trade-off between power supply efficiency and EMI / transient ringing. Slower turn-on slew-rates lessen EMI and ringing problems but can increase switching losses and vice versa.

In normal quasi-resonant flyback-converter operation, the power switch operates at both ZVS and also non-ZVS valley switching depending on operating conditions. The valley switching occurs at zero transformer current. Therefore, there are no switching cross-over losses in quasi-resonant converters. The only switching loss is the switch-node capacitive loss during valley switching. So the turn-on slew rate has no impact on the converter loss. This seems to indicate to use the slowest turn-on slew rate setting. The turn-on slew rate setting, however, can have a secondary impact on converter loss from the switch turn-on delay.

Depending on how the quasi-resonant controller implements valley switching, the switch turn-on delay can cause the power-converter to switch after the valley and increase capacitive switching losses. Since the switch turn-on delay increases as the turn-on slew rate is decreased, using slower turn-on slew rates can increase power supply losses. If the quasi-resonant controller compensates for switch turn-on delay, then there is no loss penalty for using the slowest turn-on slew rate setting. Otherwise, design optimization between switching noise problems and switching losses must be performed.

The turn-on slew rate is programmed by setting R_{DRV} to the recommended typical programming resistance shown in the *Turn-On Slew-Rate Control* section.

8.2.2.2 Current-Sense Design

The current sense resistor R_{CS1} is calculated as described in the *Current-Sense Emulation* section where a traditional current-sense resistor design calculation is first performed and then muliplied by the current-sense emulation inverse gain. The traditional current-sense resistor design calculation, denoted $R_{CS(trad)}$, is for when the current-sense resistor is in series with the power switch and is sensing the full power-switch current.

$$R_{CS1} = 612 * R_{CS(trad)} \quad (5)$$

R_{CS2} may or may not exist depending on the quasi-resonant controller. If R_{CS2} is used, keep in mind the R_{CS2} design calculation may assume a traditional current-sense resistor with a very small value that has no impact on the R_{CS2} calculation. Be careful to ensure the R_{CS2} calculation accounts for the significant R_{CS1} value.

8.2.3 Application Curves

The following waveforms show typical switching waveforms. The blue trace is the LMG2622 drain voltage (switch node voltage) and the red trace is the CS pin current-sense emulation voltage.

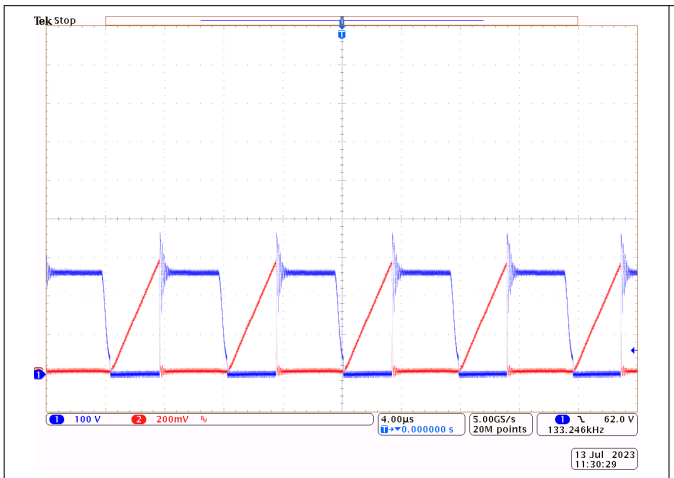


Figure 8-2. V_{IN} = 115 VAC V_{OUT} = 20 V I_{OUT} = 3.25 A

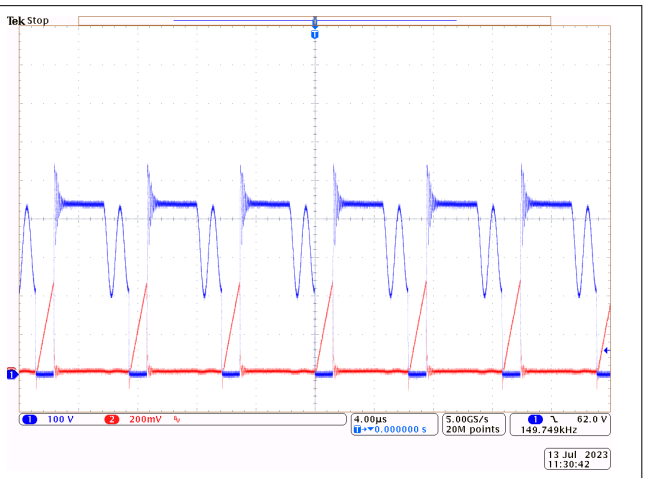


Figure 8-3. V_{IN} = 230 VAC V_{OUT} = 20 V I_{OUT} = 3.25 A

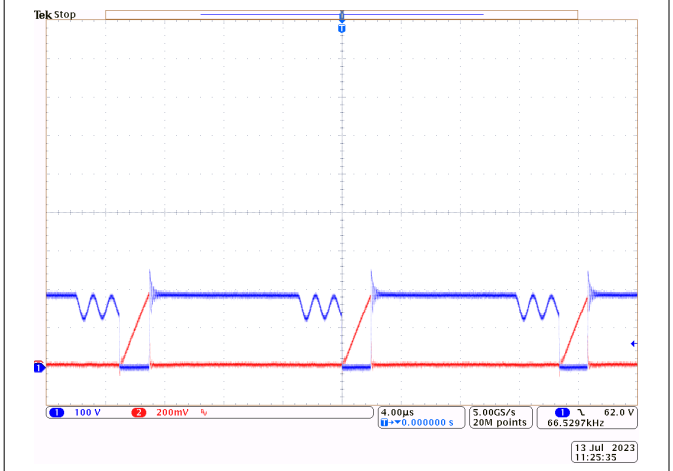


Figure 8-4. V_{IN} = 115 VAC V_{OUT} = 5 V I_{OUT} = 3 A

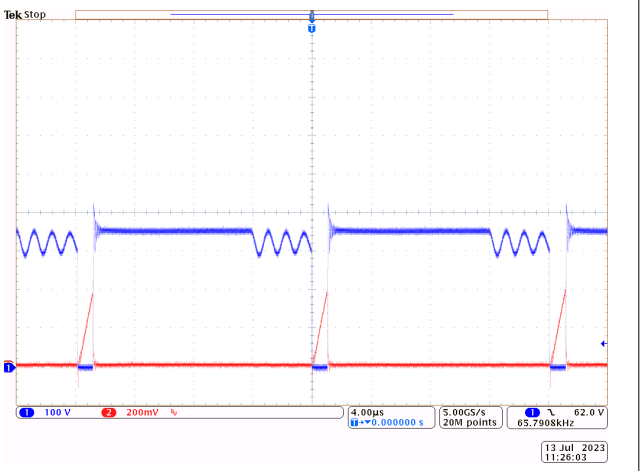


Figure 8-5. V_{IN} = 230 VAC V_{OUT} = 5 V I_{OUT} = 3 A

8.3 Power Supply Recommendations

The LMG3626 operates from a single input supply connected to the AUX pin. The LMG3626 supports being operated from the same supply managed and used by the power supply controller. The wide recommended AUX voltage range of 10 V to 26 V overlaps common-controller supply-pin turn-on and UVLO voltage limits.

The AUX external capacitance is recommended to be a ceramic capacitor that is at least 0.03 µF over operating conditions.

8.4 Layout

8.4.1 Layout Guidelines

8.4.1.1 Solder-Joint Stress Relief

Large QFN packages can experience high solder-joint stress. Several best practices are recommended to provide solder-joint stress relief. First, the instructions for the NC1, NC2, and NC3 anchor pins found in Table 4-1 must be followed. Second, all the board solder pads must be non-solder-mask defined (NSMD) as shown in the land pattern example in the *Mechanical, Packaging, and Orderable Infromation* section. Finally, any board trace connected to an NSMD pad must be less than two thirds the width of the pad on the pad side where it is

connected. The trace must maintain this two-thirds width limit for as long as it is not covered by solder mask. After the trace is under solder mask, there are no limits on the trace dimensions. All these recommendations are followed in the *Layout Example* section.

8.4.1.2 Signal-Ground Connection

Design the power supply with separate signal and power grounds that only connect in one location. Connect the LMG3626 AGND pin to signal ground. Connect the LMG3626 SL pin and PAD thermal pad to power ground. This serves as the single connection point between the signal and power grounds since the AGND pin, S pin, and PAD thermal pad are connected internally. Do not connect the signal and power grounds anywhere else on the board except as recommended in the next sentence. To facillitate board debug with the LMG3626 not installed, connect the AGND pad to the PAD thermal pad as shown in the *Layout Example* section.

8.4.1.3 CS Pin Signal

As seen with Equation 4, the current-sense signal impedance is three orders of magnitude higher than a traditional current-sense signal. This higher impedance has implications for current-sense signal noise susceptibility. Minimize routing the current-sense signal near any noisy traces. Place the current-sense resistor and any filtering capacitors at the far end of the trace next to the controller current-sense input pin.

8.4.2 Layout Example

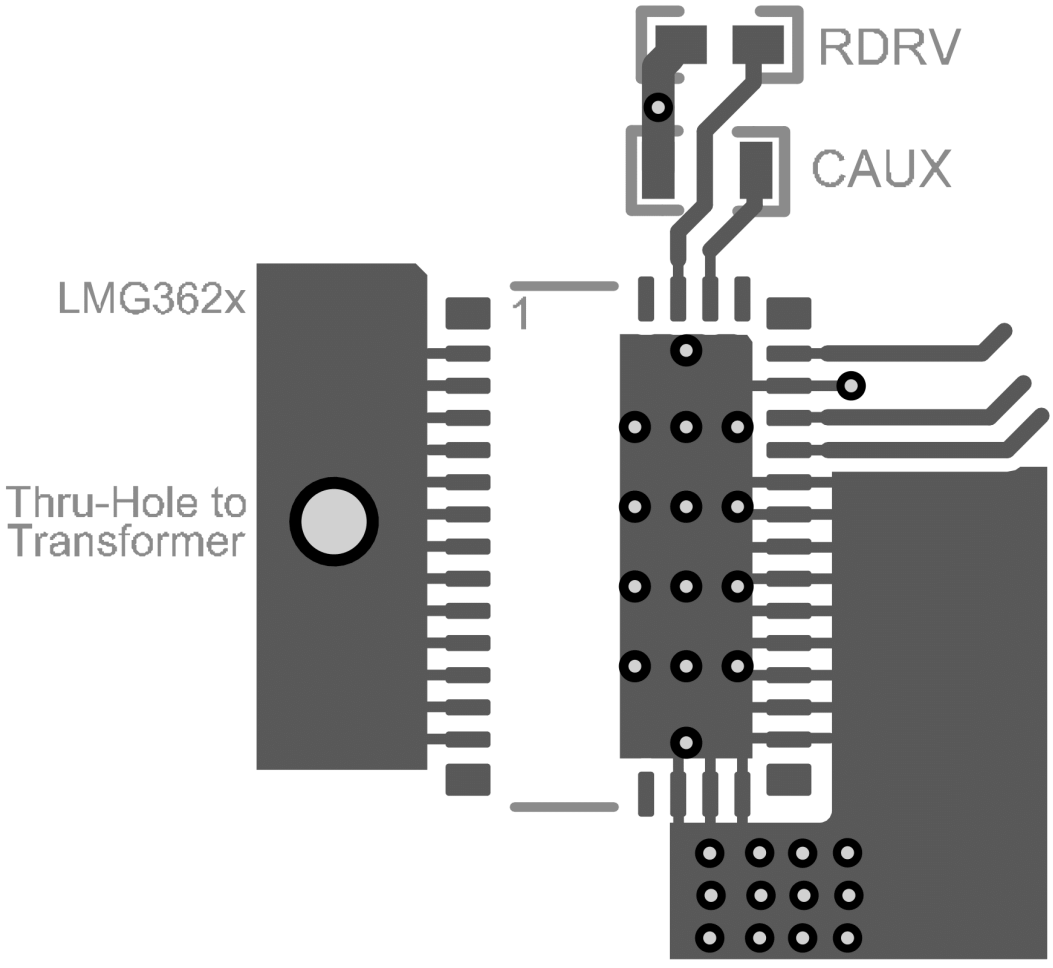


Figure 8-6. PCB Top Layer (First Layer)

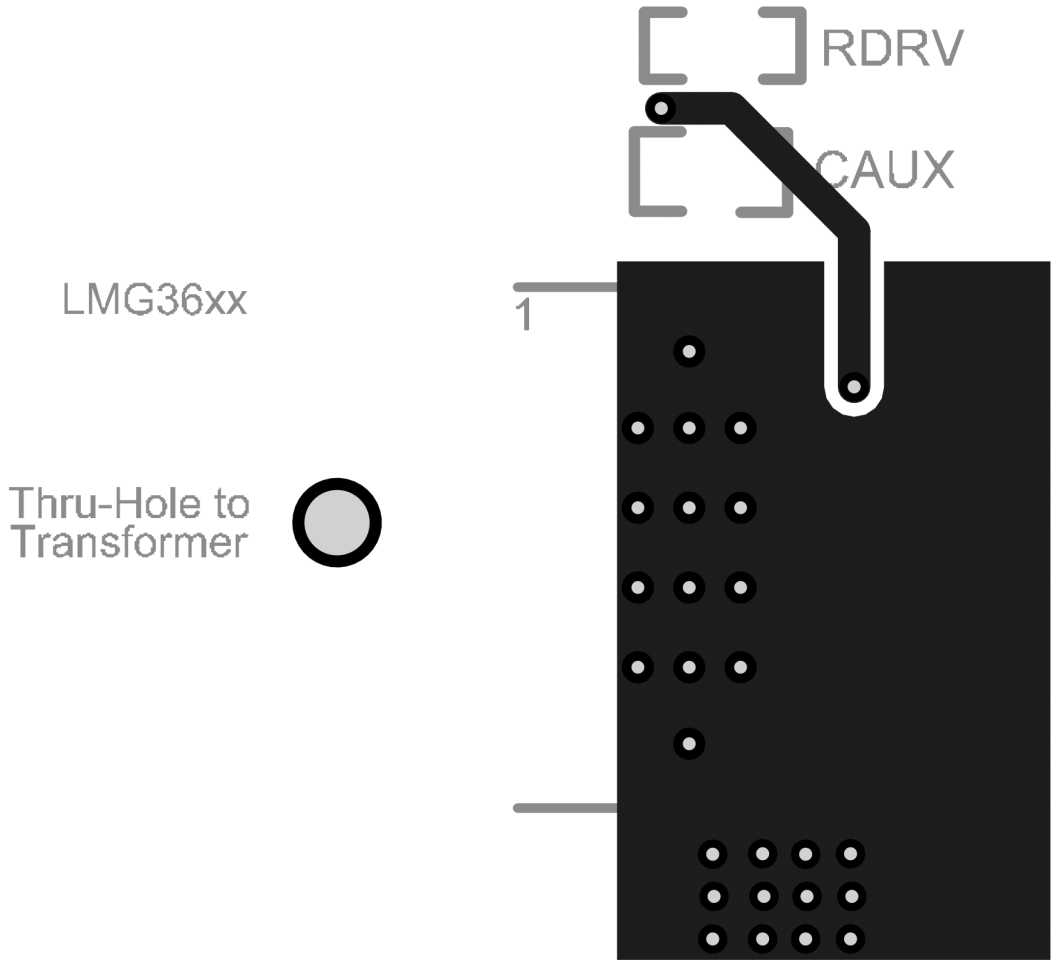


Figure 8-7. PCB Bottom Layer (Second Layer)

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

The *LMG362XX Quasi-Resonant Power-Stage Design Calculator* is an Excel-based calculation tool for LMG3626 design.

The *Using the LMG3626EVM-074 65-W USB-C PD High-Density Quasi-Resonant Flyback Converter* is a user's guide for the EVM.

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2023) to Revision A (November 2023)	Page
• Changed the document status from Advance Information to Production Data	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMG3626REQR	ACTIVE	VQFN	REQ	38	2000	RoHS-Exempt & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	LMG3626 NNNNC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

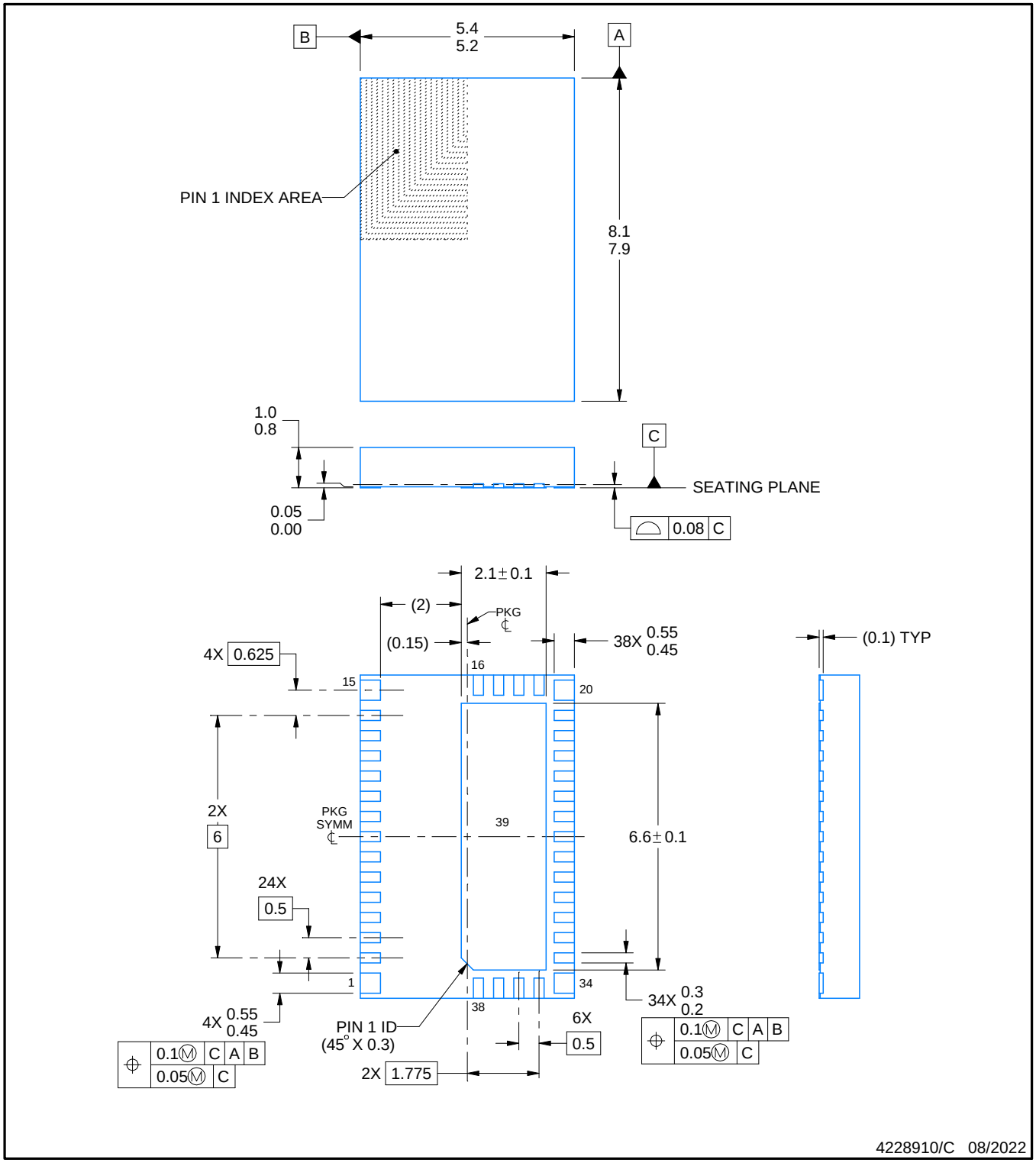
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

REQ0038A

PACKAGE OUTLINE

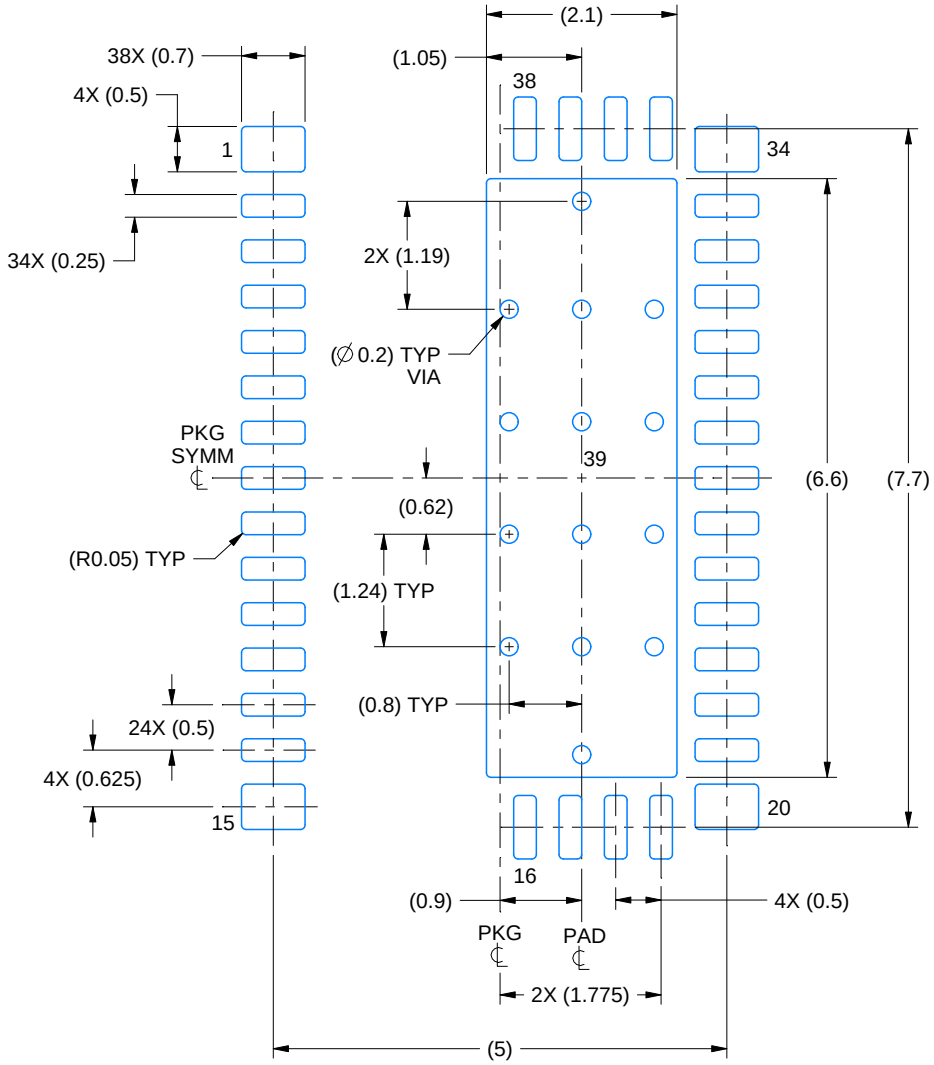
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



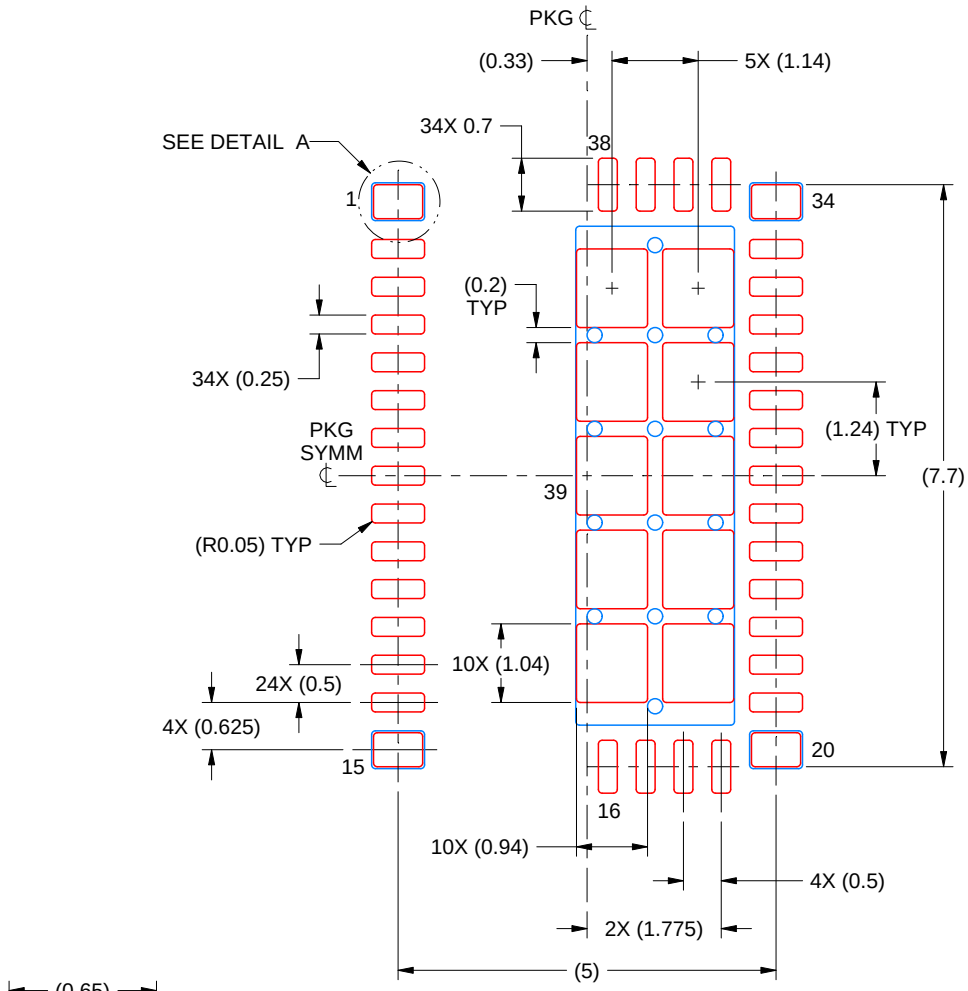
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

SOLDER MASK DETAILS

4228910/C 08/2022

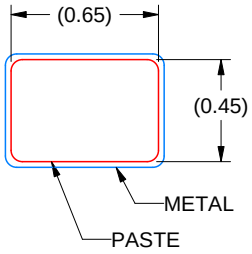
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 39:
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:10X



DETAIL A
4X, SCALE: 30X

4228910/C 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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