

# LP5811 Synchronous Boost 4-Channel RGBW LED Driver with Autonomous Control

## 1 Features

- Operating voltage range:
  - Input voltage ( $V_{IN}$ ) range: 0.5V to 5.5V
  - 1.8V minimum input voltage for start-up
  - Logic pins compatible with 1.8V, 3.3V, and 5V
- High efficiency synchronous boost converter
  - Output voltage ( $V_{OUT}$ ) range: 3V to 5.5V
  - 140m $\Omega$  (HS) / 60m $\Omega$  (LS) MOSFETs
  - 1.6A valley switching current limit
  - 95% efficiency at  $V_{IN} = 4.2V$ ,  $V_{OUT} = 5.0V$ ,  $I_{OUT} = 300mA$
  - Pass-through mode when  $V_{IN} > V_{OUT}$  setting
  - True disconnection between input and output during shutdown
- 4 constant current sinks with high precision:
  - 0.1mA to 51mA per current sink
  - Device-to-device error: max  $\pm 5\%$
  - Channel-to-channel error: max  $\pm 5\%$
  - Ultra-low headroom voltage: 110mV (typ.) at 25.5mA; 210mV (typ.) at 51mA
  - PWM phase shift configurable for each LED
- Ultra-low power consumption:
  - Shutdown:  $I_{SD} = 0.1\mu A$  (typical) when EN = Low
  - Standby:  $I_{STB} = 26\mu A$  (typical) when EN = High and CHIP\_EN = 0 (data retained)
  - Active:  $I_{NOR} = 0.45mA$  (typical) when LED current = 25.5mA
- Analog dimming (current gain control)
  - Global 1-bit Maximum Current (MC): 25.5mA or 51mA
  - Individual 8-bit Dot Current (DC) setting
- PWM dimming up to audible-noise-free 24kHz
  - Individual 8-bit PWM dimming resolution
  - Linear or exponential dimming curves
- Autonomous animation engine control
- Individual LED dot open/short detection
- Integrated de-ghosting function
- 1MHz (max.) I<sup>2</sup>C interface
- 40°C to 85°C operating temperature range

## 2 Applications

LED animation and indication for:

- Portable and wearable electronics - earbud and charging case, E-cigarette, smart watch
- Gaming and home entertainment - smart speaker, RGB mouse, VR headset, and controller
- Internet-of-Things (IOT) - E-tag, video doorbell
- Networkings - router, access point
- Industrial HMI - EV charger, factory automation

## 3 Description

The LP5811 is a synchronous boost 4-channel RGBW LED driver with autonomous animation engine control. The device is ideal to support battery-powered applications with 0.5V to 5.5V input voltage range, and it has ultra-low normal operation current with 0.4mA (typical) when illuminate LEDs.

The integrated synchronous boost converter maintains excellent efficiency and keeps the brightness of LEDs stable over a wide operating voltage range. Output voltage can be selected for different LED forward voltage from 3V to 5.5V with 0.1V step. The boost converter can power not only the LEDs driven by the device itself, but also other loads in the system. If the boost converter need to be bypassed,  $V_{OUT}$  is used as the power supply input for the LED driver blocks.

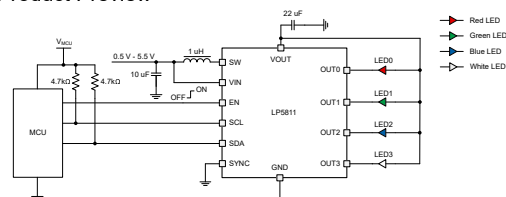
Both analog dimming and PWM dimming methods are adopted to achieve powerful dimming performance. The output current of each LED can be adjusted with 256 steps from 0.1mA to 25.5mA or 0.2mA to 51mA. The 8-bit PWM generator enables smooth and audible-noise-free dimming control for LED brightness.

The autonomous animation engine can significantly reduce the real-time loading of controller. Each LED can be configured through the related registers to realize vivid and fancy lighting effects. The device can generate 6MHz clock signal and use it for synchronizing the lighting effects among multiple devices.

### Package Information

| PART NUMBER | PACKAGE <sup>(1)</sup> | BODY SIZE (NOM) |
|-------------|------------------------|-----------------|
| LP5811      | DSBGA (12)             | 1.84mm × 1.43mm |
|             | WSO (12)               | 3mm × 3mm       |

(1) Product Preview



**Simplified Schematic**



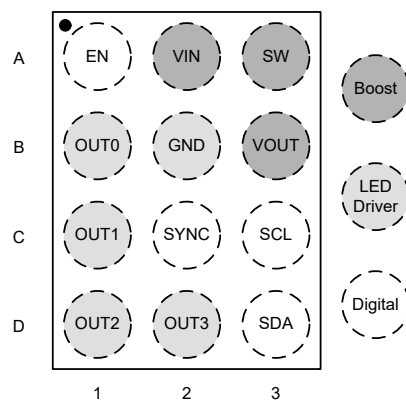
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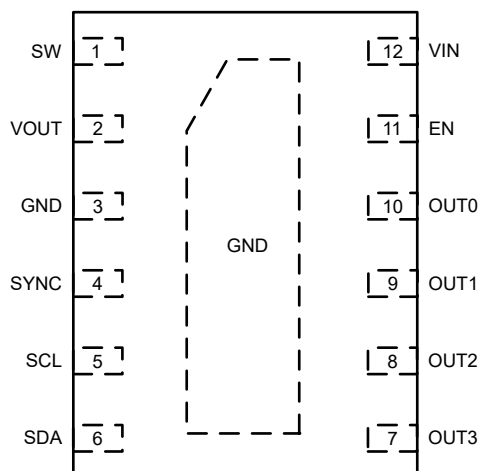
## 4 Device Comparison

| PART<br>NUMBER | Max LED<br>Number | Power<br>Stage | PACKAGE  | MATERIAL    | I <sup>2</sup> C Chip Address |       | SOFTWARE<br>COMPATIBLE |
|----------------|-------------------|----------------|----------|-------------|-------------------------------|-------|------------------------|
|                |                   |                |          |             | Bit 4                         | Bit 3 |                        |
| LP5813         | 12                | Boost          | DSBGA-12 | LP5813AYBHR | 0                             | 0     | Yes                    |
|                |                   |                |          | LP5813BYBHR | 0                             | 1     |                        |
|                |                   |                |          | LP5813CYBHR | 1                             | 0     |                        |
|                |                   |                |          | LP5813DYBHR | 1                             | 1     |                        |
|                |                   |                | WSON-12  | LP5813ADRRR | 0                             | 0     |                        |
|                |                   |                |          | LP5813BDRRR | 0                             | 1     |                        |
|                |                   |                |          | LP5813CDRRR | 1                             | 0     |                        |
|                |                   |                |          | LP5813DDRRR | 1                             | 1     |                        |
| LP5812         | 12                | Linear         | DSBGA-9  | LP5812AYBHR | 0                             | 0     |                        |
|                |                   |                |          | LP5812BYBHR | 0                             | 1     |                        |
|                |                   |                |          | LP5812CYBHR | 1                             | 0     |                        |
|                |                   |                |          | LP5812DYBHR | 1                             | 1     |                        |
|                |                   |                | WSON-8   | LP5812ADSDR | 0                             | 0     |                        |
|                |                   |                |          | LP5812BDSDR | 0                             | 1     |                        |
|                |                   |                |          | LP5812CDSDR | 1                             | 0     |                        |
|                |                   |                |          | LP5812DDSDR | 1                             | 1     |                        |
| LP5811         | 4                 | Boost          | DSBGA-12 | LP5811AYBHR | 0                             | 0     |                        |
|                |                   |                |          | LP5811BYBHR | 0                             | 1     |                        |
|                |                   |                |          | LP5811CYBHR | 1                             | 0     |                        |
|                |                   |                |          | LP5811DYBHR | 1                             | 1     |                        |
|                |                   |                | WSON-12  | LP5811ADRRR | 0                             | 0     |                        |
|                |                   |                |          | LP5811BDRRR | 0                             | 1     |                        |
|                |                   |                |          | LP5811CDRRR | 1                             | 0     |                        |
|                |                   |                |          | LP5811DDRRR | 1                             | 1     |                        |
| LP5810         | 4                 | Linear         | DSBGA-9  | LP5810AYBHR | 0                             | 0     |                        |
|                |                   |                |          | LP5810BYBHR | 0                             | 1     |                        |
|                |                   |                |          | LP5810CYBHR | 1                             | 0     |                        |
|                |                   |                |          | LP5810DYBHR | 1                             | 1     |                        |
|                |                   |                | WSON-8   | LP5810ADSDR | 0                             | 0     |                        |
|                |                   |                |          | LP5810BDSDR | 0                             | 1     |                        |
|                |                   |                |          | LP5810CDSDR | 1                             | 0     |                        |
|                |                   |                |          | LP5810DDSDR | 1                             | 1     |                        |

## 5 Pin Configuration and Functions



**Figure 5-1. LP5811 YBH Package 12-Pin DSBGA Top View**



**Figure 5-2. LP5811 DRR Package 12-Pin WSON Top View**

**Table 5-1. Pin Functions**

| PIN  |     |     | TYPE <sup>(1)</sup> | DESCRIPTION   |
|------|-----|-----|---------------------|---|
| NAME | YBH | DRR |                     |   |
| EN   | A1  | 11  | I                   | Enable input of the integrated boost converter.   |
| VIN  | A2  | 12  | P                   | Power supply of the device. A 10 $\mu$ F capacitor is recommended to be connected between this pin with GND and be placed as close to the device as possible.               |
| SW   | A3  | 1   | P                   | Switch pin of the integrated boost converter, which is connected to the drain of low-side power FET and source of high-side rectifier FET. Connect the inductor to this pin |
| OUT0 | B1  | 10  | O                   | Output 0 which contains current sink 0 and high-side scan FET 0. If not used, this pin must be floating.  |
| GND  | B2  | 3   | G                   | Ground. Must be connected to the common ground plane  |
| VOUT | B3  | 2   | P                   | Boost converter output. A 22 $\mu$ F capacitor is recommended to be connected between this pin with GND and be placed as close to the device as possible.                   |
| OUT1 | C1  | 9   | O                   | Output 1 which contains current sink 1 and high-side scan FET 1. If not used, this pin must be floating.  |
| SYNC | C2  | 4   | I/O                 | Synchronous between multiple devices. If not used, this pin can be connected to ground to save power.   |
| SCL  | C3  | 5   | I                   | I <sup>2</sup> C serial interface clock input.  |
| OUT2 | D1  | 8   | O                   | Output 2 which contains current sink 2 and high-side scan FET 2. If not used, this pin must be floating.  |
| OUT3 | D2  | 7   | O                   | Output 3 which contains current sink 3 and high-side scan FET 3. If not used, this pin must be floating.  |
| SDA  | D3  | 6   | I/O                 | I <sup>2</sup> C serial interface data input/output.  |

(1) P: Power Pin; I: Input Pin; I/O: Input/Output Pin; O: Output Pin.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                            |                        | MIN  | MAX | UNIT |
|----------------------------|------------------------|------|-----|------|
| Voltage range at terminals | VIN, SW, VOUT          | −0.3 | 6   | V    |
|                            | SW spike at 10 ns      | −0.7 | 8   | V    |
|                            | SW spike at 1 ns       | −0.7 | 9   | V    |
|                            | OUT0, OUT1, OUT2, OUT3 | −0.3 | 6   | V    |
|                            | EN, SCL, SDA, SYNC     | −0.3 | 6   | V    |
| T <sub>J</sub>             | Junction temperature   | −40  | 150 | °C   |
| T <sub>stg</sub>           | Storage temperature    | −65  | 150 | °C   |

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 6.2 ESD Ratings

|                    |                         |   | VALUE | UNIT |
|--------------------|-------------------------|---|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>     | ±4000 | V    |
|                    |                         | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins <sup>(2)</sup> | ±1000 |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                        |  | MIN  | NOM | MAX  | UNIT |
|------------------------|--|------|-----|------|------|
| V <sub>IN</sub>        | Input voltage range                    | 0.5  |     | 5.5  | V    |
| V <sub>OUT</sub>       | Output voltage setting range           | 3    |     | 5.5  | V    |
| L                      | Effective inductance range             | 0.37 | 1   | 2.9  | μH   |
| C <sub>IN</sub>        | Effective input capacitance range      | 1    | 4.7 |      | μF   |
| C <sub>OUT</sub>       | Effective output capacitance range     | 4    | 10  | 1000 | μF   |
| OUT0, OUT1, OUT2, OUT3 | Voltage on OUT0, OUT1, OUT2, OUT3 pins | 0    |     | 5.5  | V    |
| EN, SCL, SDA, SYNC     | Voltage on EN, SCL, SDA, SYNC pins     | 0    |     | 5.5  | V    |
| T <sub>A</sub>         | Ambient temperature                    | −40  |     | 85   | °C   |
| T <sub>J</sub>         | Operating junction temperature         | −40  |     | 125  | °C   |

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | LP5810/2    |           | LP5811/3    |           | UNIT |
|-------------------------------|--|-------------|-----------|-------------|-----------|------|
|                               |  | YBH (DSBGA) | DSD (WSO) | YBH (DSBGA) | DRR (WSO) |      |
|                               |  | 9 PINS      | 8 PINS    | 12 PINS     | 12 PINS   |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance     | 113.1       | 50.8      | 92.1        | 47.5      | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance  | 0.6         | 51.1      | 0.4         | 45.1      | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance       | 33.9        | 22.9      | 25.9        | 20.9      | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter | 0.2         | 1.1       | 0.2         | 0.7       | °C/W |

| THERMAL METRIC <sup>(1)</sup> |  | LP5810/2    |            | LP5811/3    |            | UNIT |
|-------------------------------|--|-------------|------------|-------------|------------|------|
|                               |  | YBH (DSBGA) | DSD (WSON) | YBH (DSBGA) | DRR (WSON) |      |
|                               |  | 9 PINS      | 8 PINS     | 12 PINS     | 12 PINS    |      |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 33.8        | 22.8       | 25.8        | 20.9       | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | n/a         | 8.5        | n/a         | 6.6        | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

Unless specified otherwise, typical characteristics apply over the full ambient temperature range ( $-40^{\circ}\text{C} < T_A < +85^{\circ}\text{C}$ ),  $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 5\text{ V}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$ .

| PARAMETER                 |  | TEST CONDITIONS  | MIN | TYP  | MAX  | UNIT          |
|---------------------------|--|--|-----|------|------|---------------|
| <b>Power Supply</b>       |  |  |     |      |      |               |
| $V_{IN}$                  | Input voltage range                          |  | 0.5 |      | 5.5  | V             |
| $V_{IN\_UVLO}$            | Under-voltage lockout threshold              | $V_{IN}$ rising  |     | 1.7  | 1.8  | V             |
|                           |  | $V_{IN}$ falling   |     | 0.4  | 0.5  | V             |
| $I_{SD}$                  | Shutdown current into VIN and SW pin         | IC disabled (EN = Low), $V_{IN} = 3.6\text{ V}$ , $T_A = 25^{\circ}\text{C}$   |     | 0.1  | 0.35 | $\mu\text{A}$ |
| $I_{STB}$                 | Standby current into VIN and SW pin          | CHIP_EN = 0 (bit), Boost enabled (EN = High), $V_{IN} = 3.6\text{ V}$ , VOUT set to 3 V, Pass-through mode   |     | 26   | 29   | $\mu\text{A}$ |
|                           | Standby current into VOUT pin                | CHIP_EN = 0 (bit), Boost disabled (EN = Low), VIN no supply, VOUT force to 5 V   |     | 25   | 28   | $\mu\text{A}$ |
| $I_{NOR}$                 | Normal operation current into VIN and SW pin | CHIP_EN = 1 (bit), Boost enabled (EN = High), $V_{IN} = 3.6\text{ V}$ , VOUT set to 3 V, Pass-through mode, $I_{OUT0} = I_{OUT1} = I_{OUT2} = I_{OUT3} = 25.5\text{ mA}$ (MC = 0, DC = 255, PWM = 255) |     | 0.45 | 0.65 | mA            |
|                           | Normal operation current into VOUT pin       | CHIP_EN = 1 (bit), Boost disabled (EN = Low), VOUT force to 3.6 V, $I_{OUT0} = I_{OUT1} = I_{OUT2} = I_{OUT3} = 25.5\text{ mA}$ (MC = 0, DC = 255, PWM = 255)  |     | 0.4  | 0.6  | mA            |
| <b>Boost Output</b>       |  |  |     |      |      |               |
| $V_{OUT}$                 | Output voltage setting range                 |  | 3   |      | 5.5  | V             |
| $V_{OVP}$                 | Output over-voltage protection threshold     | $V_{OUT}$ rising   | 5.5 | 5.7  | 5.9  | V             |
| $V_{OVP\_HYS}$            | Over-voltage protection hysteresis           |  |     | 0.2  |      | V             |
| $t_{SS}$                  | Soft startup time                            | From active EN to VOUT regulation. $V_{IN} = 1.8\text{ V}$ , $C_{OUT} = 22\text{ }\mu\text{F}$ , $I_{VOUT} = 0\text{ mA}$  |     | 450  |      | $\mu\text{s}$ |
| <b>Boost Power Switch</b> |  |  |     |      |      |               |
| $R_{DS(on)}$              | High-side MOSFET on resistance               | $V_{VOUT} = 5\text{ V}$  |     | 140  |      | m $\Omega$    |
|                           | Low-side MOSFET on resistance                | $V_{VOUT} = 5\text{ V}$  |     | 60   |      | m $\Omega$    |
| $f_{SW}$                  | Switching frequency                          | $V_{IN} = 3.6\text{ V}$ , $V_{OUT}$ set to 5.0 V, PWM mode   |     | 1    |      | MHz           |
|                           |  | $V_{IN} = 1.0\text{ V}$ , $V_{OUT}$ set to 5.0 V, PFM mode   |     | 0.5  |      | MHz           |
| $I_{LIM\_SW}$             | Valley current limit                         | $V_{IN} = 3.6\text{ V}$ , $V_{OUT}$ set to 5.0 V   |     | 1.6  |      | A             |
| $I_{PRECHG}$              | Pre-charge current                           | $V_{IN} = 3.6\text{ V}$  |     | 350  |      | mA            |
| <b>LED Driver Output</b>  |  |  |     |      |      |               |
| $I_{CS}$                  | Constant current sink output range           | $V_{IN} = 3.6\text{ V}$ , $V_{OUT}$ set to 5 V, MC = 0, manual_pwm_x = FFh (100% ON)   | 0.1 |      | 25.5 | mA            |
|                           |  | $V_{IN} = 3.6\text{ V}$ , $V_{OUT}$ set to 5 V, MC = 1, manual_pwm_x = FFh (100% ON)   | 0.2 |      | 51   | mA            |

**LP5811**

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Unless specified otherwise, typical characteristics apply over the full ambient temperature range ( $-40^{\circ}\text{C} < \text{TA} < +85^{\circ}\text{C}$ ),  $\text{V}_{\text{IN}} = 3.6\text{ V}$ ,  $\text{V}_{\text{OUT}} = 5\text{ V}$ ,  $\text{C}_{\text{IN}} = 1\text{ }\mu\text{F}$ ,  $\text{C}_{\text{OUT}} = 1\text{ }\mu\text{F}$ .

| PARAMETER                     |  | TEST CONDITIONS   | MIN                            | TYP  | MAX  | UNIT          |
|-------------------------------|--|---|--------------------------------|------|------|---------------|
| $\text{I}_{\text{CS\_LKG}}$   | Constant current sink leakage current  | $\text{V}_{\text{IN}} = 3.6\text{ V}$ , $\text{OUTx} = 1\text{ V}$ , $\text{manual\_pwm\_x} = 0$ (0%)   |                                | 0.1  | 1    | $\mu\text{A}$ |
| $\text{I}_{\text{ERR\_D2D}}$  | Device to device current error,<br>$\text{I}_{\text{ERR\_D2D}} = (\text{I}_{\text{AVE}} - \text{I}_{\text{SET}}) / \text{I}_{\text{SET}} \times 100\%$   | All LEDs turn ON. Current set to 0.1 mA ( $\text{max\_current} = 0$ , $\text{manual\_dc\_x} = 01\text{h}$ , $\text{manual\_pwm\_x} = \text{FFh}$ )  | -5                             |      | 5    | %             |
|                               |  | All LEDs turn ON. Current set to 0.2 mA ( $\text{max\_current} = 1$ , $\text{manual\_dc\_x} = 01\text{h}$ , $\text{manual\_pwm\_x} = \text{FFh}$ )  | -3                             |      | 3    | %             |
|                               |  | All LEDs turn ON. Current set to 1 mA ( $\text{max\_current} = 0$ , $\text{manual\_dc\_x} = 0Ah$ , $\text{manual\_pwm\_x} = \text{FFh}$ )           | -5                             |      | 5    | %             |
|                               |  | All LEDs turn ON. Current set to 1 mA ( $\text{max\_current} = 1$ , $\text{manual\_dc\_x} = 05\text{h}$ , $\text{manual\_pwm\_x} = \text{FFh}$ )    | -3                             |      | 3    | %             |
|                               |  | All LEDs turn ON. Current set to 25.5 mA ( $\text{max\_current} = 0$ , $\text{manual\_dc\_x} = \text{FFh}$ , $\text{manual\_pwm\_x} = \text{FFh}$ ) | -5                             |      | 5    | %             |
|                               |  | All LEDs turn ON. Current set to 51 mA ( $\text{max\_current} = 1$ , $\text{manual\_dc\_x} = \text{FFh}$ , $\text{manual\_pwm\_x} = \text{FFh}$ )   | -3                             |      | 3    | %             |
| $\text{I}_{\text{ERR\_C2C}}$  | Channel to Channel current error<br>$\text{I}_{\text{ERR\_C2C}} = (\text{I}_{\text{OUTx}} - \text{I}_{\text{AVE}}) / \text{I}_{\text{AVE}} \times 100\%$ | All LEDs turn ON. Current set to 0.1 mA ( $\text{max\_current} = 0$ , $\text{manual\_dc\_x} = 01\text{h}$ , $\text{manual\_pwm\_x} = \text{FFh}$ )  | -5                             |      | 5    | %             |
|                               |  | All LEDs turn ON. Current set to 0.2 mA ( $\text{max\_current} = 1$ , $\text{manual\_dc\_x} = 01\text{h}$ , $\text{manual\_pwm\_x} = \text{FFh}$ )  | -3                             |      | 3    | %             |
|                               |  | All LEDs turn ON. Current set to 1 mA ( $\text{max\_current} = 0$ , $\text{manual\_dc\_x} = 0Ah$ , $\text{manual\_pwm\_x} = \text{FFh}$ )           | -5                             |      | 5    | %             |
|                               |  | All LEDs turn ON. Current set to 1 mA ( $\text{max\_current} = 1$ , $\text{manual\_dc\_x} = 05\text{h}$ , $\text{manual\_pwm\_x} = \text{FFh}$ )    | -3                             |      | 3    | %             |
|                               |  | All LEDs turn ON. Current set to 25.5 mA ( $\text{max\_current} = 0$ , $\text{manual\_dc\_x} = \text{FFh}$ , $\text{manual\_pwm\_x} = \text{FFh}$ ) | -5                             |      | 5    | %             |
|                               |  | All LEDs turn ON. Current set to 51 mA ( $\text{max\_current} = 1$ , $\text{manual\_dc\_x} = \text{FFh}$ , $\text{manual\_pwm\_x} = \text{FFh}$ )   | -3                             |      | 3    | %             |
| $\text{V}_{\text{HR}}$        | LED driver output hearroom voltage   | All LEDs turn ON. Current set to 25.5 mA ( $\text{max\_current} = 0$ , $\text{manual\_dc\_x} = \text{FFh}$ )  |                                | 0.11 | 0.15 | V             |
|                               |  | All LEDs turn ON. Current set to 51 mA ( $\text{max\_current} = 1$ , $\text{manual\_dc\_x} = \text{FFh}$ )  |                                | 0.21 | 0.28 | V             |
| $\text{f}_{\text{LED\_PWM}}$  | LED PWM frequency  | $\text{pwm\_fre} = 0$   |                                | 24   |      | kHz           |
|                               |  | $\text{pwm\_fre} = 1$   |                                | 12   |      | kHz           |
| $\text{f}_{\text{OSC}}$       | Internal oscillator frequency  | $\text{vsync\_out\_en} = 1$   |                                | 6    |      | MHz           |
| <b>Logic Interface</b>        |  |   |                                |      |      |               |
| $\text{V}_{\text{EN\_H}}$     | EN logic high  | $\text{V}_{\text{IN}} > 1.8\text{ V}$   | 1.2                            |      |      | V             |
| $\text{V}_{\text{EN\_L}}$     | EN logic low   | $\text{V}_{\text{IN}} > 1.8\text{ V}$   |                                |      | 0.35 | V             |
| $\text{V}_{\text{IH\_LOGIC}}$ | High level input voltage of SDA, SCL, SYNC   |   | 1.4                            |      |      | V             |
| $\text{V}_{\text{IL\_LOGIC}}$ | Low level input voltage of SDA, SCL, SYNC  |   |                                |      | 0.4  | V             |
| $\text{V}_{\text{OH\_LOGIC}}$ | High level output voltage of SYNC  |   | $\text{V}_{\text{VOUT}} - 0.2$ |      |      | V             |



Unless specified otherwise, typical characteristics apply over the full ambient temperature range ( $-40^{\circ}\text{C} < T_A < +85^{\circ}\text{C}$ ),  $V_{\text{IN}} = 3.6\text{ V}$ ,  $V_{\text{OUT}} = 5\text{ V}$ ,  $C_{\text{IN}} = 1\text{ }\mu\text{F}$ ,  $C_{\text{OUT}} = 1\text{ }\mu\text{F}$ .

| PARAMETER              |   | TEST CONDITIONS   | MIN                          | TYP                          | MAX                          | UNIT               |
|------------------------|---|---|------------------------------|------------------------------|------------------------------|--------------------|
| $V_{\text{OL\_LOGIC}}$ | Low level output voltage of SDA, SYNC               |   |                              |                              | 0.4                          | V                  |
| <b>Protection</b>      |   |   |                              |                              |                              |                    |
| $T_{\text{SD}}$        | Thermal shutdown threshold for LED driver part      | $T_J$ rising  |                              | 150                          |                              | $^{\circ}\text{C}$ |
|                        | Thermal shutdown threshold for Boost converter part | $T_J$ rising  |                              | 155                          |                              | $^{\circ}\text{C}$ |
| $T_{\text{SD\_HYS}}$   | Thermal shutdown hysteresis                         | $T_J$ falling below $T_{\text{SD}}$                         |                              | 15                           |                              | $^{\circ}\text{C}$ |
| $V_{\text{LOD\_TH}}$   | LED open detection threshold                        | Current set to 25.5 mA (max_current = 0, manual_dc_x = FFh) | 70                           | 90                           | 110                          | mV                 |
|                        |   | Current set to 51 mA (max_current = 1, manual_dc_x = FFh)   | 150                          | 180                          | 220                          | mV                 |
| $V_{\text{LSD\_TH}}$   | LED short detection threshold                       | lsd_th = 00h  | $0.32 \times V_{\text{OUT}}$ | $0.35 \times V_{\text{OUT}}$ | $0.38 \times V_{\text{OUT}}$ | V                  |
|                        |   | lsd_th = 01h  | $0.42 \times V_{\text{OUT}}$ | $0.45 \times V_{\text{OUT}}$ | $0.48 \times V_{\text{OUT}}$ | V                  |
|                        |   | lsd_th = 10h  | $0.52 \times V_{\text{OUT}}$ | $0.55 \times V_{\text{OUT}}$ | $0.58 \times V_{\text{OUT}}$ | V                  |
|                        |   | lsd_th = 11h  | $0.62 \times V_{\text{OUT}}$ | $0.65 \times V_{\text{OUT}}$ | $0.68 \times V_{\text{OUT}}$ | V                  |

## 6.6 Timing Requirements

Unless specified otherwise, typical characteristics apply over the full ambient temperature range ( $-40^{\circ}\text{C} < T_A < +85^{\circ}\text{C}$ ),  $V_{\text{IN}} = 3.6\text{ V}$ ,  $V_{\text{CC}} = 5\text{ V}$ ,  $C_{\text{IN}} = 1\text{ }\mu\text{F}$ ,  $C_{\text{OUT}} = 1\text{ }\mu\text{F}$ .

| I <sup>2</sup> C Timing Requirements |  | MIN | NOM | MAX  | UNIT          |
|--------------------------------------|--|-----|-----|------|---------------|
| <b>Standard-mode</b>                 |  |     |     |      |               |
| $f_{\text{SCL}}$                     | SCL clock frequency  | 0   |     | 100  | kHz           |
| $t_{\text{HD\_STA}}$                 | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 4   |     |      | $\mu\text{s}$ |
| $t_{\text{LOW}}$                     | LOW period of the SCL clock  | 4.7 |     |      | $\mu\text{s}$ |
| $t_{\text{HIGH}}$                    | HIGH period of the SCL clock   | 4   |     |      | $\mu\text{s}$ |
| $t_{\text{SU\_STA}}$                 | Set-up time for a repeated START condition   | 4.7 |     |      | $\mu\text{s}$ |
| $t_{\text{HD\_DAT}}$                 | Data hold time   | 0   |     |      | $\mu\text{s}$ |
| $t_{\text{SU\_DAT}}$                 | Data set-up time   | 250 |     |      | ns            |
| $t_r$                                | Rise time of both SDA and SCL signals  |     |     | 1000 | ns            |
| $t_f$                                | Fall time of both SDA and SCL signals  |     |     | 300  | ns            |
| $t_{\text{SU\_STO}}$                 | Set-up time for STOP condition   | 4   |     |      | $\mu\text{s}$ |
| $t_{\text{BUF}}$                     | Bus free time between a STOP and START condition   | 4.7 |     |      | $\mu\text{s}$ |
| $C_b$                                | Capacitive load for each bus line  |     |     | 400  | pF            |
| <b>Fast-mode</b>                     |  |     |     |      |               |
| $f_{\text{SCL}}$                     | SCL clock frequency  | 0   |     | 400  | kHz           |
| $t_{\text{HD\_STA}}$                 | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 0.6 |     |      | $\mu\text{s}$ |
| $t_{\text{LOW}}$                     | LOW period of the SCL clock  | 1.3 |     |      | $\mu\text{s}$ |
| $t_{\text{HIGH}}$                    | HIGH period of the SCL clock   | 0.6 |     |      | $\mu\text{s}$ |
| $t_{\text{SU\_STA}}$                 | Set-up time for a repeated START condition   | 0.6 |     |      | $\mu\text{s}$ |
| $t_{\text{HD\_DAT}}$                 | Data hold time   | 0   |     |      | $\mu\text{s}$ |
| $t_{\text{SU\_DAT}}$                 | Data set-up time   | 100 |     |      | ns            |
| $t_r$                                | Rise time of both SDA and SCL signals  |     |     | 300  | ns            |

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Unless specified otherwise, typical characteristics apply over the full ambient temperature range ( $-40^{\circ}\text{C} < T_A < +85^{\circ}\text{C}$ ),  $V_{\text{IN}} = 3.6\text{ V}$ ,  $V_{\text{CC}} = 5\text{ V}$ ,  $C_{\text{IN}} = 1\text{ }\mu\text{F}$ ,  $C_{\text{OUT}} = 1\text{ }\mu\text{F}$ .

| I <sup>2</sup> C Timing Requirements |  | MIN  | NOM | MAX  | UNIT          |
|--------------------------------------|--|------|-----|------|---------------|
| $t_f$                                | Fall time of both SDA and SCL signals  |      |     | 300  | ns            |
| $t_{\text{SU\_STO}}$                 | Set-up time for STOP condition   | 0.6  |     |      | $\mu\text{s}$ |
| $t_{\text{BUF}}$                     | Bus free time between a STOP and START condition   | 1.3  |     |      | $\mu\text{s}$ |
| $C_b$                                | Capacitive load for each bus line  |      |     | 400  | pF            |
| <b>Fast-mode Plus</b>                |  |      |     |      |               |
| $f_{\text{SCL}}$                     | SCL clock frequency  | 0    |     | 1000 | kHz           |
| $t_{\text{HD\_STA}}$                 | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 0.26 |     |      | $\mu\text{s}$ |
| $t_{\text{LOW}}$                     | LOW period of the SCL clock  | 0.5  |     |      | $\mu\text{s}$ |
| $t_{\text{HIGH}}$                    | HIGH period of the SCL clock   | 0.26 |     |      | $\mu\text{s}$ |
| $t_{\text{SU\_STA}}$                 | Set-up time for a repeated START condition   | 0.26 |     |      | $\mu\text{s}$ |
| $t_{\text{HD\_DAT}}$                 | Data hold time   | 0    |     |      | $\mu\text{s}$ |
| $t_{\text{SU\_DAT}}$                 | Data set-up time   | 50   |     |      | ns            |
| $t_r$                                | Rise time of both SDA and SCL signals  |      |     | 120  | ns            |
| $t_f$                                | Fall time of both SDA and SCL signals  |      |     | 120  | ns            |
| $t_{\text{SU\_STO}}$                 | Set-up time for STOP condition   | 0.26 |     |      | $\mu\text{s}$ |
| $t_{\text{BUF}}$                     | Bus free time between a STOP and START condition   | 0.5  |     |      | $\mu\text{s}$ |
| $C_b$                                | Capacitive load for each bus line  |      |     | 550  | pF            |
| <b>Misc. Timing Requirements</b>     |  |      |     |      |               |
| $f_{\text{CLK\_EX}}$                 | VSYN input clock frequency   |      | 6   |      | MHz           |

## 6.7 Typical Characteristics

Unless specified otherwise, typical characteristics apply over the full ambient temperature range ( $-40^{\circ}\text{C} < T_A < +85^{\circ}\text{C}$ ),  $V_{\text{IN}} = 3.6\text{ V}$ ,  $C_{\text{IN}} = 1\text{ }\mu\text{F}$ ,  $C_{\text{OUT}} = 1\text{ }\mu\text{F}$

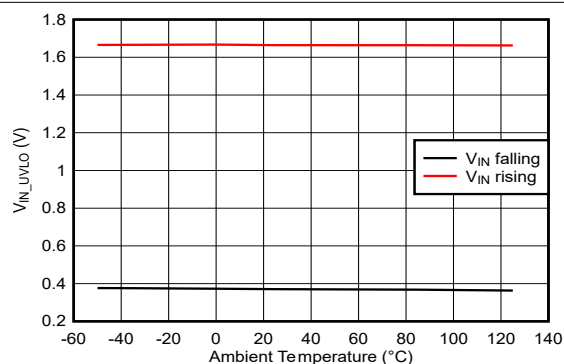


Figure 6-1. VIN UVLO Rising and Falling Thresholds

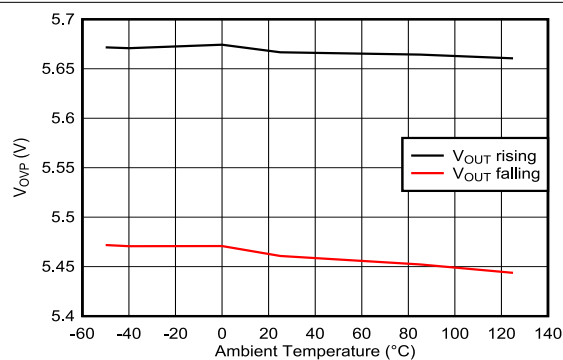


Figure 6-2. VOUT OVP Thresholds

## 6.7 Typical Characteristics (continued)

Unless specified otherwise, typical characteristics apply over the full ambient temperature range ( $-40^{\circ}\text{C} < T_A < +85^{\circ}\text{C}$ ),  $V_{\text{IN}} = 3.6\text{V}$ ,  $C_{\text{IN}} = 1\mu\text{F}$ ,  $C_{\text{OUT}} = 1\mu\text{F}$

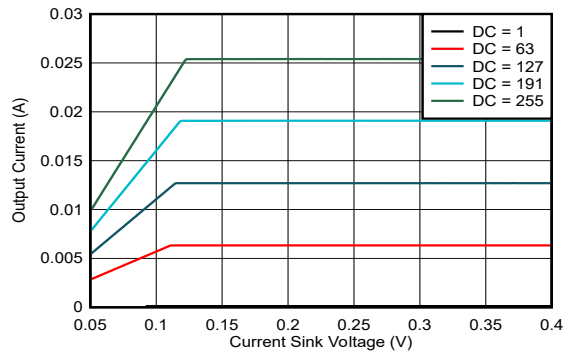


Figure 6-3. Current Sinks Voltage vs Current (MC = 0)

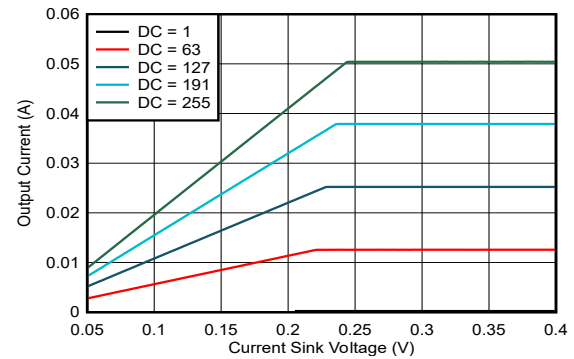


Figure 6-4. Current Sinks Voltage vs Current (MC = 1)

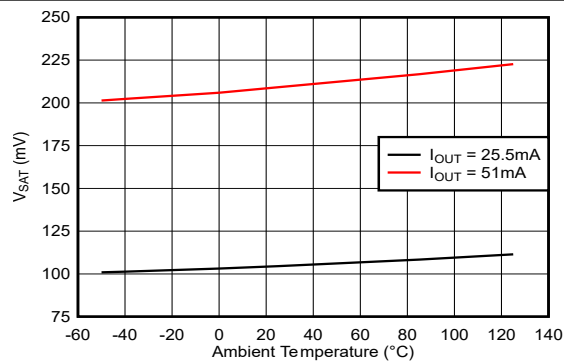


Figure 6-5.  $V_{\text{SAT}}$  vs Temperature

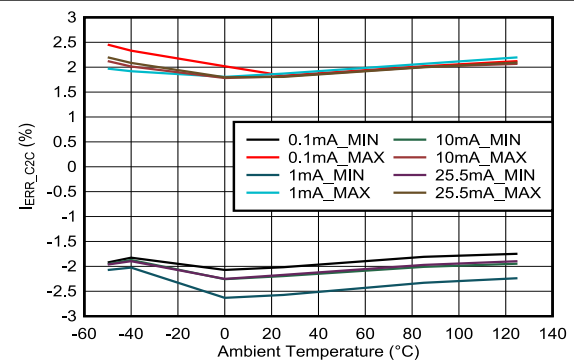


Figure 6-6. Channel-to-Channel Current Accuracy vs Temperature (MC = 0)

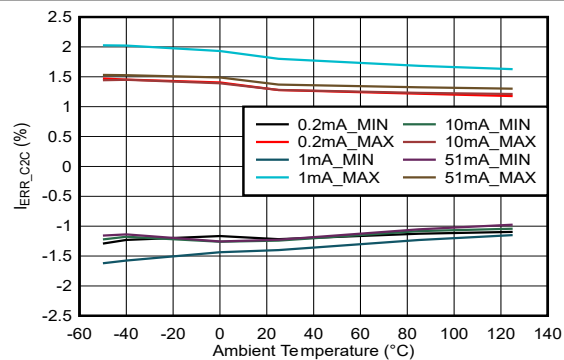


Figure 6-7. Channel-to-Channel Current Accuracy vs Temperature (MC = 1)

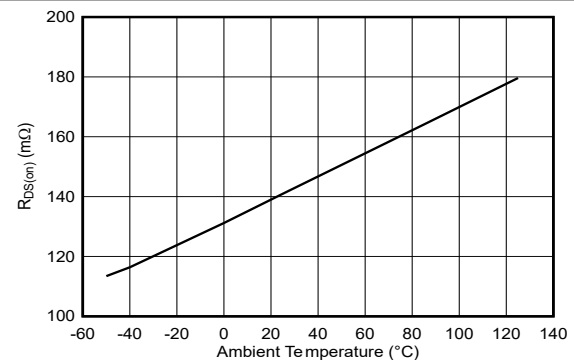


Figure 6-8. Boost High-Side MOSFET  $R_{\text{DS(on)}}$

## 6.7 Typical Characteristics (continued)

Unless specified otherwise, typical characteristics apply over the full ambient temperature range ( $-40^{\circ}\text{C} < T_A < +85^{\circ}\text{C}$ ),  $V_{\text{IN}} = 3.6\text{V}$ ,  $C_{\text{IN}} = 1\mu\text{F}$ ,  $C_{\text{OUT}} = 1\mu\text{F}$

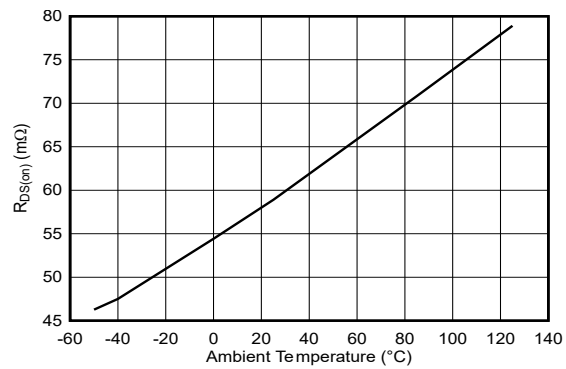


Figure 6-9. Boost Low-Side MOSFET  $R_{\text{DS(on)}}$

## 7 Detailed Description

### 7.1 Overview

The LP5811 is a synchronous boost 4-channel RGBW LED driver with autonomous animation engine control. The device can support 1.8V minimum start-up voltage and 0.5V to 5.5V input voltage range during operation. The integrated synchronous boost converter can output 3V to 5.5V, to provide enough forward voltage of LEDs.

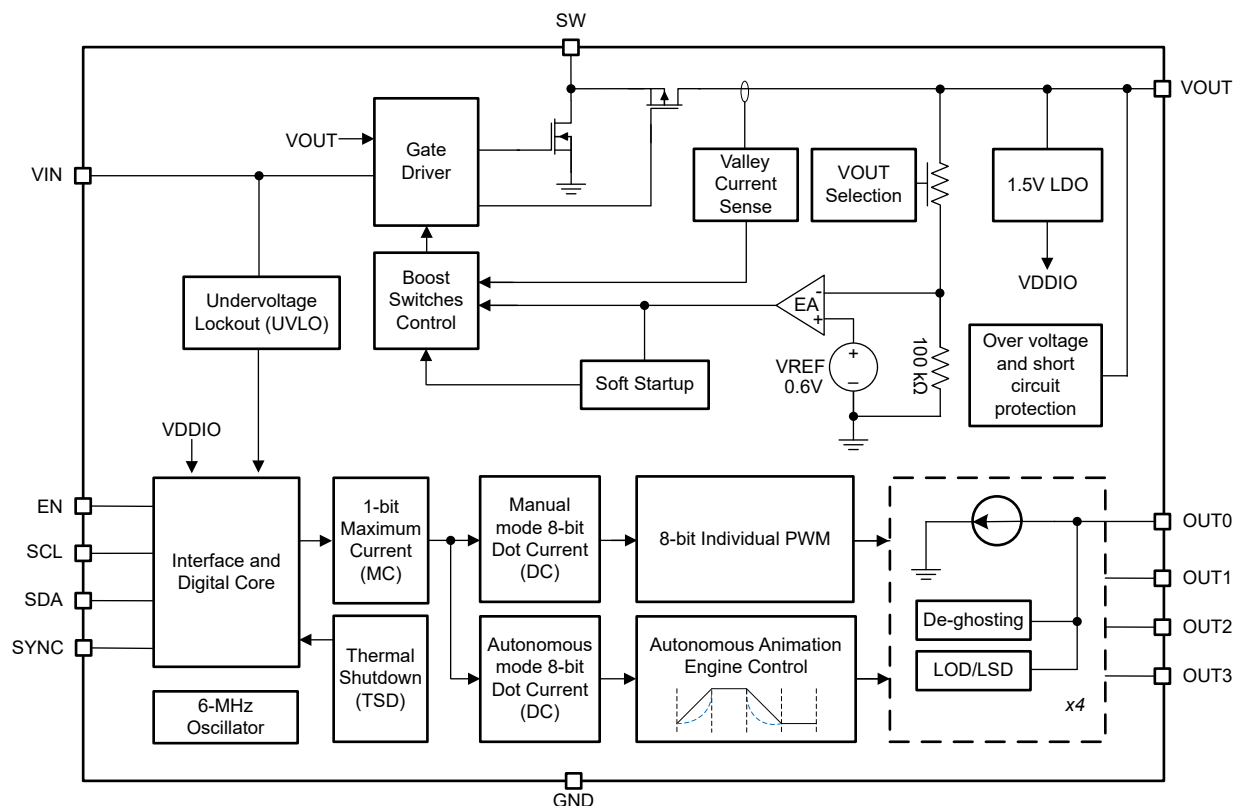
The LP5811 has ultra-low operation current at active mode, consuming about 0.4mA when LED maximum current setting is 25.5mA. If all LEDs are turned off, the device will enter standby state to reduce power consumption with data retained. When 'chip\_enable' bit setting is 0, initial state is entered with minimum power consumption to save power.

The LP5811 supports both analog dimming and PWM dimming. In analog dimming, the output current of each LED can be adjusted with 256 steps. In PWM dimming, the integrated 8-bit configurable PWM generator enables smooth brightness dimming control. Optional exponential PWM dimming can be activated for individual LED to achieve a human-eye-friendly visual performance.

The LP5811 integrates autonomous animation engine, with no need for brightness control commands from controller. Each LED has an individual animation engine which can be configured through the related registers. The device can generate a 6 MHz clock signal, which synchronizes the lighting effects among multiple devices.

The LP5811 has 4 different material versions with different I<sup>2</sup>C chip address. Up to 4 LP581x devices can be connected to the same I<sup>2</sup>C bus and controlled individually. The LP5811 materials and corresponding chip addresses are shown in [Section 4](#).

### 7.2 Functional Block Diagram



**Figure 7-1. Functional Block Diagram**

## 7.3 Feature Description

### 7.3.1 Synchronous Boost Converter

The integrated synchronous boost converter is designed to operate with 0.5V to 5.5V input voltage supply with 1.6A (typ.) valley switch current limit. The LP5811 operates at quasi-constant frequency pulse width modulation (PWM) mode, when driving moderate and heavy load. The switching frequency is 1MHz when the input voltage is above 1.5V. The frequency is reduced to 0.5MHz gradually when the input voltage decreases from 1.5V to 1V, and keeps at 0.5MHz when the input voltage is below 1V. At light load conditions, the boost converter operates at pulse frequency modulation (PFM) mode. During PWM operation, the converter works at adaptive constant on-time valley current mode to achieve excellent line regulation and load regulation, by which a smaller inductor and ceramic capacitors can be supported. Internal loop compensation simplifies the design complexity, and also minimizes the external components.

When powering up, the default output voltage is 3V. The output voltage can be configured at 'Dev\_config\_0' register from 3V to 5.5V, with 0.1V step. The integrated boost works as a general boost converter, which can power not only the LEDs driven by the device itself, but also other loads in the system.

#### 7.3.1.1 Undervoltage Lockout

The LP5811 has a built-in undervoltage lockout (UVLO) circuit to make sure the device working properly. When the input voltage is above the UVLO rising threshold 1.8V, the boost of LP5811 can be enabled. After the LP5811 completes soft-start process and the output voltage rises above 2.2V, the LP5811 can work with the input voltage down to 0.5V. When the input voltage is below UVLO falling threshold 0.4V, the device shuts down.

#### 7.3.1.2 Enable and Soft Start

When the input voltage is above the UVLO rising threshold 1.8V and the EN pin is pulled to a voltage above 1.2V, the boost of LP5811 is enabled and starts up. At the beginning, the LP5811 charges the boost output capacitor with a constant current when the output voltage is below 0.4V. When the output voltage is charged above 0.4V, the LP5811 has capability to drive 200mA load. After the output voltage reaches the input voltage, the boost of LP5811 starts switching, and the output voltage continually ramps up to default voltage 3V. The typical start-up time is 450μs from EN pulled high to output reaching default voltage 3V, at the application that input voltage is 2.5V, output effective capacitance is 10μF, and no load. When the EN is below 0.42V, the internal enable comparator turns the device into shutdown mode. In the shutdown mode, the device is entirely turned off and the output is disconnected from input power supply.

#### 7.3.1.3 Switching Frequency

The LP5811 switches at quasi-constant 1MHz frequency when the input voltage is above 1.5V. When the input voltage is lower than 1.5V, the switching frequency is reduced gradually to 0.5MHz, which improves the boost efficiency and gets higher boost ratio. When the input voltage is below 1V, the switching frequency is fixed at quasi-constant 0.5MHz.

#### 7.3.1.4 Current Limit Operation

The LP5811 uses a valley current limit sensing scheme. The inductor current is detected during the switching off-time, by sensing the voltage across the synchronous rectifier.

When the load current increases, such that the inductor current is above the current limit within the whole switching cycle, the off-time increases to discharge the inductor current. The current decreases below the limit before the next on-time. When the current limit is reached, the output voltage decreases if the load current continually increases.

The maximum continuous output current ( $I_{OUT(CL)}$ ), before entering current limit (CL) operation, can be defined by [Equation 1](#).

$$I_{OUT(CL)} = (1 - D) \times \left( I_{LIM} + \frac{1}{2} \Delta I_{L(P-P)} \right) \quad (1)$$

where

- D is the duty cycle
- $\Delta I_{L(P-P)}$  is the inductor ripple current

The duty cycle can be estimated by [Equation 2](#).

$$D = 1 - \frac{V_{IN} \times \eta}{V_{OUT}} \quad (2)$$

where

- $V_{OUT}$  is the output voltage of the boost converter
- $V_{IN}$  is the input voltage of the boost converter
- $\eta$  is the efficiency of the converter, use 90% for most applications

The peak-to-peak inductor ripple current is calculated by [Equation 3](#).

$$\Delta I_{L(P-P)} = \frac{V_{IN} \times D}{L \times f_{SW}} \quad (3)$$

where

- L is the inductance value of the inductor
- $f_{SW}$  is the switching frequency
- D is the duty cycle
- $V_{IN}$  is the input voltage of the boost converter

#### 7.3.1.5 Boost PWM Mode

The LP5811 uses a quasi-constant 1.0MHz frequency pulse width modulation (PWM) at moderate to heavy load current. Based on the input voltage to output voltage ratio, a circuit predicts the required on-time. At the beginning of the switching cycle, the main switching low-side FET is turned on. The input voltage is applied across the inductor and the inductor current ramps up. In this phase, the output capacitor is discharged by the load current. When the on-time expires, the low-side FET is turned off, and the high-side rectifier FET is turned on. The inductor transfers its stored energy to replenish the output capacitor and supplies the load. The inductor current declines because the output voltage is higher than the input voltage. When the inductor current hits the valley current threshold determined by the output of the error amplifier, the next switching cycle starts again.

The LP5811 has a built-in compensation circuit that can accommodate a wide range of input voltage, output voltage, inductor value, and output capacitor value for stable operation.

#### 7.3.1.6 Boost PFM Mode

The LP5811 works at PFM to improve efficiency at light load. When the load current decreases, the inductor valley current set by the output of the error amplifier no longer regulates the output voltage. When the inductor valley current hits the low limit, the output voltage exceeds the setting voltage as the load current decreases further. When the feedback voltage hits the PFM reference voltage (0.6V typical), the LP5811 works at PFM. When the feedback voltage rises and hits the PFM reference voltage, the device continues switching for several cycles because of the delay time of the internal comparator — then it stops switching. The load is supplied by the output capacitor, and the output voltage declines. When the feedback voltage falls below the PFM reference voltage, after the delay time of the comparator, the device starts switching again to ramp up the output voltage. [Figure 7-2](#) shows the waveform of voltage when the device works at PWM and PFM.

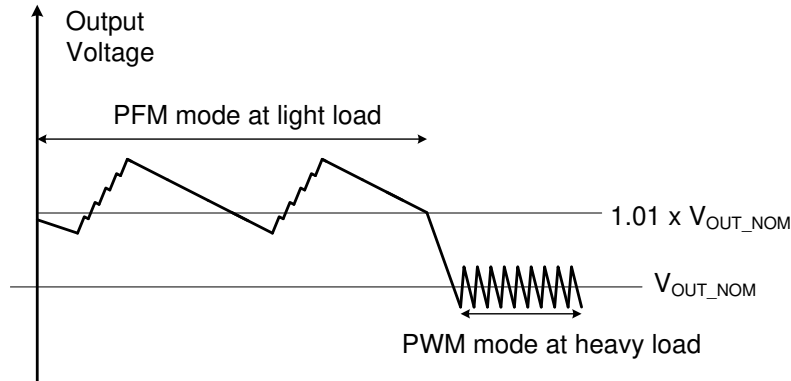


Figure 7-2. Output Voltage in PWM Mode and PFM

### 7.3.2 Analog Dimming

The current gain of each LED can be controlled by 2 methods to achieve analog dimming in the LP5811.

- Global 1-bit Maximum Current (MC) control for all LEDs without external resistor
- Individual 8-bit Dot Current (DC) control for each LED

The maximum output current  $I_{OUT\_max}$  of each current sink can be programmed by the 1-bit max\_current. The default value of max\_current is 0h, which means the LED maximum current is set to 25.5mA in default.

Table 7-1. Maximum Current (MC) Bit Setting

| 1 bit Maximum Current (MC) |             | $I_{OUT\_MAX}$ (mA) |
|----------------------------|-------------|---------------------|
| Binary                     | Decimal     |                     |
| 0 (default)                | 0 (default) | 25.5 (default)      |
| 1                          | 1           | 51                  |

The LP5811 can individually adjust the peak current of each LED by using Dot Current (DC) function. The brightness deviation among the LED bins can be minimized, to achieve uniform display performance. The current is adjusted with 256 steps from 0 to 100% of  $I_{OUT\_MAX}$ , which is programmed in an 8-bit register whose default value is 80h.

Table 7-2. Dot Current (DC) Bits Setting

| 8-bits Dot Current (DC) Register |               | Ratio of $I_{OUT\_MAX}$ |
|----------------------------------|---------------|-------------------------|
| Binary                           | Decimal       |                         |
| 0000 0000                        | 0             | 0%                      |
| 0000 0001                        | 1             | 0.39%                   |
| 0000 0010                        | 2             | 0.78%                   |
| ---                              | ---           | ---                     |
| 1000 0000 (default)              | 128 (default) | 50.2% (default)         |
| ---                              | ---           | ---                     |
| 1111 1101                        | 253           | 99.2%                   |
| 1111 1110                        | 254           | 99.6%                   |
| 1111 1111                        | 255           | 100%                    |

By configuring the MC and DC, the peak current of each current sink can be calculated as [Equation 4](#):

$$I_{OUT} (mA) = I_{OUT\_max} \times \frac{DC}{255} \quad (4)$$

The average current of each LED in TCM drive mode and mix drive mode is shown as [Equation 5](#):



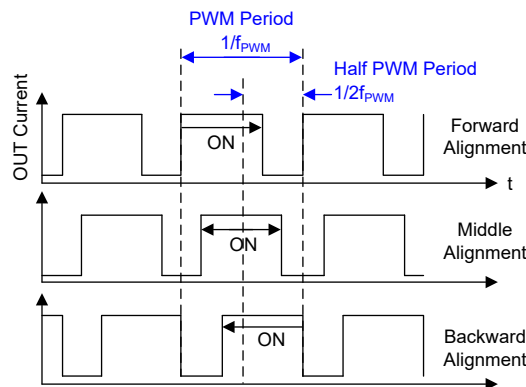
$$I_{AVE} (mA) = \frac{I_{OUT}}{N} \times \frac{DC}{255} \times D_{PWM} \quad (5)$$

- N is the total scan number setting.
- $D_{PWM}$  is the PWM duty.

### 7.3.3 PWM Dimming

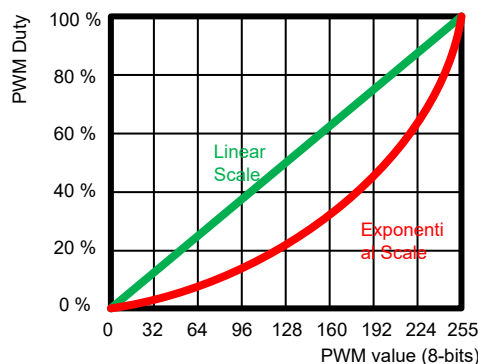
The LP5811 supports 8-bit PWM dimming with 24kHz or 12kHz frequency, which is configured by 'PWM\_Fre' bit in Dev\_config\_1 register. An internal 6MHz oscillator is used to generate the PWM clock. SYNC pin can be configured as PWM clock input or output by configure 'vsync\_out\_en' bit in Dev\_Config\_11 register. If multiple LP5811 are used in the system with autonomous animation engine control, all devices can refer the same clock signal, which comes from one of LP5811 or external controller, to avoid animation mismatch in long time operation.

Each LED can be configured into 3 different PWM alignment phases: Forward, Middle, and Backward. The alignment phase of each LED is set by 'phase\_align' bits in Dev\_Config\_7 to Dev\_Config\_10 registers. By turning on the LEDs in different phase, the peak current load from boost or the system power supply is greatly decreased. The input current ripple and ceramic-capacitor audible ringing can also be reduced. Figure 7-3 shows the PWM alignment phases. In the forward alignment, the rising edge of PWM pulse is fixed at the beginning of PWM period. In the middle alignment, the middle point of PWM pulse is fixed at the middle of PWM period, while the pulse spreads to both directions. In the backward alignment, the falling edge of PWM pulse is fixed at the end of PWM period.



**Figure 7-3. PWM Alignment Scheme**

The LP5811 allow users to configure the dimming scale as exponential curve or linear curve, through the 'exp\_en' bits in Dev\_Config\_5 and Dev\_Config\_6 registers. A human-eye-friendly visual performance can be achieved by using the internal exponential scale. The linear scale has great linearity between PWM duty cycle and PWM setting value, which provides flexible approach for external controlled gamma correction algorithm. The 8-bit linear and exponential curves are shown as Figure 7-4.



**Figure 7-4. Linear and Exponential PWM Dimming Curves**

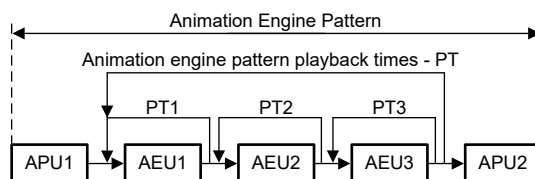
### 7.3.4 Autonomous Animation Engine Control

The LP5811 supports both manual mode and autonomous mode to control the DC and PWM of each LED. In manual mode, the LEDs are directly controlled by the related configuration registers and reflect the value immediately. In autonomous mode, the autonomous animation engine is applied for each LED, which can realize vivid lighting effects without external processor control. The animation engine pattern is composed by 3 animation engine units (AEU) and 2 animation pause units (APU) for complex and flexible control. One AEU is formed by 4 slopers, which is used for fading effect.

After setting up all animation engine pattern configurations, sending start\_cmd to the device can let the animation running autonomously, to free external controller real-time loading. The PWM value and unit status of each LED can be read from PWM\_value registers and pattern\_status registers. To make sure the precision of reading results, sending pause\_cmd to pause the animation firstly is recommended.

#### 7.3.4.1 Animation Engine Pattern

Each LED of the LP5811 has own animation engine, to achieve premium visual lighting effects. One whole animation engine pattern is defined as [Figure 7-5](#). 3 animation engine units (AEU) and 2 animation pause units (APU) compose the animation engine pattern. AEU2 and AEU3 can be skipped by setting the playback times to 0. The LED current of each LEDs in the autonomous mode is set through the Autonomous\_DC registers.



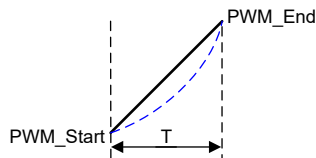
**Figure 7-5. Animation engine pattern**

The whole animation pattern includes two APUs and three AEUs with several playback times:

- APU<sub>x</sub> (x = 1, 2): Animation pause unit, each unit includes one timing value T.
- AEU<sub>x</sub> (x = 1, 2, 3): Animation engine unit, including 5 PWM values PWM1 to PWM5 and 4 time values T1 to T4.
- PT: Playback times of AEU1+AEU2+AEU3, which has 2-bit value to set 0/1/2/Infinite times.
- PT<sub>x</sub>: Playback times of AEU<sub>x</sub> (x=1/2/3), which has 2-bit value to set 0/1/2/Infinite times.

#### 7.3.4.2 Sloper

Sloper is the basic element to achieve autonomous fade-in and fade-out animations. It can achieve 256 steps fade-in or fade-out effects from 'PWM\_Start' to 'PWM\_End' within a target time period T as [Figure 7-6](#). The 8-bit PWM steps, which is configurable in animation pattern PWM setting registers, help to achieve extremely smooth effects. Exponential dimming curve can also be supported in the sloper.



**Figure 7-6. Sloper curve demonstration**

The programmable time T is selectable from 0 to around 8s with 16 levels shown in [Table 7-3](#).

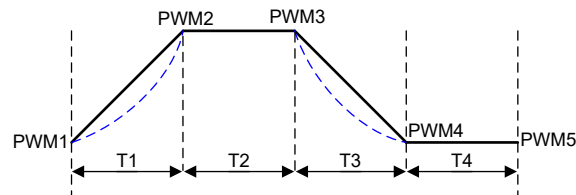
**Table 7-3. Programmable time options**

| Register value | 0h  | 1h     | 2h     | 3h     | 4h     | 5h     | 6h     | 7h     | 8h     | 9h     | Ah     | Bh     | Ch     | Dh     | Eh     | Fh     |
|----------------|-----|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| Time (Typ.)    | 0 s | 0.09 s | 0.18 s | 0.36 s | 0.54 s | 0.80 s | 1.07 s | 1.52 s | 2.06 s | 2.50 s | 3.04 s | 4.02 s | 5.01 s | 5.99 s | 7.06 s | 8.05 s |

#### 7.3.4.3 Animation Engine Unit (AEU)

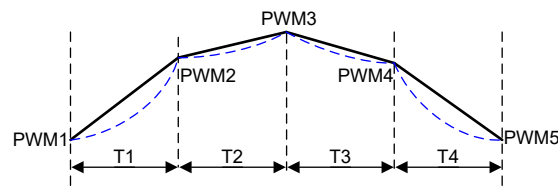
The AEU is the most important unit to achieve autonomous animation effects. One AEU is formed by 4 slopers. There are 5 PWM values and 4 time values can be configured in the AEU. Each PWMx (x = 1, 2,..., 5) can be arbitrarily programmed from 0 to 255, The Tx (x = 1, 2, 3, 4) is selectable from 0 to 8 s with 16 levels referring to [Table 7-3](#). If two adjacent PWM values are equal, the brightness keeps unchange within the time setting. When a Tx is set to 0, this sloper is skipped. To avoid flicker happens due to PWM value suddenly changes, the begin and end PWM of this sloper need to be the same.

Typical breathing effect example is illustrated as [Figure 7-7](#).



**Figure 7-7. Animation engine unit - Example 1**

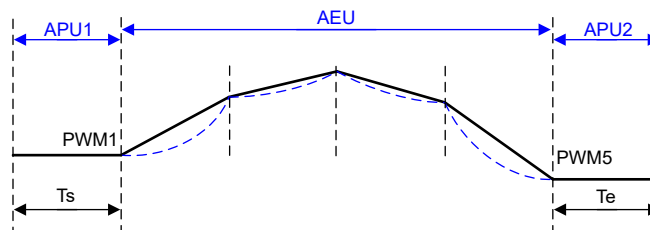
Advanced breathing effect example is shown in [Figure 7-8](#). 2 different fading speeds are set in the PWM rising and falling phases, to achieve a complex animation.



**Figure 7-8. Animation engine unit - Example 2**

#### 7.3.4.4 Animation Pause Unit (APU)

The APU is defined as the pausing time at the beginning and the end of the animation pattern. The APU contains 1 time value which is selectable from 0 to 8s with 16 levels referring to [Table 7-3](#). If the value is set as 0, the APU is skipped. The brightness of APU1 uses the PWM1 value of the AEU following the APU1, while the brightness of APU2 uses the PWM5 value of the AEU in front of APU2. One animation pattern example is shown in [Figure 7-9](#). Only AEU2 is enabled in the pattern, so that the brightness of APU1 uses the PWM1 value of AEU2, and the brightness of APU2 uses PWM5 value of AEU2.



**Figure 7-9. APU example**

### 7.3.5 Protections and Diagnostics

#### 7.3.5.1 Overvoltage Protection

The boost of LP5811 has an output overvoltage protection (OVP) to protect the device. When the output voltage is above 5.7V, the boost stops switching. Once the output voltage falls 0.1V below the OVP threshold, the boost resumes operating again.

### 7.3.5.2 Output Short-to-Ground Protection

The boost of LP5811 starts to limit the boost current when the boost output voltage is below 1.8V. The lower the boost output voltage reaches, the smaller the output current decreases. When the VOUT pin is short to ground and the boost output voltage is less than 0.4V, the output current is limited to approximately 350mA. Once the short circuit is released, the LP5811 goes through the soft start-up again to the regulated output voltage.

### 7.3.5.3 LED Open Detections

The LP5811 integrates LED open detection (LOD) for the fault caused by any open LED. The threshold for LOD is 90 mV when max current is set as 25.5 mA, and 180 mV when max current is set as 51 mA. To have enough detection time, LOD can only be performed when the PWM setting of this LED is above 25. If the voltage on the cathode of this LED is lower than the LOD threshold in continuously 3 cycles, LED open of this LED is reported to the corresponding LOD\_status register.

The LOD flags can be cleared by writing 1h to 'lod\_clear' bit in Fault\_Clear register. If the LED open status is removed, the related 'lod\_status' bit is set to 0 automatically.

The 'lod\_action' bit in Dev\_config\_12 register can determine the action once open fault is detected. When the 'lod\_action' bit is set to 1h, the dot where LED open happens is turned off to avoid any unpredictable issue. When the 'lod\_action' bit is 0, no additional action is taken after LOD is detected. LED open fault detection and action is only executed in NORMAL state.

### 7.3.5.4 LED Short Detections

The LP5811 integrates LED short detection (LSD) for the fault caused by any short LED. The threshold of LSD is able to configure from  $(0.35 \times V_{OUT})$  V to  $(0.65 \times V_{OUT})$  V by configuring `lzd_threshold` in `Dev_config_12` register. To have enough detection time, LSD can only be performed when the PWM setting of this LED is above 25. If the voltage on the cathode of this LED is higher than the LSD threshold in continuously 3 cycles, LED short of this LED is reported to the corresponding `LSD_status` register.

The LSD flags can be cleared by writing 1h to `lzd_clear` in `Fault_CLR` register. If the LED short status is removed, the related `lzd_status` bit is set to 0 automatically.

The 'lzd\_action' bit in `Dev_config_12` register can determine the reaction once open fault is detected. When the 'lzd\_action' bit is set to 1h, all LEDs are turned off which is called one fails all fail (OFAF) action, to prevent potential damage caused by the short issue. The device enters to `STANDBY` state after sending 'lzd\_clear' command. When the 'lzd\_action' bit is 0, no additional action is taken after LSD is detected. LSD detection is only executed in `NORMAL` state.

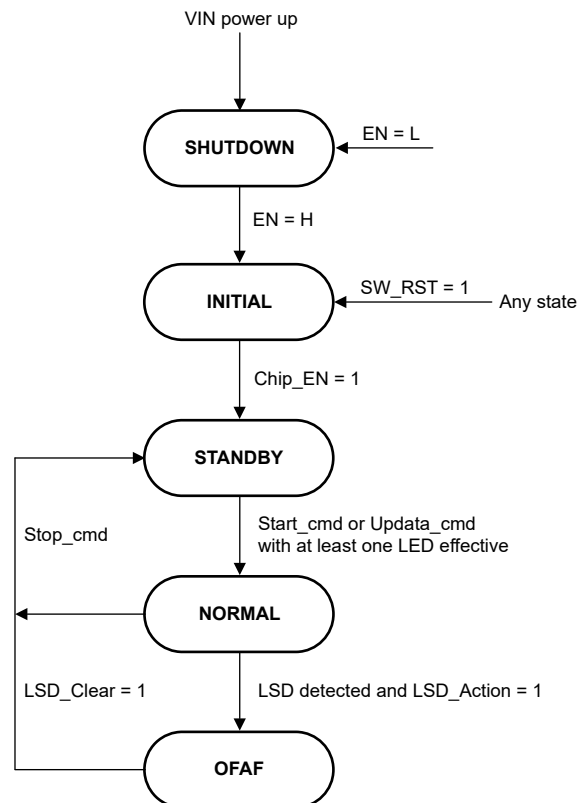
### 7.3.5.5 Thermal Shutdown

The LED driver of LP5811 goes into thermal shutdown state once the junction temperature exceeds 150°C. All LEDs turn off to avoid damaging the device. When the junction temperature drops below the thermal shutdown recovery temperature 130°C, the LED driver starts operating again.

The boost converter of LP5811 stops switching and is shutdown once the junction temperature exceeds 155°C, and the power on reset of the LED driver part is also triggered. When the junction temperature drops below the thermal shutdown recovery temperature, typically 130°C, the LP5811 enters shutdown state, and then the device needs to be configured again for normal operations.

## 7.4 Device Functional Modes

The [Figure 7-10](#) shows the main state machine of the LED driver.



**Figure 7-10. LP5811 Functional Modes**

- **SHUTDOWN:** The device enters into SHUTDOWN after VIN power up.
- **INITIAL:** The device enters into INITIAL state from SHUTDOWN when EN is pulled high.
- **STANDBY:** The device enters into STANDBY state from INITIAL when Chip\_EN is set to 1. The device can also enter into STANDBY from NORMAL when no LED is effective, or Stop\_cmd is received, or from OFAF when LSD\_Clear = 1.
- **NORMAL:** The device enters NORMAL state from STANDBY when one or more LEDs are effective: for manual mode, at least one LED is enable (PWM and DC setting is not 0); for autonomous mode, at least one LED is enable and Start\_cmd is received.
- **OFAF:** The device enters OFAF (one fail all fail) state when LED short is detected and LSD\_Action =1. In OFAF mode, all LEDs are turned off. Once LSD\_Clear is written to 1, the device enters back to STANDBY state.

## 7.5 Programming

The LP5811 is compatible with I<sup>2</sup>C standard specification. The device supports standard mode (100-kHz maximum), fast mode (400-kHz maximum), and fast plus mode (1-MHz maximum). The device has 4 different chip address versions, which allows connecting up to four parallel devices in one I<sup>2</sup>C bus.

### I<sup>2</sup>C Data Transactions

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when clock signal is LOW. START and STOP conditions classify the beginning and the end of the data transfer session. A START condition is defined as the SDA signal transitioning from HIGH to LOW while SCL line is HIGH. A STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The bus leader always generates START and STOP conditions. The bus is considered to be busy after a START condition and free after a STOP condition. During data transmission, the bus leader can generate repeated START conditions. First START and repeated START conditions are functionally equivalent.

Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the leader. The leader releases the SDA line (HIGH) during the acknowledge clock pulse. The device pulls down the SDA line during the 9<sup>th</sup> clock pulse, signifying an acknowledge. The device generates an acknowledge after each byte has been received.

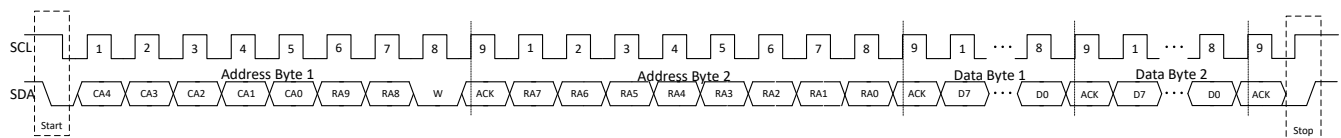
There is one exception to the acknowledge after every byte rule. When the leader is the receiver, the receiver must indicate to the transmitter an end of data by not acknowledging (*negative acknowledge*) the last byte clocked out of the follower. This negative acknowledge still includes the acknowledge clock pulse (generated by the leader), but the SDA line is not pulled down.

### I<sup>2</sup>C Data Format

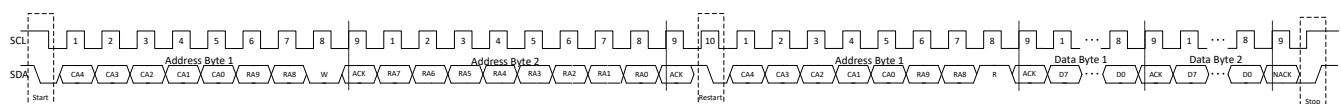
The address and data bits are transmitted MSB first with 8-bits length format in each cycle. Each transmission is started with Address Byte 1, which are divided into 5 bits of the chip address, 2 higher bits of the register address, and 1 read/write bit. The other 8 lower bits of register address are put in Address Byte 2. The device supports both independent mode and broadcast mode. The auto-increment feature allows writing / reading several consecutive registers within one transmission. If not consecutive, a new transmission must be started. The Bit 4 and Bit 3 are determined by the device, which can refer to [Section 4](#).

**Table 7-4. I<sup>2</sup>C Data Format**

| Address Byte1 | Chip Address        |                     |                     |                     |                     | Register Address    |                     | R/W       |
|---------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|-----------|
|               | Bit 7               | Bit 6               | Bit 5               | Bit 4               | Bit 3               | Bit 2               | Bit 1               | Bit 0     |
| Independent   | 1                   | 0                   | 1                   | Bit 4               | Bit 3               | 9 <sup>th</sup> bit | 8 <sup>th</sup> bit | R: 1 W: 0 |
| Broadcast     | 1                   | 1                   | 0                   | 1                   | 1                   |                     |                     |           |
| Address Byte2 | Register Address    |                     |                     |                     |                     |                     |                     |           |
|               | Bit 7               | Bit 6               | Bit 5               | Bit 4               | Bit 3               | Bit 2               | Bit 1               | Bit 0     |
|               | 7 <sup>th</sup> bit | 6 <sup>th</sup> bit | 5 <sup>th</sup> bit | 4 <sup>th</sup> bit | 3 <sup>rd</sup> bit | 2 <sup>nd</sup> bit | 1 <sup>st</sup> bit | 0 bit     |



**Figure 7-11. I<sup>2</sup>C Write Timing**



**Figure 7-12. I<sup>2</sup>C Read Timing**

## 7.6 Register Maps

This section provides a summary of the LP5811 register maps.

**Table 7-5. Register Section/Block Access Type Codes**

| Access Type                   | Code         | Description                                   |
|-------------------------------|--------------|---|
| <b>Read Type</b>              |              |   |
| R                             | R            | Read  |
| RC                            | R<br>C       | Read<br>to Clear                              |
| R-0                           | R<br>-0      | Read<br>Returns 0s                            |
| <b>Write Type</b>             |              |   |
| W                             | W            | Write   |
| W0CP                          | W<br>0C<br>P | W<br>0 to clear<br>Requires privileged access |
| <b>Reset or Default Value</b> |              |   |
| -n                            |              | Value after reset or the default value        |

**Table 7-6. LP5811 Registers Map**

| Register Group | Register Acronym             | Address(Hex.) | Function  | Type |
|----------------|------------------------------|---------------|---|------|
| ChipEN         | Chip_en                      | 000           | Chip enable   | R/W  |
| CONFIG         | Dev_config0 ~ Dev_config12   | 001 ~ 00D     | Device configuration registers  | R/W  |
| Update CMD     | Update_cmd                   | 010           | Configuration update command: CONFIG registers will ONLY be effective by sending this command         | R/W  |
| Start CMD      | Start_cmd                    | 011           | Autonomous control start command or restart with the latest setting                                   | R/W  |
| Stop CMD       | Stop_cmd                     | 012           | LED driver stop command, LED driver goes to INITIAL state with this command from all the other states | R/W  |
| Pause CMD      | Pause_cmd                    | 013           | Autonomous control pause command  | R/W  |
| Continue CMD   | Continue_cmd                 | 014           | Autonomous control continue command   | R/W  |
| LED EN         | LED_EN1                      | 020           | LED enable registers  | R/W  |
| Fault CLR      | Fault_Clear                  | 022           | Fault clear registers to clear TSD/LOD/LSD faults   | R/W  |
| RESET          | Reset                        | 023           | Software reset  | W    |
| DC_Manual      | DC0 ~ DC3                    | 030 ~ 033     | LED current setting at manual mode  | R/W  |
| PWM_Manual     | PWM0 ~ PWM3                  | 040 ~ 043     | LED PWM setting at manual mode  | R/W  |
| DC_Auto        | DC_Auto0 ~ DC_Auto3          | 050 ~ 053     | LED current setting at autonomous mode  | R/W  |
| LED0 AEP       | Tp, PT, PWM1 ~ PWM5, T1 ~ T4 | 080 ~ 099     | LED0 Animation Engine Pattern parameters  | R/W  |
| LED1 AEP       | Tp, PT, PWM1 ~ PWM5, T1 ~ T4 | 09A ~ 0B3     | LED1 Animation Engine Pattern parameters  | R/W  |
| LED2 AEP       | Tp, PT, PWM1 ~ PWM5, T1 ~ T4 | 0B4 ~ 0CD     | LED2 Animation Engine Pattern parameters  | R/W  |
| LED3 AEP       | Tp, PT, PWM1 ~ PWM5, T1 ~ T4 | 0CE ~ 0E7     | LED3 Animation Engine Pattern parameters  | R/W  |



**Table 7-6. LP5811 Registers Map (continued)**

|        |                                   |           |   |   |
|--------|-----------------------------------|-----------|---|---|
| STATUS | TSD_Config_Status                 | 300       | TSD status and Configuration error indication register              | R |
|        | LOD_Status1 ~ LOD_Status2         | 301 ~ 302 | LOD status registers  | R |
|        | LSD_Status1 ~ LSD_Status2         | 303 ~ 304 | LSD status registers  | R |
|        | PWM_Internal0 ~ PWM_Internal_D2   | 305 ~ 314 | Internal PWM values for LED0 ~ LED_D2                               | R |
|        | PATTERN_Status1 ~ PATTERN_Status8 | 315 ~ 31C | AEP status registers to indicate pattern progress for LED0 ~ LED_D2 | R |

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

The LP5811 is a 4-ch synchronous boost RGB LED driver with autonomous animation engine control. The device is ideal to support battery-powered applications with 0.5V to 5.5V input voltage range. The LP5811 has ultra-low operation current at active mode, and it only consumes 0.4mA when LED current is set at 25mA. In battery powered applications like e-tag, earbud, e-cigarettes, VR headset, RGB mouse, smart speaker, and other handheld devices, LP5811 is ideal to provide premium LED lighting effects with low power consumption and small package.

### 8.2 Typical Application

#### 8.2.1 Application

Figure 8-1 shows an example of typical application, which uses one LP5811 to drive RGBW LEDs through I<sup>2</sup>C communication.

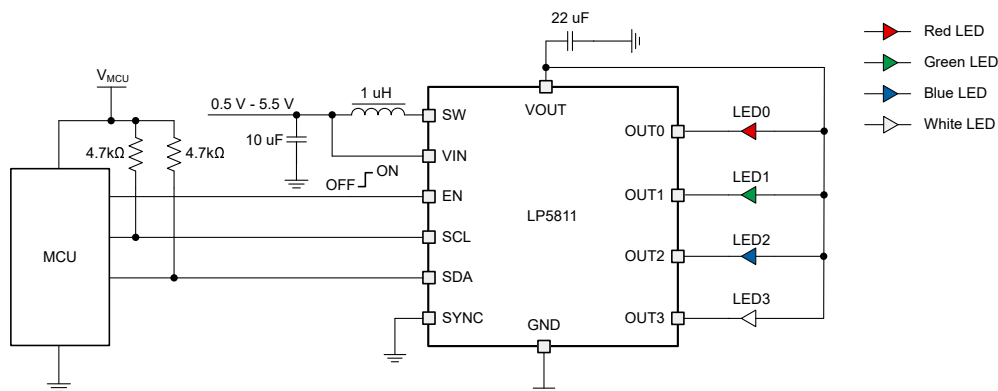


Figure 8-1. Typical Application - LP5811 Driving RGBW LEDs

## 8.2.2 Design Parameters

Design Parameters shows the typical design parameters of [Figure 8-1](#).

**Table 8-1. Design Parameters**

| PARAMETER   | VALUE                                  |
|---|--|
| Input voltage   | 3.6V to 4.2V by one Li-on battery cell |
| Output voltage  | 4.5V                                   |
| Inductor  | 1μH                                    |
| Output capacitor                                      | 22μF                                   |
| LED count   | 4                                      |
| LED maximum average current (red, green, blue, white) | 51mA, 40mA, 40mA, 40mA                 |
| LED PWM frequency                                     | 24kHz                                  |

## 8.2.3 Detailed Design Procedure

This section will showcase the detailed design procedures for LP5811 including boost components selection, LED driver manual and autonomous modes application examples.

### 8.2.3.1 Inductor Selection

The inductor is the most important component in power regulator design, which affects steady-state operation, transient behavior, and loop stability. There are three important inductor specifications, inductor value, saturation current, and dc resistance (DCR).

The integrated boost converter in LP5811 is designed to work with inductor values between 0.37μH and 2.9μH. 1μH is recommended in typical application. The inductor peak current can be calculated by [Equation 8](#). Using the minimum input voltage, maximum output voltage, and maximum load current of the application can calculate the worst case.

In a boost regulator, the inductor dc current can be calculated by [Equation 6](#).

$$\Delta I_{L(DC)} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (6)$$

where

- $V_{OUT}$  is the output voltage of the boost converter
- $I_{OUT}$  is the output current of the boost converter
- $V_{IN}$  is the input voltage of the boost converter
- $\eta$  is the power-conversion efficiency, use 90% for most cases

The inductor ripple current is calculated by [Equation 7](#).

$$\Delta I_{L(P-P)} = \frac{V_{IN} \times D}{L \times f_{SW}} \quad (7)$$

where

- $D$  is the duty cycle, which can be calculated by
- $L$  is the inductance value of the inductor
- $f_{SW}$  is the switching frequency
- $V_{IN}$  is the input voltage of the boost converter

Therefore, the inductor peak current is calculated by [Equation 8](#).

$$\Delta I_{L(P)} = \Delta I_{L(DC)} + \frac{\Delta I_{L(P-P)}}{2} \quad (8)$$

Inductor peak-to-peak current is recommended to be designed less than 40% of the average inductor current, with maximum output current setting. Large inductor value reduces the magnetic hysteresis losses in the inductor and improves EMI performance with small inductor ripple, but the load transient response time increases. The saturation current of the inductor must be higher than the calculated peak inductor current.

### 8.2.3.2 Output Capacitor Selection

The output capacitor is selected to meet the requirements of output ripple and loop stability. The ripple voltage is related to capacitor capacitance and equivalent series resistance (ESR). Assuming a ceramic capacitor with zero ESR, the minimum capacitance for a given ripple voltage can be calculated by [Equation 9](#).

$$C_{OUT} = \frac{I_{OUT} \times D_{MAX}}{f_{SW} \times V_{RIPPLE}} \quad (9)$$

where

- $D_{MAX}$  is the maximum switching duty cycle
- $V_{RIPPLE}$  is the peak-to-peak output ripple voltage
- $I_{OUT}$  is the maximum output current
- $f_{SW}$  is the switching frequency

The ESR impact on the output ripple must be considered if tantalum or aluminum electrolytic capacitors are used. The output peak-to-peak ripple voltage caused by the ESR of the output capacitors can be calculated by [Equation 10](#).

$$V_{RIPPLE(ESR)} = I_{L(P)} \times R_{ESR} \quad (10)$$

The derating of a ceramic capacitor under dc bias voltage, aging, and ac signal need to be considered during design. For example, the dc bias voltage can significantly reduce capacitance. A ceramic capacitor can lose more than 50% of capacitance at the rated voltage. Therefore, enough the voltage rating margin must be left to get adequate capacitance at the required output voltage. Increasing the output capacitor can make the output ripple voltage smaller in PWM mode.

TI recommends using the X5R or X7R ceramic output capacitor in the range of 4μF to 1000μF effective capacitance. 10μF effective capacitance is recommended in typical application, which means around 22μF rated capacitance. If the output capacitor is below the range, the boost regulator can potentially become unstable.

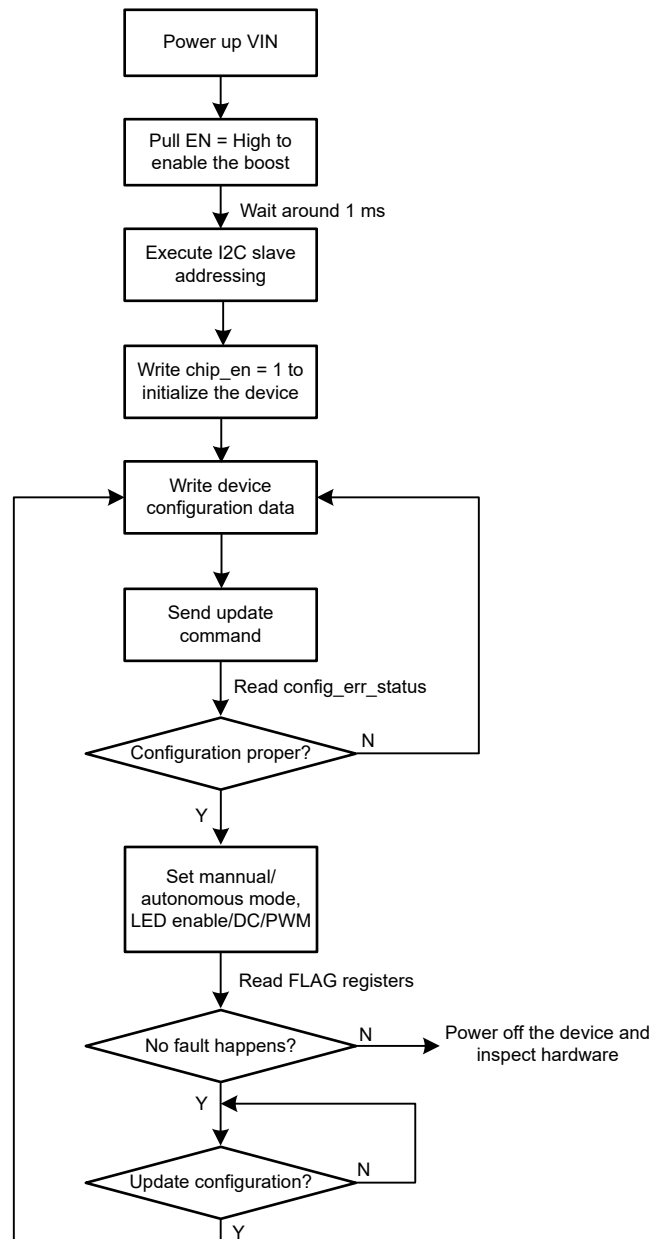
### 8.2.3.3 Input Capacitor Selection

Multilayer X5R or X7R ceramic capacitors are excellent choices for the input decoupling of the integrated boost converter, because of the extremely low ESR and small footprint. Input capacitors must be located as close as possible to the device. While a 10μF input capacitor is sufficient for most applications, large capacitance is used to reduce input current ripple. When the input power is supplied through long wire and only ceramic capacitor is put, the load step at the output induces ringing at the VIN pin. This ringing couples back to the output and influence loop stability or even damage the device. In this circumstance, placing additional bulk capacitance (tantalum or aluminum electrolytic capacitor) between ceramic input capacitor and the power supply can reduce the ringing

#### 8.2.3.4 Program Procedure

After VIN powering up, the boost converter can be enabled by pulling EN to High. After around 1ms for boost output and internal oscillator stable, the device can be initialized by configuring chip\_en = 1 after executing I<sup>2</sup>C slave addressing. Then the CONFIG registers can be set to the expected configuration. After updating the CONFIG registers, one update command must be sent to make the configuration effective. Either manual mode or autonomous mode can be selected for each LED. A new configuration is only effective once update command is received.

The detailed program procedure is illustrated as:



**Figure 8-2. Program Procedure**

#### 8.2.3.5 Programming Example

To get the design parameters in [Section 8.2.2](#), the following program steps can be referred.

After VIN powering up, the boost converter being enabled by pulling EN to High and waiting around 1 ms,

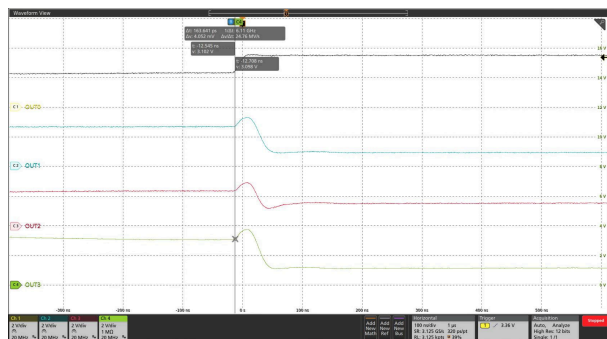
1. Execute I<sup>2</sup>C slave addressing, for details refer to the [sample code](#)
2. Set chip\_en = 1 to enable the device (**Write 01h to register 000h**)
3. Set boost\_vout = Fh to set 4.5V boost output voltage, and max\_current = 1h to set 51mA maximum output LED current. (**Write 1Fh to register 001h**)
4. Set lsd\_threshold = 3h is recommended to avoid incorrect LSD detection. (**Write 0Bh to register 00Dh**)

Leave the PWM frequency, manual or autonomous mode, linear or exponential dimming curve, phase align method, vsync mode, blank time as default. (In other application requirements, these functions can be set)

5. Send update command to complete configuration settings (**Write 55h to register 010h**)
6. Read back config\_err\_status to check if the configuration is proper (**Read register 300h**)
7. Enable all 4 LEDs (**Write 0Fh to register 020h**)
8. Set 51 mA peak current for red LEDs, 40 mA peak current for green, blue and white LEDs (**write FFh to register 30h, write CCh to registers 031h - 033h**)
9. Set 100% duty cycle to illuminate the LEDs (**Write FFh to registers 040h - 043h**)

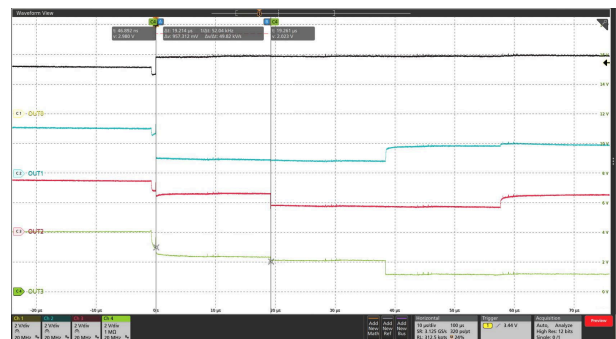
## 8.2.4 Application Performance Plots

The following figures show the application performance plots.



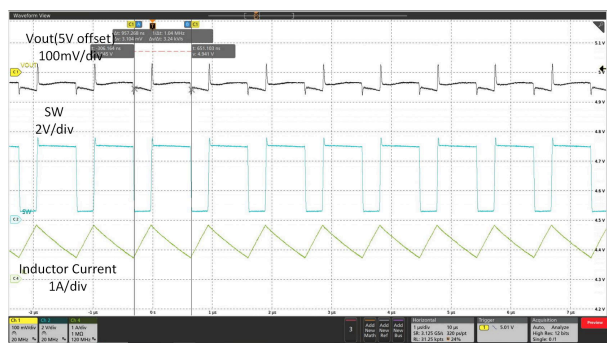
phase\_align\_a0 = 0h, phase\_align\_a1 = 0h, phase\_align\_a2 = 0h, PWM = 127

**Figure 8-3. PWM Alignment Disabled**



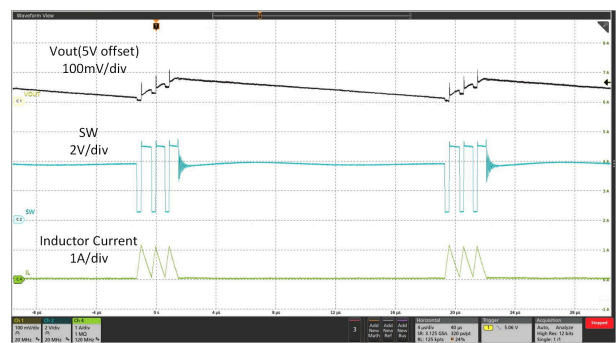
phase\_align\_a0 = 1h, phase\_align\_a1 = 2h, phase\_align\_a2 = 3h, PWM = 127

**Figure 8-4. PWM Alignment Enabled**



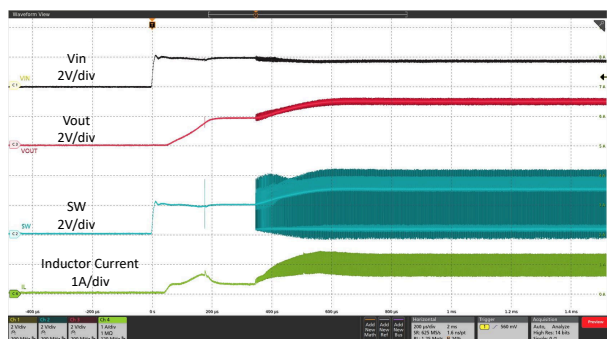
$V_{IN} = 3.6V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 1A$

**Figure 8-5. Switching Waveform at Heavy Load**



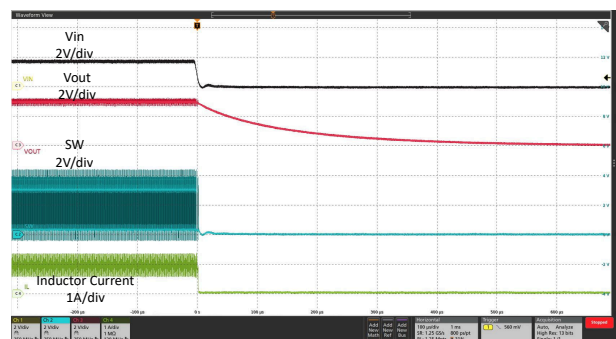
$V_{IN} = 3.6V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 50mA$

**Figure 8-6. Switching Waveform at Light Load**



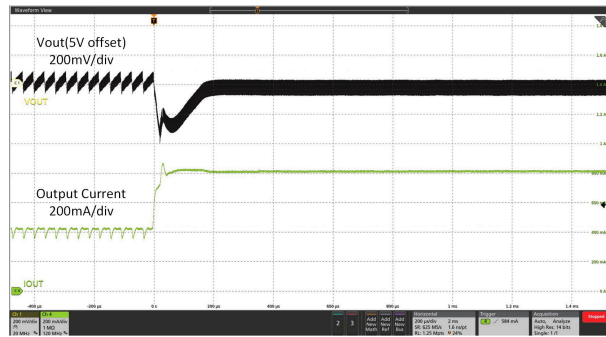
$V_{IN} = 2.0V$ ,  $V_{OUT} = 3.3V$ , 6.6 $\Omega$  resistance load

**Figure 8-7. Start-up Waveform**



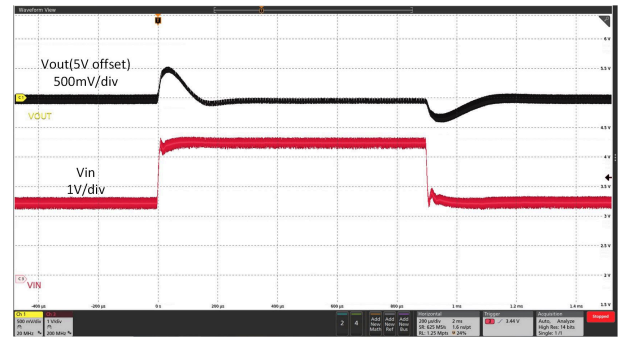
$V_{IN} = 2.0V$ ,  $V_{OUT} = 3.3V$ , 6.6 $\Omega$  resistance load

**Figure 8-8. Shutdown Waveform**



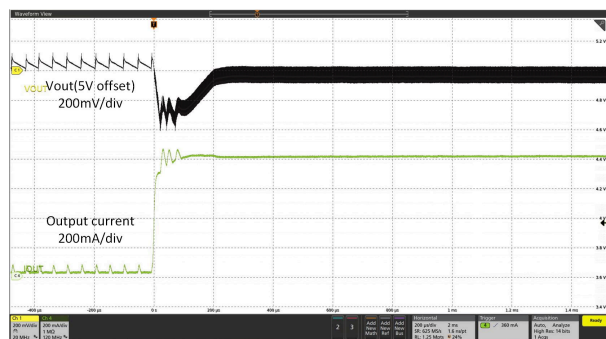
$V_{IN} = 3.6V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 400mA$  to  $800mA$  with  $20\mu s$  slew rate

**Figure 8-9. Load Transient**



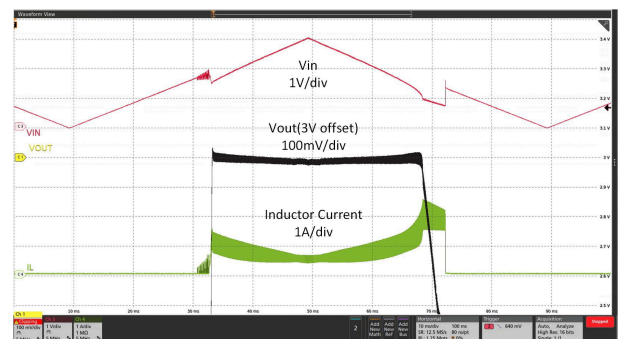
$V_{IN} = 2.5V$  to  $4.6V$  with  $20\mu s$  slew rate,  $V_{OUT} = 5V$   
 $I_{OUT} = 800mA$

**Figure 8-10. Line Transient**



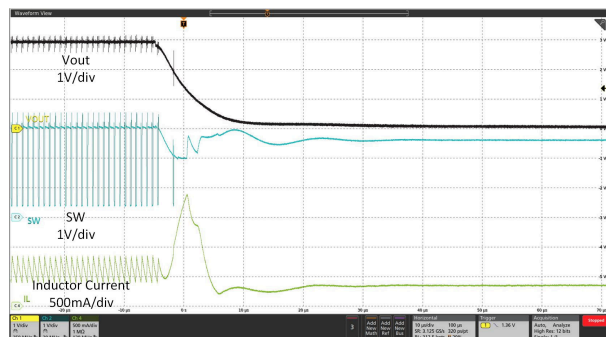
$V_{IN} = 3.6V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 0A$  to  $800mA$  Sweep

**Figure 8-11. Load Sweep**



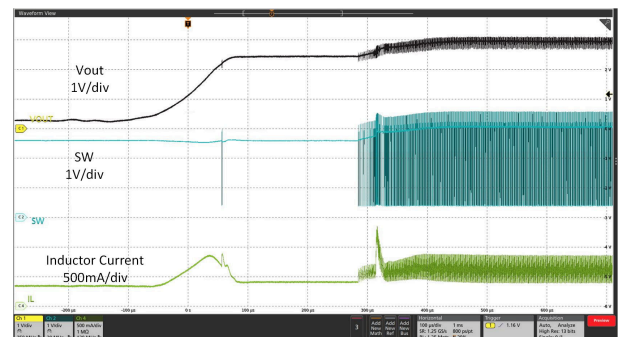
$V_{IN} = 0V$  to  $3V$  Sweep,  $V_{OUT} = 3V$ ,  $6.6\Omega$  resistance load

**Figure 8-12. Line Sweep**



$V_{IN} = 2.5V$ ,  $V_{OUT} = 3V$ ,  $6.6\Omega$  resistance load

**Figure 8-13. Output Short Protection (Entry)**



$V_{IN} = 2.5V$ ,  $V_{OUT} = 3V$ ,  $6.6\Omega$  resistance load

**Figure 8-14. Output Short Protection (Recover)**

## 8.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 0.5V to 5.5V, with minimum 1.8V start up input voltage. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance is required near to the ceramic bypass capacitors. A typical choice is a tantalum or aluminum electrolytic capacitor with a value of 100µF.

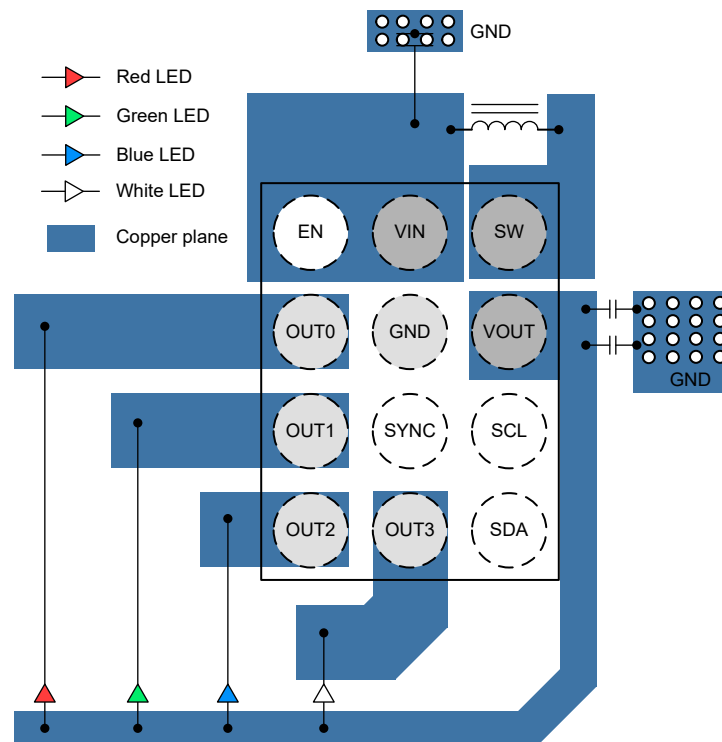
## 8.4 Layout

### 8.4.1 Layout Guidelines

As for all switching power supplies, especially those running at high switching frequency and high currents, layout is an important design step. If the layout is not carefully done, the regulator could suffer from instability and noise problems. To maximize efficiency, switch rise and fall time are very fast. To prevent radiation of high



### 8.4.2 Layout Example



**Figure 8-15. LP5811 DSBGA Package Layout Example**

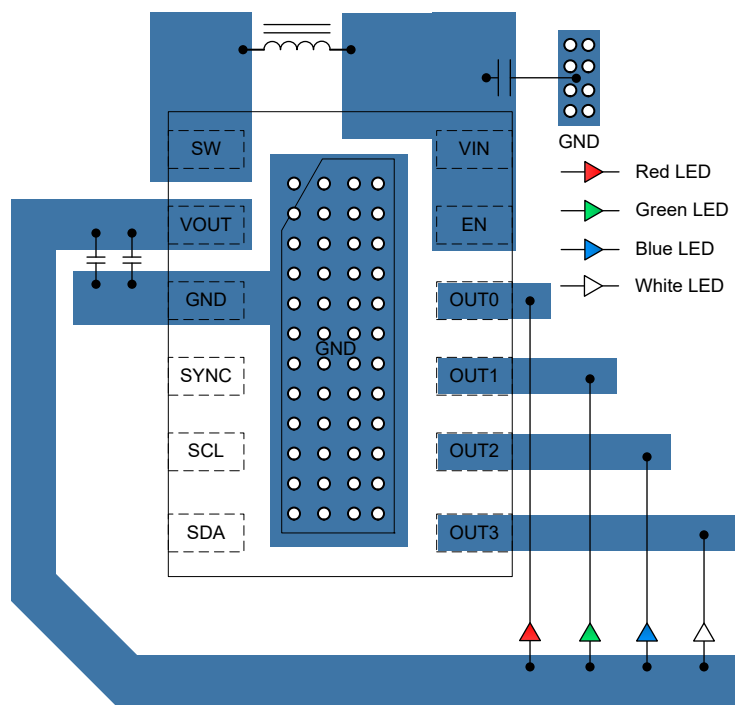


Figure 8-16. LP5811 WSON Package Layout Example

## 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 9.1 Documentation Support

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision B (December 2024) to Revision C (February 2025) Page

- Added URL to Sample Code..... 29

### Changes from Revision A (September 2024) to Revision B (December 2024) Page

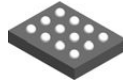
- Added Pin Configuration Section..... 4
- Updated Functional Modes image ..... 21
- Updated parameters in Design Parameters table..... 27
- Removed Recommended Inductors table..... 27
- Changed Program Procedure..... 29
- Changed Program Example..... 29
- Removed Scan Lines and Current Sinks Waveforms of OUT0, OUT1, OUT2, OUT3, removed Scan Lines  
Switching Waveforms of OUT0, OUT1, OUT2, OUT3..... 31
- Added WSON Package Layout Example..... 33

### Changes from Revision \* (October 2023) to Revision A (September 2024) Page

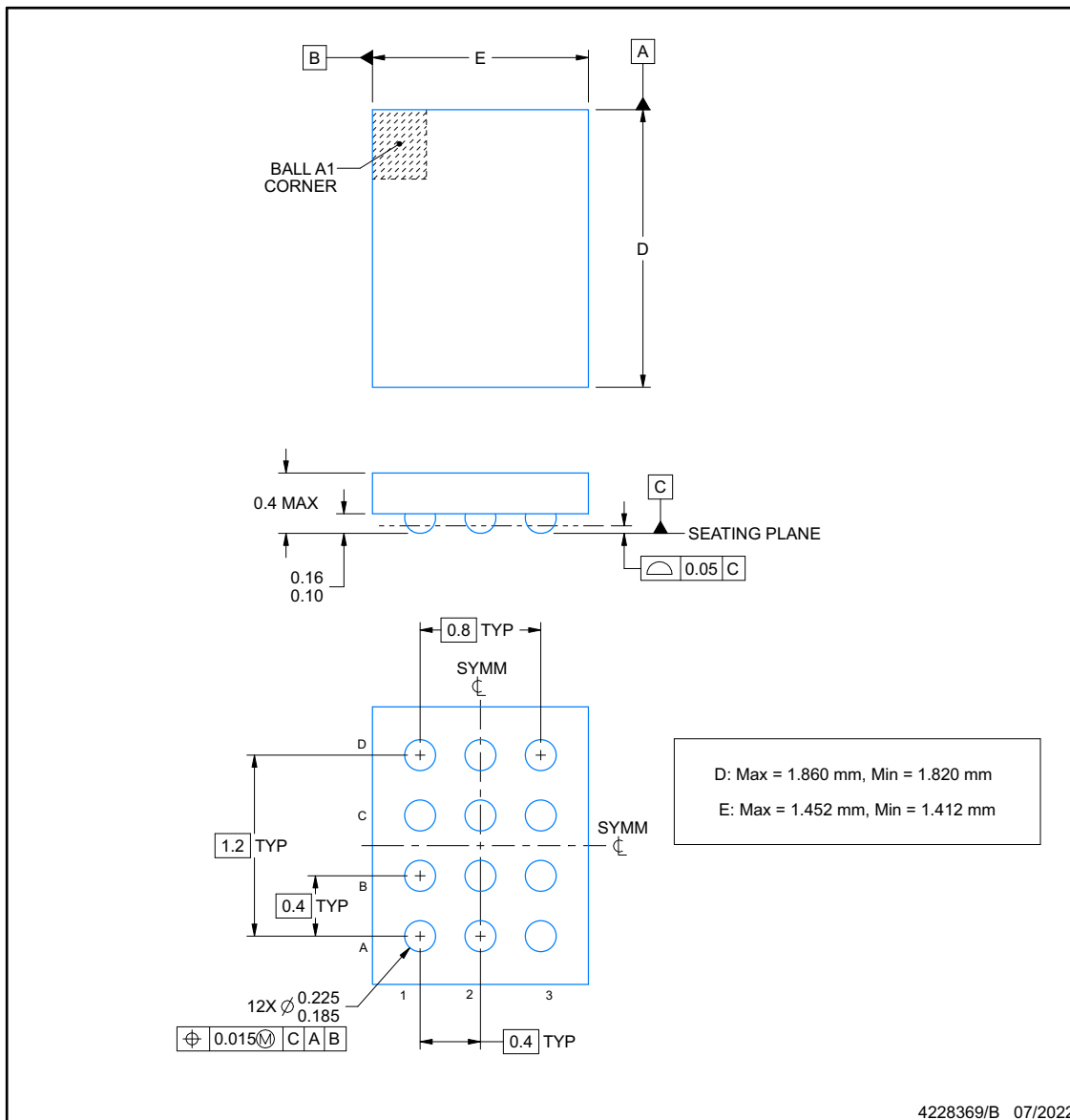
- Added WCSP package..... 1
- Updated Electrical Specifications Table ..... 6
- Added DRR (WSON) Thermal Information..... 6
- Updated Electrical Specifications Table ..... 6
- Added Programming Example..... 29

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**YBH0012-C01****PACKAGE OUTLINE****DSBGA - 0.4 mm max height**

DIE SIZE BALL GRID ARRAY

**NOTES:**

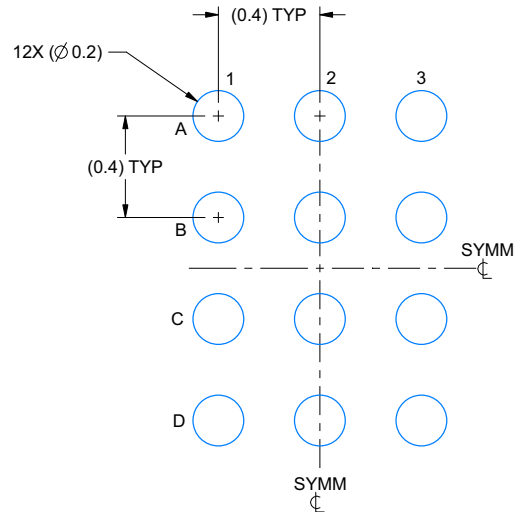
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

## EXAMPLE BOARD LAYOUT

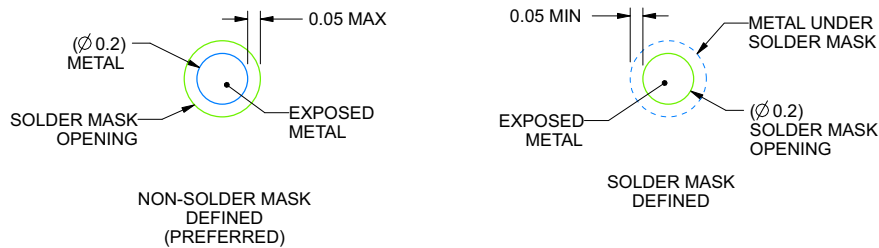
**YBH0012-C01**

**DSBGA - 0.4 mm max height**

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 40X



SOLDER MASK DETAILS  
NOT TO SCALE

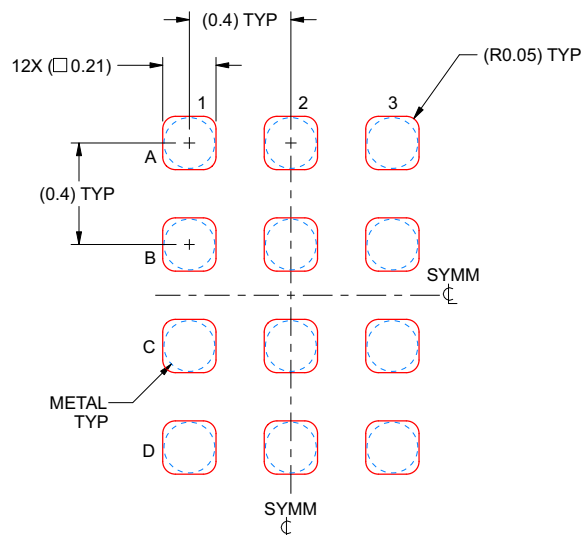
4228369/B 07/2022

NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

**EXAMPLE STENCIL DESIGN****YBH0012-C01****DSBGA - 0.4 mm max height**

DIE SIZE BALL GRID ARRAY



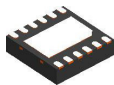
**SOLDER PASTE EXAMPLE**  
 BASED ON 0.075 mm THICK STENCIL  
 SCALE: 40X

4228369/B 07/2022

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



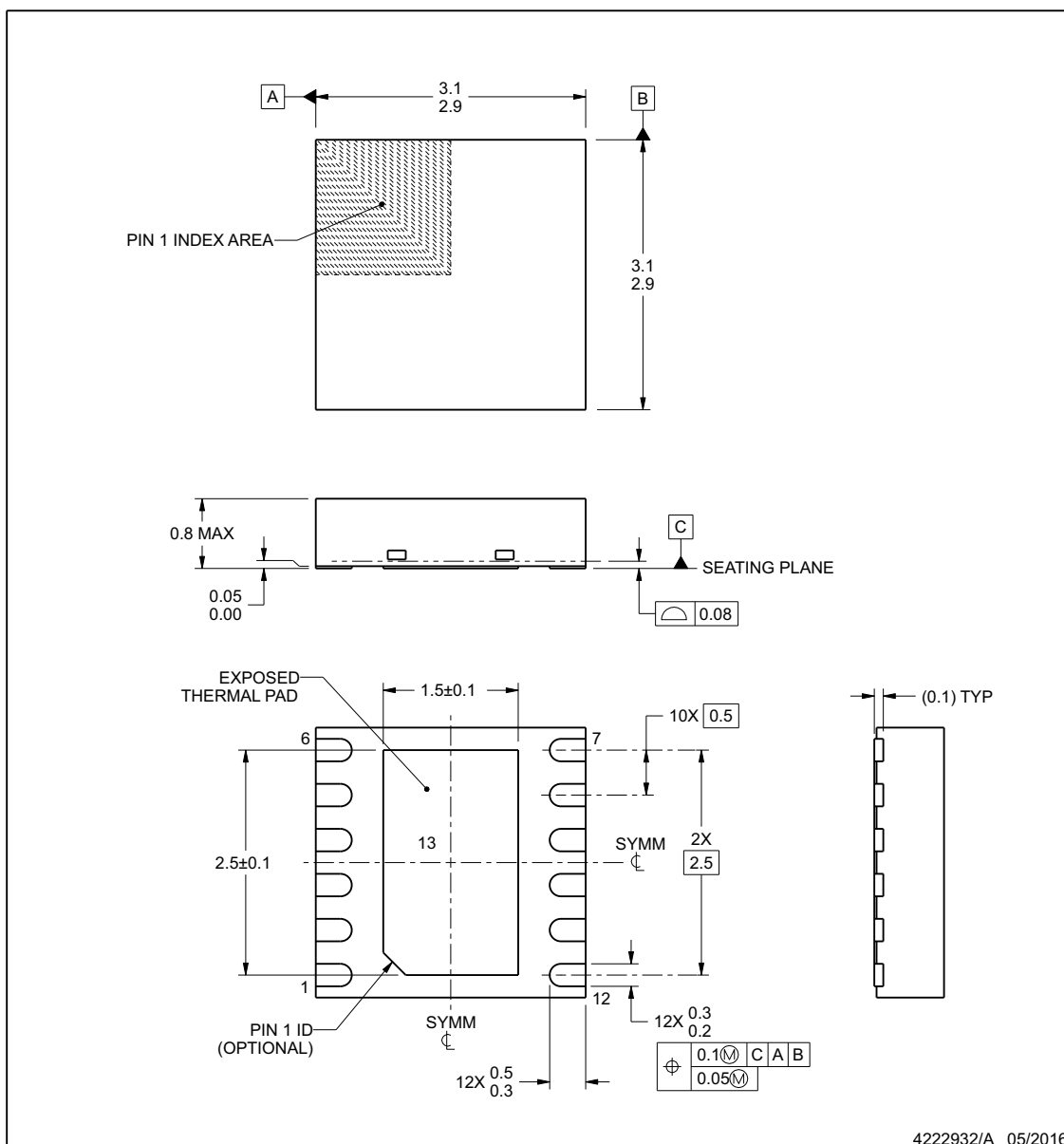


**DRR0012C**

## PACKAGE OUTLINE

**WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



### NOTES:

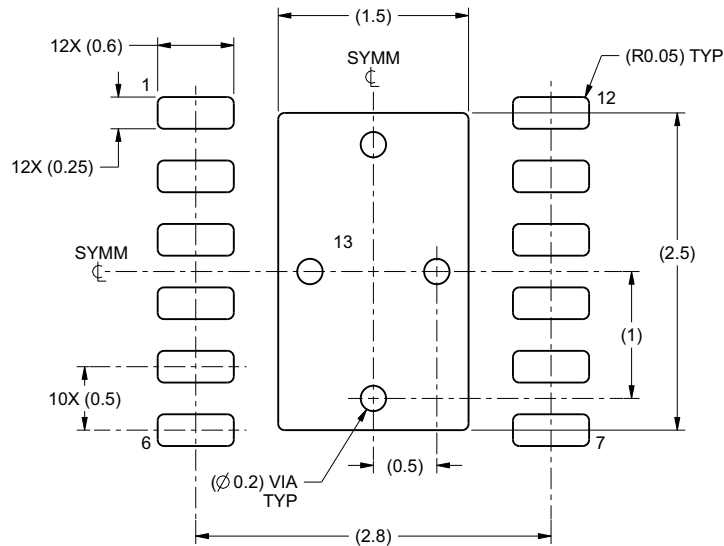
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

## EXAMPLE BOARD LAYOUT

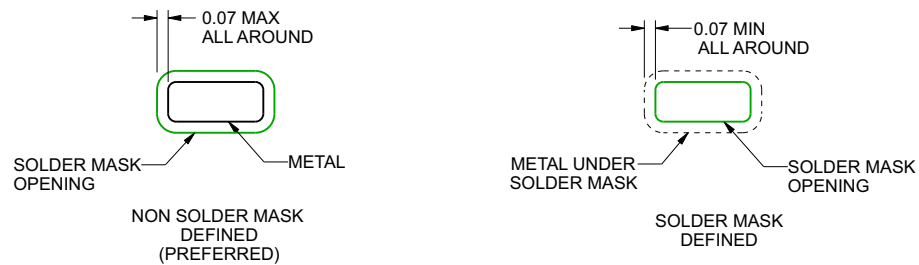
**DRR0012C**

**WSN - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



## SOLDER MASK DETAILS

4222932/A 05/2016

NOTES: (continued)

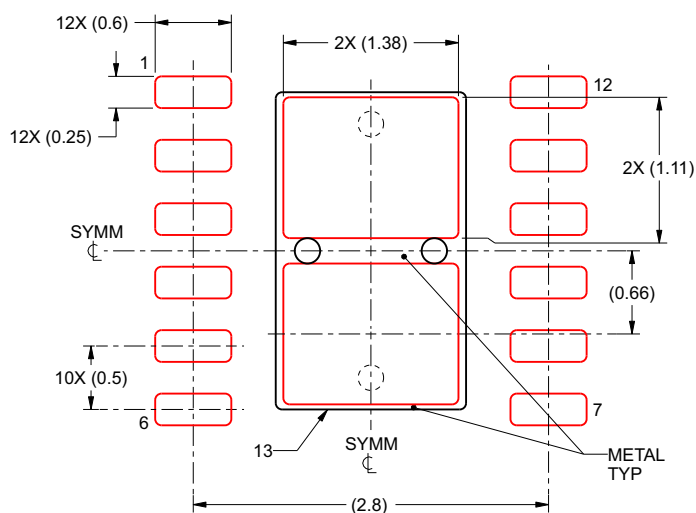
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sl原因271](http://www.ti.com/lit/sl原因271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

## EXAMPLE STENCIL DESIGN

**DRR0012C**

**WSN - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 13  
81.7% PRINTED SOLDER COVERAGE BY AREA  
SCALE:20X

4222932/A 05/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| LP5811ADRRR      | ACTIVE        | WSON         | DRR             | 12   | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | 5811A                   | <a href="#">Samples</a> |
| LP5811AYBHR      | ACTIVE        | DSBGA        | YBH             | 12   | 3000        | RoHS & Green    | SNAGCU                               | Level-1-260C-UNLIM   | -40 to 85    | 5811A                   | <a href="#">Samples</a> |
| LP5811BDRRR      | ACTIVE        | WSON         | DRR             | 12   | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | 5811B                   | <a href="#">Samples</a> |
| LP5811BYBHR      | ACTIVE        | DSBGA        | YBH             | 12   | 3000        | RoHS & Green    | SNAGCU                               | Level-1-260C-UNLIM   | -40 to 85    | 5811B                   | <a href="#">Samples</a> |
| LP5811CDRRR      | ACTIVE        | WSON         | DRR             | 12   | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | 5811C                   | <a href="#">Samples</a> |
| LP5811CYBHR      | ACTIVE        | DSBGA        | YBH             | 12   | 3000        | RoHS & Green    | SNAGCU                               | Level-1-260C-UNLIM   | -40 to 85    | 5811C                   | <a href="#">Samples</a> |
| LP5811DDRRR      | ACTIVE        | WSON         | DRR             | 12   | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | 5811D                   | <a href="#">Samples</a> |
| LP5811DYBHR      | ACTIVE        | DSBGA        | YBH             | 12   | 3000        | RoHS & Green    | SNAGCU                               | Level-1-260C-UNLIM   | -40 to 85    | 5811D                   | <a href="#">Samples</a> |
| LP5813ADRRR      | ACTIVE        | WSON         | DRR             | 12   | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | 5813A                   | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LP5811ADRRR | WSO          | DRR             | 12   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |
| LP5811AYBHR | DSBGA        | YBH             | 12   | 3000 | 180.0              | 8.4                | 1.54    | 2.0     | 0.54    | 4.0     | 8.0    | Q1            |
| LP5811BDRRR | WSO          | DRR             | 12   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |
| LP5811BYBHR | DSBGA        | YBH             | 12   | 3000 | 180.0              | 8.4                | 1.54    | 2.0     | 0.54    | 4.0     | 8.0    | Q1            |
| LP5811CDRRR | WSO          | DRR             | 12   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |
| LP5811CYBHR | DSBGA        | YBH             | 12   | 3000 | 180.0              | 8.4                | 1.54    | 2.0     | 0.54    | 4.0     | 8.0    | Q1            |
| LP5811DDRRR | WSO          | DRR             | 12   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |
| LP5811DYBHR | DSBGA        | YBH             | 12   | 3000 | 180.0              | 8.4                | 1.54    | 2.0     | 0.54    | 4.0     | 8.0    | Q1            |
| LP5813ADRRR | WSO          | DRR             | 12   | 3000 | 330.0              | 12.4               | 3.3     | 3.3     | 1.1     | 8.0     | 12.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LP5811ADRRR | WSN          | DRR             | 12   | 3000 | 367.0       | 367.0      | 35.0        |
| LP5811AYBHR | DSBGA        | YBH             | 12   | 3000 | 182.0       | 182.0      | 20.0        |
| LP5811BDRRR | WSN          | DRR             | 12   | 3000 | 367.0       | 367.0      | 35.0        |
| LP5811BYBHR | DSBGA        | YBH             | 12   | 3000 | 182.0       | 182.0      | 20.0        |
| LP5811CDRRR | WSN          | DRR             | 12   | 3000 | 367.0       | 367.0      | 35.0        |
| LP5811CYBHR | DSBGA        | YBH             | 12   | 3000 | 182.0       | 182.0      | 20.0        |
| LP5811DDRRR | WSN          | DRR             | 12   | 3000 | 367.0       | 367.0      | 35.0        |
| LP5811DYBHR | DSBGA        | YBH             | 12   | 3000 | 182.0       | 182.0      | 20.0        |
| LP5813ADRRR | WSN          | DRR             | 12   | 3000 | 367.0       | 367.0      | 35.0        |

## GENERIC PACKAGE VIEW

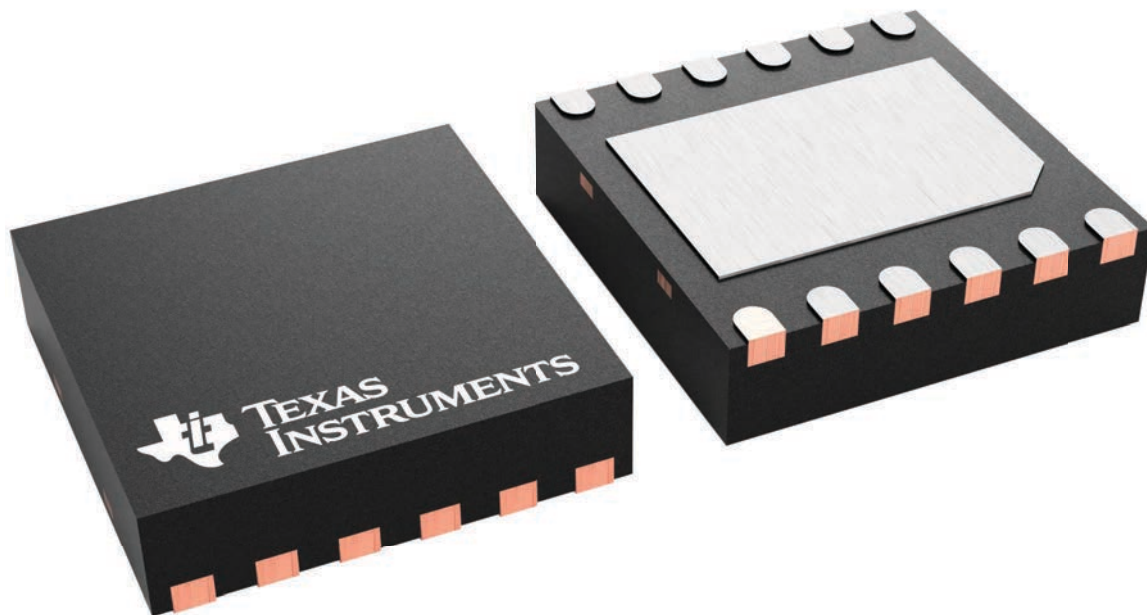
**DRR 12**

**WSON - 0.8 mm max height**

3 x 3, 0.5 mm pitch

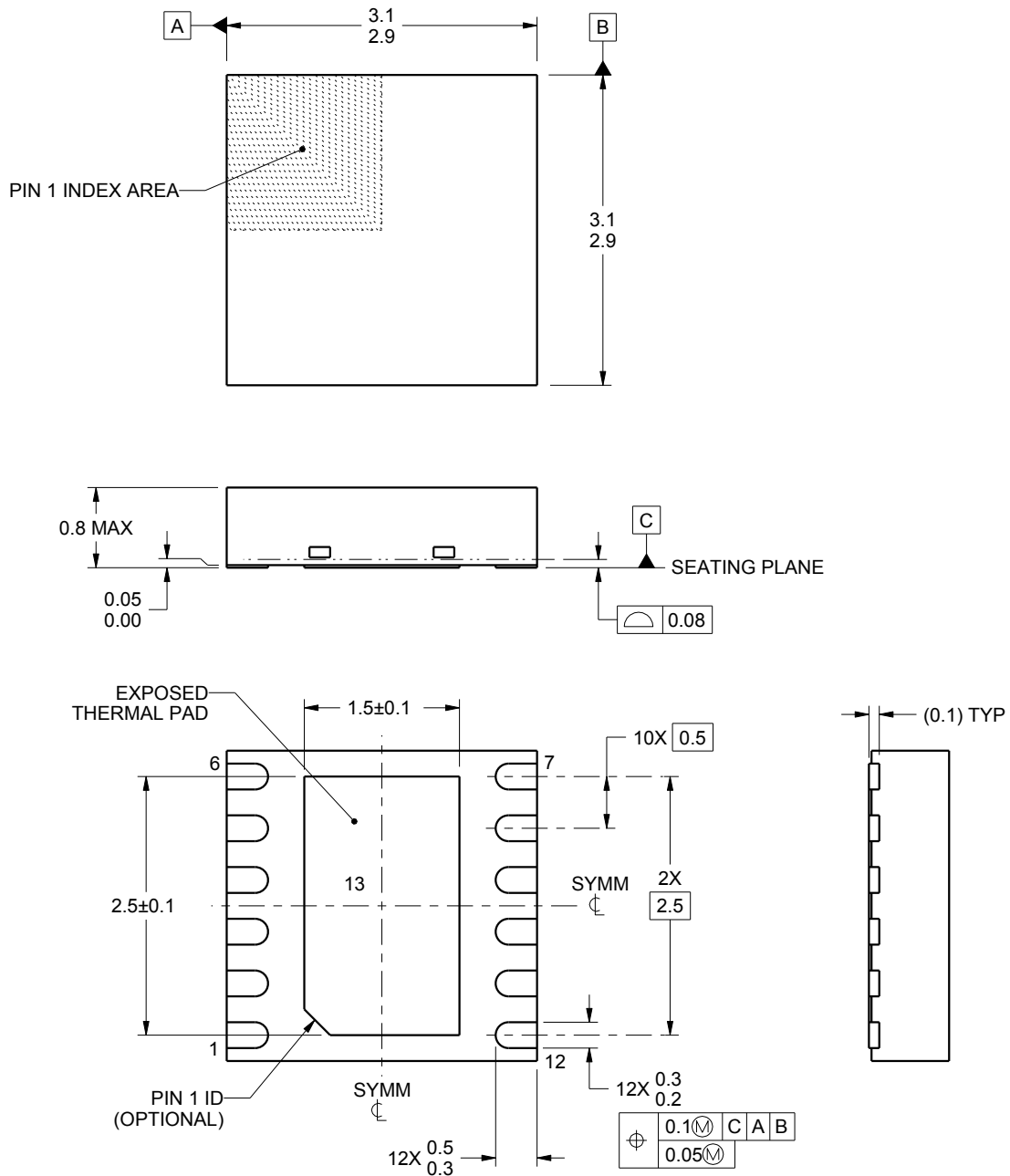
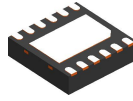
PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4223490/B





4222932/A 05/2016

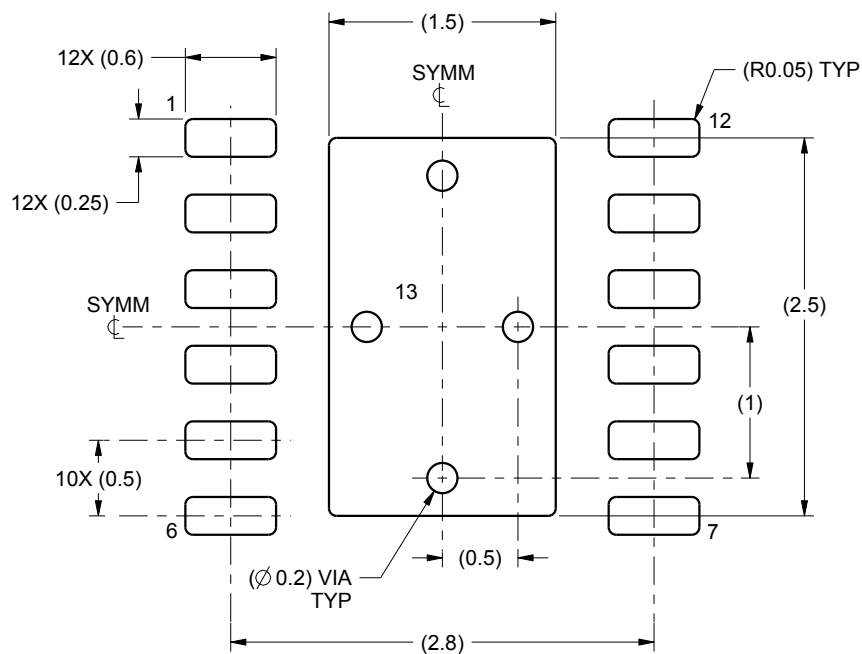
**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

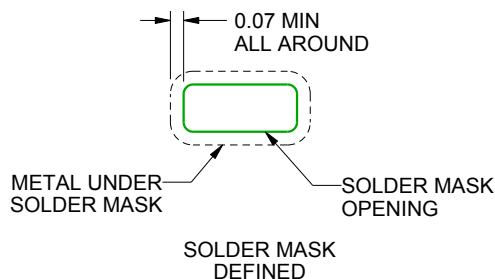
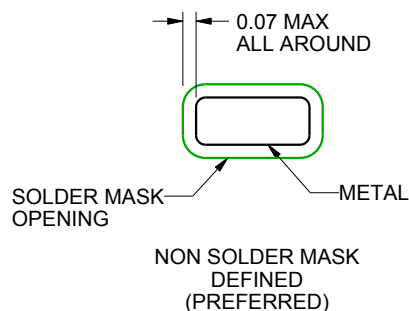
**DRR0012C**

**WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



## SOLDER MASK DETAILS

4222932/A 05/2016

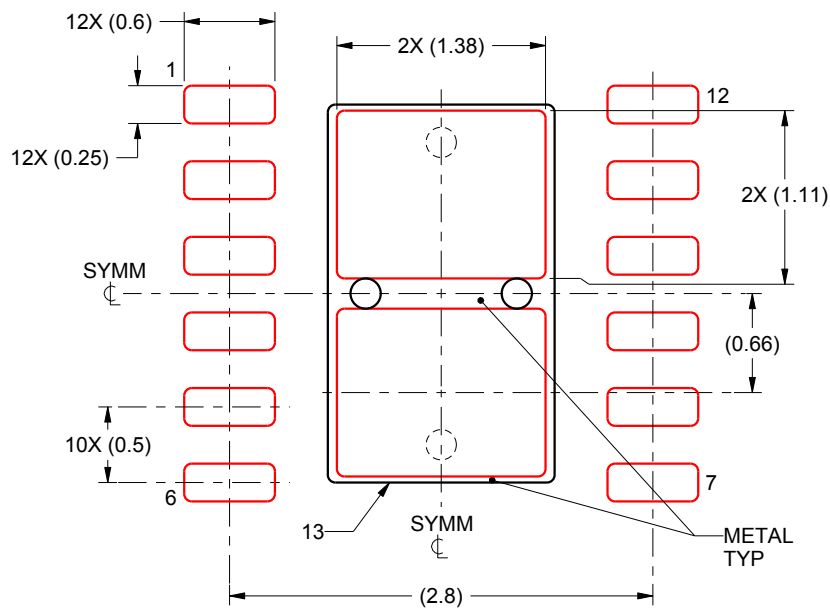
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

**DRR0012C**

**WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



## SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 13  
81.7% PRINTED SOLDER COVERAGE BY AREA  
SCALE:20X

4222932/A 05/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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