LTC2980-24

24-Channel PMBus Power System Manager

FEATURES

- **Sequence, Trim, Margin and Supervise 24 Power Supplies**
- **Manage Faults, Monitor Telemetry and Create Fault Logs**
- **PMBus Compliant Command Set**
- **Supported by LTpowerPlay® GUI**
- **Margin or Trim Supplies to within 0.15% of Target**
- **Fast OV/UV Supervisors Per Channel**
- **Coordinate Sequencing and Fault Management Across Multiple ADI PSM Devices**
- **Automatic Fault Logging to Internal EEPROM**
- **Operate Autonomously without Additional Software**
- Internal Temperature and Input Voltage Supervisors
- Accurate Monitoring of 24 Output Voltages, Three Input Voltages and Internal Die Temperature
- I^2C/SMBus Serial Interface
- Can Be Powered from 3.3V, or 4.5V to 15V
- Programmable Watchdog Timer
- Available in 210-Lead 8.1mm × 16.9mm BGA Package

APPLICATIONS

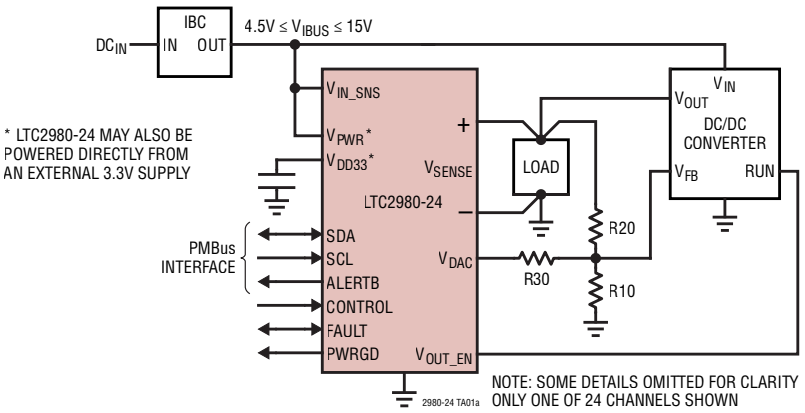
- Computers and Network Servers
- Industrial Test and Measurement
- High Reliability Systems
- Medical Imaging
- Video

DESCRIPTION

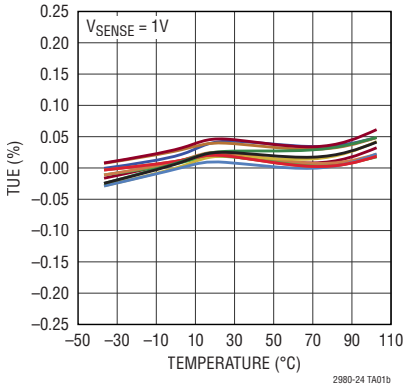
The LTC®2980-24 is a 24-channel Power System Manager used to sequence, trim (servo), margin, supervise, manage faults, provide telemetry and create fault logs. PMBus commands support power supply sequencing, precision point-of-load voltage adjustment and margining. DACs use a proprietary soft-connect algorithm to minimize supply disturbances. Supervisory functions include overvoltage and undervoltage threshold limits for 24 power supply output channels and three power supply input channels, as well as over and under temperature limits. Programmable fault responses can disable the power supplies with optional retry after a fault is detected. Faults that disable a power supply can automatically trigger black box EEPROM storage of fault status and associated telemetry. An internal 16-bit ADC monitors 24 output voltages, three input voltages, and die temperature. In addition, odd numbered channels can be configured to measure the voltage across a current sense resistor. A programmable watchdog timer monitors microprocessor activity for a stalled condition and resets the microprocessor if necessary. A single wire bus synchronizes power supplies across multiple ADI Power System Management (PSM) devices. Configuration EEPROM with ECC supports autonomous operation without additional software.

TYPICAL APPLICATION

24-Channel PMBus Power System Manager



LTC2980-24 Servo Accuracy vs Temp



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ABSOLUTE MAXIMUM RATINGS (Notes 1, 2, 3)

Supply Voltages:
- V_{PWR} ..... –0.3V to 15V
- V_{IN_SNS} ..... –0.3V to 15V
- V_{DD33} ..... –0.3V to 3.6V
- V_{DD25} ..... –0.3V to 2.75V

Digital Input/Output Voltages:
- ALERTB, SDA, SCL, CONTROL0, CONTROL1 ..... –0.3V to 5.5V
- PWRGD, SHARE_CLK, WDI/RESETB, WP ..... –0.3V to V_{DD33} + 0.3V
- FAULTB00, FAULTB01, FAULTB10, FAULTB11 ..... –0.3V to V_{DD33} + 0.3V
- ASEL0, ASEL1 ..... –0.3V to V_{DD33} + 0.3V

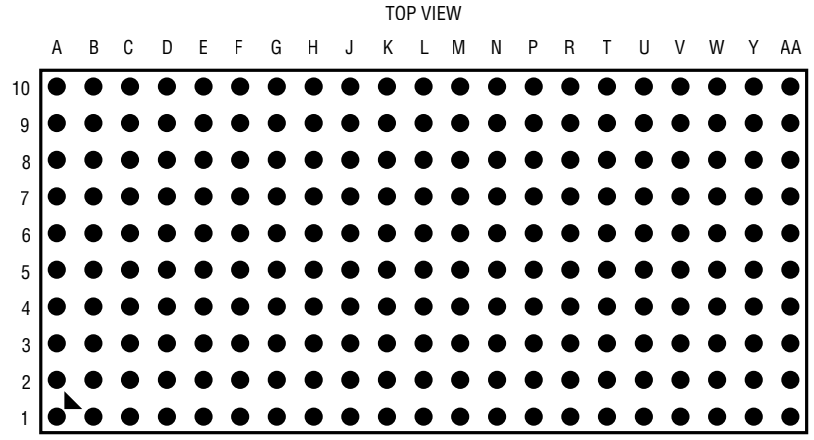
Analog Voltages:
- REFP ..... –0.3V to 1.35V
- REFM ..... –0.3V to 0.3V
- $V_{SENSEP[7:0]}$ ..... –0.3V to 6V
- $V_{SENSEM[7:0]}$ ..... –0.3V to 6V
- $V_{OUT\_EN[3:0]}$, V_{IN_EN} ..... –0.3V to 15V
- $V_{OUT\_EN[7:4]}$ ..... –0.3V to 6V
- $V_{DACP[7:0]}$ ..... –0.3V to 6V
- $V_{DACM[7:0]}$ ..... –0.3V to 0.3V

Operating Junction Temperature Range:
- LTC2980-24A ..... –40°C to 105°C

ABSMAX T_J ..... 125°C
Storage Temperature Range ..... –55°C to 125°C*
Maximum Solder Temperature ..... 260°C

*See Operation section for detailed EEPROM derating information for junction temperatures in excess of 105°C.

PIN CONFIGURATION



BGA PACKAGE
210-LEAD (16.9mm × 8.1mm × 1.52mm)
T_{JMAX} = 125°C, θ_{JA} = 32°C/W, θ_{JCtop} = 11°C/W, $\theta_{JCbottom}$ = 15°C/W, θ_{JB} = 18°C/W,
WEIGHT = 1.6g, VALUES DETERMINED PER JEDEC 51-9, 51-12

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	OPERATING JUNCTION TEMPERATURE RANGE
		DEVICE	FINISH CODE			
LTC2980AY-24#PBF	SAC305 (RoHS)	LTC2980Y-24	e1	BGA	3	–40°C to 105°C

- Contact the factory for parts specified with wider operating temperature ranges. *Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. V_{PWR} = V_{IN_SNS} = 12V, V_{DD33}, V_{DD25} and REF pins floating, unless otherwise indicated. (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Characteristics							
V_{PWR}	V_{PWR} Supply Input Operating Range		●	4.5		15	V
I_{PWR}	V_{PWR} Supply Current	4.5V ≤ V_{PWR} ≤ 15V, V_{DD33} Floating	●		10	13	mA
I_{VDD33}	V_{DD33} Supply Current	3.13V ≤ V_{DD33} ≤ 3.47V, V_{PWR} = V_{DD33}	●		10	13	mA
V_{UVLO_VDD33}	V_{DD33} Undervoltage Lockout	V_{DD33} Ramping Up, V_{PWR} = V_{DD33}	●	2.35	2.55	2.8	V
	V_{DD33} Undervoltage Lockout Hysteresis				120		mV
V_{DD33}	Supply Input Operating Range	V_{PWR} = V_{DD33}	●	3.13		3.47	V
	Regulator Output Voltage	4.5V ≤ V_{PWR} ≤ 15V	●	3.13	3.26	3.47	V
	Regulator Output Short-Circuit Current	V_{PWR} = 4.5V, V_{DD33} = 0V			90		mA
V_{DD25}	Regulator Output Voltage	3.13V ≤ V_{DD33} ≤ 3.47V	●	2.35	2.5	2.6	V
	Regulator Output Short-Circuit Current	V_{PWR} = V_{DD33} = 3.47V, V_{DD25} = 0V			55		mA
t_{INIT}	Initialization Time	Time from V_{IN} Applied Until the TON_DELAY Timer Starts			42		ms
Voltage Reference Characteristics							
V_{REF}	Output Voltage	(Note 4)			1.232		V
	Temperature Coefficient				3		ppm/°C
	Hysteresis	(Note 5)			100		ppm
ADC Characteristics							
V_{IN_ADC}	Voltage Sense Input Range	Differential Voltage: V_{IN_ADC} = ($V_{SENSEPn}$ – $V_{SENSEMn}$)	●	0		6	V
		Single-Ended Voltage: $V_{SENSEMn}$	●	–0.1		0.1	V
	Current Sense Input Range (Odd Numbered Channels Only)	Single-Ended Voltage: $V_{SENSEPn}$, $V_{SENSEMn}$	●	–0.1		6	V
		Differential Voltage: V_{IN_ADC}	●	–170		170	mV
N_ADC	Voltage Sense Resolution (Uses L16 Format)	0V ≤ V_{IN_ADC} ≤ 6V Mfr_config_adc_hires = 0			122		µV/LSB
	Current Sense Resolution (Odd Numbered Channels Only)	0mV ≤ |V_{IN_ADC}| < 16mV (Note 6) 16mV ≤ |V_{IN_ADC}| < 32mV 32mV ≤ |V_{IN_ADC}| < 63.9mV 63.9mV ≤ |V_{IN_ADC}| < 127.9mV 127.9mV ≤ |V_{IN_ADC}| Mfr_config_adc_hires = 1			15.625 31.25 62.5 125 250		µV/LSB µV/LSB µV/LSB µV/LSB µV/LSB
TUE_ADC_VOLT_SNS	Total Unadjusted Error (Note 4)	Voltage Sense Mode V_{IN_ADC} ≥ 1V	●			±0.15	% of Reading
		Voltage Sense Mode 0 ≤ V_{IN_ADC} ≤ 1V	●			±1.5	mV
TUE_ADC_CURR_SNS	Total Unadjusted Error (Note 4)	Current Sense Mode, Odd Numbered Channels Only, 20mV ≤ V_{IN_ADC} ≤ 170mV	●			±0.7	% of Reading
		Current Sense Mode, Odd Numbered Channels Only, V_{IN_ADC} ≤ 20mV	●			±140	µV
V_{OS_ADC}	Offset Error	Current Sense Mode, Odd Numbered Channels Only	●			±100	µV
t_{CONV_ADC}	Conversion Time	Voltage Sense Mode (Note 7)			6.15		ms
		Current Sense Mode (Note 7)			24.6		ms
		Temperature Input (Note 7)			24.6		ms

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{UPDATE_ADC}	Update Time	Odd Numbered Channels in Current Sense Mode (Note 7)			160		ms
C_{IN_ADC}	Input Sampling Capacitance				1		pF
f_{IN_ADC}	Input Sampling Frequency				62.5		kHz
I_{IN_ADC}	Input Leakage Current	V_{IN_ADC} = 0V, 0V ≤ $V_{COMMONMODE}$ ≤ 6V, Current Sense Mode	●			±0.5	µA
	Differential Input Current	V_{IN_ADC} = 0.17V, Current Sense Mode	●		80	250	nA
		V_{IN_ADC} = 6V, Voltage Sense Mode	●		10	15	µA
DAC Output Characteristics							
N_V_{DACP}	Resolution				10		Bits
V_{FS_VDACP}	Full-Scale Output Voltage (Programmable)	DAC Code = 0x3FF, DAC Polarity = 1, Buffer Gain Setting_0	● ●	1.29 2.48	1.38 2.65	1.46 2.80	V V
INL_V_{DACP}	Integral Nonlinearity	(Note 8)				±2	LSB
DNL_V_{DACP}	Differential Nonlinearity	(Note 8)	●			±2.4	LSB
V_{OS_VDACP}	Offset Voltage	(Note 8)	●			±10	mV
V_{DACP}	Load Regulation (V_{DACPn} – V_{DACMn})	V_{DACPn} = 2.65V, I_{VDACPn} Sourcing = 2mA			100		ppm/mA
		V_{DACPn} = 0.1V, I_{VDACPn} Sinking = 2mA			100		ppm/mA
	PSRR (V_{DACPn} – V_{DACMn})	DC: 3.13V ≤ V_{DD33} ≤ 3.47V, V_{PWR} = V_{DD33}			60		dB
		100mV Step in 20ns with 50pF Load			40		dB
	DC CMRR (V_{DACPn} – V_{DACMn})	–0.1V ≤ V_{DACMn} ≤ 0.1V			60		dB
	Leakage Current	V_{DACPn} Hi-Z, 0V ≤ V_{DACPn} ≤ 6V	●			±100	nA
	Short-Circuit Current Low	V_{DACPn} Shorted to GND	●	–10		–4	mA
	Short-Circuit Current High	V_{DACPn} Shorted to V_{DD33}	●	4		10	mA
C_{OUT}	Output Capacitance	V_{DACPn} Hi-Z			10		pF
t_{S_VDACP}	DAC Output Update Rate	Fast Servo Mode			500		µs
DAC Soft-Connect Comparator Characteristics							
V_{OS_CMP}	Offset Voltage	V_{DACPn} = 0.2V	●		±1	±18	mV
		V_{DACPn} = 1.3V	●		±2	±26	mV
		V_{DACPn} = 2.65V	●		±3	±52	mV
Voltage Supervisor Characteristics							
V_{IN_VS}	Input Voltage Range (Programmable)	V_{IN_VS} = ($V_{SENSEPn}$ – $V_{SENSEMn}$), Low Resolution Mode	●	0		6	V
		V_{IN_VS} = ($V_{SENSEPn}$ – $V_{SENSEMn}$), High Resolution Mode	●	0		3.8	V
		Single-Ended Voltage: $V_{SENSEMn}$	●	–0.1		0.1	V
N_VS	Voltage Sensing Resolution	0V to 3.8V Range: High Resolution Mode			4		mV/LSB
		0V to 6V Range: Low Resolution Mode			8		mV/LSB
TUE_VS	Total Unadjusted Error	2V ≤ V_{IN_VS} ≤ 6V, Low Resolution Mode	●			±1.25	% of Reading
		1.5V < V_{IN_VS} ≤ 3.8V, High Resolution Mode	●			±1.0	% of Reading
		0.8V ≤ V_{IN_VS} ≤ 1.5V, High Resolution Mode	●			±1.5	% of Reading
t_{S_VS}	Update Period				12.21		µs

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN_SNS} Input Characteristics							
V_{VIN_SNS}	V_{IN_SNS} Input Voltage Range		●	0		15	V
R_{VIN_SNS}	V_{IN_SNS} Input Resistance		●	70	90	110	kΩ
TUE_{VIN_SNS}	VIN_ON, VIN_OFF Threshold Total Unadjusted Error	3V ≤ V_{VIN_SNS} ≤ 8V	●			±2.0	% of Reading
		V_{VIN_SNS} > 8V	●			±1.0	% of Reading
	READ_VIN Total Unadjusted Error	3V ≤ V_{VIN_SNS} ≤ 8V	●			±1.5	% of Reading
		V_{VIN_SNS} > 8V	●			±1.0	% of Reading
Temperature Sensor Characteristics							
TUE_TS	Total Unadjusted Error				±1		°C
V_{OUT} Enable Output (V_{OUT_EN} [3:0]) Characteristics							
V_{VOUT_ENn}	Output High Voltage (Note 9)	I_{VOUT_ENn} = –5µA, V_{DD33} = 3.3V	●	10	12.5	14.7	V
I_{VOUT_ENn}	Output Sourcing Current	V_{VOUT_ENn} Pull-Up Enabled, V_{VOUT_ENn} = 1V	●	–5	–6	–8	µA
	Output Sinking Current	Strong Pull-Down Enabled, V_{VOUT_ENn} = 0.4V	●	3	5	8	mA
		Weak Pull-Down Enabled, V_{VOUT_ENn} = 0.4V	●	28	43	60	µA
	Output Leakage Current	Internal Pull-Up Disabled, 0V ≤ V_{VOUT_ENn} ≤ 15V	●			±1	µA
V_{OUT} Enable Output (V_{OUT_EN} [7:4]) Characteristics							
I_{VOUT_ENn}	Output Sinking Current	Strong Pull-Down Enabled, V_{OUT_ENn} = 0.1V			6		mA
	Output Leakage Current	0V ≤ V_{VOUT_ENn} ≤ 6V	●			±2	µA
V_{IN} Enable Output (V_{IN_EN}) Characteristics							
V_{VIN_EN}	Output High Voltage	I_{VIN_EN} = –5µA, V_{DD33} = 3.3V	●	10	12.5	14.7	V
I_{VIN_EN}	Output Sourcing Current	V_{IN_EN} Pull-Up Enabled, V_{VIN_EN} = 1V	●	–5	–6	–8	µA
	Output Sinking Current	V_{VIN_EN} = 0.4V	●	3	5	8	mA
	Leakage Current	Internal Pull-Up Disabled, 0V ≤ V_{VIN_EN} ≤ 15V	●			±2	µA
EEPROM Characteristics							
Endurance	(Notes 10, 11)	0°C < T_J < 85°C During EEPROM Write Operations	●	10,000			Cycles
Retention	(Notes 10, 11)	T_J < 105°C	●	20			Years
t_{MASS_WRITE}	Mass Write Operation Time (Note 12)	STORE_USER_ALL, 0°C < T_J < 85°C During EEPROM Write Operations	●		440	4100	ms
Digital Inputs SCL, SDA, CONTROL0, CONTROL1, WDI/RESETB, FAULTB00, FAULTB01, FAULTB10, FAULTB11, WP							
V_{IH}	High Level Input Voltage		●	2.1			V
V_{IL}	Low Level Input Voltage		●			1.5	V
V_{HYST}	Input Hysteresis				20		mV
I_{LEAK}	Input Leakage Current	0V ≤ V_{PIN} ≤ 5.5V, SDA, SCL, CONTROL*n* Pins Only	●			±2	µA
		0V ≤ V_{PIN} ≤ V_{DD33} + 0.3V, FAULTB*zn*, WDI/RESETB, WP Pins Only	●			±2	µA

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{SP}	Pulse Width of Spike Suppressed	FAULTB*zn*, CONTROL*n* Pins Only			10		µs
		SDA, SCL Pins Only			98		ns
t_{FAULT_MIN}	Minimum Low Pulse Width for Externally Generated Faults			110			ms
t_{RESETB}	Pulse Width to Assert Reset	$V_{WDI/RESETB} \leq 1.5V$	●	300			µs
t_{WDI}	Pulse Width to Reset Watchdog Timer	$V_{WDI/RESETB} \leq 1.5V$	●	0.3		200	µs
f_{WDI}	Watchdog Interrupt Input Frequency		●			1	MHz
C_{IN}	Digital Input Capacitance				10		pF
Digital Input SHARE_CLK							
V_{IH}	High Level Input Voltage		●	1.6			V
V_{IL}	Low Level Input Voltage		●			0.8	V
$f_{SHARE\_CLK\_IN}$	Input Frequency Operating Range		●	90		110	kHz
t_{LOW}	Assertion Low Time	$V_{SHARE\_CLK} < 0.8V$	●	0.825		1.1	µs
t_{RISE}	Rise Time	$V_{SHARE\_CLK} < 0.8V$ to $V_{SHARE\_CLK} > 1.6V$	●			450	ns
I_{LEAK}	Input Leakage Current	$0V \leq V_{SHARE\_CLK} \leq V_{DD33} + 0.3V$	●			±1	µA
C_{IN}	Input Capacitance				10		pF
Digital Outputs SDA, ALERTB, PWRGD, SHARE_CLK, FAULTB00, FAULTB01, FAULTB10, FAULTB11							
V_{OL}	Digital Output Low Voltage	I_{SINK} = 3mA	●			0.4	V
$f_{SHARE\_CLK\_OUT}$	Output Frequency Operating Range	5.49kΩ Pull-Up to V_{DD33}	●	90	100	110	kHz
Digital Inputs ASEL0,ASEL1							
V_{IH}	Input High Threshold Voltage		●	$V_{DD33} - 0.5$			V
V_{IL}	Input Low Threshold Voltage		●			0.5	V
I_{IH}, I_{IL}	High, Low Input Current	ASEL[1:0] = 0, V_{DD33}	●			±95	µA
I_{HIZ}	Hi-Z Input Current		●			±24	µA
C_{IN}	Input Capacitance				10		pF
Serial Bus Timing Characteristics							
f_{SCL}	Serial Clock Frequency (Note 13)		●	10		400	kHz
t_{LOW}	Serial Clock Low Period (Note 13)		●	1.3			µs
t_{HIGH}	Serial Clock High Period (Note 13)		●	0.6			µs
t_{BUF}	Bus Free Time Between Stop and Start (Note 13)		●	1.3			µs
$t_{HD,STA}$	Start Condition Hold Time (Note 13)		●	600			ns
$t_{SU,STA}$	Start Condition Setup Time (Note 13)		●	600			ns
$t_{SU,STO}$	Stop Condition Setup Time (Note 13)		●	600			ns
$t_{HD,DAT}$	Data Hold Time (LTC2980-24 Receiving Data) (Note 13)		●	0			ns
	Data Hold Time (LTC2980-24 Transmitting Data) (Note 13)		●	300		900	ns
$t_{SU,DAT}$	Data Setup Time (Note 13)		●	100			ns
t_{SP}	Pulse Width of Spike Suppressed (Note 13)				98		ns

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{TIMEOUT\_BUS}$	Time Allowed to Complete any PMBus Command After Which Time SDA Will Be Released and Command Terminated	Mfr_config_all_longer_pmbus_timeout = 0 Mfr_config_all_longer_pmbus_timeout = 1	● ●		25 200	35 280	ms ms
Additional Digital Timing Characteristics							
t_{OFF_MIN}	Minimum Off Time for Any Channel				100		ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive. All currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified. If power is supplied to the chip via the V_{DD33} pin only, connect V_{PWR} and V_{DD33} pins together.

Note 3: The LTC2980-24 electrical characteristics apply to all three LTC2977 sections within the LTC2980-24 device, unless otherwise noted. The specifications and functions are the same for Device A pins, Device B pins and Device C pins.

Note 4: The ADC total unadjusted error includes all error sources. First, a two-point analog trim is performed to achieve a flat reference voltage (V_{REF}) over temperature. This results in minimal temperature coefficient, but the absolute voltage can still vary. To compensate for this, a high-resolution, drift-free, and noiseless digital trim is applied at the output of the ADC, resulting in a very high accuracy measurement.

Note 5: Hysteresis in the output voltage is created by package stress that differs depending on whether the module was previously at a higher or lower temperature. Output voltage is always measured at 25°C, but the module is cycled to 105°C or –40°C before successive measurements. Hysteresis is roughly proportional to the square of the temperature change.

Note 6: The current sense resolution is determined by the L11 format and the mV units of the returned value. For example a full scale value of 170mV returns a L11 value of 0xF2A8 = 680 • 2^{-2} = 170. This is the lowest range that can represent this value without overflowing the L11 mantissa and the resolution for 1LSB in this range is 2^{-2} mV = 250µV. Each successively lower range improves resolution by cutting the LSB size in half.

Note 7: The time between successive ADC conversions (latency of the ADC) for any given channel is given as: 36.9ms + (6.15ms • number of ADC channels configured in Low Resolution mode) + (24.6ms • number of ADC channels configured in High Resolution mode).

Note 8: Nonlinearity is defined from the first code that is greater than or equal to the maximum offset specification to full-scale code, 1023.

Note 9: Output enable pins are charge pumped from V_{DD33}.

Note 10: EEPROM endurance and retention are guaranteed by design, characterization and correlation with statistical process controls. The minimum retention specification applies for devices whose EEPROM has been cycled less than the minimum endurance specification.

Note 11: EEPROM endurance and retention will be degraded when T_J > 105°C.

Note 12: The LTC2980-24 will not acknowledge any PMBus commands while a mass write operation is being executed. This includes the STORE_USER_ALL and MFR_FAULT_LOG_STORE commands or a fault log store initiated by a channel faulting off.

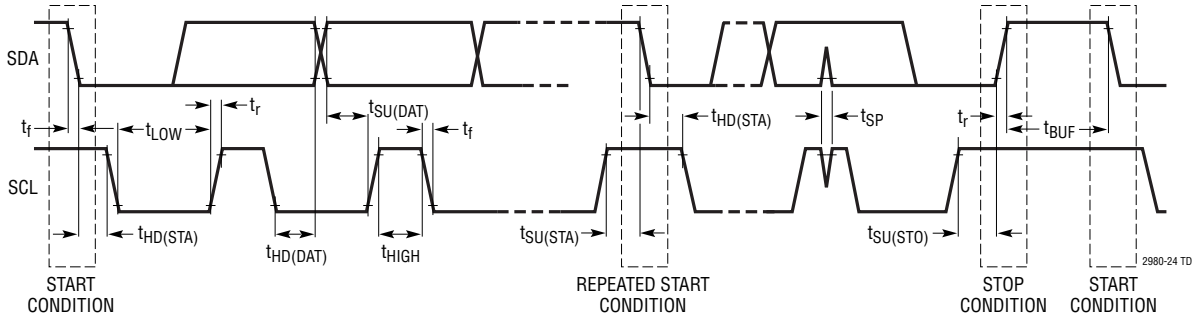
Note 13: Maximum capacitive load, C_B, for SCL and SDA is 400pF. Data and clock rise time (t_r) and fall time (t_f) are:

$(20 + 0.1 \cdot C_B)$ (ns) < t_r < 300ns and $(20 + 0.1 \cdot C_B)$ (ns) < t_f < 300ns.

C_B = capacitance of one bus line in pF. SCL and SDA external pull-up voltage, V_{IO}, is 3.13V < V_{IO} < 5.5V.

Note 14: The LTC2980-24 is specified over the –40°C to 105°C operating junction temperature range. High Junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 105°C. Note the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

PMBUS TIMING DIAGRAM



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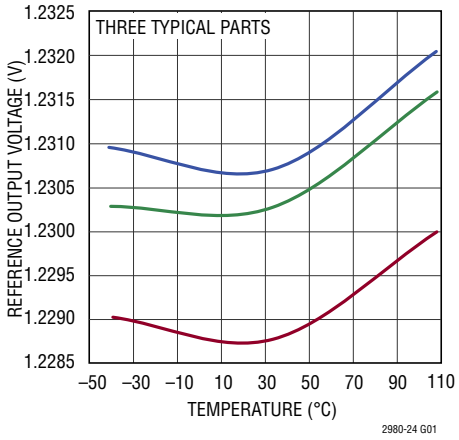
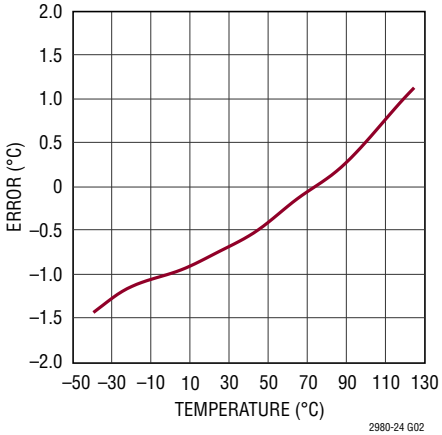
TYPICAL PERFORMANCE CHARACTERISTICS

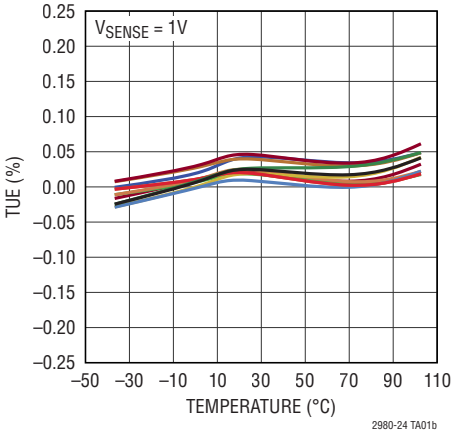
Reference Voltage vs Temperature



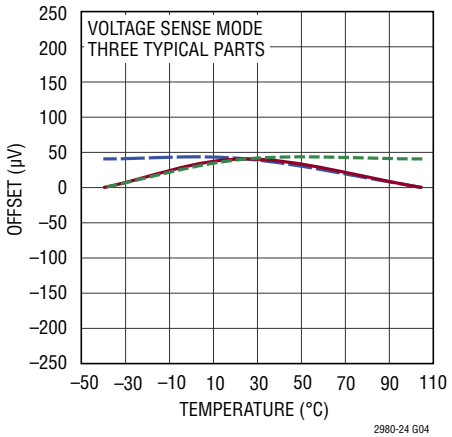
Temperature Sensor Error vs Temperature



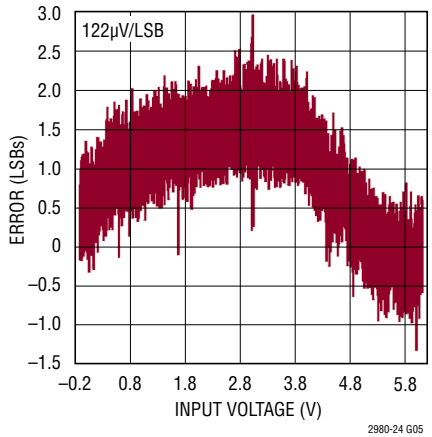
ADC Total Unadjusted Error vs Temperature



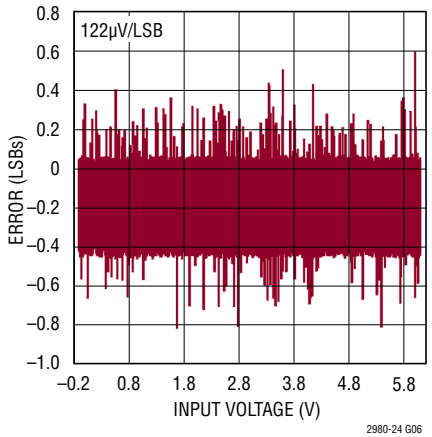
ADC Zero Code Center Offset Voltage vs Temperature



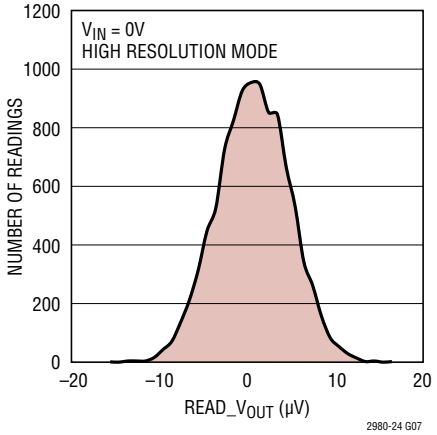
ADC INL



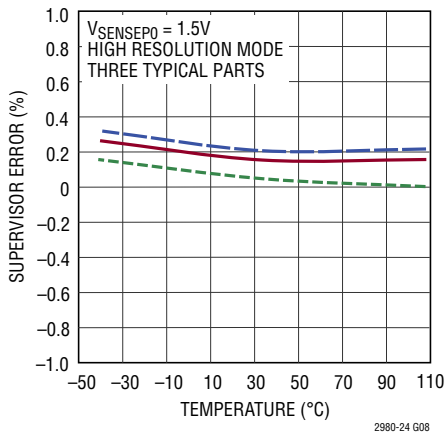
ADC DNL



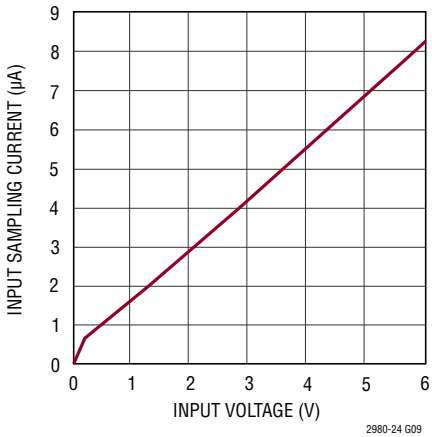
ADC Noise Histogram



Voltage Supervisor Total Unadjusted Error vs Temperature

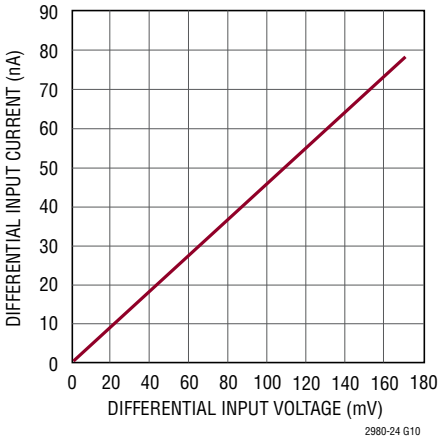


Input Sampling Current vs Differential Input Voltage

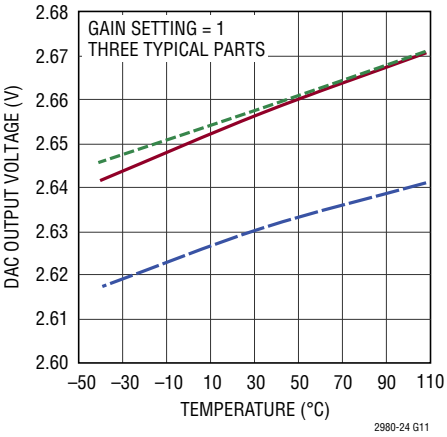


TYPICAL PERFORMANCE CHARACTERISTICS

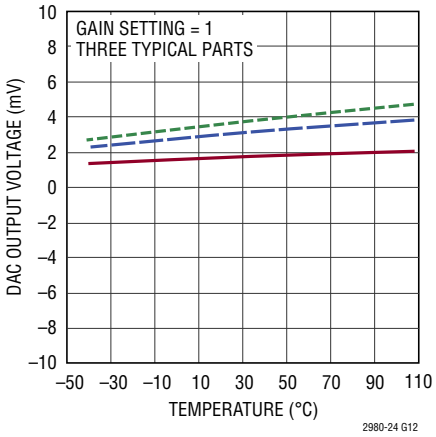
ADC High Resolution Mode Differential Input Current



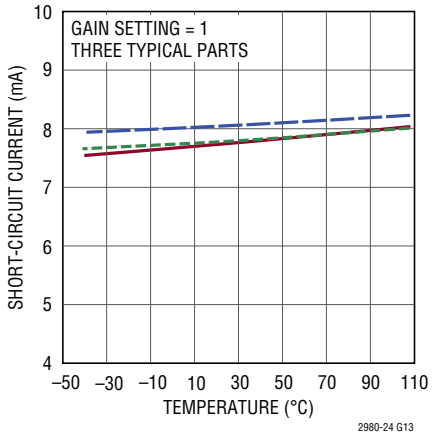
DAC Full-Scale Output Voltage vs Temperature



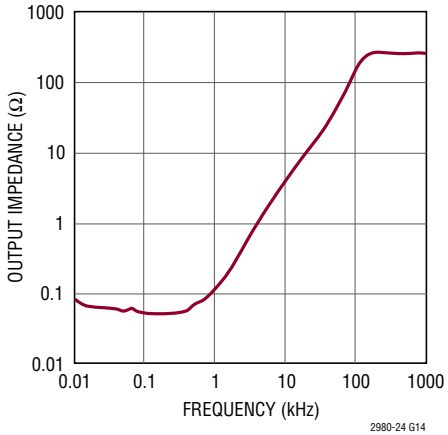
DAC Offset Voltage vs Temperature



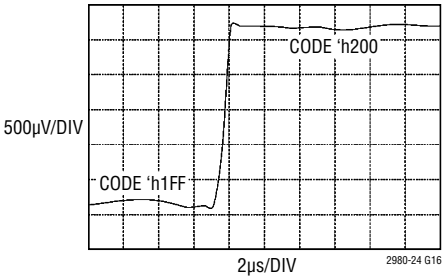
DAC Short-Circuit Current vs Temperature



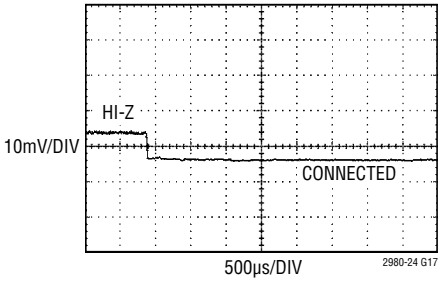
DAC Output Impedance vs Frequency



DAC Transient Response to 1LSB DAC Code Change

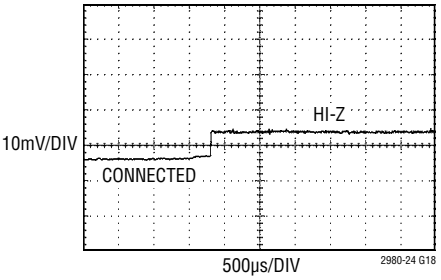


DAC Soft-Connect Transient Response When Transitioning from Hi-Z State to ON State



100k SERIES RESISTANCE ON
CODE: 'h1FF

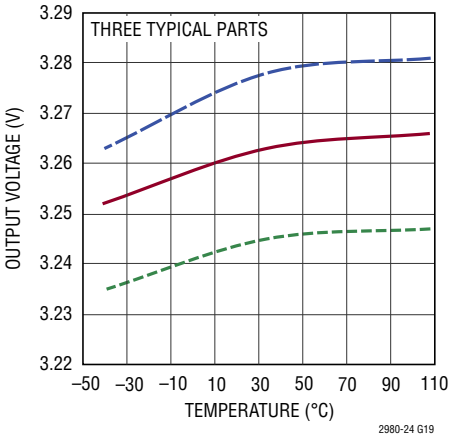
DAC Soft-Connect Transient Response When Transitioning from ON State to Hi-Z State



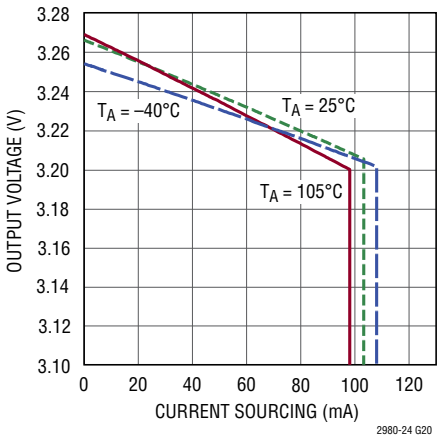
100k SERIES RESISTANCE ON
CODE: 'h1FF

TYPICAL PERFORMANCE CHARACTERISTICS

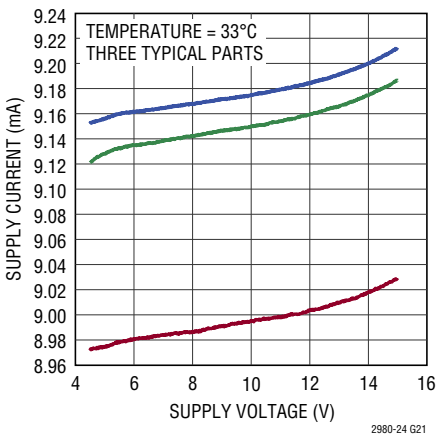
V_{DD33} Regulator Output Voltage vs Temperature



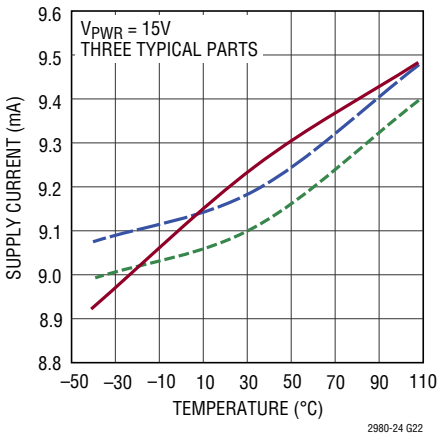
V_{DD33} Regulator Load Regulation



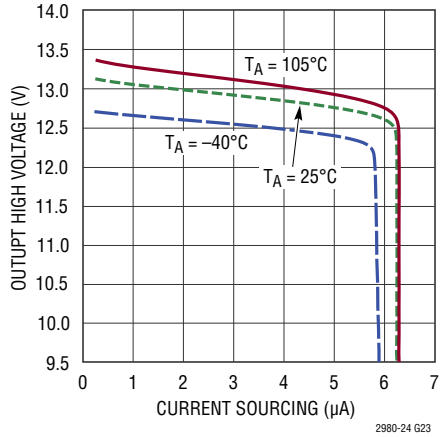
Supply Current vs Supply Voltage (1/3 LTC2980-24)



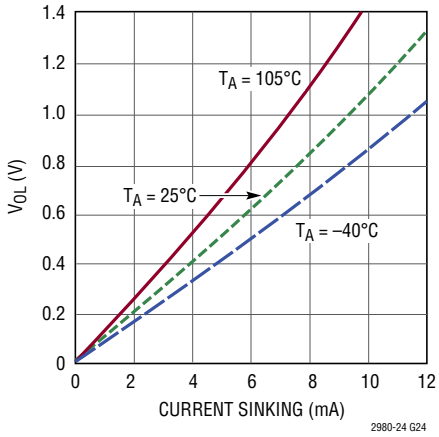
Supply Current vs Temperature (1/3 LTC2980-24)



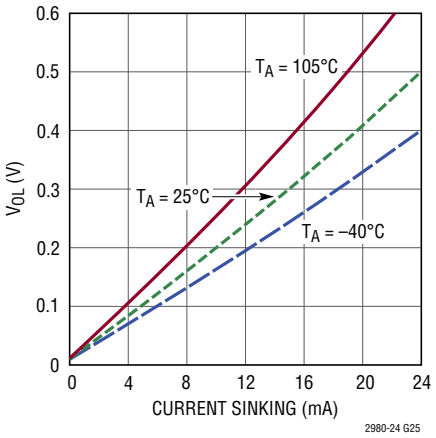
$V_{OUT\_EN[3:0]}$ and V_{IN_EN} Output High Voltage vs Current



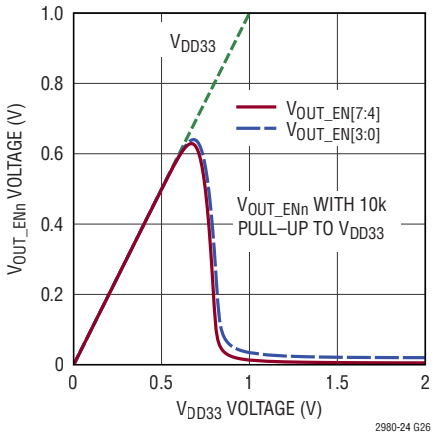
$V_{OUT\_EN[3:0]}$ and V_{IN_EN} Output V_{OL} vs Current



$V_{OUT\_EN[7:4]}$ V_{OL} vs Current



$V_{OUT\_EN[7:0]}$ Output Voltage vs V_{DD33}



PIN FUNCTIONS

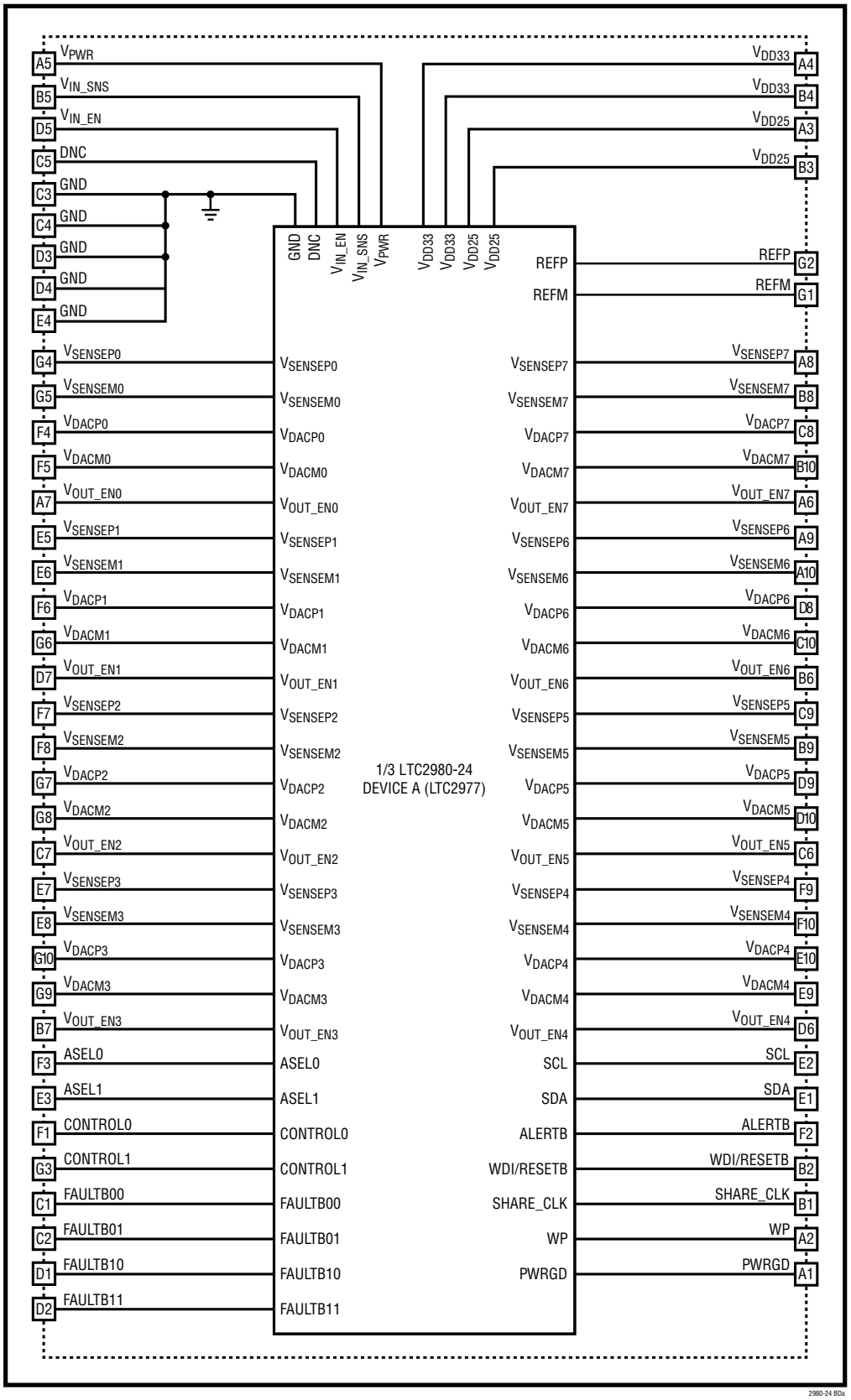
PIN NAME	PIN			PIN TYPE	DESCRIPTION
	DEVICE A	DEVICE B	DEVICE C		
$V_{SENSEP0}$	G4	P4	AA4	In	DC/DC Converter Differential (+) Output Voltage-0 Sensing Pin
$V_{SENSEM0}$	G5	P5	AA5	In	DC/DC Converter Differential (–) Output Voltage-0 Sensing Pin
$V_{SENSEP1}$	E5	M5	W5	In	DC/DC Converter Differential (+) Output Voltage or Current-1 Sensing Pins
$V_{SENSEM1}$	E6	M6	W6	In	DC/DC Converter Differential (–) Output Voltage or Current-1 Sensing Pins
$V_{SENSEP2}$	F7	N7	Y7	In	DC/DC Converter Differential (+) Output Voltage-2 Sensing Pin
$V_{SENSEM2}$	F8	N8	Y8	In	DC/DC Converter Differential (–) Output Voltage-2 Sensing Pin
$V_{SENSEP3}$	E7	M7	W7	In	DC/DC Converter Differential (+) Output Voltage or Current-3 Sensing Pins
$V_{SENSEM3}$	E8	M8	W8	In	DC/DC Converter Differential (–) Output Voltage or Current-3 Sensing Pins
$V_{SENSEP4}$	F9	N9	Y9	In	DC/DC Converter Differential (+) Output Voltage-4 Sensing Pin
$V_{SENSEM4}$	F10	N10	Y10	In	DC/DC Converter Differential (–) Output Voltage-4 Sensing Pin
$V_{SENSEP5}$	C9	K9	U9	In	DC/DC Converter Differential (+) Output Voltage or Current-5 Sensing Pins
$V_{SENSEM5}$	B9	J9	T9	In	DC/DC Converter Differential (–) Output Voltage or Current-5 Sensing Pins
$V_{SENSEP6}$	A9	H9	R9	In	DC/DC Converter Differential (+) Output Voltage-6 Sensing Pin
$V_{SENSEM6}$	A10	H10	R10	In	DC/DC Converter Differential (–) Output Voltage-6 Sensing Pin
$V_{SENSEP7}$	A8	H8	R8	In	DC/DC Converter Differential (+) Output Voltage or Current-7 Sensing Pin
$V_{SENSEM7}$	B8	J8	T8	In	DC/DC Converter Differential (–) Output Voltage or Current-7 Sensing Pin
V_{OUT_EN0}	A7	H7	R7	Out	DC/DC Converter Enable-0 Pin. Output high voltage optionally pulled up to 12V by 5µA.
V_{OUT_EN1}	D7	L7	V7	Out	DC/DC Converter Enable-1 Pin. Output high voltage optionally pulled up to 12V by 5µA.
V_{OUT_EN2}	C7	K7	U7	Out	DC/DC Converter Enable-2 Pin. Output high voltage optionally pulled up to 12V by 5µA.
V_{OUT_EN3}	B7	J7	T7	Out	DC/DC Converter Enable-3 Pin. Output high voltage optionally pulled up to 12V by 5µA.
V_{OUT_EN4}	D6	L6	V6	Out	DC/DC Converter Enable-4 Pin. Open-drain pull-down output.
V_{OUT_EN5}	C6	K6	U6	Out	DC/DC Converter Enable-5 Pin. Open-drain pull-down output.
V_{OUT_EN6}	B6	J6	T6	Out	DC/DC Converter Enable-6 Pin. Open-drain pull-down output.
V_{OUT_EN7}	A6	H6	R6	Out	DC/DC Converter Enable-7 Pin. Open-drain pull-down output.
V_{IN_EN}	D5	L5	V5	Out	DC/DC Converter V_{IN} ENABLE Pin. Output high voltage optionally pulled up to 12V by 5µA.
V_{IN_SNS}	B5	J5	T5	In	V_{IN} SENSE Input. This voltage is compared against the V_{IN} on and off voltage thresholds in order to determine when to enable and disable, respectively, the downstream DC/DC converters.
V_{PWR}	A5	H5	R5	In	V_{PWR} serves as the unregulated power supply input to the chip (4.5V to 15V). If a 4.5V to 15V Supply Voltage is Unavailable, Short V_{PWR} to V_{DD33} and Power the Chip Directly from a 3.3V Supply.
V_{DD33}	A4	H4	R4	In/Out	If shorted to V_{PWR}, it serves as 3.13V to 3.47V supply input pin. Otherwise it is a 3.3V Internally Regulated Voltage Output. If using the internal regulator to provide V_{DD33}, do not connect to any component except the pull-up resistors and bypass capacitors required to support the LTC2980-24 in the application.
V_{DD33}	B4	J4	T4	In	Input for Internal 2.5V Sub-Regulator. Short pin A4 to B4 and H4 to J4 and R4 to T4. If using the internal regulator to provide V_{DD33}, do not connect to any component except the pull-up resistors and bypass capacitors required to support the LTC2980-24 in the application.
V_{DD25}	A3	H3	R3	In/Out	2.5V Internally Regulated Voltage Output. Bypass to GND with a 0.1µF capacitor. Do not connect to any component except the pull-up resistors and bypass capacitors required to support the LTC2980-24 in the application.
V_{DD25}	B3	J3	T3	In	2.5V Supply Voltage Input. Short pin A3 to B3 and H3 to J3 and R3 to T3. Do not connect to any component except the pull-up resistors and bypass capacitors required to support the LTC2980-24 in the application.
WP	A2	H2	R2	In	Digital Input. Write-protect input pin, active high.
PWRGD	A1	H1	R1	Out	Power Good Open-Drain Output. Indicates when outputs are power good. Can be used as system power-on reset. The latency of this signal may be as long as the ADC latency. See Note 7.
SHARE_CLK	B1	J1	T1	In/Out	Bidirectional Clock Sharing Pin. Connect a 5.49k pull-up resistor to V_{DD33}. Connect to all other SHARE_CLK pins in the system.

PIN FUNCTIONS

PIN NAME	PIN			PIN TYPE	DESCRIPTION
	DEVICE A	DEVICE B	DEVICE C		
WDI/RESETB	B2	J2	T2	In	Watchdog Timer Interrupt and Chip Reset Input. Connect a 10k pull-up resistor to V_{DD33}. Rising edge resets watchdog counter. Holding this pin low for more than t_{RESETB} resets the chip.
FAULTB00	C1	K1	U1	In/Out	Open-Drain Output and Digital Input. Active low bidirectional fault indicator-00. Connect a 10k pull-up resistor to V_{DD33}.
FAULTB01	C2	K2	U2	In/Out	Open-Drain Output and Digital Input. Active low bidirectional fault indicator-01. Connect a 10k pull-up resistor to V_{DD33}.
FAULTB10	D1	L1	V1	In/Out	Open-Drain Output and Digital Input. Active low bidirectional fault indicator-10. Connect a 10k pull-up resistor to V_{DD33}.
FAULTB11	D2	L2	V2	In/Out	Open-Drain Output and Digital Input. Active low bidirectional fault indicator-11. Connect a 10k pull-up resistor to V_{DD33}.
SDA	E1	M1	W1	In/Out	PMBus Bidirectional Serial Data Pin
SCL	E2	M2	W2	In	PMBus Serial Clock Input Pin (400kHz Maximum)
ALERTB	F2	N2	Y2	Out	Open-Drain Output. Generates an interrupt request in a fault/warning situation.
CONTROL0	F1	N1	Y1	In	Control Pin 0 Input
CONTROL1	G3	P3	AA3	In	Control Pin 1 Input
ASEL0	F3	N3	Y3	In	Ternary Address Select Pin 0 Input. Connect to V_{DD33}, GND or float to encode 1 of 3 logic states.
ASEL1	E3	M3	W3	In	Ternary Address Select Pin 1 Input. Connect to V_{DD33}, GND or float to encode 1 of 3 logic states.
REFP	G2	P2	AA2	Out	Reference Voltage Output
REFM	G1	P1	AA1	Out	Reference Return Pin
V_{DACP0}	F4	N4	Y4	Out	DAC0 Output
V_{DACM0}	F5	N5	Y5	Out	DAC0 Return. Connect to channel 0 DC/DC converter's GND sense or return to GND.
V_{DACP1}	F6	N6	Y6	Out	DAC1 Output
V_{DACM1}	G6	P6	AA6	Out	DAC1 Return. Connect to channel 0 DC/DC converter's GND sense or return to GND.
V_{DACP2}	G7	P7	AA7	Out	DAC2 Output
V_{DACM2}	G8	P8	AA8	Out	DAC2 Return. Connect to channel 0 DC/DC converter's GND sense or return to GND.
V_{DACP3}	G10	P10	AA10	Out	DAC3 Output
V_{DACM3}	G9	P9	AA9	Out	DAC3 Return. Connect to channel 0 DC/DC converter's GND sense or return to GND.
V_{DACP4}	E10	M10	W10	Out	DAC4 Output
V_{DACM4}	E9	M9	W9	Out	DAC4 Return. Connect to channel 0 DC/DC converter's GND sense or return to GND.
V_{DACP5}	D9	L9	V9	Out	DAC5 Output
V_{DACM5}	D10	L10	V10	Out	DAC5 Return. Connect to channel 0 DC/DC converter's GND sense or return to GND.
V_{DACP6}	D8	L8	V8	Out	DAC6 Output
V_{DACM6}	C10	K10	U10	Out	DAC6 Return. Connect to channel 0 DC/DC converter's GND sense or return to GND.
V_{DACP7}	C8	K8	U8	Out	DAC7 Output
V_{DACM7}	B10	J10	T10	Out	DAC7 Return. Connect to channel 0 DC/DC converter's GND sense or return to GND.
GND	C3, C4, D3, D4, E4	K3, K4, L3, L4, M4	U3, U4, V3, V4, W4	Ground	
DNC	C5	K5	U5	Do Not Connect	Do not connect to this pin.

*Any unused $V_{SENSEPn}$ or $V_{SENSEMn}$ or V_{DACMn} pins must be tied to GND.

BLOCK DIAGRAM



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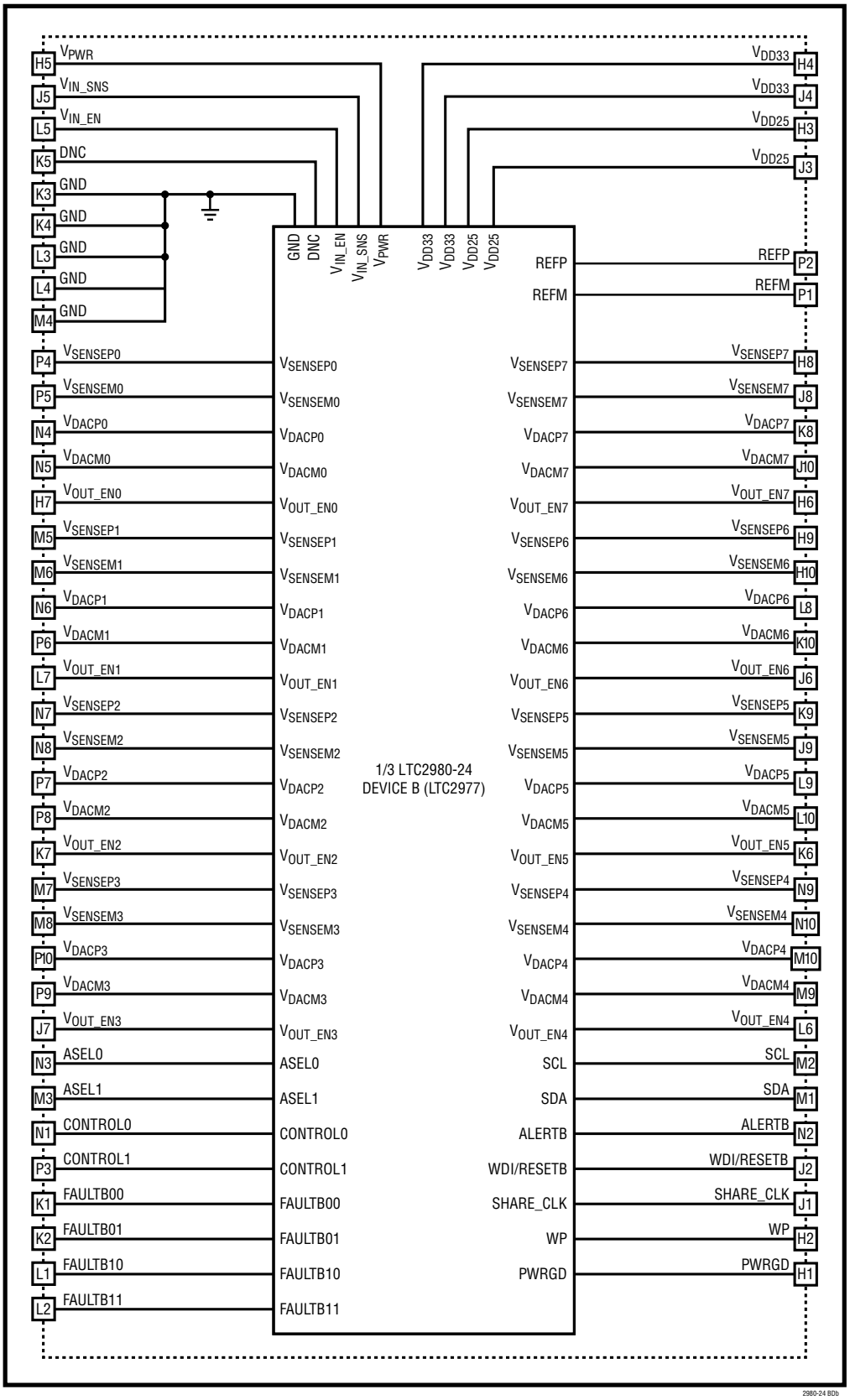

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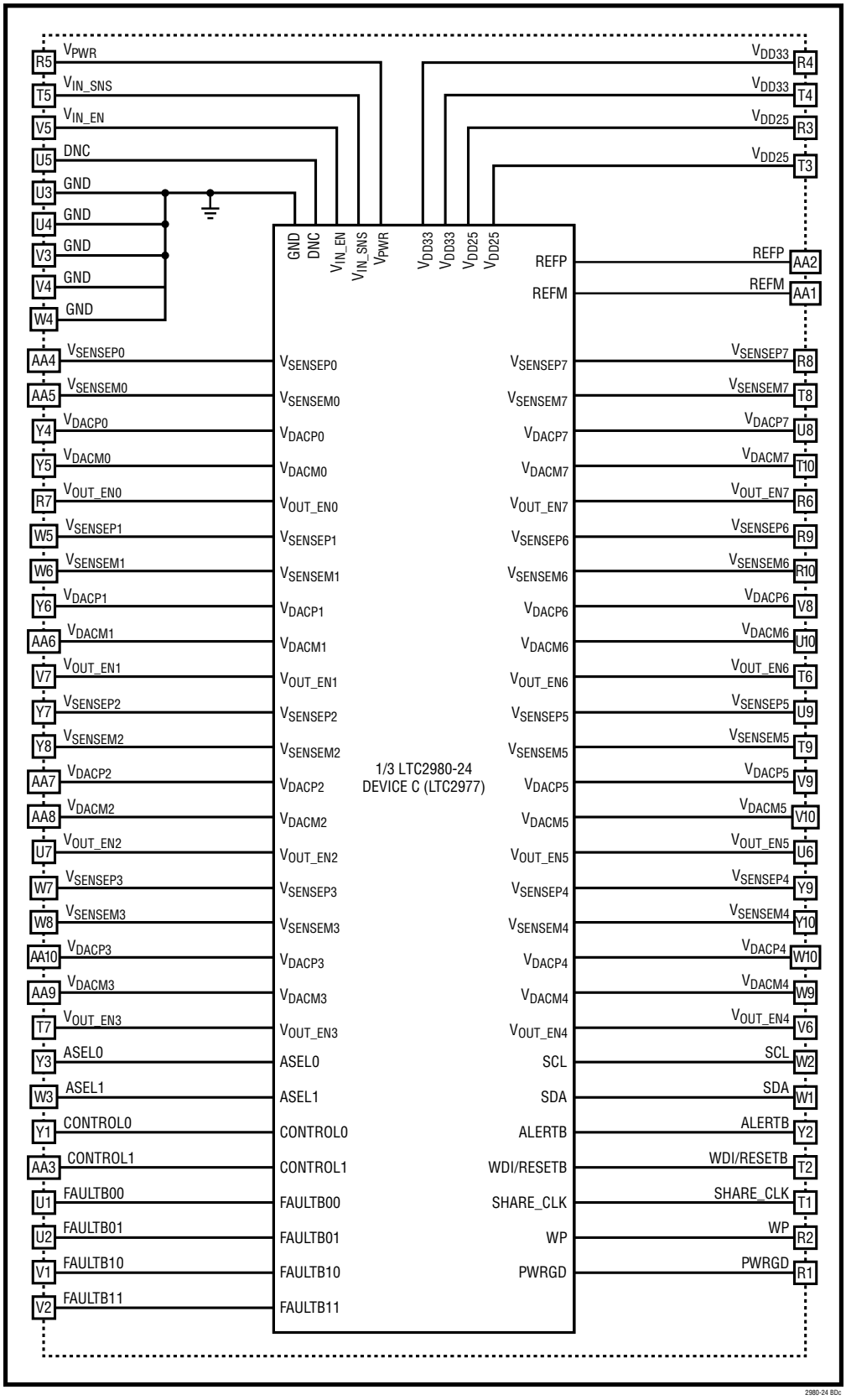


OPERATION

Overview

The LTC2980-24 contains three independent LTC2977 devices. Each third of the LTC2980-24 behaves the same as a standalone LTC2977 including independent power supply and ground pins.

Refer to the LTC2977 data sheet for a detailed description of the device operation, the PMBus command set, and applications information.

Device Address

Since the LTC2980-24 consists of three independent LTC2977 devices, each third of the LTC2980-24 must be configured for a unique address. The I^2C/SMBus addresses of the LTC2980-24 are configured in the same manner as for individual LTC2977 devices. The LTC2980-24 also responds to the LTC2977 global address and the SMBus alert response address, regardless of the state of the ASEL pins and the MFR_I2C_BASE_ADDRESS register. Please refer to the Device Address section in the LTC2977 data sheet for more details.

MFR_SPECIAL_ID

The LTC2980-24 contains unique MFR_SPECIAL_ID values to differentiate it from the LTC2977. Table 1 lists the MFR_SPECIAL_ID values for the LTC2980-24.

Table 1. LTC2980-24 MFR_SPECIAL_ID Values

LTC2980-24 DEVICE	MFR_SPECIAL_ID
Device A	0x80A1
Device B	0x80B1
Device C	0x80C1

EEPROM

The LTC2980-24 contains internal EEPROM (nonvolatile memory) with error-correcting code (ECC) to store configuration settings and fault log information. EEPROM endurance, retention, and mass write operation time are specified over the operating junction temperature range. See Electrical Characteristics and Absolute Maximum Ratings sections.

Nondestructive operation above T_J = 105°C is possible although the Electrical Characteristics are not guaranteed and the EEPROM will be degraded.

Operating the EEPROM above 105°C may result in a degradation of retention characteristics. The fault logging function, which is useful in debugging system problems that may occur at high temperatures, only writes to fault log EEPROM locations. If occasional writes to these registers occur above 105°C, a slight degradation in the data retention characteristics of the fault log may occur.

It is recommended that the EEPROM not be written using STORE_USER_ALL or bulk programming when T_J > 85°C.

The degradation in EEPROM retention for temperatures >105°C can be approximated by calculating the dimensionless acceleration factor using the following equation

$$AF = e^{\left[\left(\frac{Ea}{k}\right)\bullet\left(\frac{1}{T_{USE}+273}-\frac{1}{T_{STRESS}+273}\right)\right]}$$

where:

AF = acceleration factor

Ea = activation energy = 1.4 eV

$k = 8.617 \times 10^{-5}$ eV/°K

T_{USE} = 105°C specified junction temperature

T_{STRESS} = actual junction temperature °C

Example: Calculate the effect on retention when operating at a junction temperature of 125°C for 10 hours.

T_{STRESS} = 125°C

T_{USE} = 105°C

AF = 8.65

Equivalent operating time at 105°C = 86.5 hours.

The overall retention of the EEPROM was degraded by 76.5 hours as a result of operation at a junction temperature of 125°C for 10 hours. Note that the effect of this overstress is negligible when compared to the overall EEPROM retention rating of 175,200 hours at a maximum junction temperature of 105°C.

APPLICATIONS INFORMATION

OVERVIEW

The LTC2980-24 is a digital power system manager that is capable of sequencing, margining, trimming, supervising output voltage for OV/UV conditions, providing fault management, and voltage readback for twenty-four DC/DC converters. Input voltage and LTC2980-24 junction temperature readback are also available. Odd numbered channels can be configured to read back current sense resistor voltages. Multiple LTC2980-24s devices can be synchronized to operate in unison using the SHARE_CLK, FAULTB and CONTROL pins. The LTC2980-24 utilizes a PMBus compliant interface and command set.

POWERING THE LTC2980-24

The LTC2980-24 can be powered two ways. The first method requires that a voltage between 4.5V and 15V be applied to the V_{PWR} pin. See Figure 1. Internal linear regulators convert V_{PWR} down to 3.3V which drives all of the internal circuitry in each device. Do not tie the $V_{DD33(A)}$, $V_{DD33(B)}$ and $V_{DD33(C)}$ pins together since each third of the LTC2980-24 has independent voltage regulators.

Alternatively, power from an external 3.3V supply may be applied directly to the V_{DD33} pins using a voltage between 3.13V and 3.47V. Tie V_{PWR} to the V_{DD33} pins. See Figure 2. In this case, $V_{DD33(A)}$, $V_{DD33(B)}$ and $V_{DD33(C)}$ may be tied together. All functionality is available when using this alternate power method. The higher voltages needed for the $V_{OUT\_EN[0:3]}$ pins and bias for the V_{SENSE} pins are charge pumped from V_{DD33}.

The method used to power each device in the LTC2980-24 is independent of the other device. Either method may be used in any combination.

APPLICATION CIRCUITS

V_{IN} Sense

Voltages other than V_{IN} can be monitored and supervised using the V_{IN_SNS} pins. Each V_{IN_SNS} pin has a calibrated internal divider allowing it to directly sense voltages up to 15V.

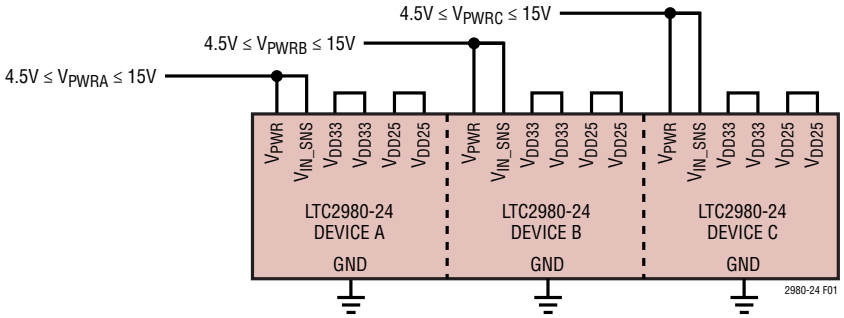


Figure 1. Powering LTC2980-24 Directly from an Intermediate Bus

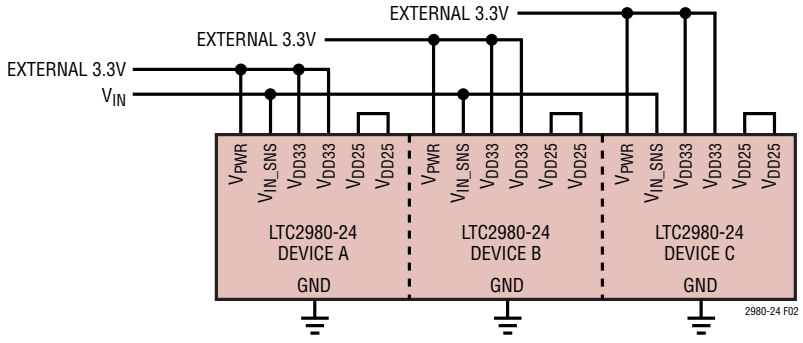


Figure 2. Powering LTC2980-24 from External 3.3V Supply

APPLICATIONS INFORMATION

Unused ADC Sense Inputs

Connect all unused ADC sense inputs ($V_{SENSEP}n$ or $V_{SENSEM}n$) to GND. In a system where the inputs are connected to removable cards and may be left floating in certain situations, connect the inputs to GND using 100k resistors, as shown in Figure 3.

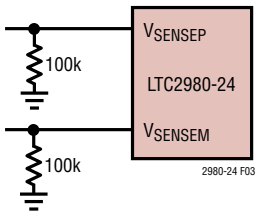


Figure 3. Connecting Unused Inputs to GND

PCB ASSEMBLY AND LAYOUT SUGGESTIONS

Bypass Capacitor Placement

The LTC2980-24 requires 0.1µF bypass capacitors between the V_{DD33} pins and GND, the V_{DD25} pins and GND, and between the REFP and REFM pins. If the chip is being powered from the V_{PWR} input, then that pin should also be bypassed to GND by a 0.1µF capacitor. In order to be effective, these capacitors should be made of high quality ceramic dielectric such as X5R or X7R and be placed as close to the chip as possible. The PCB layout should adhere to good layout guidelines. A multilayer PCB that dedicates a layer to power and ground is recommended. Low resistance and low inductance power and ground connections are important to minimize power supply noise and ensure proper device operation.

DESIGN CHECKLIST

I^2C

- Each third of the LTC2980-24 must be configured for a unique address. Unique hardware ASELn values are recommended for simplest in system programming.
- The address select pins (ASEL*n*) are tri-level; Check Table 1 of the LTC2977 data sheet.
- Check addresses for collision with other devices on the bus and any global addresses.

Output Enables

- Use appropriate pull-up resistors on all $V_{OUT\_EN}n$ pins.
- Verify that the absolute maximum ratings of the $V_{OUT\_EN}n$ pins are not exceeded.

V_{IN} Sense

- No external resistive divider is required to sense V_{IN}; V_{IN_SNS} already has an internal calibrated divider.

Logic Signals

- Verify the absolute maximum ratings of the digital pins (SCL, SDA, ALERTB, FAULTB*zn*, CONTROL*n*, SHARE_CLK, WDI, ASEL*n*, PWRGD) are not exceeded.
- Connect all SHARE_CLK pins in the system together and pull up to 3.3V with a 5.49k resistor.
- Do not leave CONTROL*n* pins floating. Pull up to 3.3V with a 10k resistor.
- Tie WDI/RESETB to V_{DD33} with a 10k resistor. Do not connect a capacitor to the WDI/RESETB pin.
- Tie WP to either VDD33 or GND. Do not leave floating.

Unused Inputs

- Connect all unused $V_{SENSEP}n$, $V_{SENSEM}n$ and DACM*n* pins to GND. Do not float unused inputs. Refer to Unused ADC Sense Inputs in the Applications Information section of the LTC2977 data sheet

DAC Outputs

- Select appropriate resistor for desired margin range. Refer to the resistor selection tool in LTpowerPlay for assistance.

Power Supplies

- If powered from V_{PWR}, do not connect the $V_{DD33(A)}$, $V_{DD33(B)}$, and $V_{DD33(C)}$ pins together. Each V_{DD33} pin has an independent, internal regulator.

For a more complete list of design considerations and a schematic checklist, see the Design Checklist on the LTC2980-24 product page.

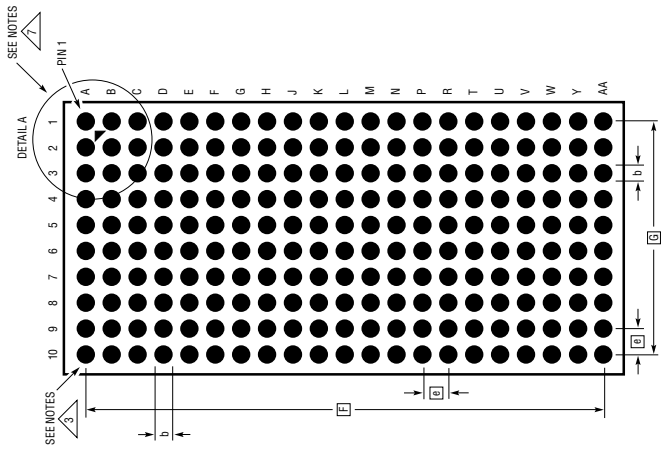
PACKAGE DESCRIPTION

LTC2980-24 Component BGA Pinout

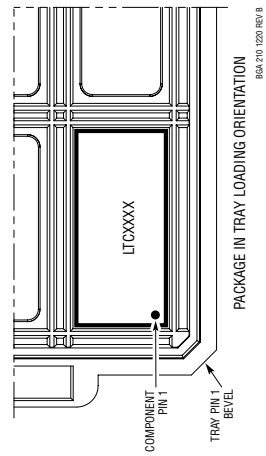
		1	2	3	4	5	6	7	8	9	10
	A	PWRGD	WP	V_{DD25}	V_{DD33}	V_{PWR}	V_{OUT_EN7}	V_{OUT_EN0}	$V_{SENSEP7}$	$V_{SENSEP6}$	$V_{SENSEM6}$
	B	SHARE–CLK	WDI/RESETB	V_{DD25}	V_{DD33}	V_{IN_SNS}	V_{OUT_EN6}	V_{OUT_EN3}	$V_{SENSEM7}$	$V_{SENSEM5}$	V_{DACM7}
	C	FAULTB00	FAULTB01	GND	GND	DNC	V_{OUT_EN5}	V_{OUT_EN2}	V_{DACP7}	$V_{SENSEP5}$	V_{DACM6}
DEVICE A	**D**	FAULTB10	FAULTB11	GND	GND	V_{IN_EN}	V_{OUT_EN4}	V_{OUT_EN1}	V_{DACP6}	V_{DACP5}	V_{DACM5}
	E	SDA	SCL	ASEL1	GND	$V_{SENSEP1}$	$V_{SENSEM1}$	$V_{SENSEP3}$	$V_{SENSEM3}$	V_{DACM4}	V_{DACP4}
	F	CONTROLO	ALERTB	ASEL0	V_{DACP0}	V_{DACM0}	V_{DACP1}	$V_{SENSEP2}$	$V_{SENSEM2}$	$V_{SENSEP4}$	$V_{SENSEM4}$
	G	REFM	REFP	CONTROL1	$V_{SENSEP0}$	$V_{SENSEM0}$	V_{DACM1}	V_{DACP2}	V_{DACM2}	V_{DACM3}	V_{DACP3}
	H	PWRGD	WP	V_{DD25}	V_{DD33}	V_{PWR}	V_{OUT_EN7}	V_{OUT_EN0}	$V_{SENSEP7}$	$V_{SENSEP6}$	$V_{SENSEM6}$
	J	SHARE–CLK	WDI/RESETB	V_{DD25}	V_{DD33}	V_{IN_SNS}	V_{OUT_EN6}	V_{OUT_EN3}	$V_{SENSEM7}$	$V_{SENSEM5}$	V_{DACM7}
	K	FAULTB00	FAULTB01	GND	GND	DNC	V_{OUT_EN5}	V_{OUT_EN2}	V_{DACP7}	$V_{SENSEP5}$	V_{DACM6}
DEVICE B	**L**	FAULTB10	FAULTB11	GND	GND	V_{IN_EN}	V_{OUT_EN4}	V_{OUT_EN1}	V_{DACP6}	V_{DACP5}	V_{DACM5}
	M	SDA	SCL	ASEL1	GND	$V_{SENSEP1}$	$V_{SENSEM1}$	$V_{SENSEP3}$	$V_{SENSEM3}$	V_{DACM4}	V_{DACP4}
	N	CONTROLO	ALERTB	ASEL0	V_{DACP0}	V_{DACM0}	V_{DACP1}	$V_{SENSEP2}$	$V_{SENSEM2}$	$V_{SENSEP4}$	$V_{SENSEM4}$
	P	REFM	REFP	CONTROL1	$V_{SENSEP0}$	$V_{SENSEM0}$	V_{DACM1}	V_{DACP2}	V_{DACM2}	V_{DACM3}	V_{DACP3}
	R	PWRGD	WP	V_{DD25}	V_{DD33}	V_{PWR}	V_{OUT_EN7}	V_{OUT_EN0}	$V_{SENSEP7}$	$V_{SENSEP6}$	$V_{SENSEM6}$
	T	SHARE–CLK	WDI/RESETB	V_{DD25}	V_{DD33}	V_{IN_SNS}	V_{OUT_EN6}	V_{OUT_EN3}	$V_{SENSEM7}$	$V_{SENSEM5}$	V_{DACM7}
	U	FAULTB00	FAULTB01	GND	GND	DNC	V_{OUT_EN5}	V_{OUT_EN2}	V_{DACP7}	$V_{SENSEP5}$	V_{DACM6}
DEVICE C	**V**	FAULTB10	FAULTB11	GND	GND	V_{IN_EN}	V_{OUT_EN4}	V_{OUT_EN1}	V_{DACP6}	V_{DACP5}	V_{DACM5}
	W	SDA	SCL	ASEL1	GND	$V_{SENSEP1}$	$V_{SENSEM1}$	$V_{SENSEP3}$	$V_{SENSEM3}$	V_{DACM4}	V_{DACP4}
	Y	CONTROLO	ALERTB	ASEL0	V_{DACP0}	V_{DACM0}	V_{DACP1}	$V_{SENSEP2}$	$V_{SENSEM2}$	$V_{SENSEP4}$	$V_{SENSEM4}$
	AA	REFM	REFP	CONTROL1	$V_{SENSEP0}$	$V_{SENSEM0}$	V_{DACM1}	V_{DACP2}	V_{DACM2}	V_{DACM3}	V_{DACP3}

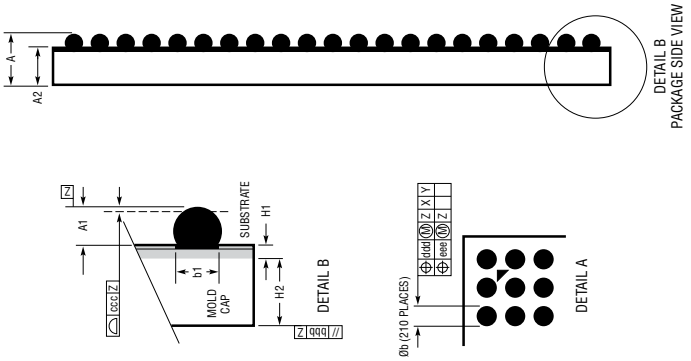
PACKAGE DESCRIPTION

BGA Package
210-Lead (16.9mm × 8.1mm × 1.52mm)
(Reference LTC DWG# 05-08-1828 Rev B)

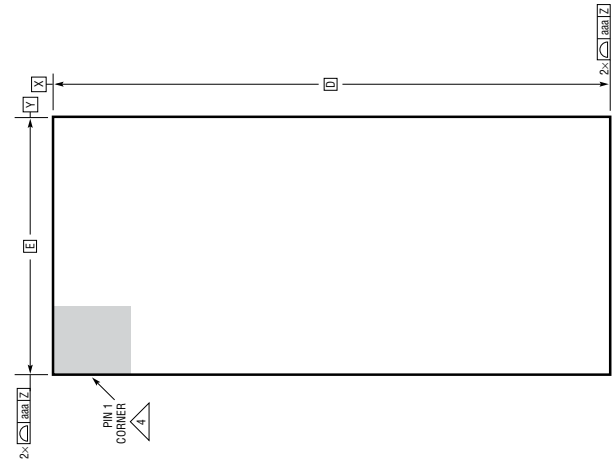


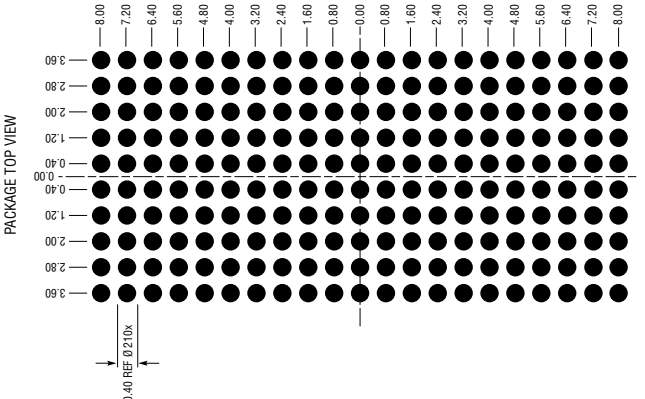
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JEP95
4. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY





DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	1.32	1.52	1.72	
A1	0.30	0.40	0.50	BALL HT
A2	1.02	1.12	1.22	
b	0.35	0.50	0.65	BALL DIMENSION
b1	0.37	0.40	0.43	PAD DIMENSION
D		16.90		
E		8.10		
e		0.80		
F		16.00		
G		7.20		
H1		0.32 REF		SUBSTRATE THK
H2		0.80 REF		MOLD CAP HT
aaa			0.15	
bbb			0.20	
ccc			0.20	
ddd			0.15	
eee			0.08	
TOTAL NUMBER OF BALLS: 210				





REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	07/22	I_{VOUT_ENn} Output Sinking Current at condition Weak Pull-Down Enabled: minimum spec changed from 33µA to 28µA and typical spec changed from 50µA to 43µA. I_{VOUT_ENn} Output Sinking Current at condition Strong Pulldown Enabled, V_{OUT_ENn} = 0.1V: spec updated to typical value only at room temp	5

TYPICAL APPLICATION

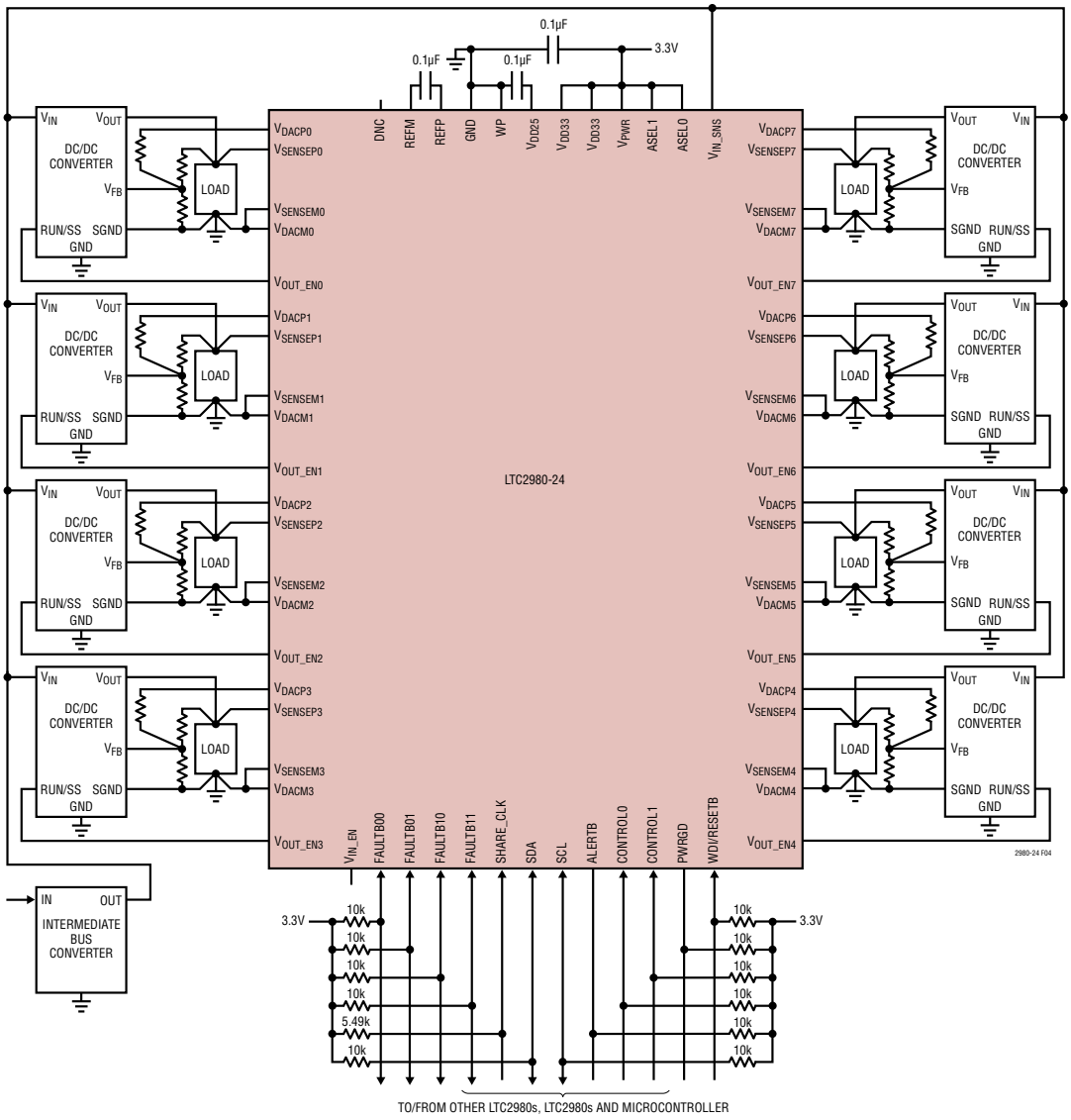


Figure 4. LTC2980-24 Application Circuit with External 3.3V Chip Power (8 of 24 Channels Shown)

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2970	Dual I²C Power Supply Monitor and Margining Controller	5V to 15V, 0.5% TUE 14-Bit ADC, 8-Bit DAC, Temperature Sensor
LTC2974	4-Channel PMBus Power System Manager	0.25% TUE 16-Bit ADC, Voltage/Current/Temperature Monitoring and Supervision
LTC2975	4-Channel PMBus Power System Manager	0.25% TUE 16-Bit ADC, Voltage/Current/Temperature Monitoring and Supervision, Input Current and Power, Input Energy Accumulator
LTC2977	8-Channel PMBus Power System Manager	0.25% TUE 16-Bit ADC, Voltage/Temperature Monitoring and Supervision
LTC2980	16-Channel PMBus Power System Manager	Dual LTC2977
LTM®2987	16-Channel µModule PMBus Power System Manager	Dual LTC2977 with Integrated Passive Components
LTC3880	Dual Output PolyPhase Step-Down DC/DC Controller	0.5% TUE 16-Bit ADC, Voltage/Current/Temperature Monitoring and Supervision
LTC2971	Two Channel ±60V Power System Manager	0.25% TUE 16-Bit ADC, Voltage/Current/Temperature Monitoring and Supervision, Input Energy Accumulator