

FEATURES

- Reduces Power Dissipation by Replacing a Power Schottky Diode with No External Components
- Internal 7A, 21mΩ N-Channel MOSFET
- 15mV Regulated Forward Voltage
- 20μA Operating Current, 0.8μA Shutdown
- Wide 0V to 40V Input Range with $V_{CC} > 2.75V$
- Fast Turn-On Minimizes Voltage Droop
- Fast Reverse Recovery Time Minimizes Reverse Transient Current
- Smooth Switchover in Diode-OR Applications
- 16-Lead 2mm × 3mm LQFN Package

APPLICATIONS

- Schottky Diode Replacement
- Industrial, Medical and Consumer Portable Devices
- Battery and Wall Adapter Diode ORing

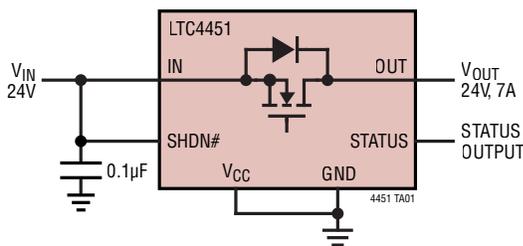
DESCRIPTION

The LTC[®]4451 is a high-performance Schottky diode replacement using an integrated N-Channel power MOSFET. It easily ORs power supplies together to increase system reliability and prevent reverse conduction.

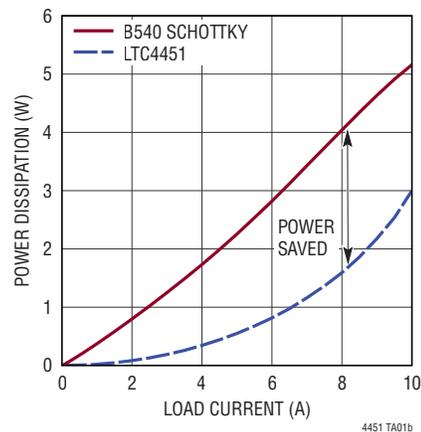
The LTC4451 regulates the forward voltage at 15mV to minimize power loss compared to Schottky diodes. Regulation ensures smooth current transfer without oscillation in diode-OR applications. When the power MOSFET is fully enhanced, the $R_{DS(ON)}$ of the transistor is 21mΩ and rated for forward conduction up to 7A while dissipating 1.34W. A high performance gate driver with fast transient response minimizes both forward power dissipation and reverse current. The V_{CC} input allows V_{IN} to work down to ground for low voltage applications. The LTC4451 is available in a small 16-Lead 2mm × 3mm LQFN Package.

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TYPICAL APPLICATION



Power Dissipation vs Load Current



4451 TA01b

LTC4451

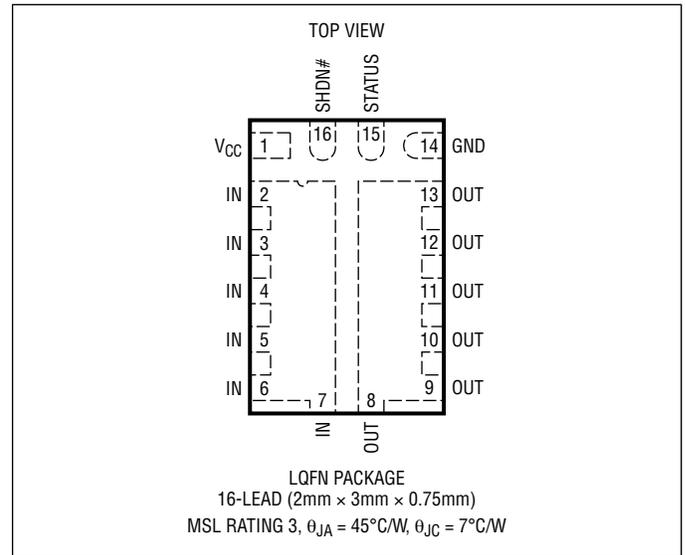
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages

IN, OUT, SHDN#, STATUS	-0.3V to 42V
V _{CC}	-0.3V to 6V
IN to OUT (Note 3)	-42V to 0.4V
Operating Junction Temperature Range	
LTC4451A	-40°C to 125°C
Storage Temperature Range	-65°C to 150°C

PIN CONFIGURATION



ORDER INFORMATION

Lead Free Finish

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4451AV#TRMPBF	LTC4451AV#TRPBF	LHKK	16-Lead (2mm × 3mm × 0.75mm) Plastic LQFN	-40°C to 125°C

TRM = 500 pieces.

Contact the factory for parts specified with wider operating temperature ranges.

Contact the factory for information on lead based finish parts.

[Tape and reel specifications](#). Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{IN} = 12\text{V}$, $V_{CC} = 0\text{V}$, $\text{SHDN}\# = 12\text{V}$, $I_{OUT} = 50\text{mA}$, unless otherwise noted.

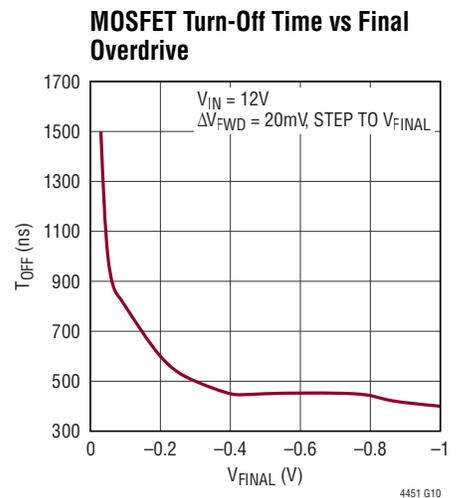
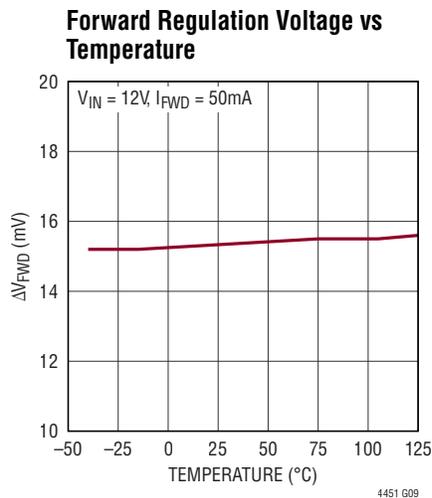
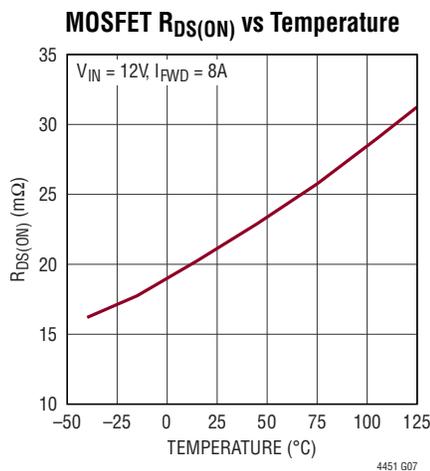
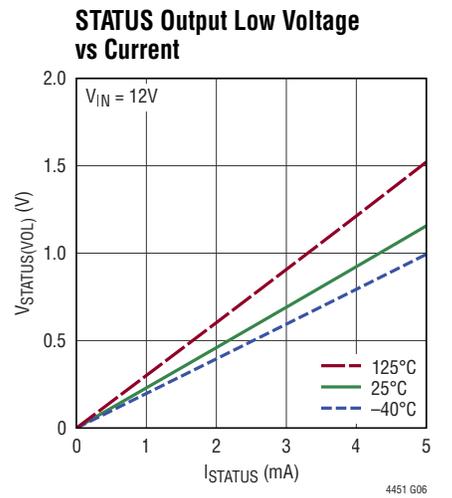
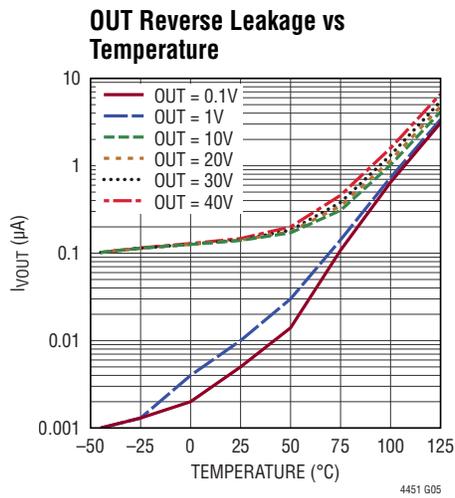
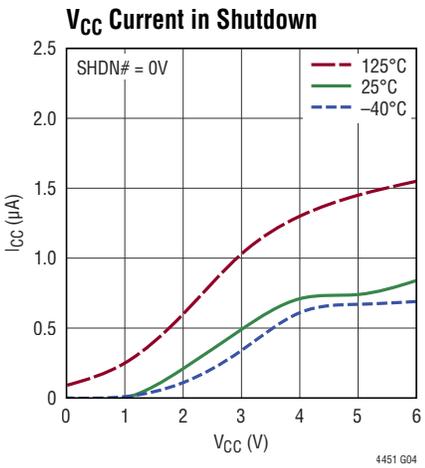
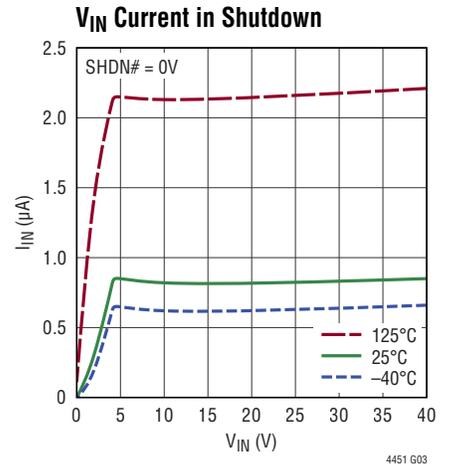
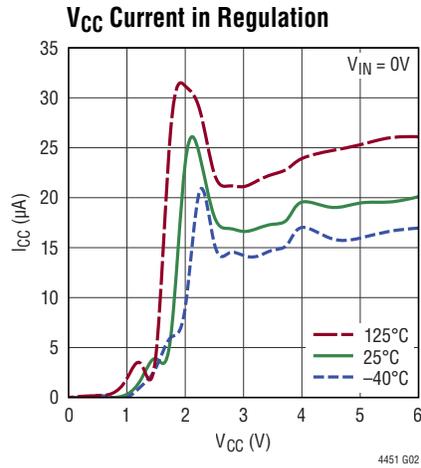
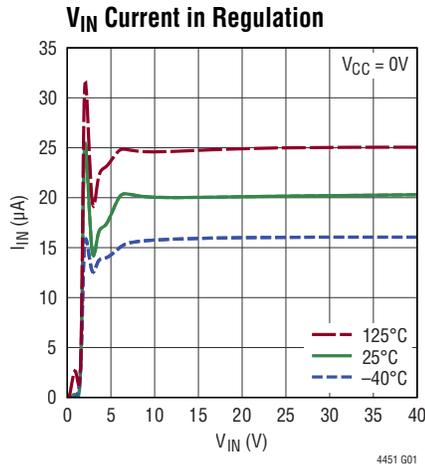
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
V_{IN}	Operating Voltage Range	$2.75\text{V} < V_{CC} < 5.5\text{V}$	● ● 0 2.75		40 40	V V	
I_{IN}	V_{IN} Net Current	$V_{IN} = 2.75\text{V}$, $V_{CC} = 5.5\text{V}$ $\text{SHDN}\# = 0\text{V}$, $I_{OUT} = 10\mu\text{A}$	● ● ●	20 0.5 0.8	45 5 5	μA μA μA	
V_{CC}	Operating Supply Range		●	2.75	5.5	V	
I_{CC}	V_{CC} Current	$V_{IN} = 2.75\text{V}$, $V_{CC} = 5.5\text{V}$ $V_{IN} = 12\text{V}$, $V_{CC} = 5.5\text{V}$ $\text{SHDN}\# = 0\text{V}$, $I_{OUT} = 10\mu\text{A}$, $V_{IN} = 0\text{V}$, $V_{CC} = 5.5\text{V}$	● ● ●	20 0 0.8	45 1 2.5	μA μA μA	
I_{REV}	N-Channel Reverse Leakage Current	$V_{IN} = 0\text{V}$, $V_{OUT} = 40\text{V}$			10	μA	
$R_{DS(ON)}$	N-Channel MOSFET On Resistance	$I_{OUT} = 8\text{A}$	●	21	45	$\text{m}\Omega$	
ΔV_{FWD}	Forward Regulation Voltage ($V_{IN} - V_{OUT}$)		●	5	15	25	mV
ΔV_{BODY}	Body Diode Forward Voltage Drop	$\text{SHDN}\# = 0\text{V}$	●	0.25	0.6	0.95	V
t_{ON}	Fast Turn-On Time	I_{OUT} Steps 50mA to 6A, $V_{IN} - V_{OUT}$ Settles within 25mV of $I_{OUT} \cdot R_{DS(ON)}$	●	0.3	1	μs	
t_{OFF}	Fast Turn-Off Time	$V_{FWD} = 15\text{mV}$ Step to -500mV , Reverse Current $< 40\text{mA}$	●	1	2	μs	
t_{START}	Start-Up Time	$\text{SHDN}\#$ Rising Edge to $(V_{IN} - V_{OUT}) < 200\text{mV}$	●	250	550	μs	
$t_{SHDN\#}$	$\text{SHDN}\#$ Turn-Off Delay	$\text{SHDN}\#$ Falling Edge to STATUS Falling Edge	●	10	20	μs	
$V_{SHDN\#(TH)}$	$\text{SHDN}\#$ Falling Threshold	$\text{SHDN}\#$ Falling	●	0.4	0.85	1.3	V
$V_{SHDN\#(HYS)}$	$\text{SHDN}\#$ Hysteresis			70		mV	
$V_{STATUS(VOL)}$	STATUS Output Voltage Low	$I_{STATUS} = 1\text{mA}$, $\text{SHDN}\# = 0\text{V}$ $I_{STATUS} = 3\text{mA}$, $\text{SHDN}\# = 0\text{V}$	● ●	0.25 0.7	0.5 1.4	V V	
I_{LEAK}	$\text{SHDN}\#$, STATUS Leakage Current	$V = 40\text{V}$	●		± 1	μA	

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive, all voltages are referenced to GND unless otherwise specified.

Note 3: This voltage is set by the MOSFET's body diode and will safely exceed 0.4V during start-up for a limited time determined by the body diode thermal dissipation.

TYPICAL PERFORMANCE CHARACTERISTICS



PIN FUNCTIONS

GND (Pin 14): Device Ground.

IN (Pins 2 - 7): Input Voltage and Positive Supply. IN is the ideal diode anode and source of the internal N-Channel MOSFET. Connect this pin to the power supply input that delivers power to the load. Bypass with a 0.1 μ F or larger capacitor to suppress load transients.

OUT (Pins 8 - 13): Output Voltage. OUT is the ideal diode cathode and drain of the internal N-Channel MOSFET. This is the common output when multiple LTC4451s are diode ORed. Bypass with a 0.1 μ F or larger capacitor.

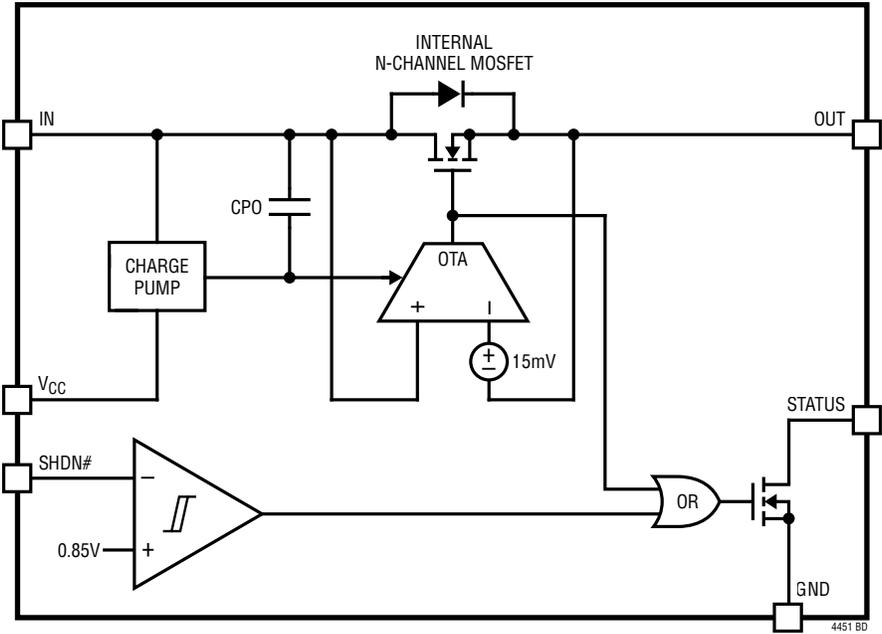
SHDN# (Pin 16): Shutdown Control Input. Driving this pin below 0.4V ($V_{SHDN\#(TH)}$) disables the internal MOSFET between IN and OUT and lowers the current consumption of LTC4451 below 5 μ A. STATUS is pulled low to indicate that the LTC4451 is disabled. When driven low, a connection from IN to OUT still exists through the MOSFET's body diode. Driving SHDN# above 0.85V ($V_{SHDN\#(TH)}$) +

0.07V ($V_{SHDN\#(HYS)}$) enables the LTC4451, allowing it to operate as an ideal diode. Connect to the highest of IN or V_{CC} or when not used. If the highest supply voltage is changing over time due to supplies being swapped in and out, connect SHDN# to a diode-OR or IN and V_{CC} when not used. Do not leave open.

STATUS (Pin 15): Gate Status Output. STATUS pulls low when the gate of the N-Channel MOSFET is pulled low indicating that the LTC4451 operates in reverse bias or in shutdown. Otherwise, STATUS pulls high indicating that the LTC4451 is operating in forward bias. Connect through a pull-up resistor to the highest of IN or V_{CC} . If the highest supply voltage is changing over time due to supplies being swapped in and out, connect to a diode-OR or IN and V_{CC} . Leave open or tie to GND when used.

V_{CC} (Pin 1): Positive Supply Input. This pin provides auxiliary power for the LTC4451 when $V_{IN} < 2.75V$. Connect to ground if unused.

BLOCK DIAGRAM



OPERATION

The LTC4451 is an 40V Schottky diode replacement consisting of an integrated N-channel power MOSFET and controller. The ideal diode regulates the forward voltage to 15mV to minimize power loss and ensure smooth current transfer without oscillation in diode-OR applications. The power MOSFET can deliver up to 7A output current from its input supply with a forward conduction resistance of 21m Ω when fully enhanced.

The LTC4451 features a high performance precision OTA which senses the voltage on the IN and OUT pins and drives the power MOSFET gate in regulation. The OTA senses when the forward voltage drop across the power MOSFET is sufficiently large and drives its gate to achieve full enhancement within 1 μ s. When the power MOSFET is fully enhanced, the forward voltage drop is equal to $R_{DS(ON)} \cdot I_{OUT}$. The OTA also senses when reverse conditions are present and drives the gate of the power MOSFET to IN within 1 μ s to disable the ideal diode allowing the LTC4451 to have a fast reverse recovery time.

The STATUS open drain output pulls low when the gate of the N-Channel MOSFET is pulled low indicating that

the LTC4451 operates in reverse bias or in shutdown. Otherwise, STATUS pulls high indicating that the LTC4451 is operating in forward bias. Connect STATUS to an external supply through a pull-up resistor. Leave open when unused.

When the SHDN# pin is pulled below 0.4V ($V_{SHDN\#(TH)}$), the gate drive for the power MOSFET is disabled and the LTC4451 enters a low current state. STATUS is pulled low and the power MOSFET body diode conducts the load current under forward biased condition. A SHDN# low to high transition allows the LTC4451 to power up and operate normally.

IN can operate down to 0V when the V_{CC} auxiliary supply voltage is above 2.75V. When either IN or V_{CC} exceeds 2.75V the LTC4451 activates an internal burst-mode charge pump to drive the gate of the N-Channel power MOSFET. The burst-mode charge pump requires t_{START} to turn on. During that delay the power MOSFET body diode conducts the load and inrush current if forward biased.

APPLICATIONS INFORMATION

Blocking diodes, commonly implemented by Schottky diodes, are typically placed in series with supply inputs for the purpose of OR'ing redundant power sources and protecting against supply reversal. The LTC4451 replaces diodes in these applications. Under forward conduction both the voltage drop and power loss are greatly reduced compared to a passive solution. When blocking voltage under reverse bias, the LTC4451 has significantly less reverse leakage than a typical Schottky diode.

The LTC4451 has a wide operating voltage range of 2.75V to 40V. When an auxiliary supply voltage is connected to V_{CC} the ideal diode can operate down to 0V making it ideal for applications that must tolerate large voltage transients.

Ideal diodes, like their non-ideal counterparts, exhibit a behavior known as reverse recovery. The presence of parasitic input inductance may cause large and

potentially damaging reverse recovery current spikes during a reverse mode commutation. Spikes and protection schemes are discussed in detail in the Input Short-Circuit Faults section.

It is important to note that the SHDN# pin, while disabling the LTC4451 and reducing its current consumption, does not disconnect the load from the input since the internal MOSFET's body diode is everpresent.

Paralleling Supplies (Diode-OR)

In many electrical systems, it is common to have a backup power source in addition to the primary power source. When the primary power source droops or is removed, the system runs from the backup power source. The outputs of two or more LTC4451s can be combined for redundancy or for droop sharing as shown in Figure 1.

APPLICATIONS INFORMATION

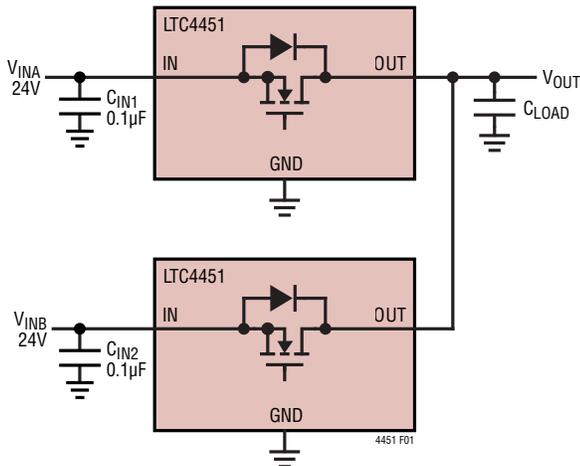


Figure 1. Redundant Diode-OR Power Supplies

For redundant supplies, the highest input supply voltage conducts all or most of the load current. If this supply's voltage droops or is short-circuited the ideal diode senses the reverse condition and activates a fast pull-down of the gate of the internal N-Channel MOSFET. The LTC4451 can withstand a reverse voltage of up to 40V differential between its power supply and output.

The reverse recovery time is dependent on the high performance OTA's transient response and gate slew rate. The reverse recovery current may cause the input supply voltage to rise, with the amount of voltage rise dependent on the input supply's impedance. The safest course of action is to use capacitors on the input supply whose voltage rating is higher than the highest voltage in the system or to consider protecting those capacitors with a TVS, for example.

Following a supply transient the output voltage droops until the ideal diode connected to the next highest supply detects a forward condition and enhances the gate of its N-Channel MOSFET. The OTA regulates the forward drop to 15mV (ΔV_{FWD}). If a larger forward drop is detected the LTC4451 fully enhances the gate of its N-Channel MOSFET within 0.3µs (t_{ON}) typical from a regulation condition and 3µs from a reverse bias condition.

To ensure there is minimal droop at the output, select a low ESR capacitor large enough to ride through the Fast-On delay time. A low ESR bulk capacitor will reduce

IR drops to the output voltage while the load current is sourced from the capacitor. To calculate the value of the load capacitor that will ride through the Fast-On delay time from reverse mode:

$$C_{LOAD} \geq \frac{I_{LOAD(MAX)} \cdot 3\mu s}{\Delta V_{OUT(DROOP)} - ESR \cdot I_{LOAD(MAX)}}$$

Shutdown Mode

Driving SHDN# below 0.4V ($V_{SHDN\#(TH)}$) reduces the current consumption of the part to less than 5µA and pulls the gate of the internal N-Channel MOSFET to IN to disable it. The STATUS pin is pulled low to indicate that the LTC4451 is disabled.

Shutdown does not interrupt forward current flow since a path is still present through the internal MOSFET's body diode. The forward voltage drop is 0.6V (ΔV_{BODY}) and power dissipation increases for a given load current. The LTC4451 enters a shutdown state within 20µs ($t_{SHDN\#}$) of a SHDN# falling edge. Driving SHDN# above 0.85V ($V_{SHDN\#(TH)} + 0.07V$ ($V_{SHDN\#(HYS)}$)) (typical) enables the gate driver allowing the LTC4451 to operate as an ideal diode. In shutdown the internal charge pump and gate drive are disabled. The part requires 250µs (t_{START}) to reactivate the charge pump and fully enhance the gate of the N-Channel MOSFET.

If the shutdown feature is not needed then connect the pin to an external supply voltage above 1.5V. SHDN# may be driven with a 3.3V or 5V logic signal or with an external pulldown transistor and pull-up resistor to an external supply as shown in Figure 2. Ensure that the pull-up resistor is low enough such that the pull-up current overcomes any leakage present at this pin. If capacitive

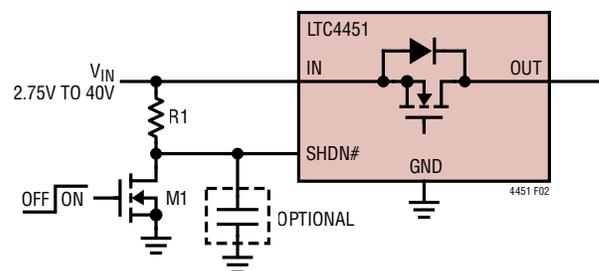


Figure 2. External SHDN# Control

APPLICATIONS INFORMATION

coupling onto the SHDN# pin is a concern, a capacitor to ground can be included.

Input Short-Circuit Faults

The dynamic behavior of an active LTC4451 ideal diode entering reverse bias mode is most accurately characterized by a delay followed by a period of reverse recovery. During the delay phase, when the gate driver is disabling the internal N-Channel MOSFET, a reverse current is present from OUT to IN. The magnitude of this current depends on the timing of the part, reverse voltage and parasitic impedances along the power path. After reverse recovery, energy stored in the parasitic inductances is transferred to other elements in the circuit, resulting in high current transients and potentially destructive voltage spikes.

High slew rates coupled with parasitic inductances in series with the input and output paths may cause potentially destructive transients to appear at the IN and OUT pins of the LTC4451 during reverse recovery.

A zero impedance short-circuit directly across the input and ground is especially troublesome because it permits the highest possible reverse current to build up during the delay phase. When the internal MOSFET turns off to interrupt the reverse current, the LTC4451 IN pin experiences a negative voltage spike while the OUT pin spikes in the positive direction.

To prevent damage to the LTC4451 under conditions of an input short-circuit, protect the IN and OUT pins as shown in Figure 3. The IN pin is protected by clamping to the GND pin with a Schottky diode. Negative spikes, seen after the MOSFET turns off during an input short are clamped by D1. D1 and C_{OUT} absorb the reverse recovery energy and protect the LTC4451. When the input short condition disappears, the current stored in the parasitic inductance, L_S , flows through the body diode of the MOSFET charging up C_{LOAD} . If C_{LOAD} is small or nonexistent, both the IN and OUT pins may rise to a level that can damage the LTC4451. In this case, D1 needs to be a TransZorb or TVS to limit the voltage difference between the IN and GND pins.

OUT is protected by the MOSFET's avalanche breakdown and C_{OUT} . Nevertheless, the internal MOSFET could be damaged by excessive current in higher voltage applications. A TVS (D2) can be used to protect the MOSFET and OUT pin. C_{OUT} also preserves the fast turn-off time when output parasitic inductance causes the IN and OUT voltages to drop quickly.

Layout Considerations

High current applications demand careful attention to trace resistances. The PCB trace associated with the IN/OUT pins should have low resistance to reduce conduction power loss. Keep the traces to the IN and OUT pins

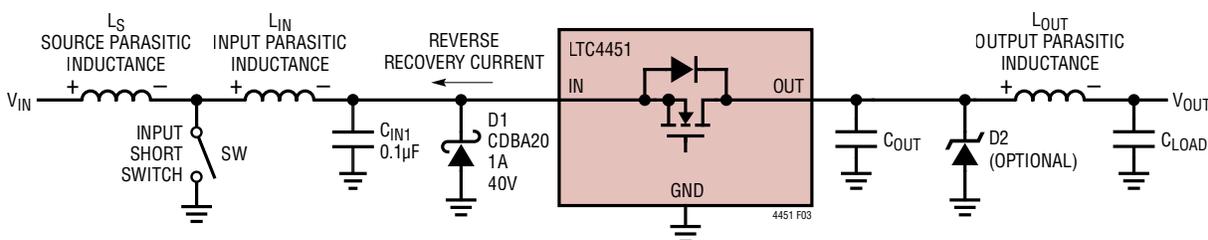


Figure 3. Input Short Protection Circuit with Parasitic Inductances

APPLICATIONS INFORMATION

wide and short to minimize resistive losses. To ensure a low contact resistance, solder the device's IN/OUT pins to the board using a reflow process. Include holes underneath the exposed pads to keep solder in place to avoid high voltage shorts between pins. The wide IN/OUT traces also act as a heat sink to remove the heat in the presence of a high current load. Place C_{OUT} , surge suppressors and necessary transient protection components close to the LTC4451 using short lead lengths. Transient voltage suppressors should have short wide traces to GND. Place decoupling capacitors close to the IN and V_{CC} pins. Figure 4 shows the recommended PCB layout for the LTC4451. The temperature rise of the recommended PCB layout with 6A load current is 25°C.

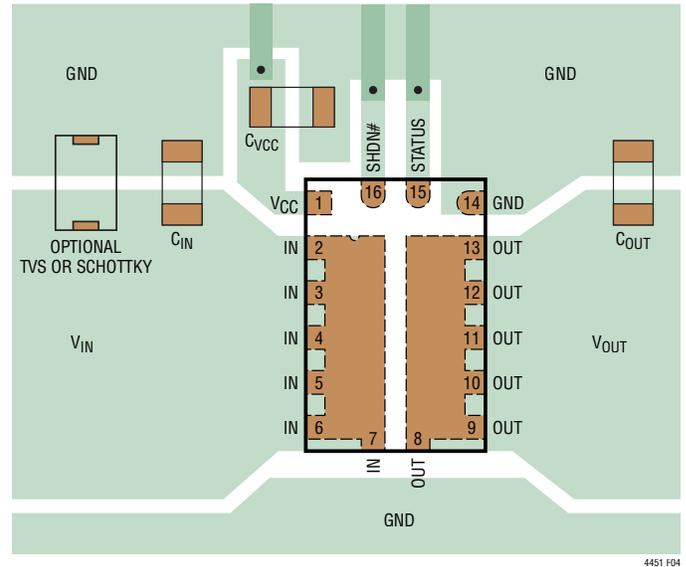


Figure 4. Recommended Layout

TYPICAL APPLICATIONS

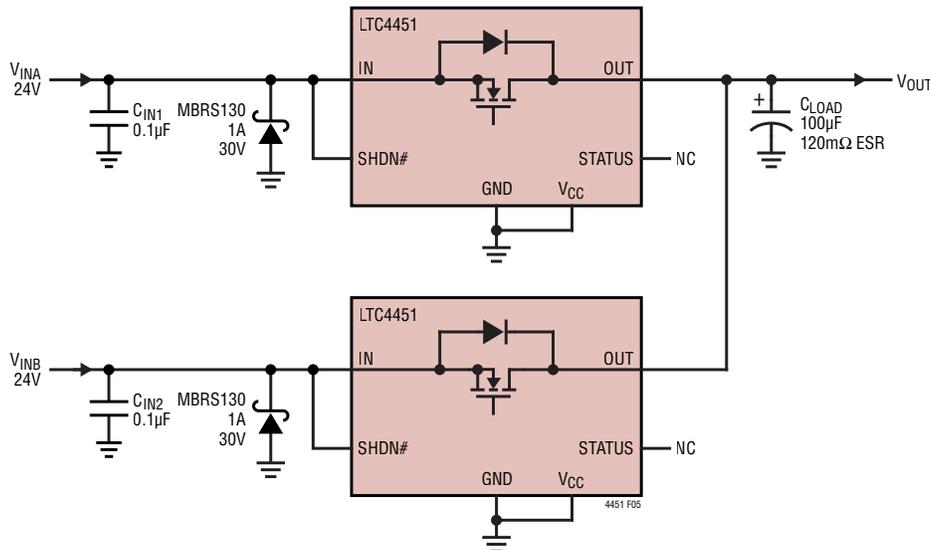


Figure 5. 24V Diode-OR with Reverse Recovery Protection

TYPICAL APPLICATIONS

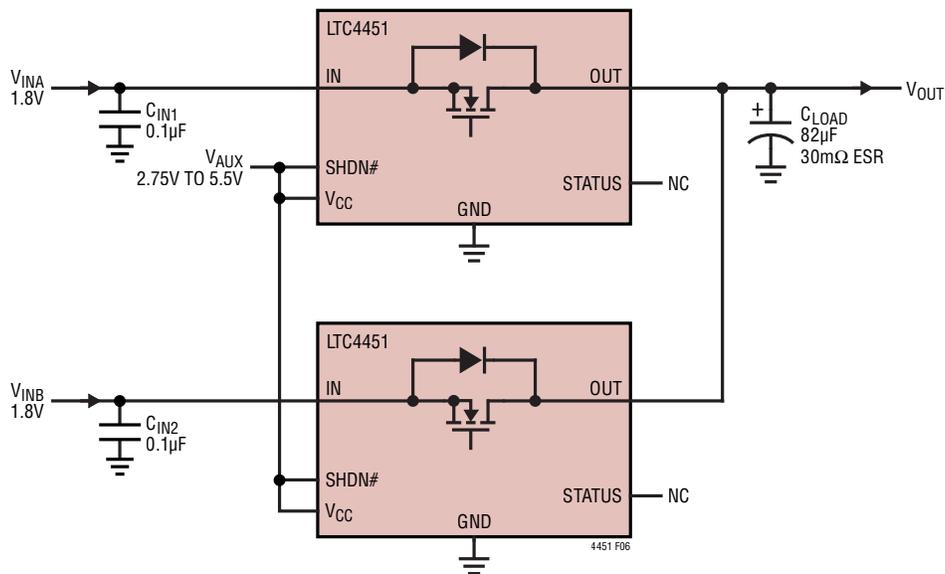


Figure 6. 1.2V Diode-OR Using Auxiliary Supply to V_{CC} for Low Voltage Operation

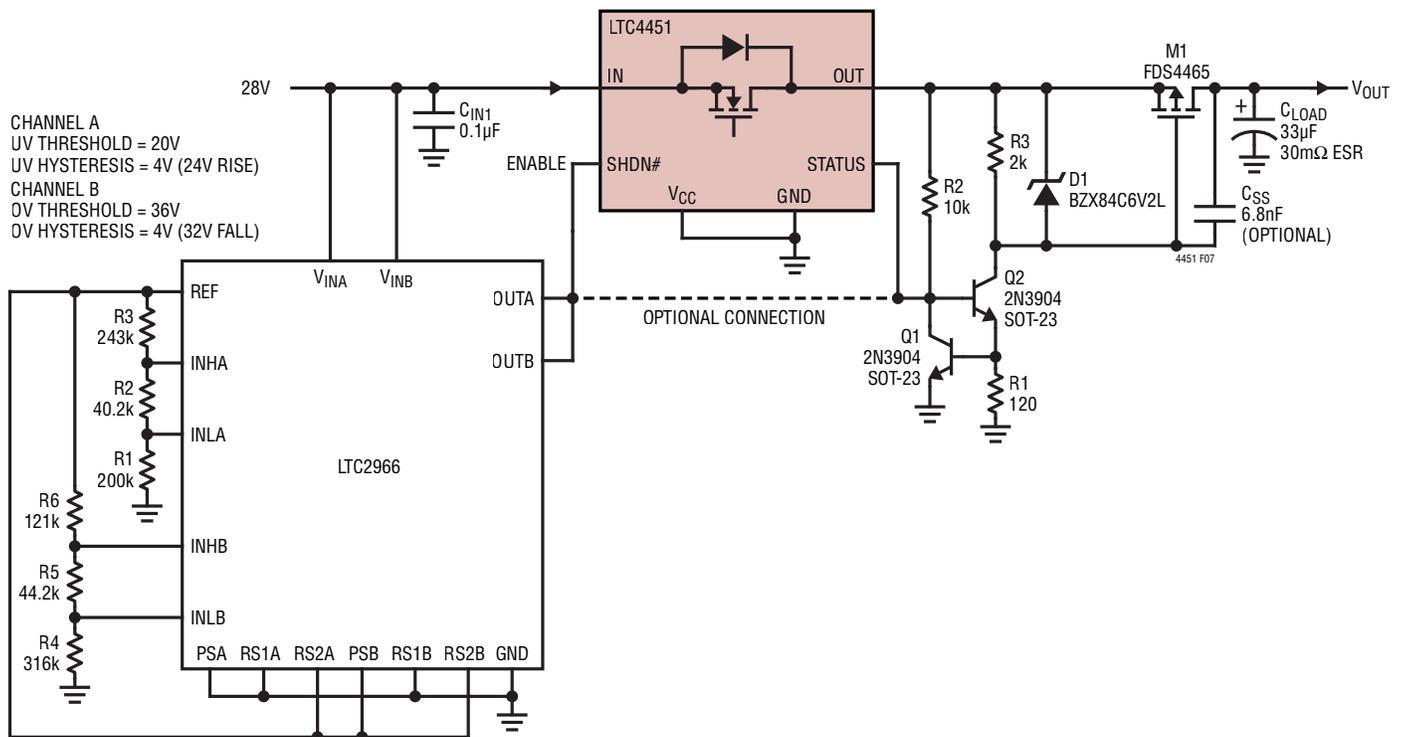


Figure 7. 28V Output Disconnect Switch Controlled by LTC2966

TYPICAL APPLICATIONS

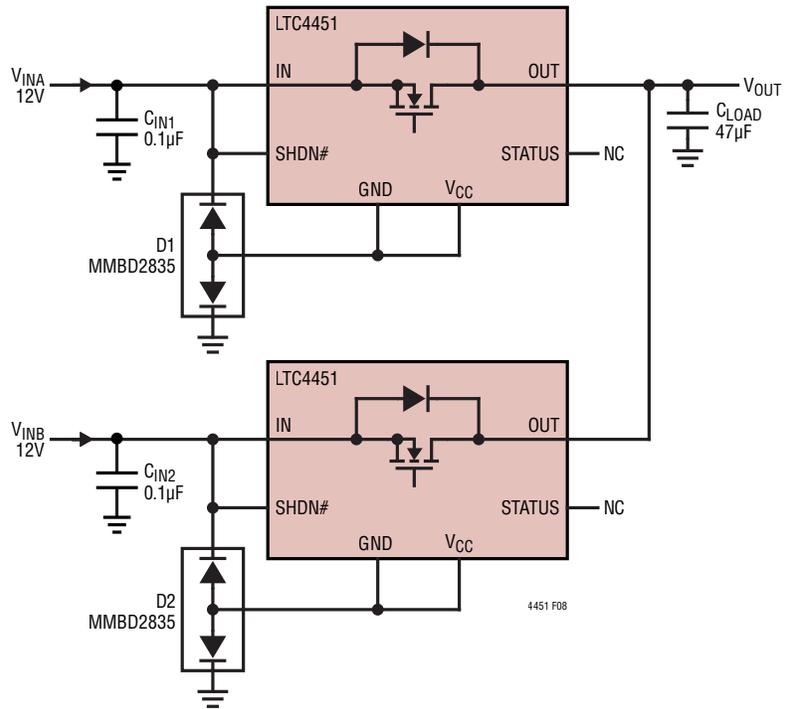
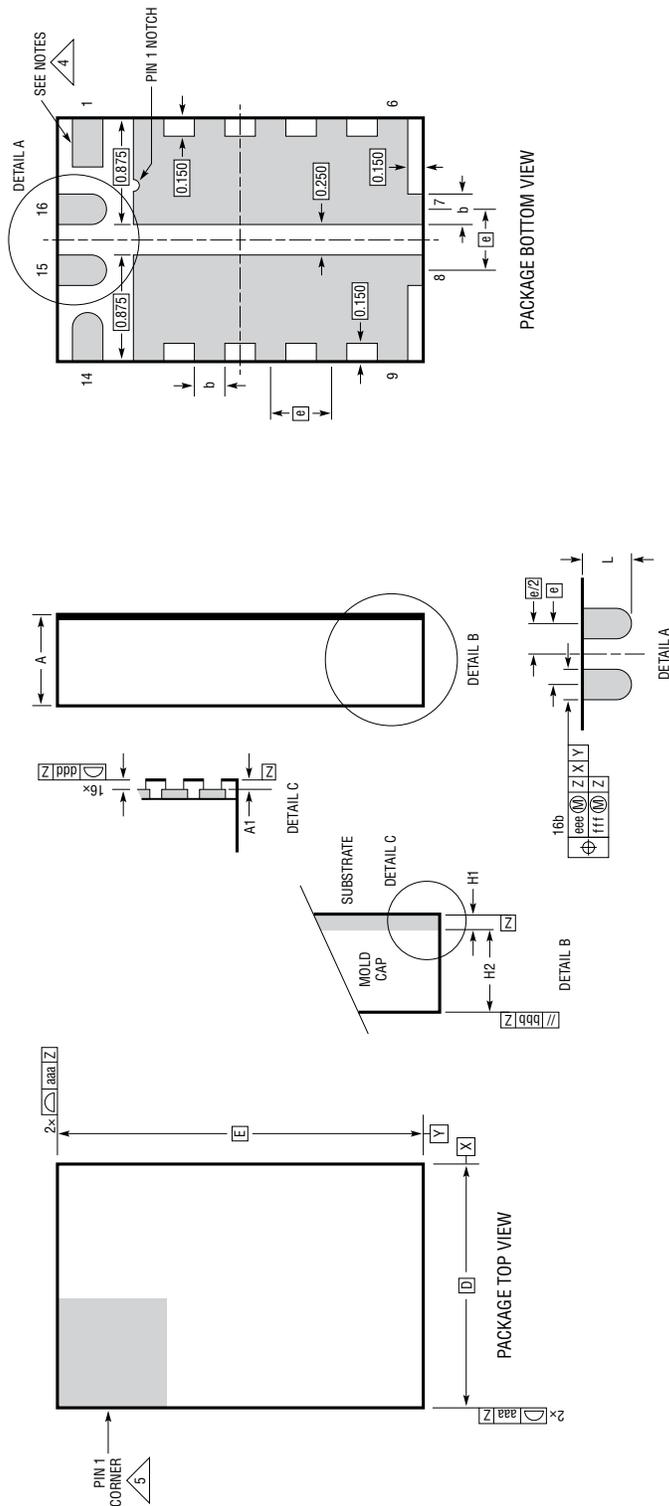


Figure 8. 12V Diode-OR with Reverse Input Voltage Protection

PACKAGE DESCRIPTION

LQFN Package
16-Lead (2mm × 3mm × 0.75mm)
 (Reference LTC DWG # 05-08-1683 Rev 0)



- NOTES:**
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 2. ALL DIMENSIONS ARE IN MILLIMETERS
 3. PRIMARY DATUM -Z- IS SEATING PLANE
 4. METAL FEATURES UNDER THE SOLDER MASK OPENING NOT SHOWN SO AS NOT TO OBSCURE THESE TERMINALS AND HEAT FEATURES
 5. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE

DIMENSIONS			
SYMBOL	MIN	NOM	MAX
A	0.65	0.75	0.85
A1	0.01	0.02	0.03
L	0.30	0.40	0.50
b	0.22	0.25	0.28
D		2.00	
E		3.00	
e		0.50	
H1		0.25 REF	
H2		0.50 REF	
aaa		0.10	SUBSTRATE THK
bbb		0.10	MOLD CAP HT
ddd		0.10	
eee		0.15	
fff		0.08	

The **SUGGESTED PCB LAYOUT TOP VIEW** shows the footprint of the package with dimensions: 3.50 ± 0.05 (width), 2.50 ± 0.05 (length), and lead dimensions including 0.70 , 1.250 , 0.750 , 0.150 , 0.250 , 0.000 , 0.250 , 0.750 , 1.250 , 0.25 , 0.875 , 0.150 , and 0.250 .

LDRN 16 1118 REV 0

