

# Linear LED Driver, 24-Channel, Bus Controlled

## LV52511MNZ

### Overview

The LV52511MN is a serial bus controlled linear low side driver for LEDs (or other loads). The 24 channels are grouped in 3 color blocks (RGB) of 8 channels each. The ON-time for each channel can be programmed by an 8bit register. The reference current is programmed by a single resistor, a 5bit register defines the current for each color block as a fraction (3 to 100%) of the reference current to adjust for color temperature.

Systems parameters can be programmed via 2 wire serial bus, or 3 wire SPI bus with EN, and I<sup>2</sup>C serial bus format (Hs-mode).

### Features

- LED Supply from 3 V to 41 V with Transient Tolerance up to 42 V
- System Supply from 3 V to 20 V with Transient Tolerance up to 24 V
- Up to 60 mA Resistor Defined Maximum Current for All Channels
- 5 bit Individually Adjustable Current for each Color Group RGB
- 8 bit Luminance Dimming for each Channel
- 2 or 3 Wire Bus Interface with up to 56 Slave Addresses
- Thermal and Undervoltage Lock-out Protection
- Thermally Efficient Exposed Die 48 pin QFN Package for Operation up to 85°C Ambient
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

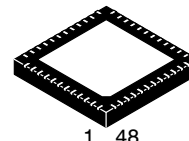
### Typical Applications

- Gaming (Slot Machine) and Entertainment Equipment
- LED Displays
- Digital Information Signs



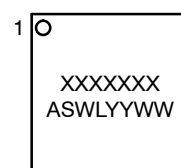
ON Semiconductor®

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QFN48 7x7  
CASE 485EB

### MARKING DIAGRAM



XXX = Specific Device Code  
AS = Assembly Location Code  
WL = Wafer Lot Code  
YY = Year  
WW = Work Week

### ORDERING INFORMATION

| Device        | Package                             | Shipping <sup>†</sup>  |
|---------------|-------------------------------------|------------------------|
| LV52511MNZTXG | QFN48<br>(Pb-Free/<br>Halogen Free) | 2,500 /<br>Tape & Reel |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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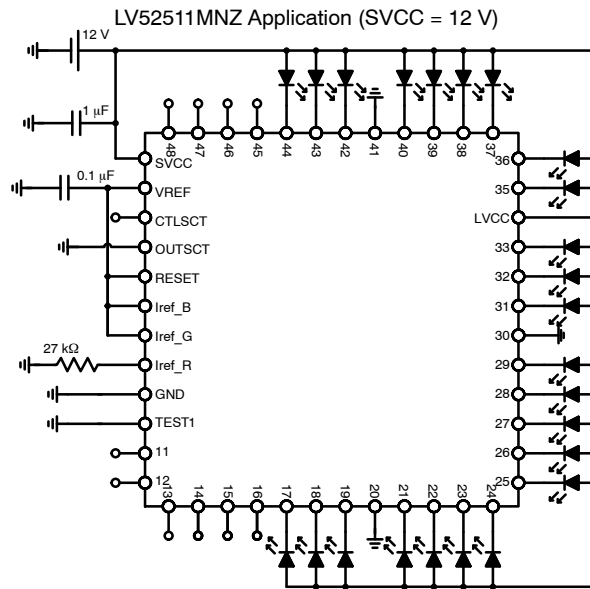


Figure 1. Typical Application Diagram

## PINOUT

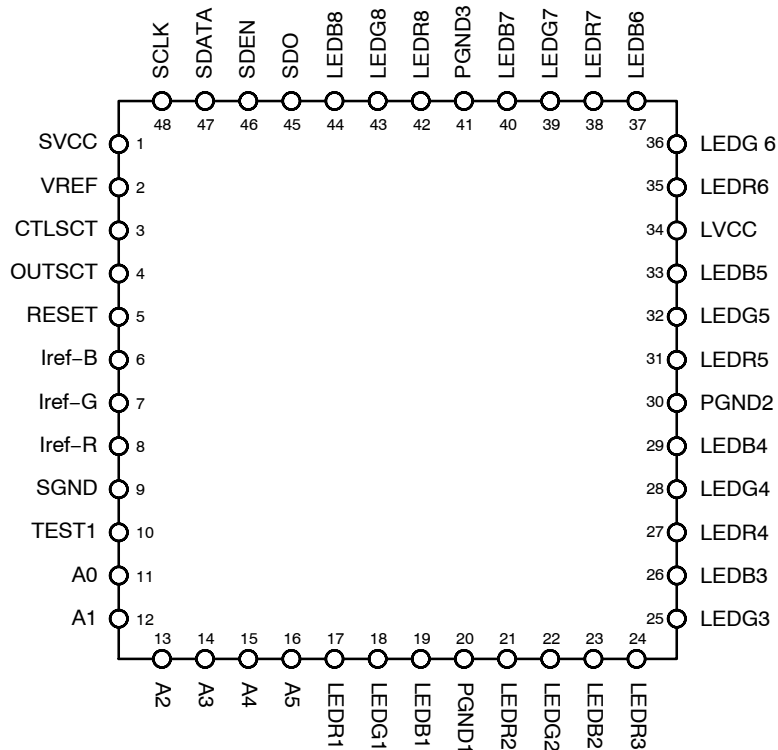


Figure 2. Pin Assignment

# LV52511MNZ

## PIN DESCRIPTIONS

| Pin No. | Pin Name | I/O | Description                                                                                                                                                                                              | Pin Circuit |
|---------|----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| 1       | SVCC     | –   | System power supply input. For LED supply voltages from 3 to 20 V connect directly to LED supply. For higher LED voltages SVCC must be limited to 24 V (max)                                             |             |
| 2       | VREF     | O   | Internal supply output pin. Regulates to 5 V if SVCC is higher than 5 V. Bypass with a 0.1 $\mu$ F capacitor                                                                                             |             |
| 3       | CTLSCT   | I   | Select pin for 2-wire or 3-wire interface and I <sup>2</sup> C. Tie to GND for 3-wire, tie to VREF for 2-wire bus, open for I <sup>2</sup> C bus                                                         | TYPE 1      |
| 4       | OUTSCT   | I   | Analog three level selection pin to set current characteristics for the output channels. See “OUTSCT Setting” on page 10 for details                                                                     | TYPE 1      |
| 5       | RESET    | I   | Active high reset input pin. Clears all register settings. Power on reset connect with VREF.                                                                                                             | TYPE 2      |
| 6       | Iref_B   | O   | Maximum reference current programming pin. Connect a resistor > 10 k $\Omega$ from this pin to GND to define maximum LED current according to the following formula:<br>$I_{REF} = 1.2 \times 580 / R_T$ | TYPE 3      |
| 7       | Iref_G   | O   | Maximum reference current programming pin. Connect a resistor > 10 k $\Omega$ from this pin to GND to define maximum LED current according to the following formula:<br>$I_{REF} = 1.2 \times 580 / R_T$ | TYPE 3      |
| 8       | Iref_R   | O   | Maximum reference current programming pin. Connect a resistor > 10 k $\Omega$ from this pin to GND to define maximum LED current according to the following formula:<br>$I_{REF} = 1.2 \times 580 / R_T$ | TYPE 3      |
| 9       | SGND     | –   | Analog circuit GND pin                                                                                                                                                                                   |             |
| 10      | TEST1    | I   | Test1 pin (connected to GND)                                                                                                                                                                             | TYPE 4      |
| 11–16   | A0–A5    | I   | Slave address setting pin. Refer to “Slave Address Setting” on page 11 for details                                                                                                                       | TYPE 5      |
| 17      | LEDR1    | O   | LED red 1 current output pin                                                                                                                                                                             | TYPE 6      |
| 18      | LEDG1    | O   | LED green 1 current output pin                                                                                                                                                                           | TYPE 6      |
| 19      | LEDB1    | O   | LED blue 1 current output pin                                                                                                                                                                            | TYPE 6      |
| 20      | PGND1    | –   | GND pin dedicated for LED driver. Connect directly to ground plane                                                                                                                                       |             |
| 21      | LEDR2    | O   | LED red 2 current output pin                                                                                                                                                                             | TYPE 6      |
| 22      | LEDG2    | O   | LED green 2 current output pin                                                                                                                                                                           | TYPE 6      |
| 23      | LEDB2    | O   | LED blue 2 current output pin                                                                                                                                                                            | TYPE 6      |
| 24      | LEDR3    | O   | LED red 3 current output pin                                                                                                                                                                             | TYPE 6      |
| 25      | LEDG3    | O   | LED green 3 current output pin                                                                                                                                                                           | TYPE 6      |
| 26      | LEDB3    | O   | LED blue 3 current output pin                                                                                                                                                                            | TYPE 6      |
| 27      | LEDR4    | O   | LED red 4 current output pin                                                                                                                                                                             | TYPE 6      |
| 28      | LEDG4    | O   | LED green 4 current output pin                                                                                                                                                                           | TYPE 6      |
| 29      | LEDB4    | O   | LED blue 4 current output pin                                                                                                                                                                            | TYPE 6      |
| 30      | PGND2    | –   | GND pin dedicated for LED driver. Connect directly to ground plane                                                                                                                                       |             |
| 31      | LEDR5    | O   | LED red 5 current output pin                                                                                                                                                                             | TYPE 6      |
| 32      | LEDG5    | O   | LED green 5 current output pin                                                                                                                                                                           | TYPE 6      |
| 33      | LEDB5    | O   | LED blue 5 current output pin                                                                                                                                                                            | TYPE 6      |
| 34      | LVCC     | –   | Protection for LED drivers. For higher LED voltages. LVCC must be limited to 42.0 V (max)                                                                                                                |             |
| 35      | LEDR6    | O   | LED red 6 current output pin                                                                                                                                                                             | TYPE 6      |
| 36      | LEDG6    | O   | LED green 6 current output pin                                                                                                                                                                           | TYPE 6      |

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## PIN DESCRIPTIONS (continued)

| Pin No. | Pin Name    | I/O | Description                                                                                                                                    | Pin Circuit |
|---------|-------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| 37      | LEDB6       | O   | LED blue 6 current output pin                                                                                                                  | TYPE 6      |
| 38      | LEDR7       | O   | LED red 7 current output pin                                                                                                                   | TYPE 6      |
| 39      | LEDG7       | O   | LED green 7 current output pin                                                                                                                 | TYPE 6      |
| 40      | LEDB7       | O   | LED blue 7 current output pin                                                                                                                  | TYPE 6      |
| 41      | PGND3       | –   | GND pin dedicated for LED driver. Connect directly to ground plane                                                                             |             |
| 42      | LEDR8       | O   | LED red 8 current output pin                                                                                                                   | TYPE 6      |
| 43      | LEDG8       | O   | LED green 8 current output pin                                                                                                                 | TYPE 6      |
| 44      | LEDB8       | O   | LED blue 8 current output pin                                                                                                                  | TYPE 6      |
| 45      | SDO         | O   | Serial interface output pin.                                                                                                                   | TYPE 7      |
| 46      | SDEN        | I   | Active high, 3-wire SPI Mode enable signal.<br>Must go low after each SPI frame. Not used for 2 wire interface                                 | TYPE 8      |
| 47      | SDATA       | I/O | Serial interface data input / output pin.<br>Data frame consists of:<br>Slave_Address[7:0] – Register_Address[7:0] – Data1[7:0] ... DataN[7:0] | TYPE 9      |
| 48      | SCLK        | I   | Serial interface clock signal input pin.<br>Data is latched at the rising clock edge                                                           | TYPE 10     |
|         | Exposed PAD |     | Connected to ground plane                                                                                                                      |             |

## PIN CIRCUIT

|                       |                      |                      |
|-----------------------|----------------------|----------------------|
| <p><b>TYPE 1</b></p>  | <p><b>TYPE 2</b></p> | <p><b>TYPE 3</b></p> |
| <p><b>TYPE 4</b></p>  | <p><b>TYPE 5</b></p> | <p><b>TYPE 6</b></p> |
| <p><b>TYPE 7</b></p>  | <p><b>TYPE 8</b></p> | <p><b>TYPE 9</b></p> |
| <p><b>TYPE 10</b></p> |                      |                      |

# LV52511MNZ

## SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS (Note 2)

| Symbol              | Parameter                      | Conditions                     | Ratings     | Unit |
|---------------------|--------------------------------|--------------------------------|-------------|------|
| V <sub>CC</sub> max | Maximum Supply Voltage         |                                | 24          | V    |
| V <sub>LED</sub>    |                                |                                | 42          | V    |
| V <sub>REF</sub>    |                                |                                | 5.8         | V    |
| V <sub>O</sub> max  | Output Voltage                 | LED off                        | 42          | V    |
| I <sub>O</sub> max  | Output Current                 | SVCC = 5.0 to 20 V             | 60/80       | mA   |
| I <sub>O</sub> max  | Output Current                 | SVCC = 3.0 to 5 V              | 30/80       | mA   |
| P <sub>d</sub> max  | Allowable Power Dissipation    | T <sub>A</sub> ≤ 25°C (Note 1) | 4.15        | W    |
| T <sub>opr</sub>    | Operating Temperature          |                                | -25 to +85  | °C   |
| T <sub>j</sub>      | Operating Junction Temperature |                                | -25 to +150 | °C   |
| T <sub>stg</sub>    | Storage Temperature            |                                | -40 to +150 | °C   |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Specified board: 110 mm × 90 mm × 1.6 mm, glass epoxy board. Exposed Die-pad area is not a substrate mounting.
2. If you should intend to use this IC continuously under high temperature, high current, high voltage, or drastic temperature change, even if it is used within the range of absolute maximum ratings or operating conditions, there is a possibility of decrease reliability. Please contact us for a confirmation.

### RECOMMENDED OPERATING CONDITIONS

| Symbol              | Parameter                      | Conditions | Ratings    | Unit |
|---------------------|--------------------------------|------------|------------|------|
| V <sub>CC</sub> op  | Operating Supply Voltage Range | SVCC       | 3.0 to 20  | V    |
| V <sub>LED</sub> op |                                | LVCC       | 3.0 to 41  | V    |
| V <sub>REF</sub> op |                                | VREF       | 3.0 to 5.5 | V    |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

### ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C, 3.3 V < SVCC < 20 V)

| Symbol           | Parameter                     | Conditions                                                   | Min   | Typ   | Max   | Unit |
|------------------|-------------------------------|--------------------------------------------------------------|-------|-------|-------|------|
| I <sub>CC1</sub> | Supply Current1               | SVCC = 12 V/RESET = H LED OFF                                | 1.2   | 1.9   | 2.6   | mA   |
| I <sub>CC2</sub> | Supply Current2               | SVCC = 12 V/RESET = H LED OFF SCLK = 5 MHz                   | 1.8   | 3.0   | 4.2   | mA   |
| IMAX1R           | LED Driver Output Current Rch | I <sub>ref-R</sub> = 27 kΩ, OUTSCT = L                       | 24.25 | 25.80 | 27.35 | mA   |
| IMAX1G           | LED Driver Output Current Gch | I <sub>ref-G</sub> = 27 kΩ, OUTSCT = L                       | 24.25 | 25.80 | 27.35 | mA   |
| IMAX1B           | LED Driver Output Current Bch | I <sub>ref-B</sub> = 27 kΩ, OUTSCT = L                       | 24.25 | 25.80 | 27.35 | mA   |
| ΔIL              | Line Regulation               | V <sub>O</sub> = 0.7 to 4.0 V (Same channel line regulation) | -5    | -     | -     | %    |
| Ron1             | LED Output on Resistance 1    | I <sub>O</sub> = 10 mA                                       | -     | 10    | 20    | Ω    |
| Ileak            | OFF Leak Current              | LED OFF                                                      | -     | -     | 1     | μA   |
| VPOR             | VCC Power on RESET Voltage    | POR release voltage threshold                                | -     | 2.5   | -     | V    |
| VRST             |                               | Undervoltage lockout threshold                               | -     | 2.3   | -     | V    |
| VREF1            | VREF Voltage                  | SVCC = 12 V, I <sub>O</sub> = 30 mA                          | 4.8   | 5.1   | 5.4   | V    |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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### CONTROL CIRCUIT (T<sub>A</sub> = 25°C, SVCC = 5.0 to 20 V)

| Symbol | Parameter | Conditions                      | Min | Typ | Max | Unit |
|--------|-----------|---------------------------------|-----|-----|-----|------|
| VH1    | H Level 1 | Input H level OUTSCT/CTLSCT     | 4.5 | –   | 5.0 | V    |
| VM1    | M Level 1 | Input M level OUTSCT/CTLSCT     | 1.8 | –   | 3.0 | V    |
| VL1    | L Level 1 | Input L level OUTSCT/CTLSCT     | 0   | –   | 0.5 | V    |
| VH2    | H Level 2 | Input H level RESET             | 4.0 | –   | 5.0 | V    |
| VL2    | L Level 2 | Input L level RESET             | 0   | –   | 1.0 | V    |
| VH3    | H Level 3 | Input H level A0 to A5          | 3.5 | –   | 5.0 | V    |
| VL3    | L Level 3 | Input L level A0 to A5          | 0   | –   | 0.5 | V    |
| VH4    | H Level 4 | Input H level SCLK, SDATA, SDEN | 4.0 | –   | 5.0 | V    |
| VL4    | L Level 4 | Input L level SCLK, SDATA, SDEN | 0   | –   | 1.0 | V    |

### CONTROL CIRCUIT (T<sub>A</sub> = 25°C, SVCC = 3.3 V)

| Symbol | Parameter | Conditions                      | Min | Typ | Max | Unit |
|--------|-----------|---------------------------------|-----|-----|-----|------|
| VH1    | H Level 1 | Input H level OUTSCT/CTLSCT     | 2.8 | –   | 3.3 | V    |
| VM1    | M Level 1 | Input M level OUTSCT/CTLSCT     | 1.2 | –   | 1.8 | V    |
| VL1    | L Level 1 | Input L level OUTSCT/CTLSCT     | 0   | –   | 0.5 | V    |
| VH2    | H Level 2 | Input H level RESET             | 2.7 | –   | 3.3 | V    |
| VL2    | L Level 2 | Input L level RESETT            | 0   | –   | 0.6 | V    |
| VH3    | H Level 3 | Input H level A0 to A5          | 2.7 | –   | 3.3 | V    |
| VL3    | L Level 3 | Input L level A0 to A5          | 0   | –   | 0.5 | V    |
| VH4    | H Level 4 | Input H level SCLK, SDATA, SDEN | 2.7 | –   | 3.3 | V    |
| VL4    | L Level 4 | Input L level SCLK, SDATA, SDEN | 0   | –   | 0.6 | V    |

## LV52511MNZ

### SERIAL BUS TIMING CONDITIONS AT 2-WIRE SPI, AND 3-WIRE SPI

| Symbol | Parameter       | Conditions                                    | Min | Typ | Max | Unit |
|--------|-----------------|-----------------------------------------------|-----|-----|-----|------|
| ts0    | Data Setup Time | SDEN setup time relative to the rise of SCLK  | 90  | –   | –   | ns   |
| ts1    |                 | SDATA setup time relative to the rise of SCLK | 60  | –   | –   | ns   |
| th0    | Data Hold Time  | SDEN hold time relative to the fall of SCLK   | 200 | –   | –   | ns   |
| th1    |                 | SDATA hold time relative to the fall of SCLK  | 60  | –   | –   | ns   |
| tw1L   | Pulse Width     | Low period pulse width of SCLK                | 90  | –   | –   | ns   |
| tw1H   |                 | High period pulse width of SCLK               | 90  | –   | –   | ns   |
| tw2L   |                 | Low period pulse width of SDEN                | 1   | –   | –   | μs   |

### SERIAL BUS TIMING CONDITIONS AT I<sup>2</sup>C FAST-MODE PLUS

| Symbol | Parameter           | Conditions                                       | Min  | Typ | Max  | Unit |
|--------|---------------------|--------------------------------------------------|------|-----|------|------|
| fsc1   | SCL Clock Frequency | SCLK clock frequency                             | 0    | –   | 1000 | kHz  |
| ts1    | Data Setup Time     | SCL setup time relative to the rise of SDA       | 0.26 | –   | –    | μs   |
| ts2    |                     | SDA setup time relative to the rise of SCL       | 50   | –   | –    | ns   |
| ts3    |                     | SCL setup time relative to the rise of SDA       | 0.26 | –   | –    | μs   |
| th1    | Data Hold Time      | SCL hold time relative to the fall of SDA        | –    | –   | –    | μs   |
| th2    |                     | SDA hold time relative to the fall of SCL        | 0    | –   | –    | μs   |
| tw1L   | Pulse Width         | Low period pulse width of SCL                    | 0.5  | –   | –    | μs   |
| tw1H   |                     | High period pulse width of SCL                   | 0.26 | –   | –    | μs   |
| ton    | Input Signal        | Rise time of both SDA and SCL signals            | –    | –   | 120  | ns   |
| tof    |                     | Fall time of both SDA and SCL signals            | –    | –   | 120  | ns   |
| tbuf   | Bus Free Time       | Bus free time between a STOP and START condition | 0.5  | –   | –    | μs   |

### SERIAL BUS TIMING CONDITIONS AT I<sup>2</sup>C Hs-MODE

| Symbol | Parameter           | Conditions                                 | Min | Typ | Max | Unit |
|--------|---------------------|--------------------------------------------|-----|-----|-----|------|
| fsc1   | SCL Clock Frequency | SCLK clock frequency                       | 0   | –   | 3.4 | MHz  |
| ts1    | Data Setup Time     | SCL setup time relative to the rise of SDA | 160 | –   | –   | ns   |
| ts2    |                     | SDA setup time relative to the rise of SCL | 10  | –   | –   | ns   |
| ts3    |                     | SCL setup time relative to the rise of SDA | 160 | –   | –   | ns   |
| th1    | Data Hold Time      | SCL hold time relative to the fall of SDA  | –   | –   | –   | ns   |
| th2    |                     | SDA hold time relative to the fall of SCL  | 0   | –   | 70  | ns   |
| tw1L   | Pulse Width         | Low period pulse width of SCL              | 160 | –   | –   | ns   |
| tw1H   |                     | High period pulse width of SCL             | 60  | –   | –   | ns   |
| tcon   | Input Signal        | Rise time of SCL signals                   | 10  | –   | 40  | ns   |
| tcof   |                     | Fall time of SCL signals                   | 10  | –   | 40  | ns   |
| tdon   |                     | Rise time of SDA signals                   | 10  | –   | 80  | ns   |
| Tdof   |                     | Fall time of SDA signals                   | 10  | –   | 80  | ns   |

The ACK sink capability of the SDA pin is equal to FASTMODE. In case of requirement up to 20 mA, an external MOSFET is needed.

DETAILED FUNCTIONAL DESCRIPTION

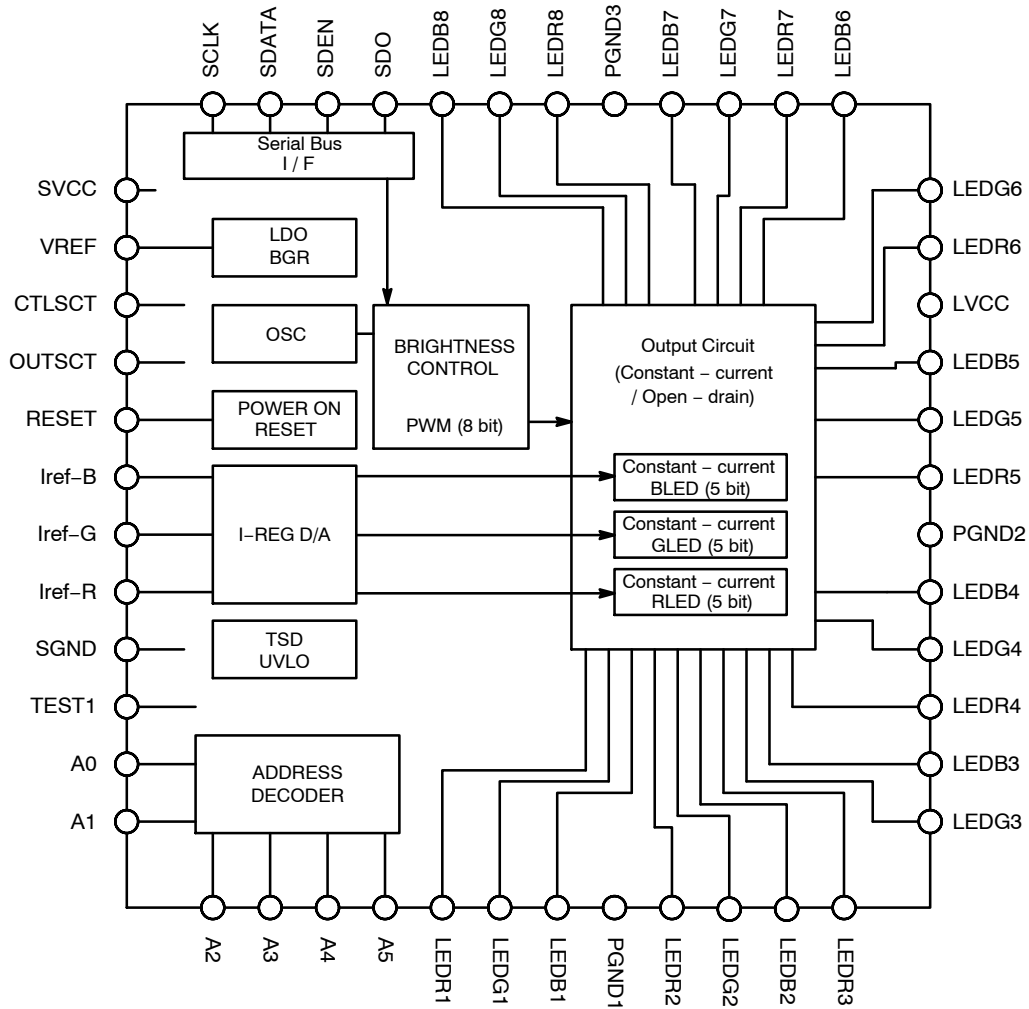


Figure 3. Block Diagram

### System Startup and Shutdown (SVCC, RESET)

The LV52511MN is supplied via SVCC. If the voltage on SVCC rises above the POR level of 2.5 V (typ) the system

setup registers are being reset to their default state, and the reference internal reference circuit at VREF starts up.

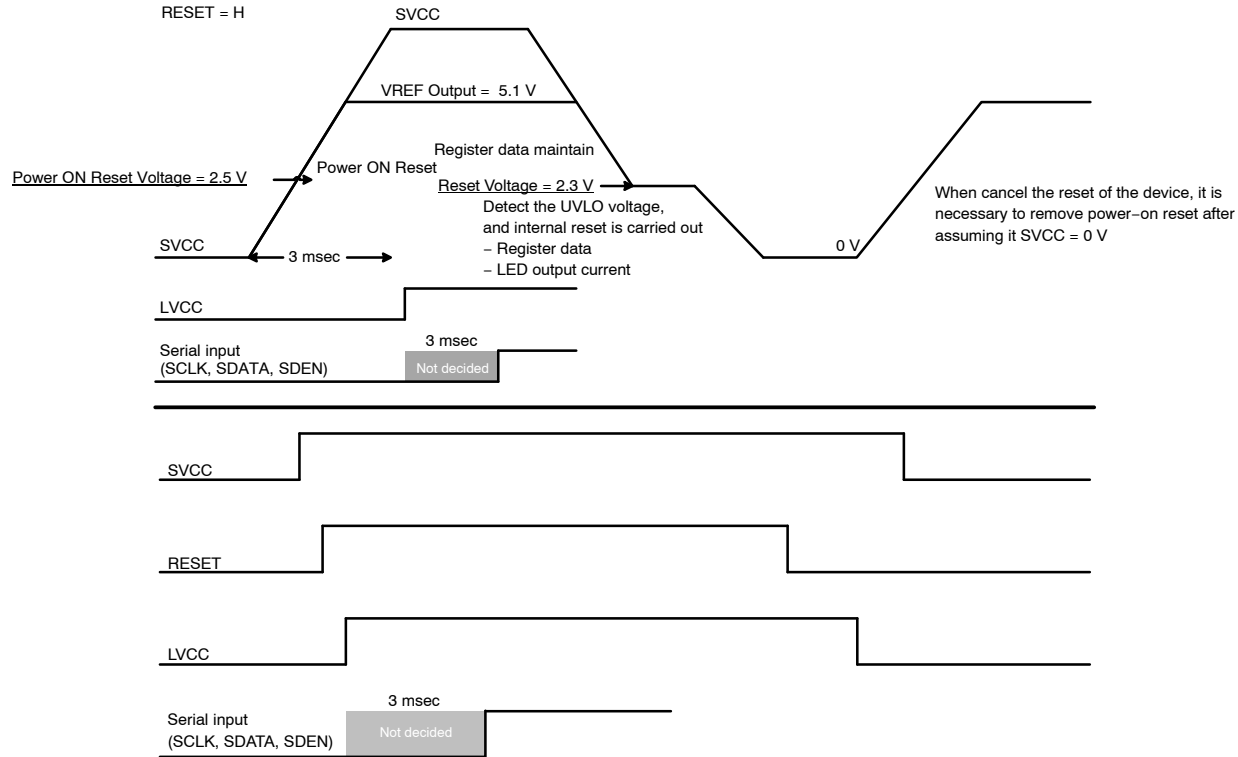


Figure 4. SVCC Startup and Shutdown

SVCC can be connected to the LED supply of the application as long as that supply is between 3 and 20 V. If the LED supply is higher than 20 V, SVCC must be supplied from a separate source.

If SVCC drops below the undervoltage lockout level of 2.3 V (typ) the system shuts down.

### Internal References (SVCC, VREF, Iref-R/G/B)

An internal voltage reference of 5 V (typ) is generated at VREF from SVCC. Do not connect external loads.

An LED reference current is defined by connecting a resistor  $R_{RT}$  between Iref-R/G/B and GND according to the formula:  $I_{MAX} = 1.2 \times 580 / R_{RT}$ . A fraction of this current (3%–100%) is applied to each LED channel.

Table 1. INTERNAL REFERENCES

| Iref-R/G/B Setting                                             | Serial Setting Pin                                                                                                                                                                                                               |
|----------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Iref-R: resistance<br>Iref-G: VREF<br>Iref-B: VREF             | The variable adjustment of the RGB electric current level by the register is possible by connecting resistance to decide a current value to only Iref-R.<br>(for 00h for 01h 02h)<br>Iref-G, Iref-B connects with VREF terminal. |
| Iref-R: resistance<br>Iref-G: resistance<br>Iref-B: resistance | The current value of RGB is fixed by connecting resistance to decide a current value to RGB unit.<br>The adjustment of the register is not possible (it becomes fixed in max)                                                    |

### LED Driver Configuration (LEDR1–8, LEDG1–8, LEDB1–8, OUTSCT)

The LEDs are connected between the system LED supply and IC channels LED\_R1–R8, LED\_G1–G8, LED\_B1–B8 such that the LED current flows into the IC. Depending on the LED drive voltage, it is possible to connect a single LED or a chain of LEDs.

The LV52511MN can adjust color temperature and brightness for up to 24 LEDs. Color temperature is adjusted by varying the LED current, and brightness (luminance) is adjusted by varying the on-time of the LED a fixed time period (duty-cycle).

#### Color Temperature Control

The 24 LED channels are organized into 3 color groups (Red, Green, Blue) of 8 channels each. The currents for each color group are programmed by a 5 bit register as

a percentage of the LED reference current  $I_{MAX}$ . Percentages of 3 to 100 are possible.

#### Luminance Control

The brightness of each LED channel is defined by the duty cycle Duty(%): the time  $t_{ON}$  the channel is active during a time window  $t_{CYCLE}$ . The duty cycle is defined by the following formula.  $Duty(\%) = 100 \times t_{ON} / t_{CYCLE}$ . Each LED channel has an 8-bit register to vary the duty cycle between OFF (0.0%) and 99.6% in steps of 0.39% each.

#### OUTSCT Settings

In addition to the settings mentioned above, it is also possible to subdivide the 8 LED channels within the color groups into 6 and 2 LED channels grouped in the following way:

**Table 2. OUTSCT SETTINGS**

| OUTSCT Level      | LED Driver Output Pin                                                                                                        |                                                                               |
|-------------------|------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------|
|                   | LEDR1–R6, LEDG1–G6, LEDB1–B6                                                                                                 | LEDR7/R8, LEDG7/G8, LEDB7/B8                                                  |
| L = -0.2 to 0.3 V | Constant current output<br>Set maximum current by built-in D/A (5 bits)<br>0.81 mA to 25.8 mA, $R_{T1} = 27 \text{ k}\Omega$ | Same as the other LEDs                                                        |
| H = 4.7 to 5.0 V  | Open drain output<br>Set current by external resistor<br>$R_{ON} = 10 \Omega$                                                | Same as the other LEDs                                                        |
| M = 1.8 to 3.0 V  | Constant current output<br>Set maximum current by built-in D/A (5 bits)<br>0.81 mA to 25.8 mA, $R_{T1} = 27 \text{ k}\Omega$ | Open drain output<br>Set current by external resistor<br>$R_{ON} = 10 \Omega$ |

### Thermal Considerations

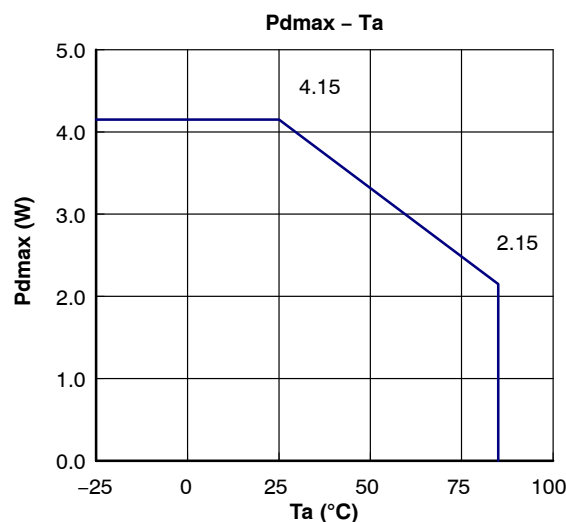
Supplying a large number of LEDs from the LV52511MN leads to a rise in chip temperature. The self-heating depends on:

- the drive current  $I_O$  flowing into the LED channel
- the voltage at the output  $V_{OUT}$  of the LED channel
- and the duty cycle  $D$  they are driven with leading to the following formula for dissipated power in each channel:

$$P_{CH} = I_O \times V_{OUT} \times D \quad (\text{eq. 1})$$

The only architecture sensitive value is  $V_{OUT}$ . It must be greater than 0.7 V (min) to allow for regulation, but also as small as possible. It is therefore advisable to connect the maximum possible number of LEDs in series to one channel.

The total power dissipation  $P_{TOT}$  of the IC is then the sum of all  $P_{CH}$  together.  $P_{TOT}$  must not exceed the power allowed by the safe operating area shown in Figure 5.



**Figure 5. Safe Operating Area**

## LV52511MNZ

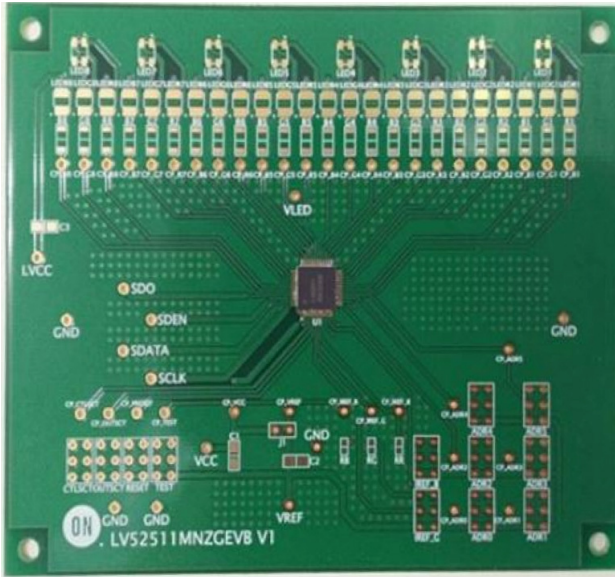


Figure 6. Board

### Over Temperature Shutoff

To protect the circuit from permanent damage or fire, overtemperature shutoff is implemented. If the junction temperature of the IC reaches 175°C, all LED outputs are turned OFF. The thermal shut down is not latched, so when the temperature falls below 130°C activity resumes.

### Serial Bus Communication (SCLK, SDATA, SDEN, CTLST)

All parameters described above are written to the LV52511MN via a single directional 2-wire or 3-wire serial bus with a clock frequency of up to 5 MHz. The bus type is defined by the state of pin CTLST (VREF = 2-wire, GND = 3-wire). Furthermore, the setting of CTLST = M supports I<sup>2</sup>C. It supports Hs-mode (3.4 MHz).

Each bus message consists of an 8bit slave (IC) address, followed by an 8bit register address, followed by one or more 8bit data words. The register address will self-increment for consecutive data words as long as the communication is valid. After the last address was written, the next data word will be written to address 00h again. For detailed information on addresses and register contents see section"

Table 3. SERIAL SETTING PIN

| CTLST Level       | Serial Setting Pin                                   |
|-------------------|------------------------------------------------------|
| L = -0.2 to 0.3 V | 3wire SPI serial bus<br>(SCLK, SDATA, SDEN) 5 MHz    |
| H = 4.7 to 5.0 V  | 2wire SPI serial bus<br>(SCLK, SDATA) 5 MHz          |
| M = 1.8 to 3.0 V  | I <sup>2</sup> C serial bus<br>(SCLK, SDATA) Hs-mode |

### Slave Address (A5–A0)

Each IC is identified by its unique slave address. The most significant two bits of the 8bit slave (IC) address are fixed to 10b. 56 Slave addresses are hardware defined by pins A0–A5 as described below.

Table 4. SLAVE ADDRESS (A5–A0)

|         | SA7 | SA6 | SA5 | SA4 | SA3 | SA2 | SA1 | SA0 |
|---------|-----|-----|-----|-----|-----|-----|-----|-----|
| ADDRESS | 1   | A5  | A4  | A3  | A2  | A1  | A0  | 0   |

| Terminal PIN (Input) |    |    |    |    |    | SLAVE ADDRESS |     |     |     |     |     |     |     |
|----------------------|----|----|----|----|----|---------------|-----|-----|-----|-----|-----|-----|-----|
| A5                   | A4 | A3 | A2 | A1 | A0 | SA7           | SA6 | SA5 | SA4 | SA3 | SA2 | SA1 | SA0 |
| L                    | L  | L  | L  | L  | L  | 1             | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| ...                  |    |    |    |    |    | 1             | A5  | A4  | A3  | A2  | A1  | A0  | 0   |
| H                    | H  | L  | H  | H  | H  | 1             | 1   | 1   | 0   | 1   | 1   | 1   | 0   |

At the time of CTLST = L, H, the SLAVE setting is possible to 56.

At the time of CTLST = M, the SLAVE setting is possible to 48.

### 3-wire Serial Bus Communication (SCLK, SDATA, and SDEN)

In 3-wire communication a frame is started with a rising edge of SDEN and terminated with a falling edge of SDEN. SCLK latches data at the rising edge. The smallest data word is 24bits long consisting of:

If the number of SCLK transitions is less than 23, Data is not latched. If it is 25 or more, the register address is automatically incremented and the next data word will be latched after eight clock cycles.

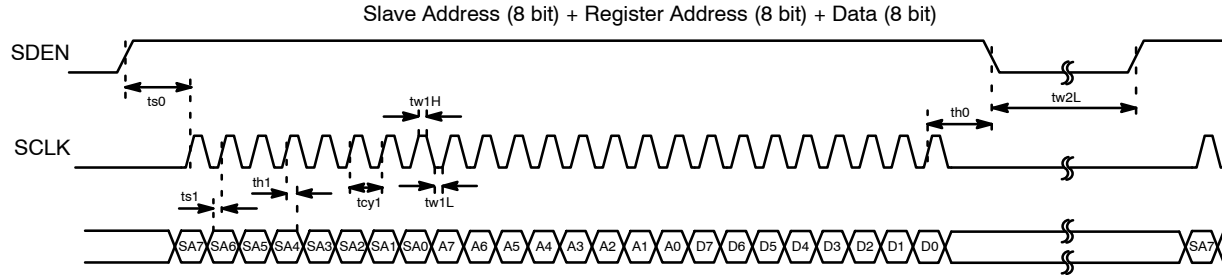


Figure 7. 3-wire Serial Data Frame

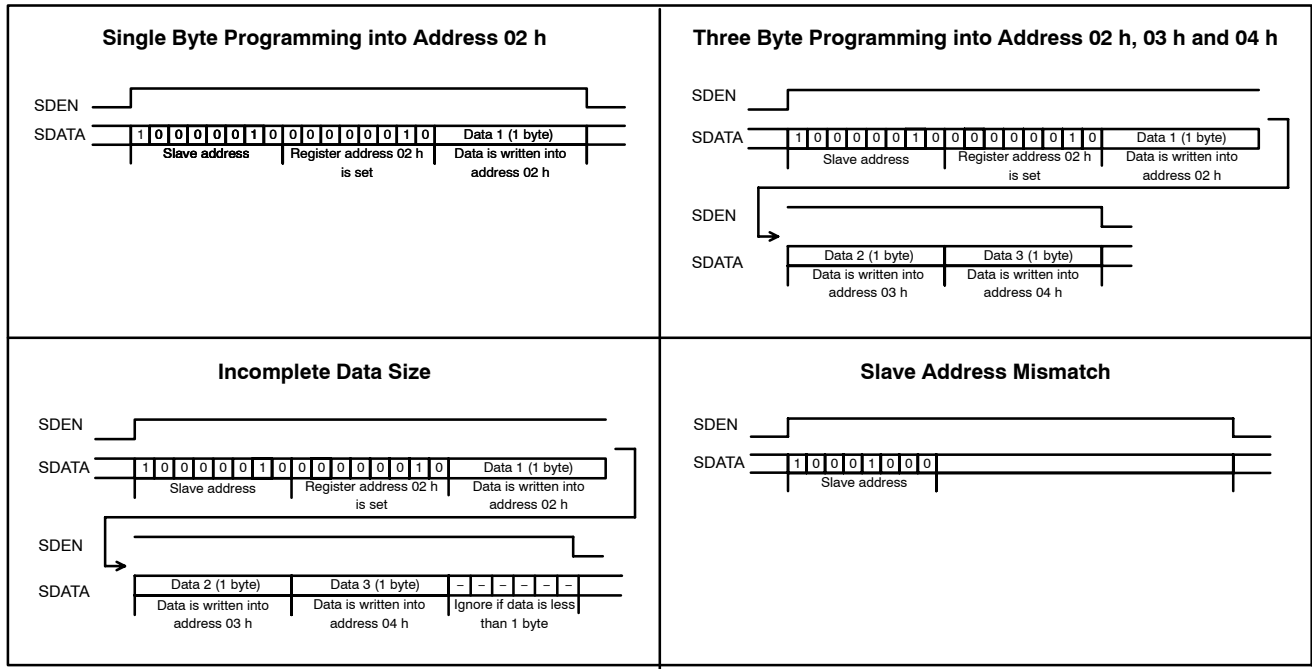


Figure 8. Data Write Examples into Slave 82h

*2-wire Serial Bus Communication (SCLK, SDATA)*

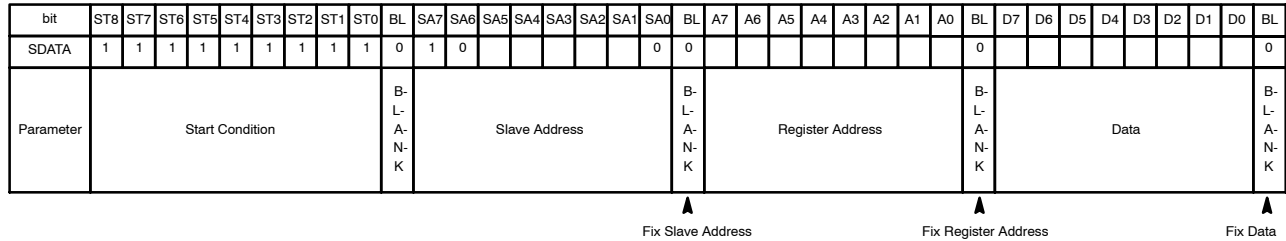
In 2-wire communication the LV52511MN watches SDATA at every rising SCLK edge. A data frame begins after START condition: nine consecutive detections of a “1” (high) followed by a “0” (BLANK). This is true even during an ongoing data transfer: serial communication will be restarted by a START condition (“11111111”) + BLANK (“0”).

After start detection, the eight bit slave address will be latched after receiving a BLANK (0h) with the ninth bit. The register address will be latched after receiving a BLANK “0”

after eight address bits. The third byte is the data byte which was addressed by the register address received before. The data byte will be latched after receiving a BLANK “0” in position nine after eight data bits.

When data bytes continue after this, the register address will be automatically incremented after each byte transfer is completed after receiving BLANK “0”.

If the BLANK after a data transfer is “1”, including slave address and register address, the single byte data just before it will not be written, and subsequent data is ignored until another START condition is detected.



**Figure 9. 2-wire Serial Communication Frame**

Minimum Data length is 37 bits:

Start condition “11111111” (9bit) + BLANK (“0”) +  
 Slave address (8bit) + BLANK (“0”) +  
 Register address (8bit) + BLANK (“0”) +  
 Data (8bit) + BLANK (“0”).

**NOTE:** When SCLK is less than 27th clocks and/or BLANK is “1” instead of “0” after start detection, will not take in SDATA. When SCLK is higher than 28th clock track, start detection is confirmed, register address is incremented every 1 byte (8bit) + BLANK (“0”).

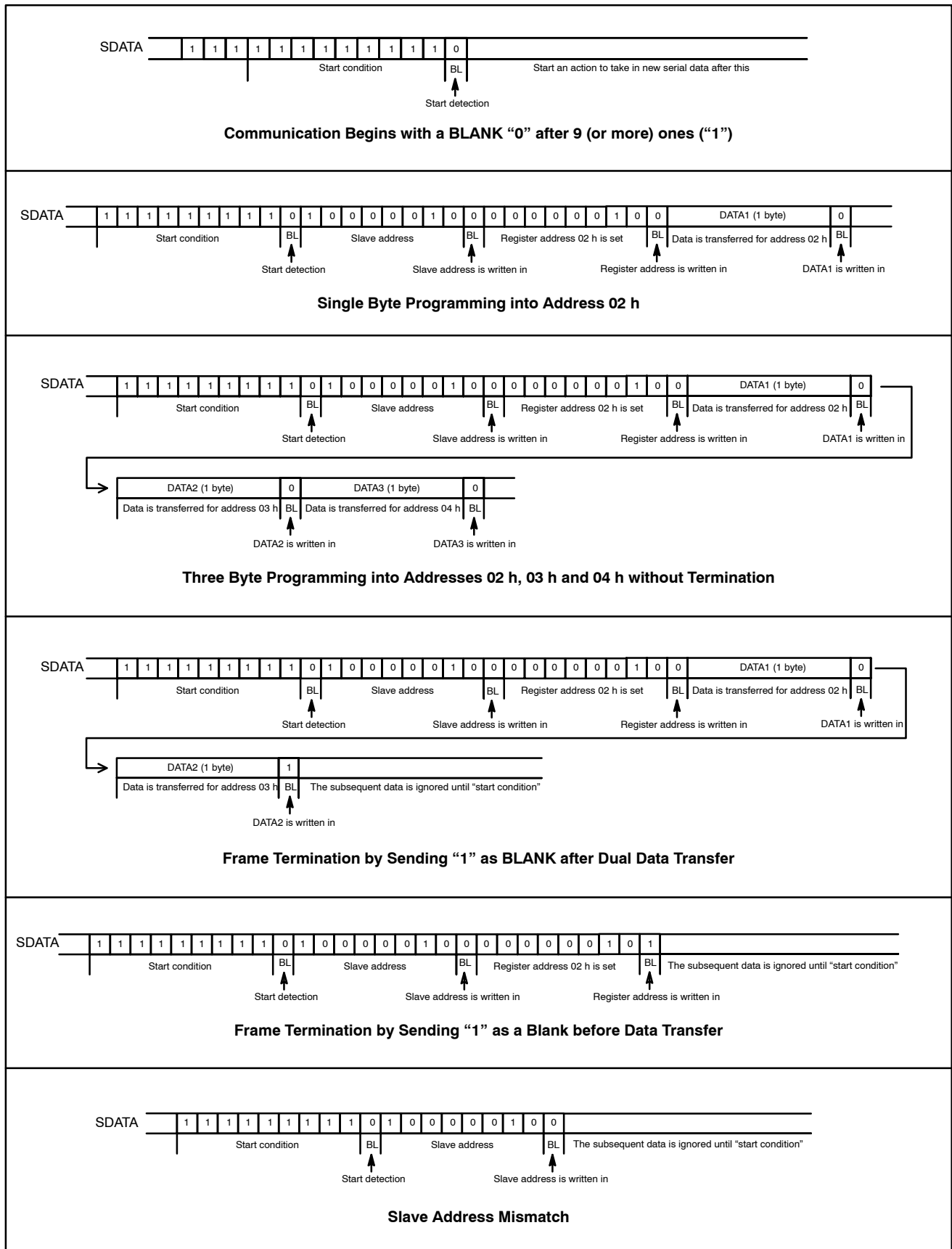


Figure 10. Data Write Examples into Slave 82h

*I<sup>2</sup>C Serial Bus Communication (SCLK, SDATA)*

In 2-wire communication, LV52511MN accepts the format corresponding to the standard of I<sup>2</sup>C.

It is Fast-mode Plus and higher-speed communicating Hs-mode.

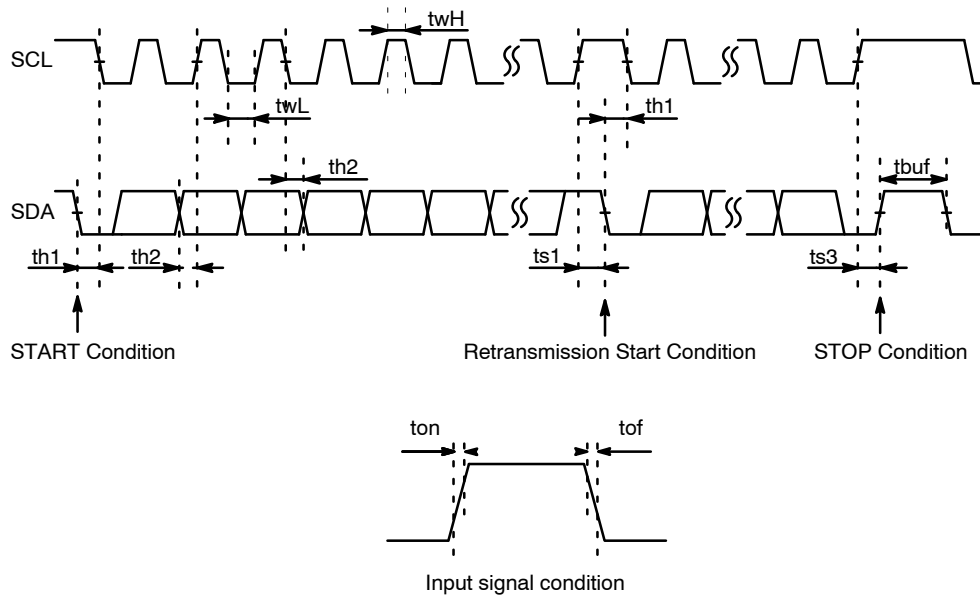


Figure 11.

As for start condition and the stop condition I<sup>2</sup>C bus, SCL has that SDA is kept between “H” by the constant state like the chart below during movement performing data transmission basically.

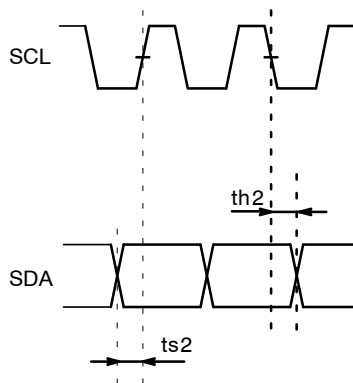


Figure 12.

The READ mode does not support.

In addition, SCL and SDA are in a condition of “H” together when data transmission is not carried out. It becomes, and, at the time of this SCL = SDA = H, access is started by a start condition when I change SDA into L from H.

When SCL changes SDA into “H” from “L” at the time of H, it becomes a stop condition and becomes the end of the access.

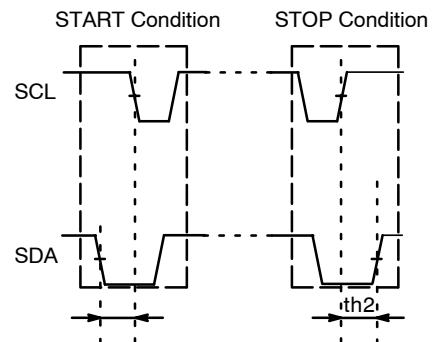


Figure 13.

## REGISTER MAP

After POR all registers are cleared.

Table 5. COLOR TEMPERATURE REGISTERS

| Addr. | Register     | D[7] | D[6] | D[5] | D[4]        | D[3] | D[2] | D[1] | D[0] | Description                        |                         |
|-------|--------------|------|------|------|-------------|------|------|------|------|------------------------------------|-------------------------|
| 00h   | LEDR Current |      |      |      | I_LEDR[4:0] |      |      |      |      | LEDR Current Setting (LEDR1~LEDR8) |                         |
|       |              | 0    | 0    | 0    | 0           | 0    | 0    | 0    | 0    | 3% of I <sub>max</sub>             | (0.81 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0           | 0    | 0    | 0    | 1    | 6% of I <sub>max</sub>             | (1.61 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0           | 0    | 0    | 1    | 0    | 9% of I <sub>max</sub>             | (2.42 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0           | 0    | 0    | 1    | 1    | 13% of I <sub>max</sub>            | (3.23 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0           | 0    | 1    | 0    | 0    | 16% of I <sub>max</sub>            | (4.03 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0           | 0    | 1    | 0    | 1    | 19% of I <sub>max</sub>            | (4.84 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0           | 0    | 1    | 1    | 0    | 22% of I <sub>max</sub>            | (5.64 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0           | 0    | 1    | 1    | 1    | 25% of I <sub>max</sub>            | (6.45 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0           | 1    | 0    | 0    | 0    | 28% of I <sub>max</sub>            | (7.26 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0           | 1    | 0    | 0    | 1    | 31% of I <sub>max</sub>            | (8.06 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0           | 1    | 0    | 1    | 0    | 34% of I <sub>max</sub>            | (8.87 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0           | 1    | 0    | 1    | 1    | 38% of I <sub>max</sub>            | (9.68 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0           | 1    | 1    | 0    | 0    | 41% of I <sub>max</sub>            | (10.48 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 0           | 1    | 1    | 0    | 1    | 44% of I <sub>max</sub>            | (11.29 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 0           | 1    | 1    | 1    | 0    | 47% of I <sub>max</sub>            | (12.09 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 0           | 1    | 1    | 1    | 1    | 50% of I <sub>max</sub>            | (12.90 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1           | 0    | 0    | 0    | 0    | 53% of I <sub>max</sub>            | (13.71 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1           | 0    | 0    | 0    | 1    | 56% of I <sub>max</sub>            | (14.51 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1           | 0    | 0    | 1    | 0    | 59% of I <sub>max</sub>            | (15.32 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1           | 0    | 0    | 1    | 1    | 63% of I <sub>max</sub>            | (16.13 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1           | 0    | 1    | 0    | 0    | 66% of I <sub>max</sub>            | (16.93 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1           | 0    | 1    | 0    | 1    | 69% of I <sub>max</sub>            | (17.74 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1           | 0    | 1    | 1    | 0    | 72% of I <sub>max</sub>            | (18.54 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1           | 0    | 1    | 1    | 1    | 75% of I <sub>max</sub>            | (19.35 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1           | 1    | 0    | 0    | 0    | 78% of I <sub>max</sub>            | (20.16 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1           | 1    | 0    | 0    | 1    | 81% of I <sub>max</sub>            | (20.96 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1           | 1    | 0    | 1    | 0    | 84% of I <sub>max</sub>            | (21.77 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1           | 1    | 0    | 1    | 1    | 88% of I <sub>max</sub>            | (22.58 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1           | 1    | 1    | 0    | 0    | 91% of I <sub>max</sub>            | (23.38 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1           | 1    | 1    | 0    | 1    | 94% of I <sub>max</sub>            | (24.19 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1           | 1    | 1    | 1    | 0    | 97% of I <sub>max</sub>            | (24.99 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1           | 1    | 1    | 1    | 1    | I <sub>max</sub>                   | (25.80 mA @ RT = 27 kΩ) |
| 01h   | LEDG Current |      |      |      | I_LEDG[4:0] |      |      |      |      | LEDG Current Setting (LEDG1~LEDG8) |                         |
|       |              | 0    | 0    | 0    | 0           | 0    | 0    | 0    | 0    | 3% of I <sub>max</sub>             | (0.81 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0           | 0    | 0    | 0    | 1    | 6% of I <sub>max</sub>             | (1.61 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0           | 0    | 0    | 1    | 0    | 9% of I <sub>max</sub>             | (2.42 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0           | 0    | 0    | 1    | 1    | 13% of I <sub>max</sub>            | (3.23 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0           | 0    | 1    | 0    | 0    | 16% of I <sub>max</sub>            | (4.03 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0           | 0    | 1    | 0    | 1    | 19% of I <sub>max</sub>            | (4.84 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0           | 0    | 1    | 1    | 0    | 22% of I <sub>max</sub>            | (5.64 mA @ RT = 27 kΩ)  |

Table 5. COLOR TEMPERATURE REGISTERS (continued)

| Addr. | Register     | D[7] | D[6] | D[5] | D[4]                     | D[3] | D[2] | D[1] | D[0] | Description                        |                         |
|-------|--------------|------|------|------|--------------------------|------|------|------|------|------------------------------------|-------------------------|
|       |              | 0    | 0    | 0    | 0                        | 0    | 1    | 1    | 1    | 25% of I <sub>max</sub>            | (6.45 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0                        | 1    | 0    | 0    | 0    | 28% of I <sub>max</sub>            | (7.26 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0                        | 1    | 0    | 0    | 1    | 31% of I <sub>max</sub>            | (8.06 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0                        | 1    | 0    | 1    | 0    | 34% of I <sub>max</sub>            | (8.87 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0                        | 1    | 0    | 1    | 1    | 38% of I <sub>max</sub>            | (9.68 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0                        | 1    | 1    | 0    | 0    | 41% of I <sub>max</sub>            | (10.48 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 0                        | 1    | 1    | 0    | 1    | 44% of I <sub>max</sub>            | (11.29 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 0                        | 1    | 1    | 1    | 0    | 47% of I <sub>max</sub>            | (12.09 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 0                        | 1    | 1    | 1    | 1    | 50% of I <sub>max</sub>            | (12.90 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1                        | 0    | 0    | 0    | 0    | 53% of I <sub>max</sub>            | (13.71 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1                        | 0    | 0    | 0    | 1    | 56% of I <sub>max</sub>            | (14.51 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1                        | 0    | 0    | 1    | 0    | 59% of I <sub>max</sub>            | (15.32 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1                        | 0    | 0    | 1    | 1    | 63% of I <sub>max</sub>            | (16.13 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1                        | 0    | 1    | 0    | 0    | 66% of I <sub>max</sub>            | (16.93 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1                        | 0    | 1    | 0    | 1    | 69% of I <sub>max</sub>            | (17.74 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1                        | 0    | 1    | 1    | 0    | 72% of I <sub>max</sub>            | (18.54 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1                        | 0    | 1    | 1    | 1    | 75% of I <sub>max</sub>            | (19.35 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1                        | 1    | 0    | 0    | 0    | 78% of I <sub>max</sub>            | (20.16 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1                        | 1    | 0    | 0    | 1    | 81% of I <sub>max</sub>            | (20.96 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1                        | 1    | 0    | 1    | 0    | 84% of I <sub>max</sub>            | (21.77 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1                        | 1    | 0    | 1    | 1    | 88% of I <sub>max</sub>            | (22.58 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1                        | 1    | 1    | 0    | 0    | 91% of I <sub>max</sub>            | (23.38 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1                        | 1    | 1    | 0    | 1    | 94% of I <sub>max</sub>            | (24.19 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1                        | 1    | 1    | 1    | 0    | 97% of I <sub>max</sub>            | (24.99 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1                        | 1    | 1    | 1    | 1    | I <sub>max</sub>                   | (25.80 mA @ RT = 27 kΩ) |
| 02h   | LEDB Current |      |      |      | I <sub>-LEDB</sub> [4:0] |      |      |      |      | LEDB Current Setting (LEDB1~LEDB8) |                         |
|       |              | 0    | 0    | 0    | 0                        | 0    | 0    | 0    | 0    | 3% of I <sub>max</sub>             | (0.81 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0                        | 0    | 0    | 0    | 1    | 6% of I <sub>max</sub>             | (1.61 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0                        | 0    | 0    | 1    | 0    | 9% of I <sub>max</sub>             | (2.42 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0                        | 0    | 0    | 1    | 1    | 13% of I <sub>max</sub>            | (3.23 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0                        | 0    | 1    | 0    | 0    | 16% of I <sub>max</sub>            | (4.03 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0                        | 0    | 1    | 0    | 1    | 19% of I <sub>max</sub>            | (4.84 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0                        | 0    | 1    | 1    | 0    | 22% of I <sub>max</sub>            | (5.64 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0                        | 0    | 1    | 1    | 1    | 25% of I <sub>max</sub>            | (6.45 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0                        | 1    | 0    | 0    | 0    | 28% of I <sub>max</sub>            | (7.26 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0                        | 1    | 0    | 0    | 1    | 31% of I <sub>max</sub>            | (8.06 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0                        | 1    | 0    | 1    | 0    | 34% of I <sub>max</sub>            | (8.87 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0                        | 1    | 0    | 1    | 1    | 38% of I <sub>max</sub>            | (9.68 mA @ RT = 27 kΩ)  |
|       |              | 0    | 0    | 0    | 0                        | 1    | 1    | 0    | 0    | 41% of I <sub>max</sub>            | (10.48 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 0                        | 1    | 1    | 0    | 1    | 44% of I <sub>max</sub>            | (11.29 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 0                        | 1    | 1    | 1    | 0    | 47% of I <sub>max</sub>            | (12.09 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 0                        | 1    | 1    | 1    | 1    | 50% of I <sub>max</sub>            | (12.90 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1                        | 0    | 0    | 0    | 0    | 53% of I <sub>max</sub>            | (13.71 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1                        | 0    | 0    | 0    | 1    | 56% of I <sub>max</sub>            | (14.51 mA @ RT = 27 kΩ) |
|       |              | 0    | 0    | 0    | 1                        | 0    | 0    | 1    | 0    | 59% of I <sub>max</sub>            | (15.32 mA @ RT = 27 kΩ) |

**Table 5. COLOR TEMPERATURE REGISTERS** (continued)

| Addr. | Register | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | Description                                        |
|-------|----------|------|------|------|------|------|------|------|------|----------------------------------------------------|
|       |          | 0    | 0    | 0    | 1    | 0    | 0    | 1    | 1    | 63% of I <sub>max</sub><br>(16.13 mA @ RT = 27 kΩ) |
|       |          | 0    | 0    | 0    | 1    | 0    | 1    | 0    | 0    | 66% of I <sub>max</sub><br>(16.93 mA @ RT = 27 kΩ) |
|       |          | 0    | 0    | 0    | 1    | 0    | 1    | 0    | 1    | 69% of I <sub>max</sub><br>(17.74 mA @ RT = 27 kΩ) |
|       |          | 0    | 0    | 0    | 1    | 0    | 1    | 1    | 0    | 72% of I <sub>max</sub><br>(18.54 mA @ RT = 27 kΩ) |
|       |          | 0    | 0    | 0    | 1    | 0    | 1    | 1    | 1    | 75% of I <sub>max</sub><br>(19.35 mA @ RT = 27 kΩ) |
|       |          | 0    | 0    | 0    | 1    | 1    | 0    | 0    | 0    | 78% of I <sub>max</sub><br>(20.16 mA @ RT = 27 kΩ) |
|       |          | 0    | 0    | 0    | 1    | 1    | 0    | 0    | 1    | 81% of I <sub>max</sub><br>(20.96 mA @ RT = 27 kΩ) |
|       |          | 0    | 0    | 0    | 1    | 1    | 0    | 1    | 0    | 84% of I <sub>max</sub><br>(21.77 mA @ RT = 27 kΩ) |
|       |          | 0    | 0    | 0    | 1    | 1    | 0    | 1    | 1    | 88% of I <sub>max</sub><br>(22.58 mA @ RT = 27 kΩ) |
|       |          | 0    | 0    | 0    | 1    | 1    | 1    | 0    | 0    | 91% of I <sub>max</sub><br>(23.38 mA @ RT = 27 kΩ) |
|       |          | 0    | 0    | 0    | 1    | 1    | 1    | 0    | 1    | 94% of I <sub>max</sub><br>(24.19 mA @ RT = 27 kΩ) |
|       |          | 0    | 0    | 0    | 1    | 1    | 1    | 1    | 0    | 97% of I <sub>max</sub><br>(24.99 mA @ RT = 27 kΩ) |
|       |          | 0    | 0    | 0    | 1    | 1    | 1    | 1    | 1    | I <sub>max</sub><br>(25.80 mA @ RT = 27 kΩ)        |

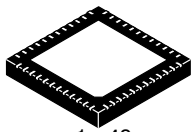
**Table 6. LUMINANCE REGISTERS**

| Addr. | Register     | D[7]    | D[6]   | D[5]   | D[4]   | D[3]   | D[2]   | D[1]   | D[0]   | Description                           |
|-------|--------------|---------|--------|--------|--------|--------|--------|--------|--------|---------------------------------------|
| 03h   | PWM SEL LEDR | R8      | R7     | R6     | R5     | R4     | R3     | R2     | R1     | Select PWM or Full on for LEDR1~LEDR8 |
|       |              | 0<br>1  | 0<br>1 | 0<br>1 | 0<br>1 | 0<br>1 | 0<br>1 | 0<br>1 | 0<br>1 | 0: PWM mode<br>1: Full on (100% PWM)  |
| 04h   | PWM SEL LEDG | G8      | G7     | G6     | G5     | G4     | G3     | G2     | G1     | Select PWM or Full on for LEDG1~LEDG8 |
|       |              | 0<br>1  | 0<br>1 | 0<br>1 | 0<br>1 | 0<br>1 | 0<br>1 | 0<br>1 | 0<br>1 | 0: PWM mode<br>1: Full on (100% PWM)  |
| 05h   | PWM SEL LEDB | B8      | B7     | B6     | B5     | B4     | B3     | B2     | B1     | Select PWM or Full on for LEDB1~LEDB8 |
|       |              | 0<br>1  | 0<br>1 | 0<br>1 | 0<br>1 | 0<br>1 | 0<br>1 | 0<br>1 | 0<br>1 | 0: PWM mode<br>1: Full on (100% PWM)  |
| 06h   | LEDR1 Duty   | R1[7]   | R1[6]  | R1[5]  | R1[4]  | R1[3]  | R1[2]  | R1[1]  | R1[0]  | PWM duty setting for LEDR1            |
|       |              | 0       | 0      | 0      | 0      | 0      | 0      | 0      | 0      | Duty(%) = 0.0%                        |
|       |              | R1[7:0] |        |        |        |        |        |        |        | Duty(%) = R1[7:0] / 256               |
|       |              | 1       | 1      | 1      | 1      | 1      | 1      | 1      | 1      | Duty(%) = 99.6%                       |
| 07h   | LEDG1 Duty   | G1[7:0] |        |        |        |        |        |        |        | Duty(%) = G1[7:0] / 256               |
| 08h   | LEDB1 Duty   | B1[7:0] |        |        |        |        |        |        |        | Duty(%) = B1[7:0] / 256               |
| 09h   | LEDR2 Duty   | R2[7:0] |        |        |        |        |        |        |        | Duty(%) = R2[7:0] / 256               |
| 0ah   | LEDG2 Duty   | G2[7:0] |        |        |        |        |        |        |        | Duty(%) = G2[7:0] / 256               |
| 0bh   | LEDB2 Duty   | B2[7:0] |        |        |        |        |        |        |        | Duty(%) = B2[7:0] / 256               |
| 0ch   | LEDR3 Duty   | R3[7:0] |        |        |        |        |        |        |        | Duty(%) = R3[7:0] / 256               |
| 0dh   | LEDG3 Duty   | G3[7:0] |        |        |        |        |        |        |        | Duty(%) = G3[7:0] / 256               |
| 0eh   | LEDB3 Duty   | B3[7:0] |        |        |        |        |        |        |        | Duty(%) = B3[7:0] / 256               |
| 0fh   | LEDR4 Duty   | R4[7:0] |        |        |        |        |        |        |        | Duty(%) = R4[7:0] / 256               |
| 10h   | LEDG4 Duty   | G4[7:0] |        |        |        |        |        |        |        | Duty(%) = G4[7:0] / 256               |
| 11h   | LEDB4 Duty   | B4[7:0] |        |        |        |        |        |        |        | Duty(%) = B4[7:0] / 256               |
| 12h   | LEDR5 Duty   | R5[7:0] |        |        |        |        |        |        |        | Duty(%) = R5[7:0] / 256               |
| 13h   | LEDG5 Duty   | G5[7:0] |        |        |        |        |        |        |        | Duty(%) = G5[7:0] / 256               |
| 14h   | LEDB5 Duty   | B5[7:0] |        |        |        |        |        |        |        | Duty(%) = B5[7:0] / 256               |
| 15h   | LEDR6 Duty   | R6[7:0] |        |        |        |        |        |        |        | Duty(%) = R6[7:0] / 256               |
| 16h   | LEDG6 Duty   | G6[7:0] |        |        |        |        |        |        |        | Duty(%) = G6[7:0] / 256               |
| 17h   | LEDB6 Duty   | B6[7:0] |        |        |        |        |        |        |        | Duty(%) = B6[7:0] / 256               |

**Table 6. LUMINANCE REGISTERS** (continued)

| Addr. | Register    | D[7]                         | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | Description                  |
|-------|-------------|------------------------------|------|------|------|------|------|------|------|------------------------------|
| 18h   | LEDR7 Duty  | R7[7:0]                      |      |      |      |      |      |      |      | Duty(%) = R7[7:0] / 256      |
| 19h   | LEDG7 Duty  | G7[7:0]                      |      |      |      |      |      |      |      | Duty(%) = G7[7:0] / 256      |
| 1ah   | LEDB7 Duty  | B7[7:0]                      |      |      |      |      |      |      |      | Duty(%) = B7[7:0] / 256      |
| 1bh   | LEDR8 Duty  | R8[7:0]                      |      |      |      |      |      |      |      | Duty(%) = R8[7:0] / 256      |
| 1ch   | LEDG8 Duty  | G8[7:0]                      |      |      |      |      |      |      |      | Duty(%) = G8[7:0] / 256      |
| 1dh   | LEDB8 Duty  | B8[7:0]                      |      |      |      |      |      |      |      | Duty(%) = B8[7:0] / 256      |
| 1eh   |             |                              |      |      |      |      |      |      |      |                              |
| 1fh   |             |                              |      |      |      |      |      |      |      |                              |
| 20h   | Group1 Duty | R1/R2/R3/R4/R5/R6/R7/R8[7:0] |      |      |      |      |      |      |      | Duty(%) = Group1 [7:0] / 256 |
| 21h   | Group2 Duty | G1/G2/G3/G4/G5/G6/G7/G8[7:0] |      |      |      |      |      |      |      | Duty(%) = Group2 [7:0] / 256 |
| 22h   | Group3 Duty | B1/B2/B3/B4/B5/B6/B7/B8[7:0] |      |      |      |      |      |      |      | Duty(%) = Group3 [7:0] / 256 |
| 23h   | Group4 Duty | R1/G1/B1/R2/G2/B2[7:0]       |      |      |      |      |      |      |      | Duty(%) = Group4 [7:0] / 256 |
| 24h   | Group5 Duty | R3/G3/B3/R4/G4/B4[7:0]       |      |      |      |      |      |      |      | Duty(%) = Group5 [7:0] / 256 |
| 25h   | Group6 Duty | R5/G5/B5/R6/G6/B6[7:0]       |      |      |      |      |      |      |      | Duty(%) = Group6 [7:0] / 256 |
| 26h   | Group7 Duty | R7/G7/B7/R8/G8/B8[7:0]       |      |      |      |      |      |      |      | Duty(%) = Group7 [7:0] / 256 |

When you transmit data of the group setting, please be careful because data of the individual setting update it.

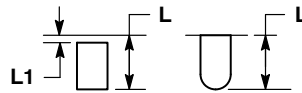
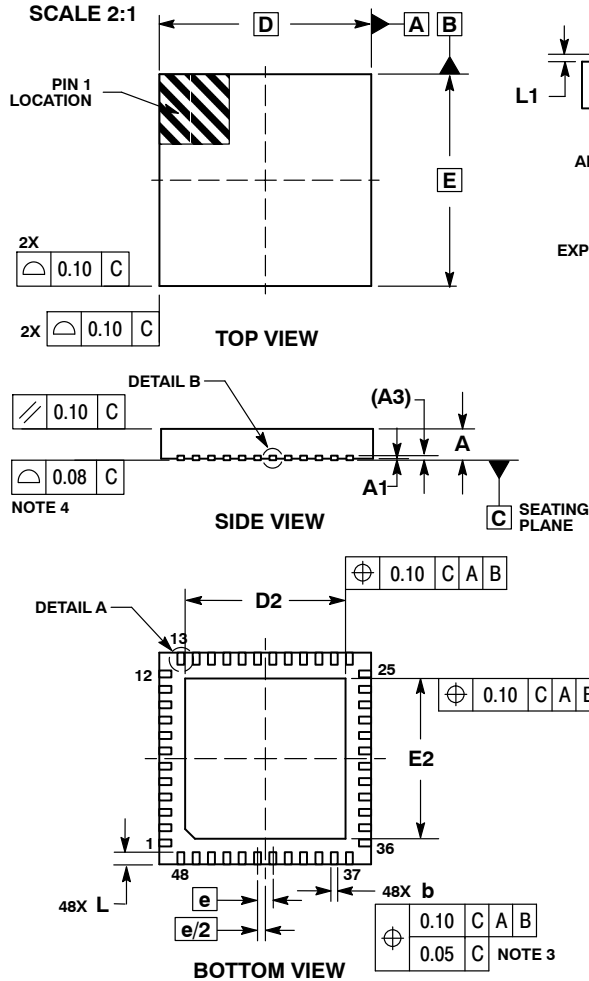


QFN48 7x7, 0.5P  
CASE 485EB  
ISSUE O

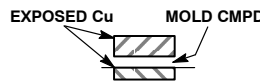
DATE 07 JUL 2015

NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION  $b$  APPLIES TO THE PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



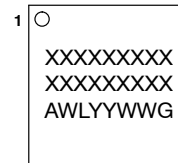
DETAIL A  
ALTERNATE TERMINAL  
CONSTRUCTIONS



DETAIL B  
ALTERNATE  
CONSTRUCTION

| MILLIMETERS |      |      |
|-------------|------|------|
| DIM         | MIN  | MAX  |
| A           | 0.80 | 0.90 |
| A1          | 0.00 | 0.05 |
| A3          | 0.20 | REF  |
| b           | 0.20 | 0.30 |
| D           | 7.00 | BSC  |
| D2          | 5.20 | 5.40 |
| E           | 7.00 | BSC  |
| E2          | 5.20 | 5.40 |
| e           | 0.50 | BSC  |
| L           | 0.35 | 0.45 |
| L1          | 0.00 | 0.15 |

GENERIC  
MARKING DIAGRAM\*

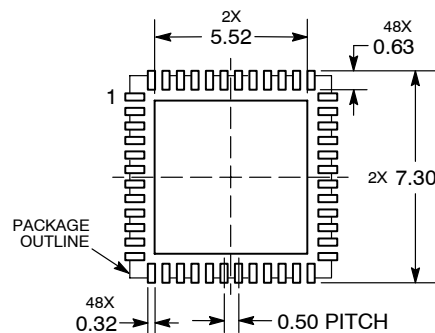


A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking.

Pb-Free indicator, "G" or microdot "▪", may or may not be present.

RECOMMENDED  
SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

|                  |                  |                                                                                                                                                                                  |
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