General Description

The MAX22204 is a two-phase stepper motor driver. It integrates two 65V, $3.8A_{MAX}$ H-Bridges. The H-Bridge FETs have very low impedance, resulting in high driving efficiency and minimal heat. The typical total R_{ON} (high-side + low-side) is 0.3Ω. The MAX22204 integrates an accurate current drive regulation circuit and a 128-microstep built-in indexer controlled by a STEP/DIR interface. The high microstep resolution and advanced control technique ensure smooth and quiet operations.

The current flowing into the two low-side FETs is sensed by a non-dissipative Integrated Current Sensing (ICS) and it is then compared with the desired step threshold current. As soon as the bridge current exceeds the threshold (I_{TRIP}), the device enforces the decay for a fixed OFF-time (t_{OFF}).

The non-dissipative ICS eliminates the bulky external power resistors normally required for this function, resulting in a dramatic space and power saving compared with mainstream applications based on the external sense resistor. Currents proportional to the internally-sensed bridge currents are output to pins ISENA and ISENB. By connecting external resistors to these pins, voltages proportional to the bridge currents are generated. These can be used for diagnostic purposes.

The maximum output current per H-Bridge is I_{MAX} = $3.8A_{MAX}$ limited by the Overcurrent Protection (OCP). The device delivers up to $2A_{RMS}$ per phase at V_M = +24V and T_A = 25°C with proper PCB ground plane for thermal dissipation. The current capability depends on the PCB thermal characteristic (PCB ground planes, heatsinks, ventilation, etc.). The maximum full-scale current per H-Bridge is I_{FS} = 2.8A and can be set by an external resistor connected from the REF pin to GND. This current is defined as the maximum current setting of the integrated drive regulation circuit.

One logic input (TRQ) allows to quickly change the current setting among two different values for fast torque control.

The MAX22204 features Overcurrent Protection (OCP), Thermal Shutdown (TSD), and Undervoltage Lockout (UVLO). An open drain active low $\overline{FAULT}$ pin is activated every time a fault condition is detected. During Thermal Shutdown and Undervoltage Lockout, the driver is disabled until normal operating conditions are restored.

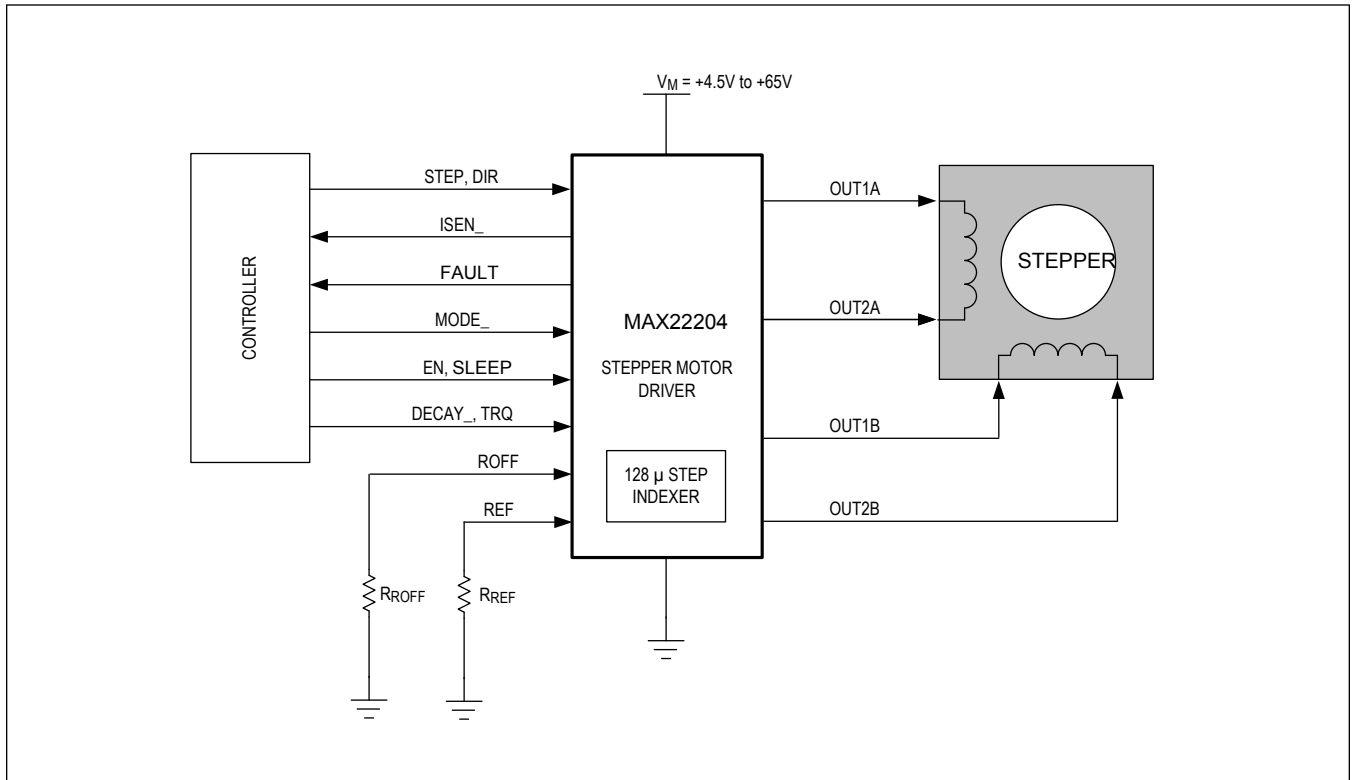The MAX22204 is packaged into a small TQFN38 5mm x 7mm and TSSOP38 9.7mm x 4.4mm packages.

Applications

- Stepper Motor Driver

Benefits and Features

- Two H-Bridges with +65V Voltage Rating
  - Total Rdson (High-Side + Low-Side): 300mΩ Typical (T_A = 25°C)
- Current Ratings per H-Bridge (Typical at T_A = 25°C):
  - I_{MAX} = $3.8A_{MAX}$ (Impulsive Current for Driving Capacitive Loads)
  - $I_{FS(MAX)}$ = 2.8A (Maximum Full Scale Current Setting for Internal Current Drive Regulation)
  - I_{RMS} = $2A_{RMS}$ per Phase (T_A = 25°C, V_M = +24V)
- Integrated Current Control
  - Full-Scale DAC Current Configurable with External Resistance
  - One Logic Input (TRQ) to Quickly Change the Torque among Two Levels
  - Internal Current Sensing (ICS) Eliminates External Bulky Resistors and Improves Efficiency
  - Built-in-Control with 128-usteps Indexer
    - STEP/DIR Interface
    - Integrated DAC and Sequencer for U-Stepping
  - Multiple Decay Modes (Slow, Mixed, Adaptive)
  - Fixed OFF Time Configurable with External Resistance
- Current-Sense Output (ISENA, ISENB) Current Monitor
- Fault Indicator Pin ($\overline{FAULT}$)
- Protections
  - Overcurrent Protection for each Individual Channel (OCP)
  - Undervoltage Lockout (UVLO)
  - Thermal Shutdown T_J = 155°C (TSD)
- Available in TQFN38 5mm x 7mm and TSSOP38 9.7mm x 4.4mm Packages

Simplified Block Diagram

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Absolute Maximum Ratings

V_M to GND .... -0.3V to +70V
V_{DD} to GND................................-0.3V to min (+2.2V, V_M + 0.3V)
PGND to GND .... -0.3V to +0.3V
OUT_ .... -0.3 to (V_M + 0.3V)
V_{CP} to GND........................ (V_M - 0.3V) to min (+74V, V_M + 6V)
C_{P2} to GND ....(V_M - 0.3V) to (V_{CP} + 0.3V)
C_{P1} to GND ....-0.3V to (V_M + 0.3V)
FAULT to GND .... -0.3V to 6V
REF to GND ....-0.3V to min (+2.2V, V_{DD} + 0.3V)
ROFF to GND..........................-0.3V to min (+2.2V, V_{DD} + 0.3V)

ISEN_ to GND..........................-0.3V to min (+2.2V, V_{DD} + 0.3V)
EN to GND ....-0.3V to 6V
STEP, DIR, MODE_ to GND.....................................-0.3V to 6V
TRQ to GND ....-0.3V to 6V
DECAY_ to GND...-0.3V to 6V
SLEEP to GND ....-0.3V to min (+70V, V_M + 0.3V)
Operating Temperature Range ....-40°C to +125°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

38-Pin TSSOP (9.7mm x 4.4mm)

Package Code	U38E+3C
Outline Number	21-0714
Land Pattern Number	90-0435
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	45°C/W
Junction to Case (θ_{JC})	1°C/W

38-Pin TQFN (5mm x 7mm)

Package Code	T3857-1C
Outline Number	21-0172
Land Pattern Number	90-0076
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	38°C/W
Junction to Case (θ_{JC})	1°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	28°C/W
Junction to Case (θ_{JC})	1°C/W

For the latest package outline information and land patterns (footprints), go to *Package Index*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *Thermal Characterization of IC Packages*.

Electrical Characteristics

(V_M = from +4.5V to +65V, R_{ROFF} = from 15kΩ to 120kΩ, R_{REF} = from 13kΩ to 60kΩ, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization, typical values are at V_M = 36V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Voltage Range	V_M		4.5		65	V
Sleep-Mode Current Consumption	I_{VM}	$\overline{SLEEP}$ = logic low			20	µA
Quiescent Current Consumption	I_{VM}	$\overline{SLEEP}$ = logic high			5	mA
1.8V Regulator Output Voltage	V_{VDD}	V_M = +4.5V, I_{LOAD} = 20mA		1.8		V
V_{DD} Current Limit	$I_{VDD(LIM)}$	V_{DD} shorted to GND	18			mA
Charge-Pump Voltage	V_{CP}			V_M + 2.7		V
LOGIC LEVEL INPUTS/OUTPUTS						
Input Voltage Level—High	V_{IH}		1.2			V
Input Voltage Level—Low	V_{IL}				0.65	V
Input Hysteresis	V_{HYS}			110		mV
Pull-Down Current	I_{PD}	Logic supply (V_L) = +3.3V	16	34	60	µA
Open-Drain Output Logic-Low Voltage	V_{OL}	I_{LOAD} = 5mA			0.4	V
Open-Drain Output Logic-High Leakage Current	I_{OH}	V_{PIN} = +3.3V	-1		+1	µA
$\overline{SLEEP}$ Voltage Level High	$V_{IH(\overline{SLEEP})}$		0.9			V
$\overline{SLEEP}$ Voltage Level Low	$V_{IL(\overline{SLEEP})}$				0.6	V
$\overline{SLEEP}$ Pull-Down Input Resistance	$R_{PD(\overline{SLEEP})}$		0.8	1.5		MΩ
OUTPUT SPECIFICATIONS						
Output On-Resistance Low-Side	$R_{ON(LS)}$			150	270	mΩ
Output On-Resistance High-Side	$R_{ON(HS)}$			150	300	mΩ
Output Leakage	I_{LEAK}	Driver off	-12		+12	µA
Dead Time	t_{DEAD}			100		ns
Output Slew Rate	SR			300		V/µs
PROTECTION CIRCUITS						
Overcurrent Protection Threshold	I_{OCP}		3.8			A
Overcurrent Protection Blanking Time	t_{OCP}			0.8	2	µs
Autoretry OCP Time	t_{RETRY}			3		ms
UVLO Threshold on V_M	V_{UVLO}	V_M rising	3.75	4	4.25	V

Electrical Characteristics (continued)

(V_M = from +4.5V to +65V, R_{ROFF} = from 15kΩ to 120kΩ, R_{REF} = from 13kΩ to 60kΩ, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization, typical values are at V_M = 36V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
UVLO Threshold on V_M Hysteresis	$V_{UVLOHYS}$				0.12		V
Thermal-Protection Threshold Temperature	T_{SD}	Temperature rising until $\overline{FAULT}$ pin goes low			+155		°C
Thermal-Protection Temperature Hysteresis	T_{SD_HYST}	Temperature falling until $\overline{FAULT}$ pin goes high			20		°C
CURRENT REGULATION							
REF Pin Resistor Range	R_{REF}			12		60	kΩ
REF Output Voltage	V_{REF}				900		mV
Full-Scale Current Constant	KIFS				36		KV
Current Regulation Accuracy (*Note 1*)	DITRIP1	I_{FS} = 2.8A	I_{TRIP} from 1.75A to I_{FS}	-5		+5	%
	DITRIP2		I_{TRIP} from 500mA to 1.75A	-10		+10	
	DITRIP3		I_{TRIP} from 250mA to 500mA	-15		+15	
Fixed OFF – Time Internal	t_{OFF}	ROFF shorted to V_{DD}		16	20	24	μs
Fixed OFF – Time Constant	KTOFF	R_{ROFF} from 15KΩ to 120KΩ			0.667		μs/kΩ
PWM Blanking Time	t_{BLK}				1.5		μs
CURRENT-SENSE MONITOR							
ISEN_ Voltage Range	V_{ISEN}	Voltage range at ISEN_ pin		0		1.1	V
Current-Monitor Scaling Factor	KISEN	Set the I_{ISEN} output-current equation in the *Current-Sense Output (CSO)—Current Monitor* section			7500		A/A
Current Monitor Accuracy (*Note 1*)	$DKISEN_1$	I_{FS} = 2.8A	I_{TRIP} from 1.1A to I_{FS}	-5		+5	%
	$DKISEN_2$		I_{TRIP} from 500mA to 1.1A	-10		+10	
	$DKISEN_3$		I_{TRIP} from 250mA to 500mA	-15		+15	
Settling Time	t_S	I_{FS} = I_{MAX}			0.5		μs
FUNCTIONAL TIMING							
Sleep Time	t_{SLEEP}	$\overline{SLEEP}$ = logic 1 to logic 0 for OUT_ to become three-state			40		μs
Wake-Up Time from Sleep	t_{WAKE}	$\overline{SLEEP}$ = logic 0 to logic 1 to resume normal operation				2.7	ms
Enable Time	t_{EN}	Time from EN pin rising edge to driver on				0.6	μs
Disable Time	t_{DIS}	Time from EN pin falling edge to driver off				1.4	μs
INDEXER TIMING							
STEP High Time	t_{STH}			1			us

Electrical Characteristics (continued)

(V_M = from +4.5V to +65V, R_{ROFF} = from 15kΩ to 120kΩ, R_{REF} = from 13kΩ to 60kΩ, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization, typical values are at V_M = 36V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STEP Low Time	t_{STL}		1			us
Setup Time MODE, DIR to STEP	t_{SETUP}		200			ns
Hold Time MODE, DIR to STEP	t_{HOLD}		200			ns

Note 1: Guaranteed by design, not production tested.

Pin Configurations

TQFN Pin Configuration

TOP VIEW

Pin	Name
31	PGNDA
30	OUT1A
29	V_M
28	V_M
27	OUT2A
26	PGNDA
25	PGNDB
24	OUT2B
23	V_M
22	V_M
21	OUT1B
20	PGNDB

Pin	Name
32	PGNDA
33	ISENB
34	ISENA
35	NC
36	REF
37	ROFF
38	GND

MAX22204

Pin	Name
19	PGNDB
18	GND
17	SLEEP
16	V_M
15	V_{CP}
14	C_{P2}
13	C_{P1}

Pin	Name
1	V_{DD}
2	STEP
3	DIR
4	MODE0
5	MODE1
6	MODE2
7	DECAY0
8	DECAY1
9	DECAY2
10	EN
11	TRQ
12	FAULT

TQFN

TSSOP Pin Configuration

TOP VIEW

Pin	Name
38	N.C.
37	ISENA
36	ISENB
35	N.C.
34	PGNDA
33	OUT1A
32	V_M
31	V_M
30	OUT2A
29	PGNDA
28	PGNDB
27	OUT2B
26	V_M
25	V_M
24	OUT1B
23	PGNDB
22	N.C.
21	GND
20	SLEEPN

MAX22204

+

Pin	Name
1	REF
2	ROFF
3	AGND
4	V_{DD}
5	STEP
6	DIR
7	MODE0
8	MODE1
9	MODE2
10	DECAY0
11	DECAY1
12	DECAY2
13	EN
14	TRQ
15	$\overline{FAULT}$
16	C_{P1}
17	C_{P2}
18	V_{CP}
19	V_M

TSSOP38
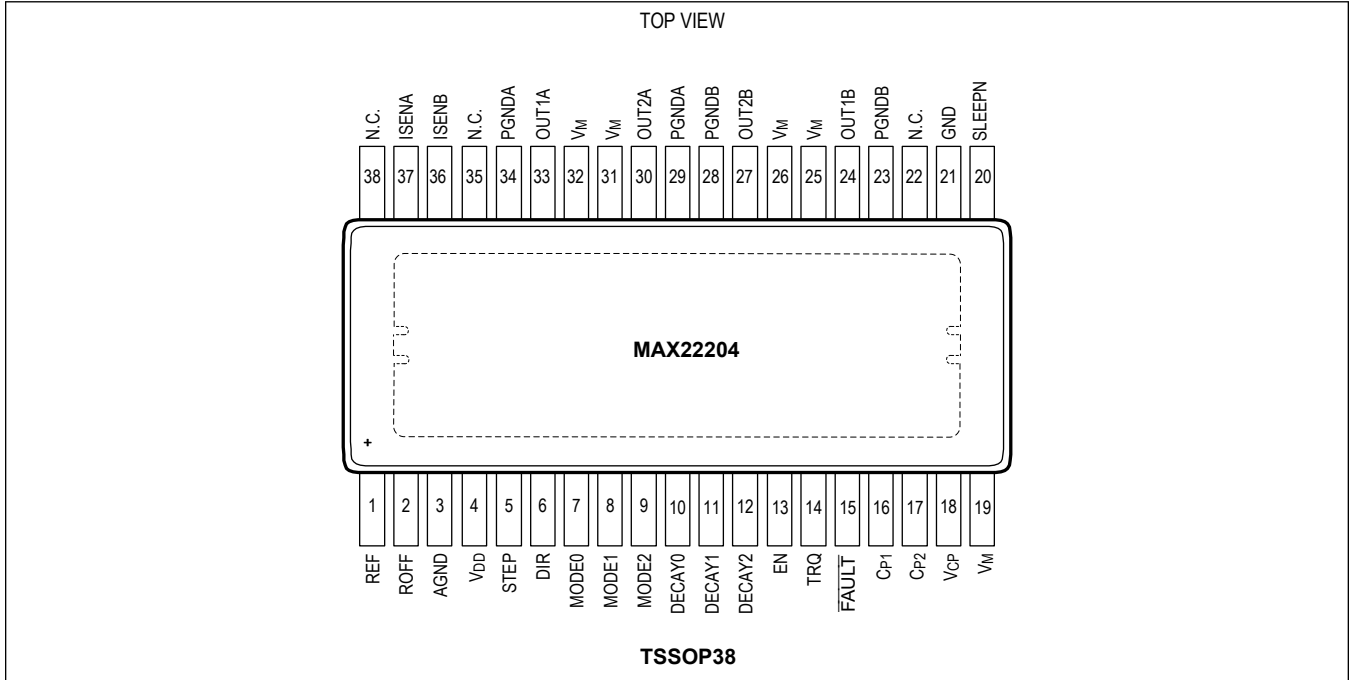
Pin Description

PIN		NAME	FUNCTION	TYPE
TQFN	TSSOP			
16, 22, 23, 28, 29	19, 25, 26, 31, 32	V_M	Supply Voltage Input. Connect at least 1µF surface-mounted device plus 10µF electrolytic bypass capacitors to GND. Higher values can be considered depending on application requirements.	Supply
15	18	V_{CP}	Charge-Pump Output. Connect a 5V, 1µF capacitor between V_{CP} and V_M as close as possible to the device.	Output
13	16	C_{P1}	Charge-Pump Flying Capacitor Pin 1. Connect a V_M-rated 22nF capacitor between C_{P1} and C_{P2} as close as possible to the device.	Output
14	17	C_{P2}	Charge-Pump Flying Capacitor Pin 2. Connect a V_M-rated 22nF capacitor between C_{P1} and C_{P2} as close as possible to the device.	Output
1	4	V_{DD}	1.8V Linear Regulator Output. Bypass V_{DD} to GND with a 5V, 2.2µF capacitor connected close to the device.	Analog Output
17	20	$\overline{SLEEP}$	Active-Low Sleep Pin.	Logic Input
21, 24, 27, 30	24, 27, 30, 33	OUT1B, OUT2B, OUT2A, OUT1A, respectively	Driver outputs.	Output
12	15	$\overline{FAULT}$	Active-Low, Open-Drain, Output Fault Indicator. $\overline{FAULT}$ goes low to indicate that one or more of the protection mechanisms has been activated. Connect a 2kΩ pull-up resistor from $\overline{FAULT}$ to the microcontroller supply voltage.	Open-Drain Output

Pin Description (continued)

PIN		NAME	FUNCTION	TYPE
TQFN	TSSOP			
33, 34	36, 37	ISEN_	Current-Sense Output Monitor. Connect a resistor to GND (see the Current-Sense Output (CSO)—Current Monitor section).	Output
10	13	EN	Logic Input Pin. Enable Pin.	Logic Input
7, 8, 9	10, 11, 12	DECAY_	Logic Input. Set the Decay Mode.	Logic Input
11	14	TRQ	Logic Input. Set Output Current Full-Scale (Torque).	Logic Input
2	5	STEP	Logic Input. Indexer step logic input. Indexer advances on rising edges of the STEP pin.	Logic Input
3	6	DIR	Logic Input. Direction Pin.	Logic Input
4, 5, 6	7, 8, 9	MODE_	Logic Input Pins. Set the Decay Mode for the current drive regulation circuit.	Logic Input
36	1	REF	Programmable Current Analog Input. Connect a resistor from REF to GND to set the full scale current.	Analog Input
37	2	ROFF	t_{OFF} Programmable Off Time Pin. Connect ROFF to V_{DD} to use the internal fixed t_{OFF} time. Connect a resistor R_{ROFF} from ROFF to GND to set the fixed OFF time to a desired value.	Analog Input
18, 38	3, 21	GND	Analog Ground. Connect to ground plane.	GND
19, 20, 25, 26, 31, 32	23, 28, 29, 34	PGND	Power GND. Connect to ground plane.	GND
EP	EP	EP	Exposed Pad. Connect to GND.	GND

Functional Diagrams
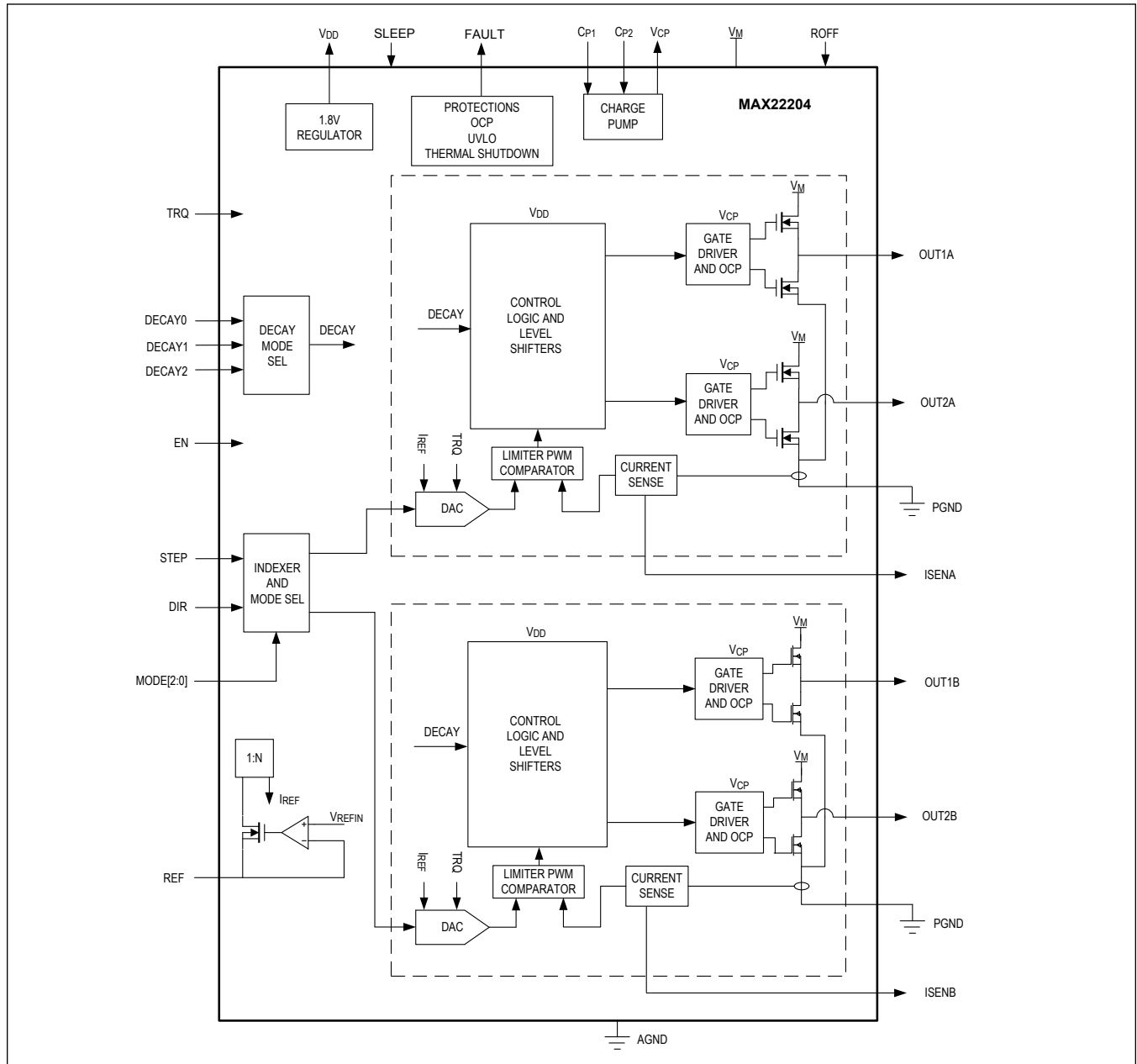
Detailed Description

The MAX22204 is a two-phase stepper motor driver. It integrates two 65V, $3.8A_{MAX}$ H-Bridges.

The H-Bridge FETs have very low impedance, resulting in high driving efficiency and minimal heat. The typical total R_{ON} (high-side + low-side) is 0.3Ω.

The MAX22204 integrates an accurate current drive regulation circuit and a 128-usteps built-in Indexer controlled by a STEP/DIR interface. The high u-stepping resolution and advanced control technique ensure smooth and quiet operations.

The bridge output current is sensed by a non-dissipative Integrated Current Sensing (ICS) and it is then compared with the desired step threshold current. As soon as the bridge current exceeds the threshold (I_{TRIP}), the device enforces the decay for a fixed OFF-time (t_{OFF}). The non-dissipative ICS eliminates the bulky external power resistors, which are normally required for this function, resulting in a dramatic space and power saving compared with mainstream applications based on the external sense resistor.

The currents proportional to the internally sensed bridge currents are output to pins ISENA and ISENB. By connecting external resistors to these pins, voltages proportional to the bridge currents are generated and can be used for diagnostic purposes.

The maximum output current per H-Bridge is $I_{MAX} = 3.8A_{MAX}$ limited by the Overcurrent Protection (OCP). The device delivers up to $2A_{RMS}$ per phase at V_M = +24V and T_A = 25°C with proper PCB ground plane for thermal dissipation. The current capability depends on the PCB thermal characteristic (PCB ground planes, heatsinks, ventilation, etc.).

The maximum full-scale current per H-Bridge is I_{FS} = 2.8A and can be set by an external resistor connected from the REF pin to GND. This current is defined as the maximum current setting of the embedded current drive regulation circuit.

One logic input (TRQ) allows to quickly change the current setting among two different values for fast torque control.

The MAX22204 features Overcurrent Protection (OCP), Thermal Shutdown (TSD), and Undervoltage Lockout (UVLO). An open-drain active low $\overline{FAULT}$ pin is activated every time a fault condition is detected.

During Thermal Shutdown and Undervoltage Lockout, the driver is disabled until normal operating conditions are restored.

The MAX22204 is packaged into a small TQFN38 5mm x 7mm and TSSOP38 9.7mm x 4.4mm packages.

Sleep Mode ($\overline{SLEEP}$ Pin)

The $\overline{SLEEP}$ pin can be driven low to place the device into the lowest power consumption mode possible, with all outputs three-stated, the internal circuits biased off, and the charge pump disabled. A pull-down resistor should be connected between $\overline{SLEEP}$ and GND to ensure the part is disabled whenever this pin is not actively driven. Driving the $\overline{SLEEP}$ pin high wakes up the device and returns it to normal mode. t_{WAKE} is 2.7ms (max).

Enable Function (EN pin)

This logic input enables/disables the output FETs. Drive EN low to tristate the two full bridges. Drive EN high to enable the outputs. The internal sequencer (indexer) remains active even when EN is set low.

Indexer Control Modes

The MAX22204 features an integrated Indexer that supports several different step modes. Logic inputs MODE[2:0] select the step mode as shown in Table 1.

Table 1. Step Mode Selection

MODE2	MODE1	MODE0	STEP MODE
0	0	0	Full Step (71% current)
0	0	1	½ Step
0	1	0	¼ Step
0	1	1	1/8 Step
1	0	0	1/16 Step
1	0	1	1/32 Step
1	1	0	1/64 Step
1	1	1	1/128 Step

Current-Sense Output (CSO)—Current Monitor

Currents proportional to the internally-sensed motor current are output to pins ISENA and ISENB for H-bridge A and B respectively. The current is sensed when one of the two low side FETs sinks the output current and it is therefore meaningful both during the energizing (t_{ON}) phase and during the Slow Decay phase (Brake). In Fast Decay, the current is not monitored and ISEN_ outputs are zero current.

The following equation shows the relationship between the current sourced at I_{SEN} and the output current:

$$I_{ISEN}(A) = \frac{I_{OUT}(A)}{K_{ISEN}}$$

Equation - ISEN Output Current

in which K_{ISEN} represents the current scaling factor between the output current and its replica at pin ISEN. K_{ISEN} is typically 7500 A/A. For instance, if the instantaneous output current is 2A, the current sourced at ISEN is 266µA.

Figure 1 shows an idealized behavior of the ISEN current when Slow or Fast Decay are used. Blanking times, delays, and rise/fall edges are ignored.
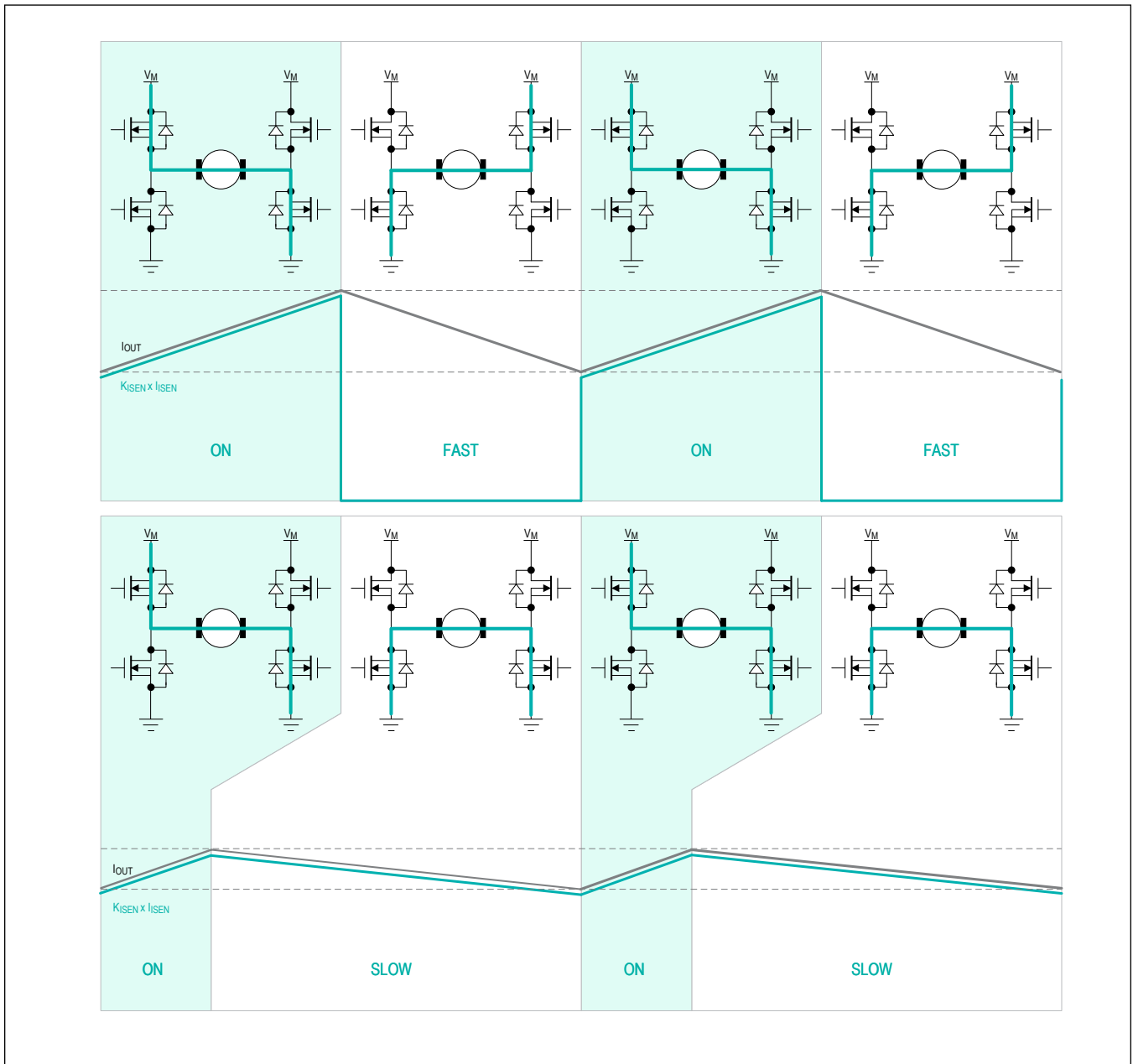
Figure 1. ISEN Current

By connecting an external signal resistor, R_{ISEN}, between ISEN and GND, a voltage proportional to the motor current is generated. The voltage built up on R_{ISEN} can be used for diagnostic purposes.

Current Drive Regulation

The MAX22204 features embedded Current Drive Regulation (CDR).

The embedded current drive regulation provides an accurate control of the current flowing into the motor windings.

The bridge current is sensed by a non-dissipative Integrated Current Sensing (ICS) circuit and it is then compared with the threshold current (I_{TRIP}). As soon as the bridge current exceeds the threshold, the device enforces the decay for a fixed OFF-time (t_{OFF}). The device supports different decay modes as described in the following paragraphs.

Once t_{OFF} elapses, the driver is re-enabled for the next PWM cycle. During current regulation, the PWM duty cycle and frequency depend on the supply voltage, on the motor inductance, and on motor speed and load conditions.

The t_{OFF} duration can be configured with an external resistor connected to the ROFF pin.

Integrated Current-Sense (ICS)

A non-dissipative current sensing is integrated. This feature eliminates the bulky external power resistors normally required for this function. This feature results in a dramatic space and power saving compared with mainstream applications based on the external sense resistor.

Setting the Full-Scale Current – Pin REF

Connect a resistor from REF to GND to set the full-scale chopping current I_{FS}.

The following equation shows the full-scale current as a function of the R_{REF} shunt resistor connected to pin REF. The proportionality constant K_{IFS} is typically 36KV. The external resistor R_{REF} can range between 13KΩ and 60KΩ, which correspondents to I_{FS} setting ranging from about 2.8A down to 0.6A.

$$I_{FS} = \frac{K_{IFS}(KV)}{R_{REF}(K\Omega)} \times TRQ(\%)$$

The current scalar factor TRQ (%) depends on the status of the logic input TRQ as shown in Table 2.

TQR is a logic input pin, which provides a rapid method to change the Torque with digital IOs.

Table 2. Torque TRQ Truth Table

TRQ	TRQ (%)
0	100%
1	50%

Bridge Current Control - Indexer

The Step mode is determined by the logic inputs MODE[2:0] (see Table 1).

The MAX22204 features a built-in indexer that supports up to 128-usteps. The indexer sets the bridge currents in the two phases for each Step mode.

At each pulse applied to the STEP pin, the sequencer of the device is increased (DIR input high) or decreased (DIR input low).

Table 3 shows the lookup table for each individual Step mode up to 32 u-stepping. Higher u-stepping modes, such as 64 or 128 u-stepping, are supported and follow a similar pattern with higher step angle resolution

When the driver is enabled (EN pin) or after exiting Sleep mode, the indexer is initialized at its 'home state', which corresponds to 45° angle. At each rising edge of the STEP input, the indexer moves to the next or previous state in the table respectively for DIR=1 or DIR=0.

After a Step mode change, rising edges of the STEP logic input cause the indexer to proceed accordingly with the former Step mode until the first valid state of the new Step mode is found. From that moment on, the indexer starts stepping accordingly with the new Step mode.

Table 3. Lookup Table up to 32 U-Steps

1/32 STEPPING	1/16 STEPPING	1/8 STEPPING	1/4 STEPPING	1/2 STEPPING	FULL STEPPING	COIL A	COIL B	STEP ANGLE
1	1	1	1	1		100.0%	0.0%	0
2						99.9%	4.9%	3
3	2					99.5%	9.8%	6

Table 3. Lookup Table up to 32 U-Steps (continued)

1/32 STEPPING	1/16 STEPPING	1/8 STEPPING	1/4 STEPPING	1/2 STEPPING	FULL STEPPING	COIL A	COIL B	STEP ANGLE
4						98.9%	14.7%	8
5	3	2				98.1%	19.5%	11
6						97.0%	24.3%	14
7	4					95.7%	29.0%	17
8						94.2%	33.7%	20
9	5	3	2			92.4%	38.3%	23
10						90.4%	42.8%	25
11	6					88.2%	47.1%	28
12						85.8%	51.4%	31
13	7	4				83.1%	55.6%	34
14						80.3%	59.6%	37
15	8					77.3%	63.4%	39
16						74.1%	67.2%	42
17	9	5	3	2	1	70.7%	70.7%	45
18						67.2%	74.1%	48
19	10					63.4%	77.3%	51
20						59.6%	80.3%	53
21	11	6				55.6%	83.1%	56
22						51.4%	85.8%	59
23	12					47.1%	88.2%	62
24						42.8%	90.4%	65
25	13	7	4			38.3%	92.4%	68
26						33.7%	94.2%	70
27	14					29.0%	95.7%	73
28						24.3%	97.0%	76
29	15	8				19.5%	98.1%	79
30						14.7%	98.9%	82
31	16					9.8%	99.5%	84
32						4.9%	99.9%	87
32	17	9	5			0.0%	100.0%	90

Setting the Fixed OFF_TIME (t$_{OFF}$)

The current regulation circuit is based on a constant t$_{OFF}$ PWM control. When the bridge current exceeds the target I$_{TRIP}$ current, an OFF phase begins and Decay modes are activated. The OFF phase has a fixed time duration (t$_{OFF}$). t$_{OFF}$ can be configured to a desired value by connecting an external resistor (R$_{ROFF}$) to pin ROFF. When the ROFF pin is shorted to V$_{DD}$, the t$_{OFF}$ time is internally set at a fixed value (20μs typical).

By connecting an external resistor to the pin ROFF, configure t$_{OFF}$ as shown in the following equation, in which R$_{ROFF}$ is an external resistor connected to the ROFF pin (in KΩ) and KT$_{OFF}$ is an internal constant equal to 0.667μs/KΩ.

$$t_{OFF}(\text{μs}) = R_{ROFF} \times K_{TOFF}$$

t$_{OFF}$ can be programmed from a range of 10μs to 80μs.

Operating Modes

During PWM chopping, the driver output alternates the Energizing (ON) and Decay phases. The MAX22204 supports different Decay modes. Slow Decay, Fast Decay, and different combinations between Slow and Fast.

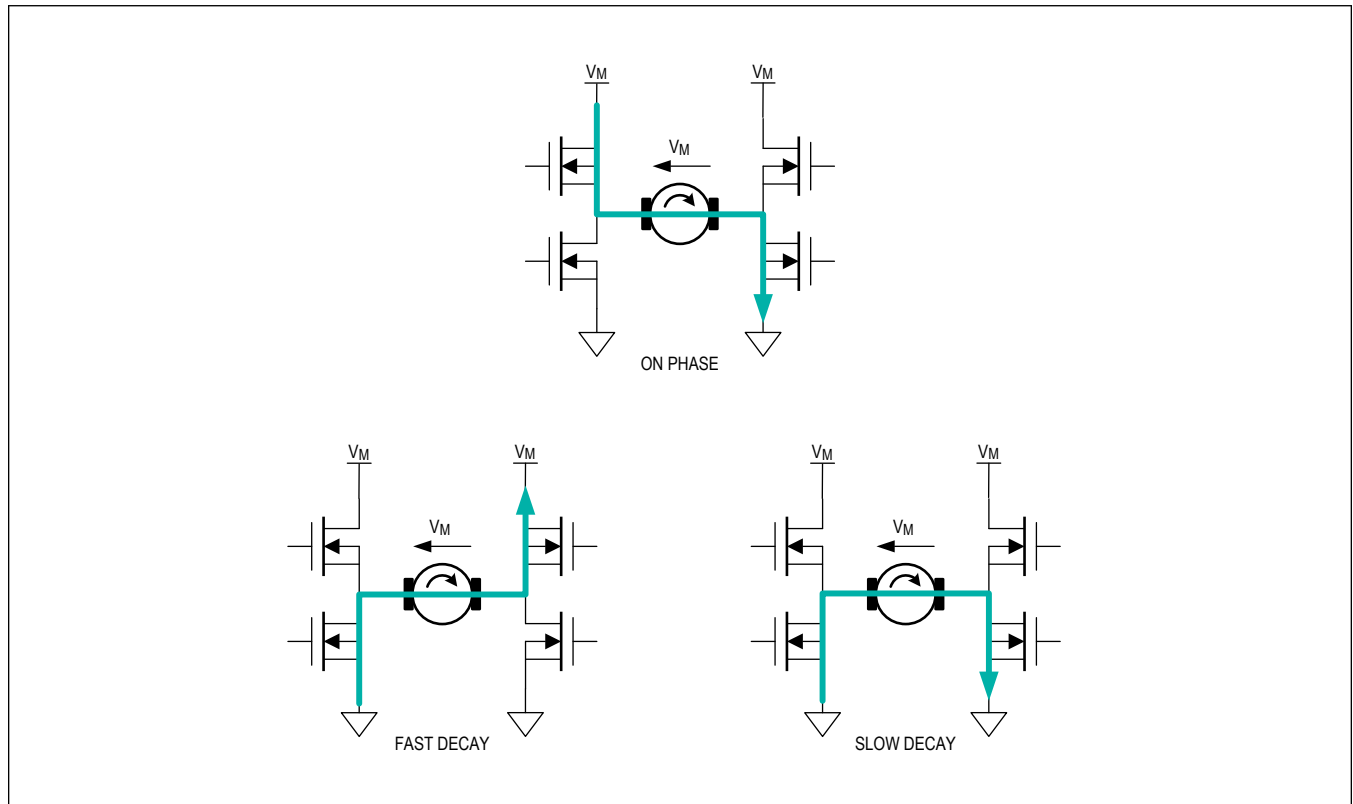Figure 2 shows the current path in the three different modes of operation.

Figure 2. Current Flow During ON and Decay Modes

Setting the Decay Mode

Three logic input pins allow to configure the Decay Mode during t_{OFF}. The MAX22204 supports Slow, Fast, and Mixed Decay modes. An Adaptive Decay Mode is also provided. The Adaptive Decay Mode automatically calculates the optimal ratio between the Slow and Fast decay as explained in the Adaptive Decay Mode paragraph.

Table 4 shows the Truth Table for the Decay Mode selection

Table 4. Decay Mode Truth Table

DECAY2	DECAY1	DECAY0	INCREASING STEPS	DECREASING STEPS
0	0	0	Slow	Mixed 30% Fast
0	0	1	Mixed 30% Fast	Mixed 30% Fast
0	1	0	Mixed 60% Fast	Mixed 60% Fast
0	1	1	Slow	Slow
1	0	0	Fast	Fast
1	0	1	Adaptive 1	Adaptive 1
1	1	0	Adaptive 2	Adaptive 2
1	1	1	Adaptive 3	Adaptive 3

Adaptive Decay Mode

The MAX22204 features three adaptive decay modes.

When the adaptive decay modes are used, the MAX22204 dynamically determines the ratio between Slow and Fast decay. The controller has to satisfy different and often conflicting requirements: to minimize the ripple for lower power consumption and better control accuracy, to ensure quick response time and low distortion of the pseudosinusoidal current waveform, to avoid generating sub-harmonic, which may fall in the audible range, etc.

The three adaptive decay algorithms provide different types of optimization. In general, the first and third algorithms are preferable for low-speed applications in which the ripple needs to be minimized. The second algorithm is recommended for high-speed applications, thanks to its fast tracking and stable characteristics.

All the three algorithms are based on current measurements during the energizing phase (t_{ON}) and during the slow decay phase (t_{SLOW}).

The algorithms distinguish three operating conditions.

Tracking-Up Phase: As a consequence of a STEP command, the current must be quickly increased to a new upper target level (STEP UP).

Tracking-Down Phase: As a consequence of a STEP command, the current must be quickly decreased to a new lower target level (STEP DW).

Settling/Steady-State Phase: Once a current target level is reached, the current stabilizes. Ripple must be minimized.

All the three algorithms behave the same during the Tracking-Up Phase: When a step-up command is received, the previous cycle is completed and then an ON time (t_{ON}) is enforced until the current reaches the new target level. See Figure 3.
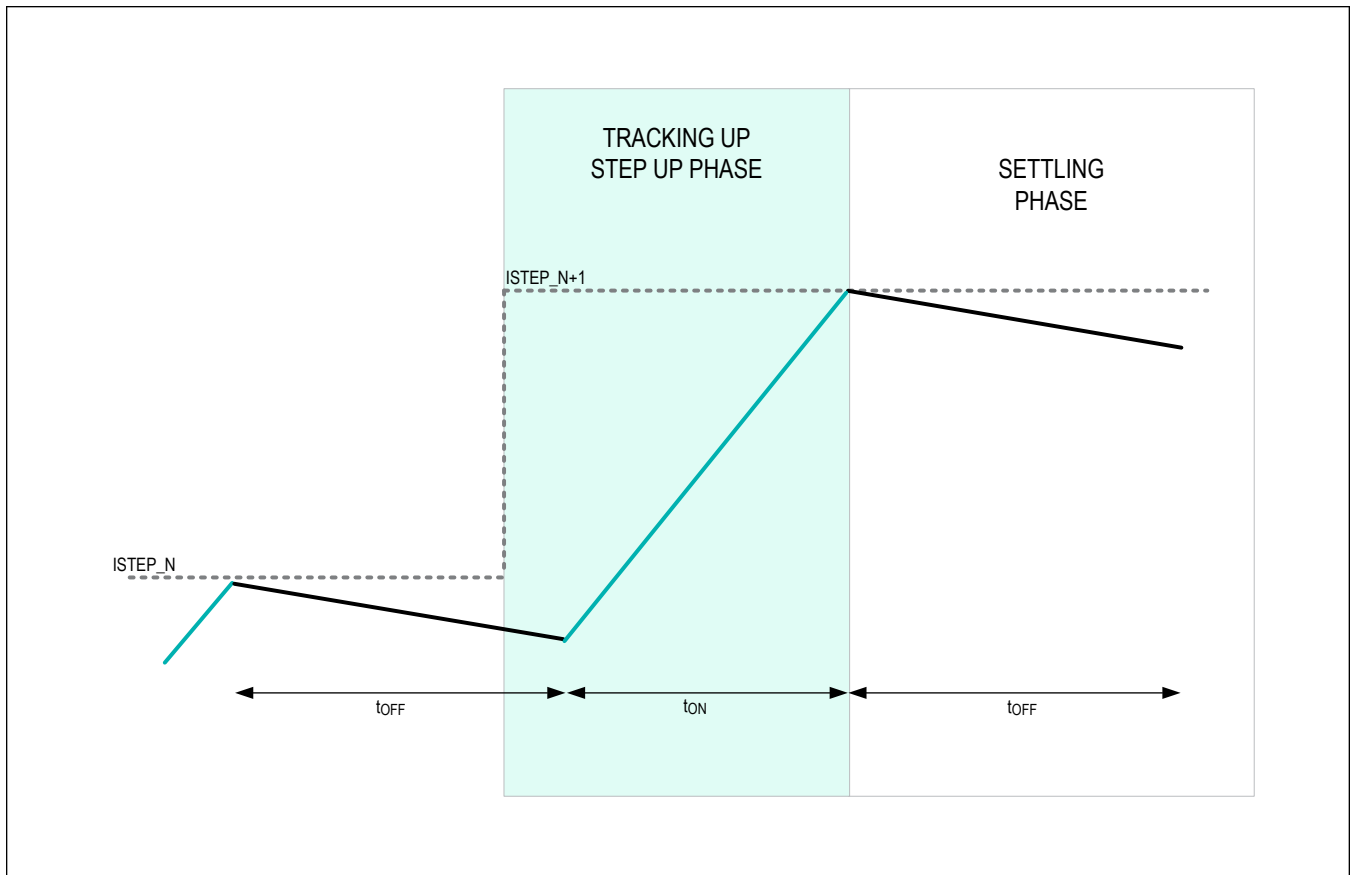
Figure 3. Adaptive Decay Step-Up

ALGORITHM #1 - DECAY[2:0]=101,

The first algorithm minimizes the ripple during the Settling/Steady-State phase.

1) **Tracking-Down Phase (Step Down)**: A mixed mode with 30% Fast Decay and 70% Slow Decay is used. When, during a Slow Decay Interval, the current is found lower than the new target, a t_{ON} phase is enforced causing the current to reach the desired level.

2) **Settling/Steady-State Phase:** Variable fixed slow decay ratios are used to minimize the ripple. Initially, a Slow Decay is enforced for a fixed OFF time (t_{OFF}). In the following cycles, the ON time interval (t_{ON}) is monitored cycle by cycle. If t_{ON} is found equal to $t_{ON(MIN)}$, a mixed mode with 10% Fast Decay is applied to the next chopping cycle.

The Fast Decay percentage dynamically increases with +10% steps if t_{ON} in the previous cycle is found equal to $t_{ON(MIN)}$.

The Fast Decay percentage dynamically decreases with -10% steps if t_{ON} in the previous cycle is found longer than $t_{ON(MIN)}$.

To facilitate the convergence of the algorithm, the Fast Decay percentage is not allowed to go back below 10%
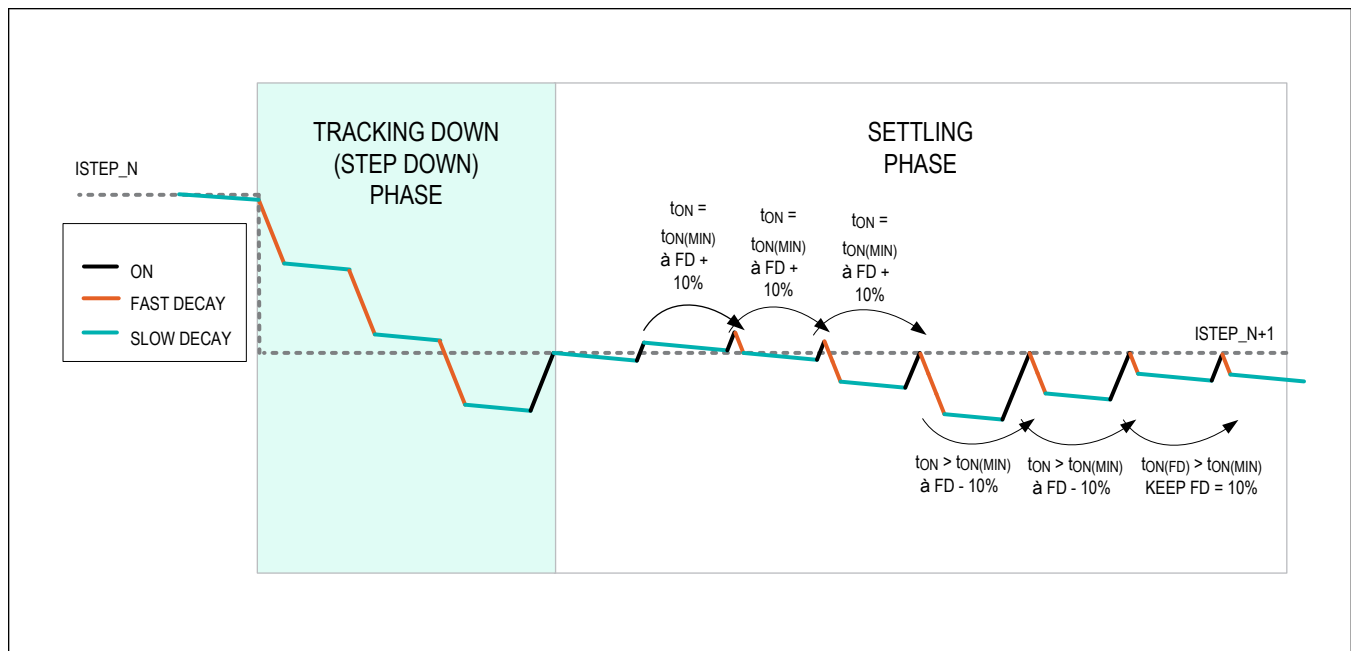
Figure 4 graphically illustrates the behavior.

Figure 4. Adaptive Decay - Algorithm #1

ALGORITHM #2 - DECAY[2:0]=110,

The second algorithm privileges dynamic response over the ripple containment. Compared with the first algorithm, a higher Fast Decay percentage is used. During the Settling/Steady-State Phase, the Fast Decay percentage increases similarly to the First Algorithm. Differently from Algorithm #1, the Fast Decay percentage can only be increased and it is never decreased. When compared with Algorithm #1, this approach results in a higher ripple but with faster settling time.

1) **Tracking-Down Phase (Step Down)**: A mixed mode with 60% Fast Decay and 40% Slow Decay is used. When, during a Slow Decay Interval, the current is found lower than the new target, a t_{ON} phase in enforced causing the current to reach the desired level.

2) **Settling/Steady-State Phase:** Variable fixed slow decay ratios are used to minimize the ripple. Initially, a Slow Decay is enforced for a fixed OFF time (t_{OFF}). In the following cycles, the ON time interval (t_{ON}) is monitored cycle by cycle. If t_{ON} is found equal to $t_{ON(MIN)}$, a mixed mode with 10% Fast Decay is applied in the next chopping cycle.

The Fast Decay percentage dynamically increases with +10% steps if t_{ON} in the previous cycle is found equal to $t_{ON(MIN)}$.

The Fast Decay percentage is kept constant if t_{ON} in the previous cycle is found longer than $t_{ON(MIN)}$.
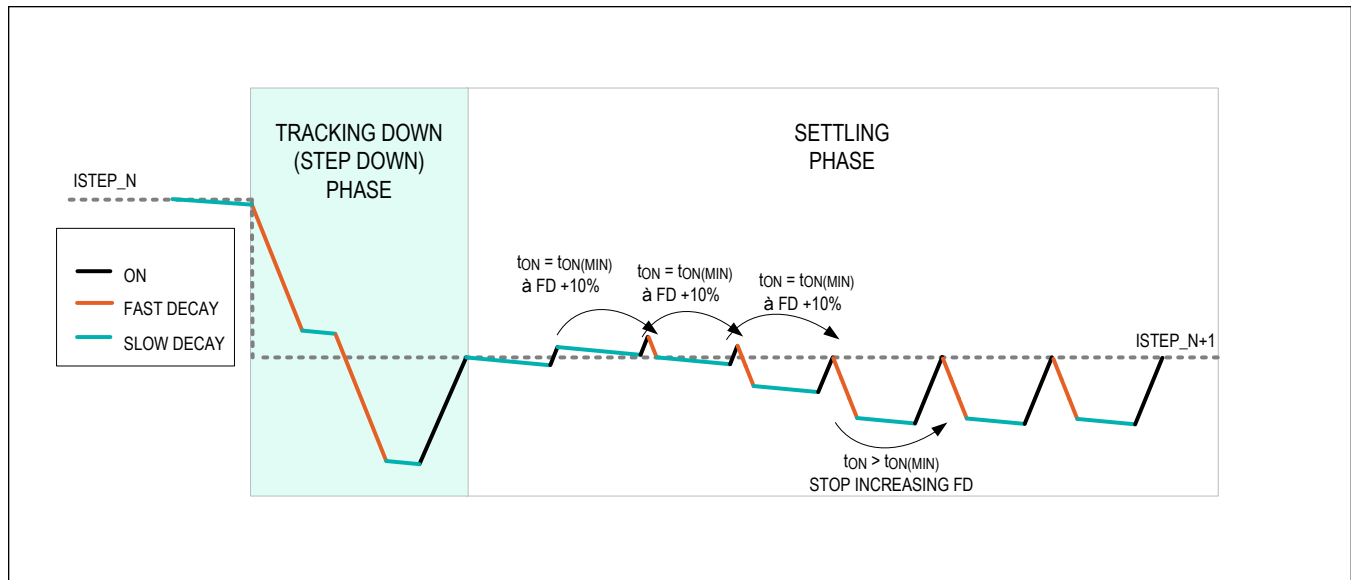
Figure 5 graphically illustrates the behavior.

Figure 5. Adaptive Decay Step-Up - Algorithm #2

ALGORITHM #3 - DECAY[2:0]=111,

Algorithm #3 is similar to Algorithm #1, the only difference being that during the Tracking-Down Phase (Step Down), the mixed decay ratio is not kept constant but depends on the amplitude of the step. For small step amplitudes, a low Fast Decay percentage is used. For relative large step amplitudes, a higher Fast Decay percentage is used.

When u-stepping control is used, steps close to the peak of the sinusoidal current waveform have small amplitudes and hence low Fast Decay percentages, whereas steps close to the zero crossing have larger amplitudes and hence high Fast Decay percentages. When compared to Algorithm #1, this approach minimizes the undershoots at each step down.

Fault Protection

Overcurrent Protection (OCP)
An OCP protects the device against short circuits to the rails (supply voltage and ground) and across the load terminals. The OCP threshold is set at 3.8A minimum. If the output current is larger than the OCP threshold for longer than the OCP blanking time, an OCP event is detected. When an OCP event is detected, the H-Bridge is immediately disabled, and a fault indication is output on the pin $\overline{FAULT}$. The H-Bridge is kept in a high impedance mode for 3ms (see t_{RETRY} specification). The H-Bridge is then re-enabled according to the current state. If the short circuit is still present, this cycle repeats. Otherwise, normal operation resumes. Avoid prolonged operation under the short-circuit failure mode as a prolonged OCP auto-retry affects the device reliability.

Thermal Shutdown
If the die temperature exceeds T_{SD} = +155°C (typ), all output pins (OUT1A, OUT2A, OUT1B, and OUT2B) are three-stated and the $\overline{FAULT}$ pin is driven low. The $\overline{FAULT}$ pin remains low and the outputs are placed in three-state mode until the die temperature falls by the hysteresis amount of 20°C (typ), after which the $\overline{FAULT}$ pin is driven high and the outputs are re-enabled.

Undervoltage-Lockout Protection (UVLO)
When the V_M supply voltage is below the UVLO threshold, all OUT_ outputs are three-stated and the $\overline{FAULT}$ pin is driven low. The OUT_ outputs automatically return to their current state (defined by EN) when the V_M supply voltage exceeds the UVLO threshold (max) and $\overline{FAULT}$ is driven high.

Typical Application Circuits

Application Diagram
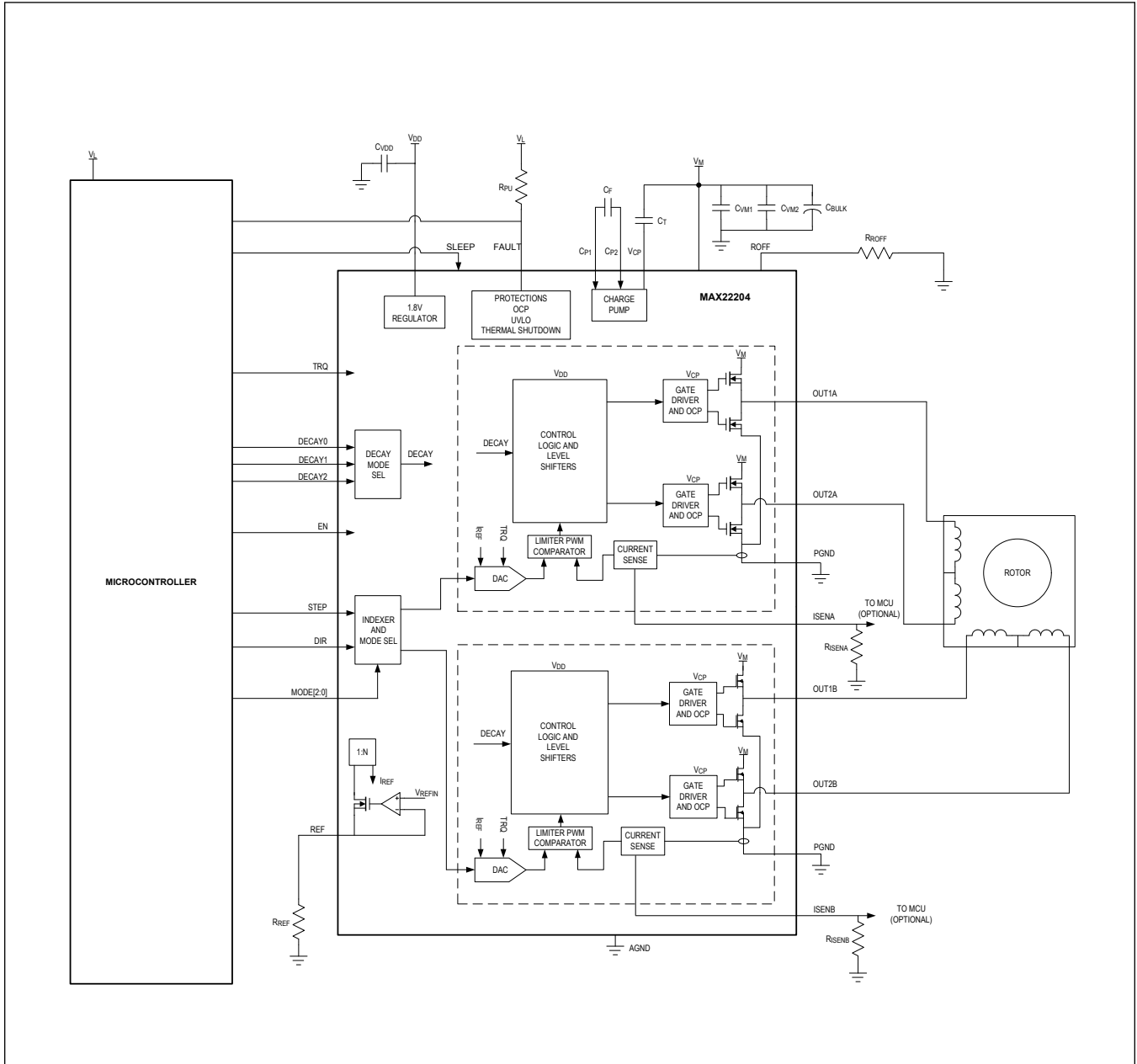
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE
MAX22204ATU+	-40°C to +125°C	38-TQFN
MAX22204ATU+T	-40°C to +125°C	38-TQFN
MAX22204AUU+	-40°C to +125°C	38-TSSOP
MAX22204AUU+T	-40°C to +125°C	38-TSSOP

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/21	Initial release	—
1	5/24	Updated the *General Description*, *Benefits and Features*, *Absolute Maximum Ratings, Package Information*, *Electrical Characteristics*, *Pin Configurations*, *Pin Description*, *Detailed Description*, and *Ordering Information* sections	1, 6-12, 14-15, 17-18, 23, 25

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