*Click **here** to ask an associate for production status of specific part numbers.*

MAX22210

36V, 3.8A Stepper Motor Driver with Integrated Current Sense and 128 Microstep Indexer

General Description

The MAX22210 is a 2-phase stepper motor driver. It integrates two 36V, $3.8A_{MAX}$ H-bridges.

The H-bridge FETs have very low impedance that result in high driving efficiency and minimal heat generated. The typical total R_{ON} (high side + low side) is 0.25Ω.

The MAX22210 integrates an accurate current drive regulation circuit and a 128-microstep built-in indexer controlled by a STEP/DIR interface. The high microstepping resolution and advanced control technique ensure smooth and quiet operation.

The current flowing into the two low-side FETs is sensed by a nondissipative integrated current sensing (ICS) and it is then compared with the desired step threshold current. As soon as the bridge current exceeds the setpoint (I_{TRIP}), the device enforces decay for a fixed OFF time (T_{OFF}). Three decay modes are supported: slow, mixed, and adaptive.

The nondissipative integrated current sensing eliminates the bulky external power resistors that are normally required for this function resulting in a dramatic space and power saving compared with mainstream applications based on external sense resistors.

The internally sensed phase currents are mirrored on two pins (ISENA, ISENB) to allow the external controller to keep monitoring the currents and can use this information for diagnostic purposes.

The maximum output current per H-bridge is I_{MAX} = $3.8A_{MAX}$, which is limited by the overcurrent protection (OCP).

The maximum RMS current per H-bridge is I_{RMS} = $2A_{RMS}$ at room temperature, assuming a 4-layer PCB. Since this current is limited by thermal considerations, the actual maximum RMS current depends on the thermal characteristic of the application such as PCB ground planes, heatsinks, ventilation, etc.

The maximum full-scale current per H-bridge is I_{FS} = 3A that can be set by an external resistor connected to IREF. This current is defined as the maximum current setting of the embedded current drive regulation circuit.

In applications where the maximum full-scale current is less than 1.5A and high-current control accuracy is desired, the half full scale (HFS) logic input pin can be set high to halve the current ratings and double the low-side FET R_{ON}. This results in better current control accuracy especially for values close to the lower boundary of the current range.

The MAX22210 features overcurrent protection, thermal shutdown (TSD), undervoltage lockout (UVLO). An open-drain, active-low $\overline{FAULT}$ pin is activated every time a fault condition is detected.

During thermal shutdown and UVLO events, the driver is disabled until normal operations are restored.

The MAX22210 is available in small, 5mm x 5mm TQFN32 and 4.4mm x 9.7mm TSSOP28 packages.

Applications

- Stepper Motor Drivers

Benefits and Features

- Two H-Bridges with 36V Rating
  - Total $R_{DS(ON)}$ (HS + LS): 250mΩ at T_A = +25°C (typ)
- Current Ratings per H-Bridge (T_A = +25°C, typ)
  - I_{MAX} = $3.8A_{MAX}$ (Impulsive Current for Driving Small Capacitive Loads)
  - I_{FS} = $3A_{MAX}$ (Full-Scale Current Setting for Internal Current-Drive Regulation)
  - I_{RMS} = $2A_{RMS}$
- Integrated Current Control
  - Full-Scale Current Configurable with External Resistance
  - One Logic Input (HFS) to Improve Current-Control Accuracy for Low Current Values
  - Internal Current Sensing (ICS) Eliminates External Bulky Resistors and Improves Efficiency
  - Built-In Control with 128 Microstep Indexer
    - STEP/DIR Interface
    - Integrated DAC and Lookup Table for Microstepping
  - Multiple Decay Modes (Slow, Mixed, Adaptive)
  - Configurable PWM OFF Time with External Resistance
- Current-Sense Output (Current Monitor) (ISENA, ISENB)
- Fault Indicator Pin ($\overline{FAULT}$)
- Protections
  - Overcurrent Protection (OCP) for Each Power FET
  - UVLO
  - Thermal Shutdown (TSD) T_J = +165°C
- Available in 5mm x 5mm TQFN32 and 4.4mm x 9.7mm TSSOP28 Packages

***Ordering Information** appears at end of data sheet.*

19-101181; Rev 1; 11/23

Simplified Block Diagram

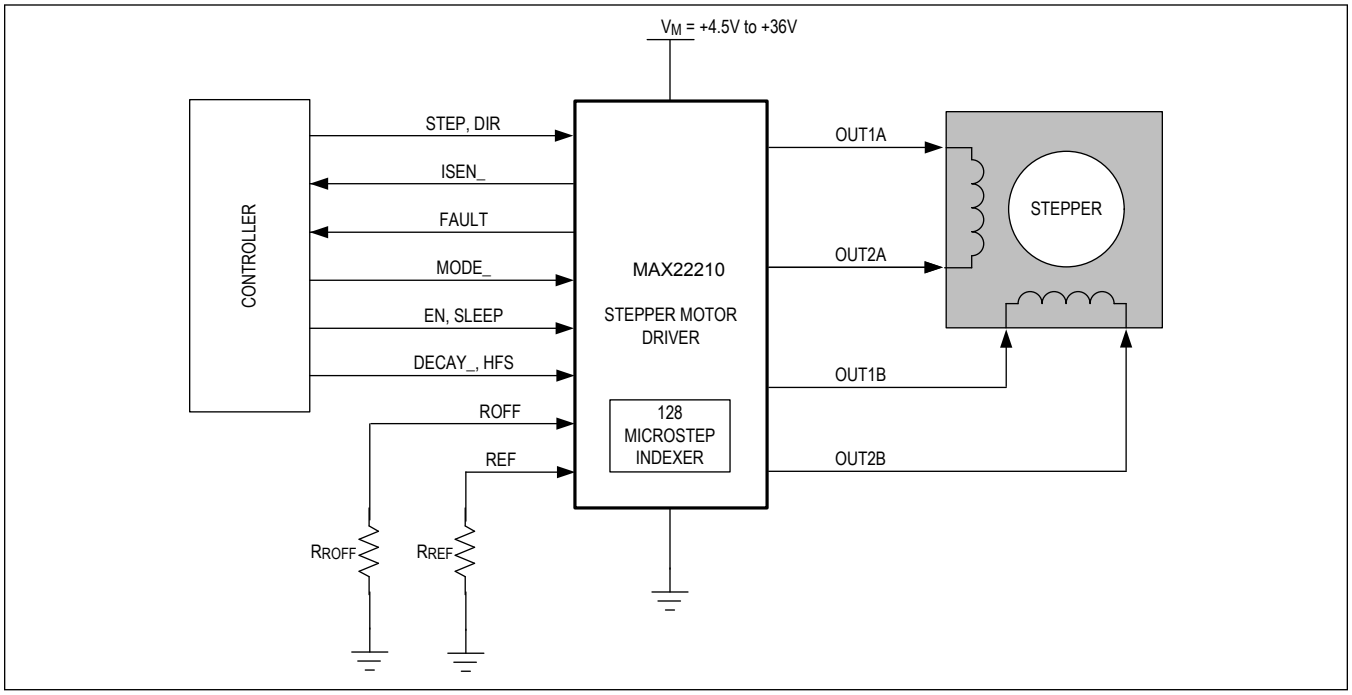


TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Absolute Maximum Ratings

V_M to GND ..... -0.3V to +42V
V_{DD} to GND..... -0.3V to min (+2.2V, V_M + 0.3V)
PGND to GND ..... -0.3V to +0.3V
OUT_..... -0.3V to (V_M + 0.3)V
V_{CP} to GND..... (V_M - 0.3V) to min (+42V, V_M + 6V)
C_{P2} to GND ..... -0.3V to min (+42V, V_M + 0.3V)
C_{P1} to GND ..... (V_M - 0.3V) to min (+42V, V_M + 6V)
FAULT to GND ..... -0.3V to +6V
TRIG_ to GND..... -0.3V to +6V
REF_ to GND ..... -0.3V to min (+2.2V, V_{DD} + 0.3V)
ROFF to GND..... -0.3V to min (+2.2V, V_{DD} + 0.3V)
ISEN_ to GND..... -0.3V to min (+2.2V, V_{DD} + 0.3V)
EN_ to GND..... -0.3V to +6V
STEP, DIR, MODE_ to GND..... -0.3V to +6V
HFS to GND..... -0.3V to +6V
DECAY_ to GND..... -0.3V to +6V
SLEEP to GND ..... -0.3V to min (+42V, V_M + 0.3V)
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +160°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

32-Pin TQFN—5mm x 5mm

Package Code	T3255-8C
Outline Number	21-0140
Land Pattern Number	90-0013
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	47°C/W
Junction to Case (θ_{JC})	1.7°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	29°C/W
Junction to Case (θ_{JC})	1.7°C/W

28-Pin TSSOP—4.4mm x 9.7mm

Package Code	U28E+5C
Outline Number	21-0108
Land Pattern Number	90-0147
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	24.65°C/W
Junction to Case (θ_{JC})	1.52°C/W

For the latest package outline information and land patterns (footprints), go to ***www.maximintegrated.com/packages***. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to ***www.maximintegrated.com/thermal-tutorial***.

Electrical Characteristics

(V_M = +4.5V to +36V, R_{ROFF} = from 15kΩ to 120kΩ , R_{REF} = from 12kΩ to 60kΩ , HFS = 0V, typical values are T_A = +25°C and V_M = +24V, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply-voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. *Note 1*.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply-Voltage Range	V_M		4.5		36	V

Electrical Characteristics (continued)

(V_M = +4.5V to +36V, R_{ROFF} = from 15kΩ to 120kΩ , R_{REF} = from 12kΩ to 60kΩ , HFS = 0V, typical values are T_A = +25°C and V_M = +24V, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply-voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. *Note 1*.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Sleep-Mode Current Consumption	I_{VM}	$\overline{SLEEP}$ = logic low		4	11	µA
Quiescent Current Consumption	I_{VM}	$\overline{SLEEP}$ = logic high		2	4	mA
1.8V Regulator Output Voltage	V_{VDD}	V_M = +4.5V, I_{LOAD} = internal consumption	1.74	1.8	1.86	V
V_{DD} Current Limit	$I_{V18(LIM)}$		20			mA
V_{DD} UVLO Rising	$UVLOV18_R$	V_{DD} rising	1.59	1.65	1.69	V
V_{DD} UVLO Falling	$UVLOV18_F$	V_{DD} falling	1.535	1.58	1.635	V
Charge-Pump Voltage	V_{CP}			V_M + 2.7		V
LOGIC LEVEL INPUTS/OUTPUTS						
Input Voltage Level—High	V_{IH}		1.2			V
Input Voltage Level—Low	V_{IL}				0.65	V
Input Hysteresis	V_{HYS}			110		mV
Pull-Down Current	I_{PD}	To GND	16	34	50	µA
Open-Drain Output Logic-Low Voltage	V_{OL}	I_{LOAD} = 5mA			0.2	V
Open-Drain Output Logic-High Leakage Current	I_{OH}	V_{PIN} = 3.3V	-1		+1	µA
$\overline{SLEEP}$ Voltage Level High	$V_{IH(\overline{SLEEP})}$		0.9			V
$\overline{SLEEP}$ Voltage Level Low	$V_{IL(\overline{SLEEP})}$				0.6	V
$\overline{SLEEP}$ Pull-Down Input Resistance	$R_{PD(\overline{SLEEP})}$		0.8	1.5		MΩ
OUTPUT SPECIFICATIONS						
Output On-Resistance Low-Side	$R_{ON(LS)}$	HFS = logic low		0.125	0.22	Ω
		HFS = logic high		0.22	0.42	
Output On-Resistance High-Side	$R_{ON(HS)}$			0.125	0.22	Ω
Output Leakage	I_{LEAK}	Driver off	-5		+5	µA
Dead Time	t_{DEAD}			100		ns
Output Slew Rate	SR			200		V/µs
PROTECTION CIRCUITS						
Overcurrent Protection Threshold	I_{OCP}		3.8			A
Overcurrent Protection Blanking Time	t_{OCP}		0.4	0.85	1.3	µs
Autoretry OCP Time	t_{RETRY}			3		ms

Electrical Characteristics (continued)

(V_M = +4.5V to +36V, R_{ROFF} = from 15kΩ to 120kΩ , R_{REF} = from 12kΩ to 60kΩ , HFS = 0V, typical values are T_A = +25°C and V_M = +24V, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply-voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Note 1.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UVLO Threshold on V_M	V_{UVLO}	V_M rising	3.85	4	4.15	V
UVLO Threshold on V_M Hysteresis	$UVLO_{HYS}$			0.12		V
Thermal Protection Threshold Temperature	TSD			+165		°C
Thermal Protection Temperature Hysteresis	TSD_{HYS}			20		°C
CURRENT REGULATION						
REF pin Resistor range	R_{REF}		12		60	kΩ
REF Output Voltage	V_{REF}		0.882	0.9	0.918	V
I_{TRIP} Current Regulation Constant	K_{IFS}	HFS = logic low		36		KV
		HFS = logic high		18.4		
Current Trip Regulation Accuracy	DITRIP1	HFS = logic low, I_{OUT} = 1.1A to 3A, GBD	-5	0.4	5	%
		HFS = logic high, I_{OUT} = 0.55A to 1.5A, GBD	-5	0.4	5	
	DITRIP2	HFS = logic low, I_{OUT} = 0.5A to 1.1A, GBD	-10	0.5	10	
		HFS = logic high, I_{OUT} = 0.25A to 0.55A, GBD	-10	0.5	10	
Fixed OFF – Time Internal	t_{OFF}	ROFF shorted to V_{DD}	16	20	24	µs
Fixed OFF – Time Constant	K_{TOFF}	R_{ROFF} from 15kΩ to 120kΩ		0.667		µs/kΩ
PWM Blanking Time	t_{BLK}		0.6	1.2	1.8	µs
CURRENT-SENSE MONITOR						
ISEN_ Voltage Range	ISEN	Voltage range at ISEN_ pins	0		1.1	V
Current-Monitor Scaling Factor	K_{ISEN}	HFS = logic low. See the I_{SEN} output-current equation in the Current Sense Output (ISEN) - Current monitor section.		7500		A/A
		HFS = logic high. See the I_{SEN} output-current equation in the Current Sense Output (ISEN) - Current monitor section.		3840		
Current-Monitor Accuracy	$DKISEN_1$	(Note 1) HFS = logic low, I_{OUT} = 0.7A to 3A	-5	0.4	+5	%
		(Note 1) HFS = logic high, I_{OUT} = 0.35A to 1.5A	-5	0.4	+5	
	$DKISEN_2$	(Note 1) HFS = logic low, I_{OUT} = 0.4A to 0.7A	-10	0.6	+10	
		(Note 1) HFS = logic high, I_{OUT} = 0.2A to 0.35A	-10	0.6	+10	

Electrical Characteristics (continued)

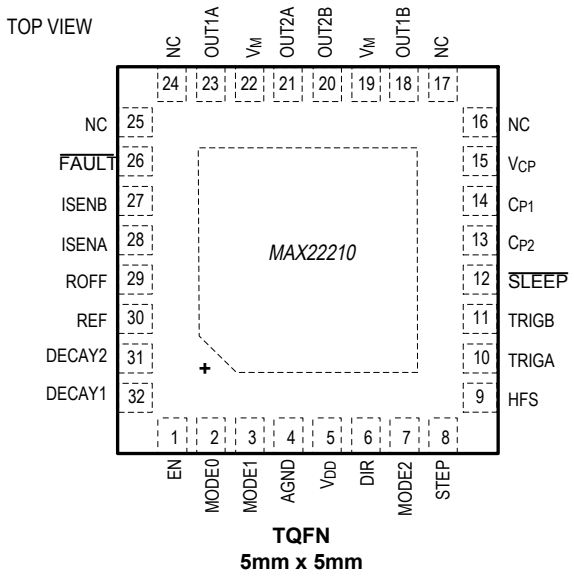
(V_M = +4.5V to +36V, R_{ROFF} = from 15kΩ to 120kΩ , R_{REF} = from 12kΩ to 60kΩ , HFS = 0V, typical values are T_A = +25°C and V_M = +24V, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply-voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. *Note 1*.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current-Sense Output -3dB Small-Signal Bandwidth	BW			400		KHz
FUNCTIONAL TIMING						
Sleep Time	t_{SLEEP}	$\overline{SLEEP}$ = logic 1 to logic 0 for OUT_ to become three-state			150	µs
Wake-Up Time from Sleep	t_{WAKE}	$\overline{SLEEP}$ = logic 0 to logic 1 to resume normal operation			3	ms
Enable Time	t_{EN}	Time from EN_ pin rising edge to driver on			0.4	µs
Disable Time	t_{DIS}	Time from EN_ pin falling edge to driver off			0.6	µs
INDEXER TIMING						
STEP High Time	t_{STH}		1			µs
STEP Low Time	t_{STL}		1			µs
Setup Time MODE, DIR to STEP	t_{SETUP}		1			µs
Hold Time MODE, DIR to STEP	t_{HOLD}		1			µs

Note 1: Guaranteed by design, not production tested.

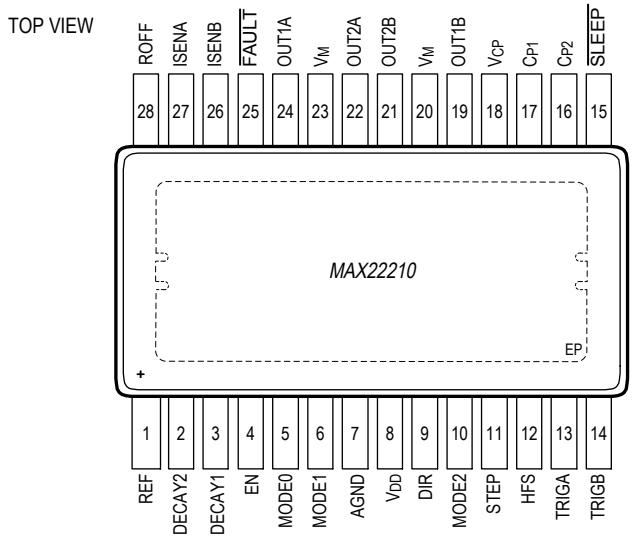
Pin Configurations

TQFN Pin Configuration



TQFN
5mm x 5mm

TSSOP Pin Configuration



TSSOP28
4.4x9.7mm

Pin Description

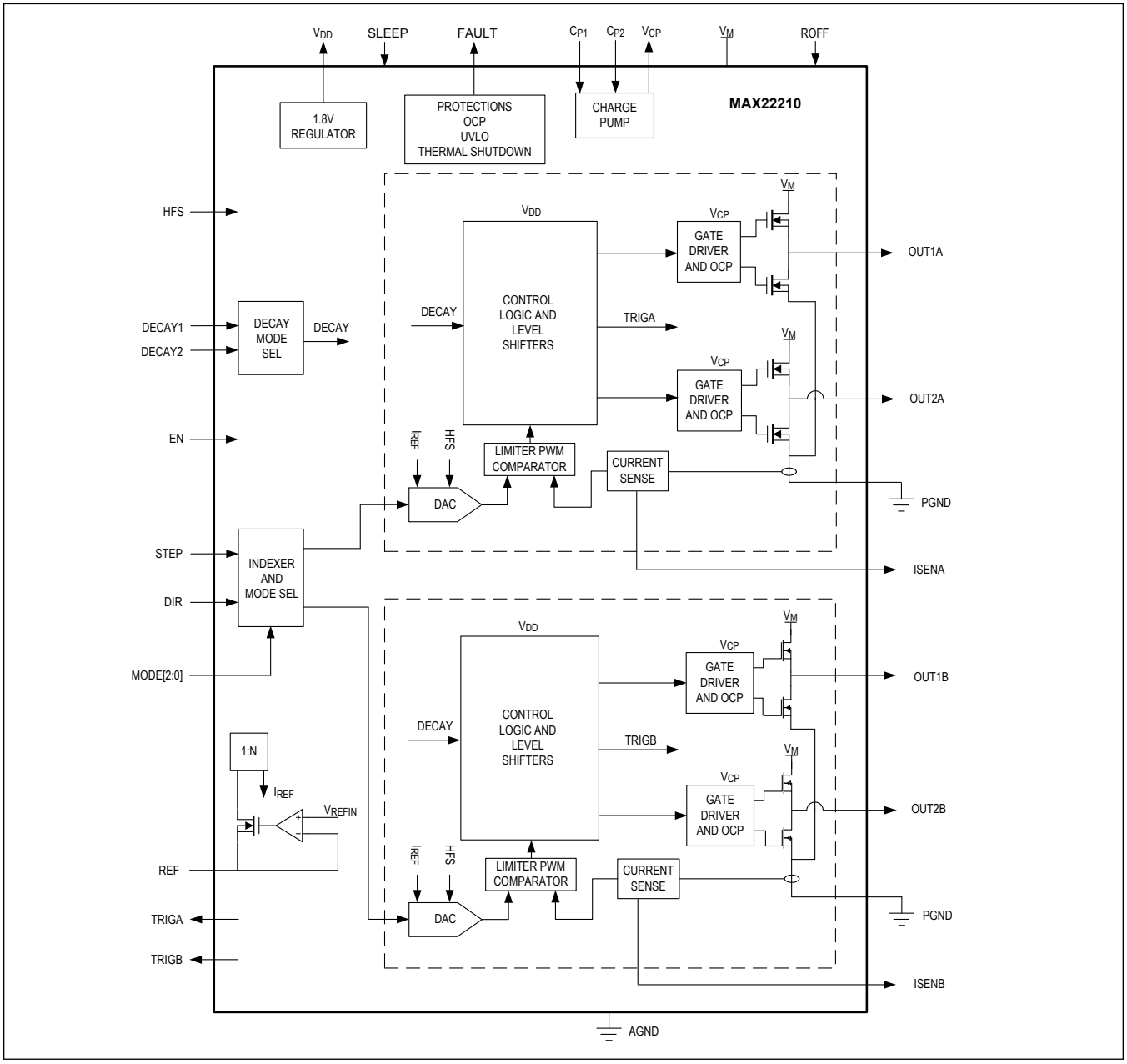
PIN		NAME	FUNCTION	TYPE
TQFN	TSSOP			
30	1	REF	Programmable Current Analog Input. Connect a resistor from REF to GND to set the full scale current.	Analog Input
29	28	ROFF	OFF Time (t_{OFF}) Programmable Resistor Pin. Connect ROFF to V_{DD} to use the internal fixed t_{OFF} time. Connect a resistor from ROFF to GND to set the fixed OFF time to a desired value.	Analog Input
26	25	$\overline{FAULT}$	Active-Low, Open-Drain, Output Fault Indicator. $\overline{FAULT}$ goes low to indicate that one or more of the protection mechanisms has been activated. Connect a pull-up resistor from $\overline{FAULT}$ to the microcontroller supply voltage.	Open Drain Output
10, 11	13, 14	TRIG_	Open Drain Output. ISEN Trigger Output.	
4	7	AGND	Analog Ground. Connect to ground plane.	GND
19, 22	20, 23	V_M	Supply Voltage Input. Connect a V_M-rated 1µF (minimum) surface-mounted device capacitor from V_M to GND close to the device, and a 10µF (minimum) electrolytic bypass capacitor from V_M to GND. Higher values can be considered depending on application requirements.	Supply

Pin Description (continued)

PIN		NAME	FUNCTION	TYPE
TQFN	TSSOP			
5	8	V_{DD}	1.8V Linear Regulator Output. Bypass V_{DD} with a 2.2µF capacitor connected close to the device.	Output
23, 21, 18, 20	24, 22, 19, 21	OUT1 to OUT4, respectively	Driver Outputs	Output
27, 28	26, 27	ISEN_	Current Sense Output Monitor.	Output
1	4	EN	Logic Input Pin. Enable Pin.	Logic Input
15	18	V_{CP}	Charge-Pump Output. Connect a 1µF capacitor between V_{CP} and V_M as close as possible to the device.	Output
14	17	C_{P1}	Charge-Pump Flying Capacitor Pin 1. Connect a 22nF capacitor between CP1 and CP2, as close as possible to the device.	Output
13	16	C_{P2}	Charge-Pump Flying Capacitor Pin 2. Connect a 22nF capacitor between CP1 and CP2, as close as possible to the device.	Output
12	15	$\overline{SLEEP}$	Active-Low Sleep Pin	Logic Input
31, 32	2, 3	DECAY_	Logic Input. Set the Decay Mode.	Logic Input
9	12	HFS	Set Output Current Full Scale. HFS = 0 coefficient is 100%. HFS = 1 coefficient is 50%.	Logic Input
8	11	STEP	Logic Input. Indexer Step logic input. Indexer advances on rising edges of the STEP pin.	Logic Input
6	9	DIR	Logic Input. Direction Pin.	Logic Input
2, 3, 7	5, 6, 10	MODE_	Logic Input Pins. Set the Decay Mode for the current drive regulation circuit.	Logic Input
EP	EP	PGND	Power GND. Connect to ground plane. The thermal exposed pad (EP) is also the electrical power GND pin and must be properly connected to GND.	GND

Functional Diagrams

Diagram



Detailed Description

The MAX22210 is a two-phase stepper motor driver. It integrates two 36V, $3.8A_{MAX}$ H-Bridges.

The H-Bridge FETs have very low impedance resulting in high driving efficiency and minimal heat generated. The typical total R_{ON} (high side + low side) is 0.25Ω.

The MAX22210 integrates an accurate current drive regulation circuit and a 128-microstep built-in Indexer controlled by a STEP/DIR interface. The high microstepping resolution and advanced control technique ensure smooth and quiet operations.

The current flowing into the two low-side FETs is sensed by a non-dissipative Integrated Current Sensing (ICS) and it is then compared with the desired step threshold current. As soon as the bridge current exceeds the setpoint (I_{TRIP}), the device enforces decay for a fixed OFF-time (T_{OFF}). Three different decay modes are supported (slow decay, mixed decay, adaptive decay).

The non-dissipative ICS eliminates the bulky external power resistors which are normally required for this function resulting in a dramatic space and power saving compared with mainstream applications based on external sense resistors.

The internally sensed phase currents are mirrored on two pins (ISENA, ISENB) to allow the external controller to keep monitoring the currents and possibly use this information for diagnostic purposes.

The maximum output current per H-Bridge is $I_{MAX} = 3.8A_{MAX}$ limited by the Overcurrent Protection (OCP).

The maximum RMS current per H-Bridge is $I_{RMS} = 2A_{RMS}$ at room temperature assuming a 4-layer PCB. Since this current is limited by thermal considerations, the actual maximum RMS current would depend on the thermal characteristic of the application (PCB ground planes, heatsinks, ventilation, etc.).

The maximum full-scale current per H-Bridge is I_{FS} = 3A and can be set by an external resistor connected to IREF. This current is defined as the maximum current setting of the embedded current drive regulation circuit.

In applications in which the requirement of maximum full-scale current is less than 1.5A and high current control accuracy is desired, the half full-scale (HFS) logic input pin can be set high to halve the current ratings and double the low-side FET R_{ON}. This results in better current control accuracy, especially for values close to the lower boundary of the current range.

The MAX22210 features Overcurrent Protection (OCP), thermal shutdown (TSD), UVLO. An open drain active low $\overline{FAULT}$ pin is activated every time a fault condition is detected.

During thermal shutdown and UVLO events, the driver is disabled until normal operations are restored.

The MAX22210 is available in a small TQFN32 5mm x 5mm package or a TSSOP28 4.4mm x 9.7mm package.

Sleep Mode ($\overline{SLEEP}$ Pin)

The $\overline{SLEEP}$ pin can be driven low to place the device into the lowest power-consumption mode possible, with all outputs three-stated, the internal circuits biased off, and the charge pump disabled. A pull-down resistor should be connected between $\overline{SLEEP}$ and GND to ensure the part is disabled whenever this pin is not actively driven. Driving the $\overline{SLEEP}$ pin high wakes up the device and returns it to normal mode. t_{WAKE} is 3ms (max).

Enable Function (EN Pin)

This input ENABLE/DISABLE the output power FETs. Drive EN low to three-state the two full bridges. Drive EN high to enable the outputs. The internal sequencer (indexer) remains active even when EN is set low.

Indexer Control Modes

The MAX22210 features an integrated Indexer which supports several different step modes. Logic inputs MODE[2:0] select the step mode as shown in Table 1.

Table 1. Step Mode Selection

MODE2	MODE1	MODE0	STEP MODE

Table 1. Step Mode Selection (continued)

0	0	0	Full Step (71% current)
0	0	1	½ step
0	1	0	¼ step
0	1	1	1/8 step
1	0	0	1/16 step
1	0	1	1/32 step
1	1	0	1/64 step
1	1	1	1/128 step

Current Sense Output (ISEN) - Current Monitor

Currents proportional to the phase currents are mirrored to pins ISENA and ISENB for the H-bridge A and B, respectively. The current is sensed when one of the two low-side FETs sinks the output current and it is therefore meaningful both during the energizing (T_{ON}) phase and during the Slow Decay phase (Brake). During the blanking time, the ISEN current is held constant. In Fast Decay, the current is not monitored and ISEN outputs a zero current.

The following equation shows the relationship between the current sourced at ISEN and the output current.

$$I_{ISEN}(A) = \frac{I_{OUT}(A)}{K_{ISEN}}$$

Equation - ISEN Output Current

where K_{ISEN} represents the current scaling factor between the output current and its replica at pin ISEN. K_{ISEN} is typically 7500 A/A when HFS = 0 and 3840 A/A when HFS = 1. For instance, if the instantaneous output current is 2A, the current sourced at ISEN is 266µA.

By connecting an external signal resistor, R_{ISEN}, between ISEN_ and GND, voltages proportional to the motor currents are generated and can input an external ADC. The controller can use the phase current information for diagnostic purposes.

The MAX22210 outputs two trigger signals on the open drain output pins TRIGA and TRIGB. These signals can be used to trigger an external ADC allowing a correct sampling of the ISEN current . The TRIG_ are pulled up by an external resistor (logic high status) during the energizing phase (ON) and actively driven to logic low during the decay phase (OFF). The TRIG_ signals are driven high while the coil is energized (T_{ON}). It is recommended inserting a blanking time just after the rising edge of the TRIG_ signal to avoid sampling transient currents due to the commutation of the power FETs. The blanking time duration is application dependent but it is typically in the range of 1µs.

The TRIG_ signal is also representative of the PWM duty cycle applied to the stepper motor. The user can choose to process this information for diagnostic purposes such as detection of stall conditions or misbehavior of the stepper motor.

Figure 1 shows an idealized behavior of the ISEN current and of the TRIG signal for Slow Decay (Case A) and Mixed Decay (Case B). Analog delays and rise/fall edges have been ignored.

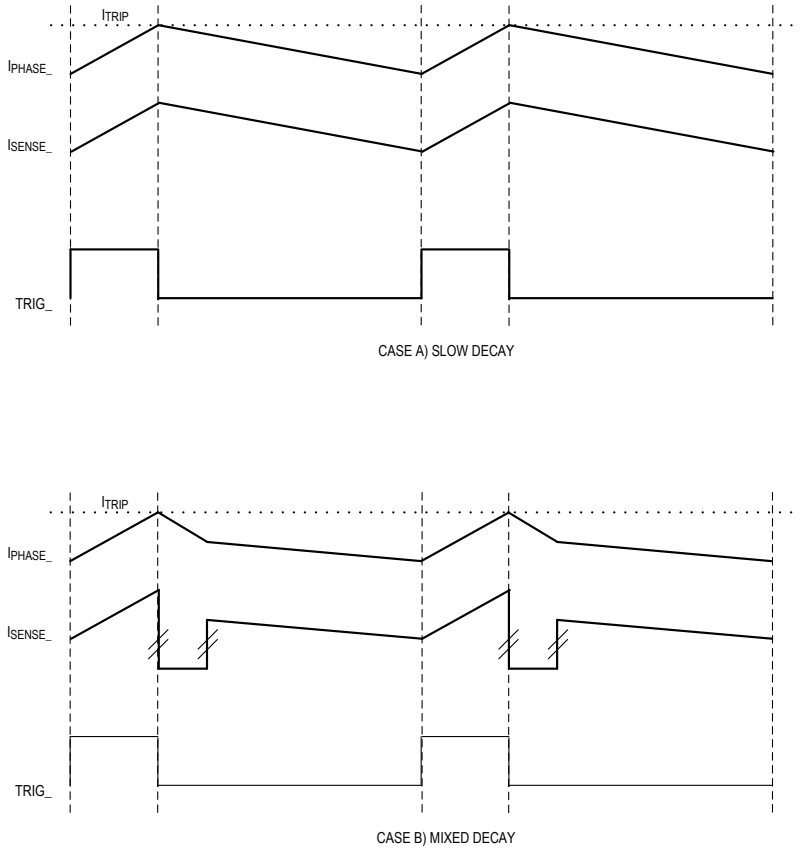


Figure 1. ISEN Current

Current Drive Regulation

The MAX22210 features embedded current drive regulation (CDR). The embedded CDR provides an accurate control of the current flowing into the motor windings. The bridge current is sensed by a non-dissipative Integrated Current Sensing (ICS) circuit and it is then compared with the threshold current (I_{TRIP}). As soon as the bridge current exceeds the threshold, the device enforces the decay for a fixed OFF-time (t_{OFF}). The device supports different decay modes as described in the following paragraphs. Once t_{OFF} has elapses, the driver is re-enabled for the next PWM cycle. During current regulation, the PWM duty cycle and frequency depend on the supply voltage, on the motor inductance, and on motor speed and load conditions. The t_{OFF} duration can be configured with an external resistor connected to the ROFF pin.

Setting the Full-Scale Current – Pin REF

Connect a resistor from REF to GND to set the full-scale current I_{FS}.

The equation below shows the full-scale current as a function of the R_{REF} shunt resistor connected to pin REF. The proportionality constant K_{IFS} depends on the status of the HFS logic pin. The external resistor R_{REF} can range between 12kΩ and 60kΩ.

When HFS is driven to logic low, the K_{IFS} is equal to 36KV and the power FETs Rdson is set to a minimum (0.25Ω - High Side plus Low Side).

When the HFS is driven to logic high, the K_{IFS} is equal to 18.4kV and the power FETs have higher Rdson (0.375Ω - High Side plus Low Side). This operating mode is recommended for applications in which the maximum current does not exceed 1.5A and high accuracy at low current is highly desirable.

$$I_{FS} = \frac{K_{IFS(KV)}}{R_{REF(K\Omega)}}$$

Equation - Full Scale Current

The Table 2 summarizes the HFS settings.

Table 2. HFS Truth Table

HFS	IFS (%)	MAXIMUM FS SETTING	TYPICAL $R_{DS(ON)}$ (HIGH-SIDE + LOW-SIDE)	NOTES
0	100%	3A	0.25Ω	Optimized efficiency and extended operating range up to $3A_{FS}$
1	50%	1.5A	0.375Ω	Reduced operating range up to $1.5A_{FS}$. Improved current accuracy control in the low current range

Bridge Current Control - Indexer

The Step Mode is determined by the logic inputs MODE[2:0] (see Table 1).

The MAX22210 features a built-in Indexer which supports up to 128 microsteps. The indexer sets the bridge currents in the two phases for each Step Mode.

At each pulse applied to the STEP pin, the sequencer of the device is increased (DIR input high) or decreased (DIR input low).

Table 3 shows the look-up table for each step mode up to 32 microstepping. Higher microstepping modes, such as 64 or 128 microstepping are supported and follow a similar pattern with higher step angle resolution.

When the driver is enabled or after exiting sleep mode, the indexer is initialized at its "home state" which corresponds to 45° angle. At each rising edge of the STEP input, the indexer moves to the next or previous state in the table for DIR = 1 or DIR = 0, respectively.

After a step mode change, rising edges of the STEP logic input cause the indexer to proceed accordingly with the former step mode until the first valid state of the new step mode is found. From that moment on, the indexer starts stepping accordingly with the new step mode.

Table 3. Look Up Table up to 32 Microsteps

1/32 STEPPING	1/16 STEPPING	1/8 STEPPING	1/4 STEPPING	1/2 STEPPING	FULL STEPPING	COIL A	COIL B	STEP ANGLE
1	1	1	1	1		100.0%	0.0%	0
2						99.9%	4.9%	3
3	2					99.5%	9.8%	6
4						98.9%	14.7%	8
5	3	2				98.1%	19.5%	11
6						97.0%	24.3%	14

Table 3. Look Up Table up to 32 Microsteps (continued)

7	4					95.7%	29.0%	17
8						94.2%	33.7%	20
9	5	3	2			92.4%	38.3%	23
10						90.4%	42.8%	25
11	6					88.2%	47.1%	28
12						85.8%	51.4%	31
13	7	4				83.1%	55.6%	34
14						80.3%	59.6%	37
15	8					77.3%	63.4%	39
16						74.1%	67.2%	42
17	**9**	**5**	**3**	**2**	**1**	**70.7%**	**70.7%**	**45**
18						67.2%	74.1%	48
19	10					63.4%	77.3%	51
20						59.6%	80.3%	53
21	11	6				55.6%	83.1%	56
22						51.4%	85.8%	59
23	12					47.1%	88.2%	62
24						42.8%	90.4%	65
25	13	7	4			38.3%	92.4%	68
26						33.7%	94.2%	70
27	14					29.0%	95.7%	73
28						24.3%	97.0%	76
29	15	8				19.5%	98.1%	79
30						14.7%	98.9%	82
31	16					9.8%	99.5%	84
32						4.9%	99.9%	87
32	17	9	5			0.0%	100.0%	90

Setting the Fixed OFF Time (t_{OFF})

The current regulation circuit is based on a constant t_{OFF} PWM control. If during the ON phase, the bridge current exceeds the target I_{TRIP} threshold, the OFF phase begins and the current decays. The OFF phase has a fixed time duration t_{OFF}.

The t_{OFF} can be configured to a desired value by connecting an external resistor to pin ROFF. When the ROFF pin is shorted to V_{DD}, the t_{OFF} time is internally set at a fixed value (20µs typical). By connecting an external resistor to the pin ROFF, the user can configure t_{OFF} as shown in the following equation in which R_{ROFF} is an external resistor (in kΩ) connected from the ROFF pin to GND and K_{TOFF} is an internal constant equal to 0.667µs/kΩ.

$$t_{OFF}(\mu s) = R_{ROFF} \times K_{TOFF}$$

The t_{OFF} can be programmed from a range of 10µs to 80µs.

Setting the Decay Mode

Two logic input pins allow the user to configure the decay mode during T_{OFF}. The MAX22210 supports slow and mixed decay mode. An adaptive decay mode is also provided. The adaptive decay mode automatically calculates the optimal ratio between the slow and fast decay as explained in the *Adaptive Decay Mode* section.

Table 4 shows the Truth Table for the Decay Mode selection.

Table 4. Decay Mode Truth Table

DECAY2	DECAY1	INCREASING STEPS	DECREASING STEPS
0	0	Slow	Slow
0	1	Mixed 30% Fast	Mixed 30% Fast
1	0	Mixed 60% Fast	Mixed 60% Fast
1	1	Adaptive	Adaptive

Adaptive Decay Mode

The MAX22210 features one adaptive decay mode.

When the adaptive decay mode is used the MAX22210 dynamically determines the ratio between slow and fast decay.

The algorithm is based on current measurements during the energizing phase (TON) and during the slow decay phase (TSLOW).

The algorithms distinguish the following three operating conditions:

- Tracking Up Phase: As a consequence of a STEP command, the current needs to be quickly increased to a new upper target level (STEP UP).
- Tracking Down Phase: As a consequence of a STEP command, the current needs to be quickly decreased to a new lower target level (STEP DW).
- Settling/Steady-State Phase: Once a current target level is reached, the current stabilizes. Ripple must be minimized.

When a Step Up command is received, the previous cycle is completed and then an ON Time (t_{ON}) is enforced until the current reaches the new target level. See Figure 2.

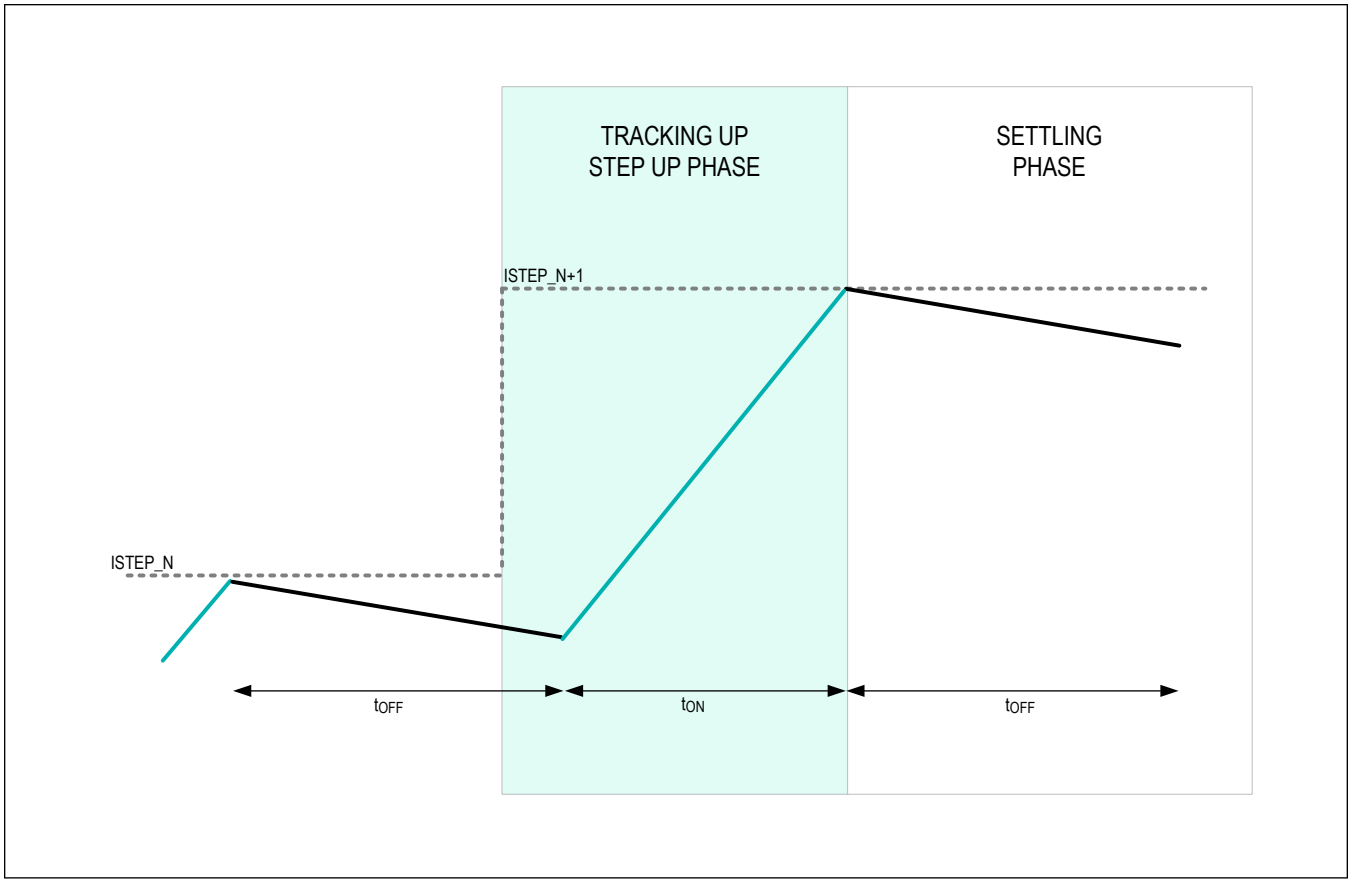


Figure 2. Adaptive Decay Step Up

When a Step Down command is received, a mixed mode with 30% Fast is enforced for fast tracking. When during a Slow Decay Interval the current is found lower than the new target, a t_{ON} phase in enforced causing the current to reach the desired level.

During the Settling/Steady-State Phase, variable fixed slow decay ratios are used with the purpose of minimizing the ripple. Initially, a slow decay is enforced for a fixed OFF time (t_{OFF}). In the following cycles, the ON time interval (t_{ON}) is monitored cycle by cycle. If t_{ON} is found equal to $t_{ON(MIN)}$, then a mixed mode with 10% fast decay is applied to the next chopping cycle.

- The fast decay percentage dynamically increases with +10% steps if t_{ON} in the previous cycle was found equal to $t_{ON(MIN)}$.
- The fast decay percentage dynamically decreases with -10% steps if t_{ON} in the previous cycle was found longer than $t_{ON(MIN)}$.

To facilitate the convergence of the algorithm, the fast decay percentage is not allowed to go back below 10%.

The Figure 3 graphically illustrates the behavior.

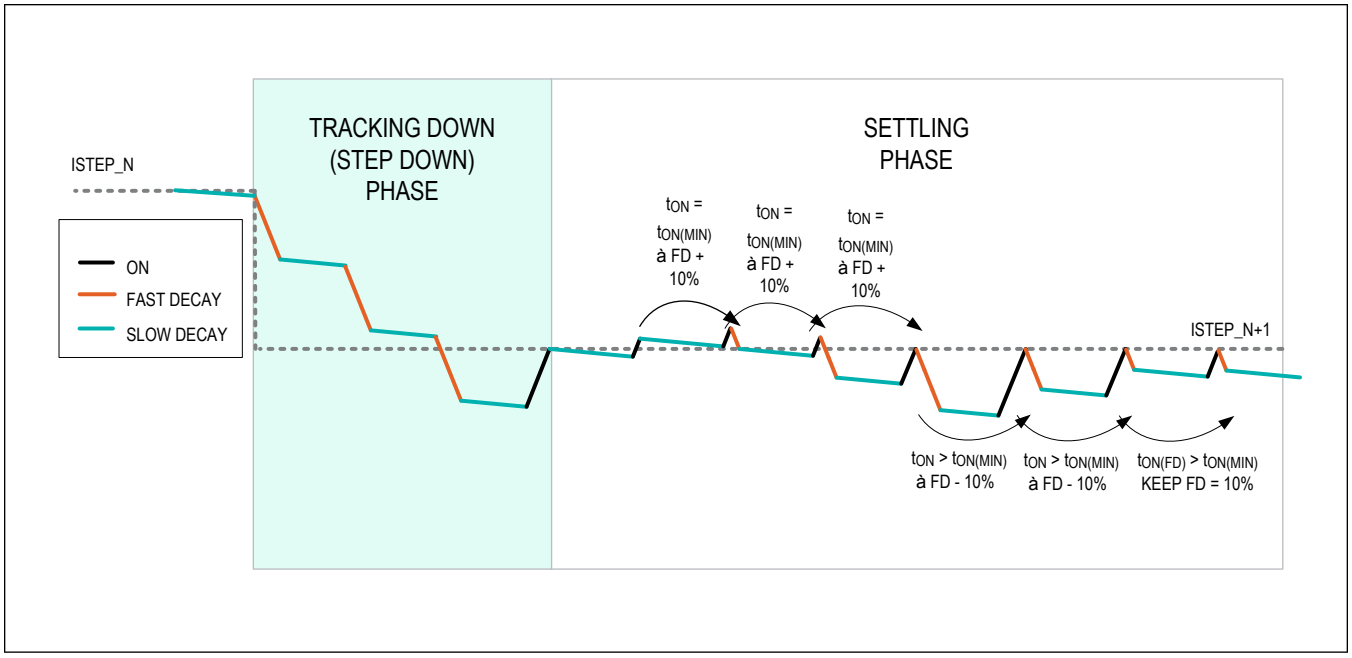


Figure 3. Adaptive Decay - Algorithm

Fault Protection

Overcurrent Protection

Overcurrent protection protects the device against short circuits to the rails (supply voltage and ground) and between the outputs (OUT1_ and OUT2_). The OCP threshold is set at 3.8A minimum. If the output current is greater than the OCP threshold for longer than the Overcurrent Protection Blanking Time (t_{OCP}), then an OCP event is detected.

When an OCP event is detected, the H-bridge is immediately disabled, and a fault indication is output on pin $\overline{FAULT}$. The H-bridge is kept in HiZ mode for 3ms (see t_{RETRY} specification). After that, the H-bridge is re-enabled according to the current state of the inputs. If the short circuit is still present, this cycle repeats otherwise normal operation resumes. Prolonged operation in a short-circuit failure mode is not recommended. Prolonged OCP events can affect the device reliability.

Thermal-Shutdown Protection

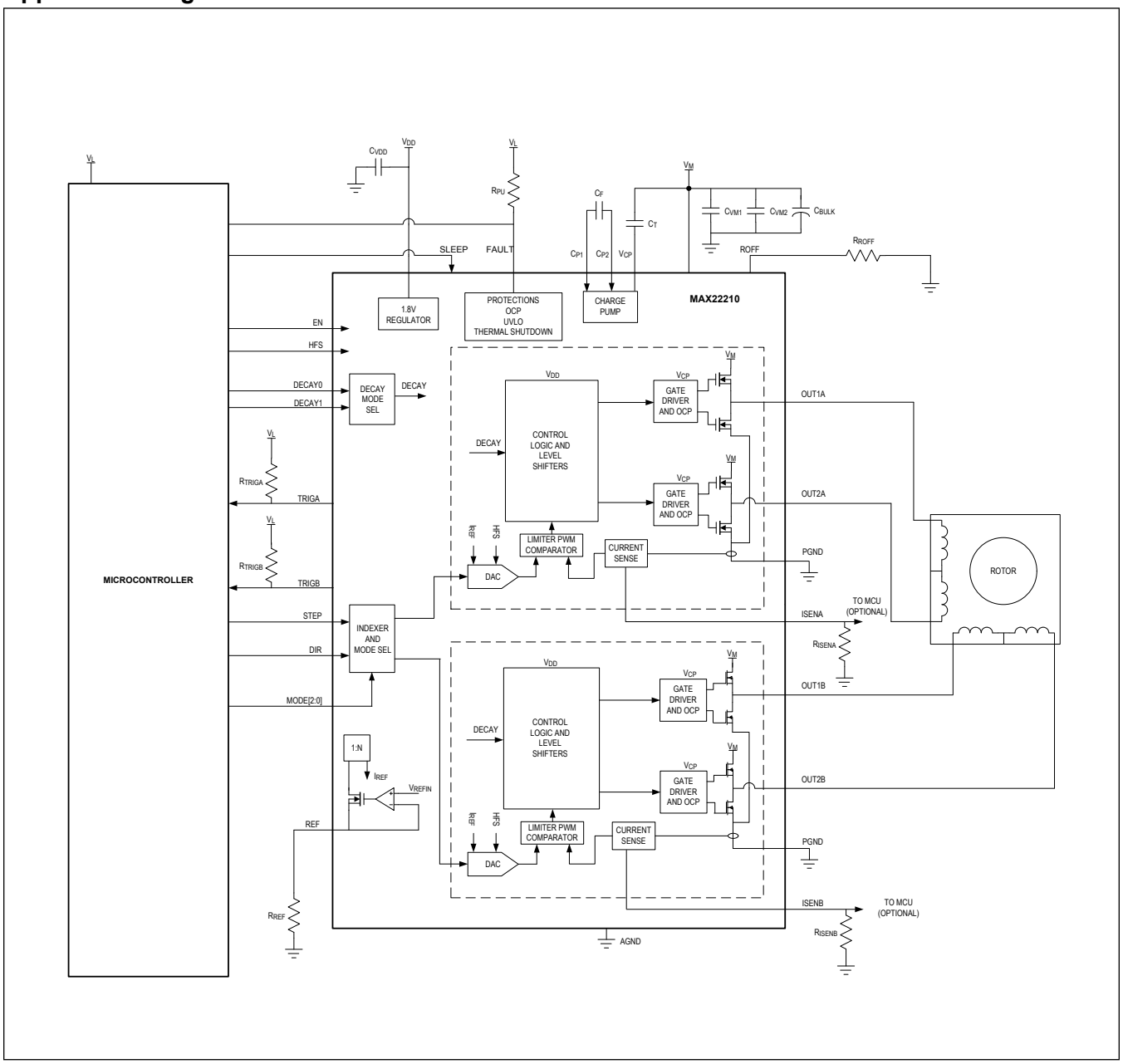
If the die temperature exceeds T_{SD} = +165°C (typ), all output pins (OUT1–OUT4) are three-stated and the $\overline{FAULT}$ pin is driven low. The $\overline{FAULT}$ pin remains low and the outputs are placed in three-state mode until the die temperature falls by the hysteresis amount of 20°C (typ), after which the $\overline{FAULT}$ pin is driven high and the outputs are re-enabled.

Undervoltage-Lockout Protection

When the V_M supply voltage is below the UVLO threshold, all OUT_ outputs are three-stated and the $\overline{FAULT}$ pin is driven low. The OUT_ outputs automatically return to their current state (defined by EN_ and DIN_) when the V_M supply voltage exceeds the OVLO threshold (max) and $\overline{FAULT}$ is driven high.

Typical Application Circuits

Application Diagram



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE
MAX22210ATJ+	-40°C to +125°C	32 TQFN - 5mm x 5mm
MAX22210AUI+	-40°C to +125°C	28 TSSOP - 4.4mm x 9.7mm

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/23	Release for Market Intro	—
1	11/23	Updated *Absolute Maximum Ratings*, *Package Information*, *Electrical Characteristics*, *Pin Configurations*, *Detailed Description*, and *Ordering Information* sections	6, 7, 8, 9, 11, 12, 14, 21, 23