

# 3.3 V/5 V ECL Quad 4-Input OR/NOR

## MC100EP101

### Description

The MC100EP101 is a Quad 4-input OR/NOR gate. The device is functionally equivalent to the E101. With AC performance faster than the E101 device, the EP101 is ideal for applications requiring the fastest AC performance available.

The 100 Series contains temperature compensation.

### Features

- 250 ps Typical Propagation Delay
- Maximum Frequency > 3 GHz Typical
- PECL Mode Operating Range:  $V_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$  with  $V_{EE} = 0\text{ V}$
- NECL Mode Operating Range:  $V_{CC} = 0\text{ V}$  with  $V_{EE} = -3.0\text{ V}$  to  $-5.5\text{ V}$
- Open Input Default State
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



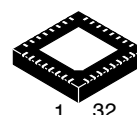
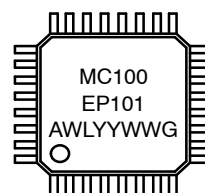
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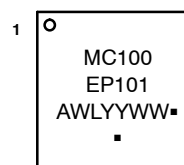
### MARKING DIAGRAMS\*



**LQFP-32**  
**FA SUFFIX**  
**CASE 561AB**



**QFN32**  
**MN SUFFIX**  
**CASE 488AM**



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G or ■ = Pb-Free Package

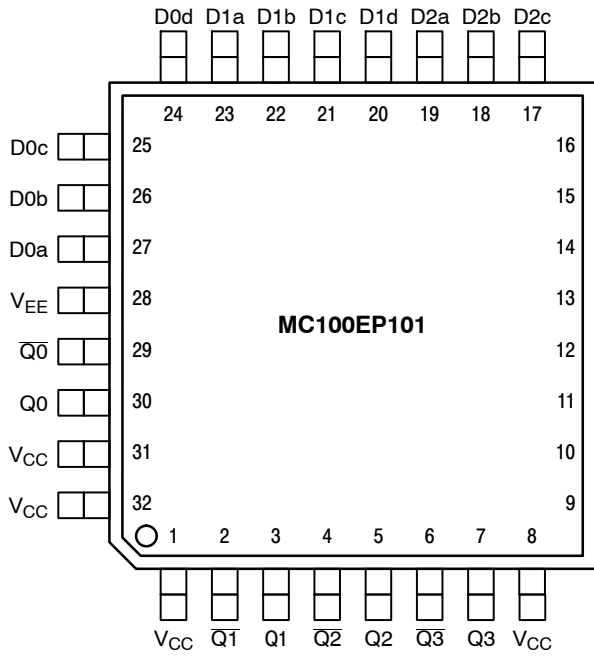
(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note [AND8002/D](#).

### ORDERING INFORMATION

Device	Package	Shipping
MC100EP101FAG	LQFP-32 (Pb-Free)	250 Units / Tray
MC100EP101MNG	QFN-32 (Pb-Free)	74 Units / Tube

# MC100EP101



Warning: All V<sub>CC</sub> and V<sub>EE</sub> pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 32-Lead LQFP Pinout (Top View)

Table 1. PIN DESCRIPTION

PIN	FUNCTION
D0a*–D3d*	ECL Data Inputs
Q0–Q3, Q0–Q3	ECL Data Outputs
V <sub>CC</sub>	Positive Supply
V <sub>EE</sub>	Negative Supply
NC	No Connect
EP for QFN–32, only	The Exposed Pad (EP) on the QFN–32 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is electrically connected to V <sub>EE</sub> .

\* Pins will default LOW when left open.

Table 2. TRUTH TABLE

Dna	Dnb	Dnc	Dnd	Qn	Qn
L	L	L	L	L	H
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L
H	H	H	H	H	L

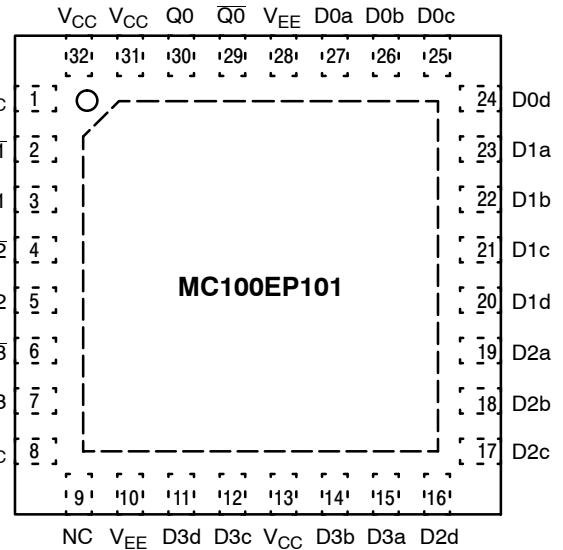


Figure 2. 32-Lead QFN Pinout (Top View)

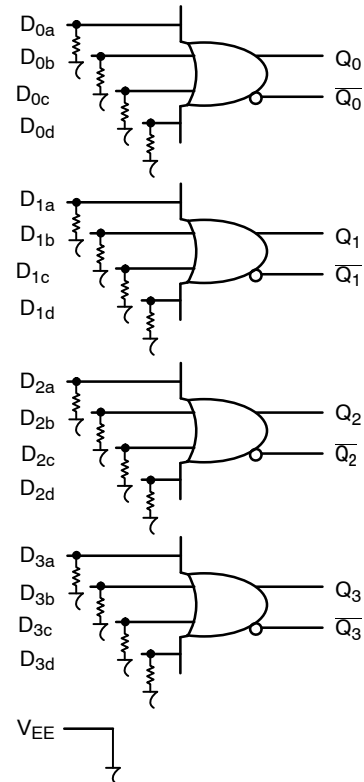


Figure 3. Logic Diagram

# MC100EP101

**Table 3. ATTRIBUTES**

Characteristics	Value
Internal Input Pulldown Resistor	75 k $\Omega$
Internal Input Pullup Resistor	N/A
ESD Protection Human Body Model Machine Model Charged Device Model	> 4 kV > 100 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb-Free Pkg
LQFP-32 QFN-32	Level 2 Level 1
Flammability Rating Oxygen Index: 28 to 34	UL-94 V-0 @ 0.125 in
Transistor Count	173 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note [AND8003/D](#).

**Table 4. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	PECL Mode Power Supply	V <sub>EE</sub> = 0 V		6	V
V <sub>EE</sub>	NECL Mode Power Supply	V <sub>CC</sub> = 0 V		-6	V
V <sub>I</sub>	PECL Mode Input Voltage NECL Mode Input Voltage	V <sub>EE</sub> = 0 V V <sub>CC</sub> = 0 V	V <sub>I</sub> ≤ V <sub>CC</sub> V <sub>I</sub> ≤ V <sub>EE</sub>	6 -6	V V
I <sub>out</sub>	Output Current	Continuous Surge		50 100	mA mA
I <sub>BB</sub>	V <sub>BB</sub> Sink/Source			±0.5	mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	32 LQFP 32 LQFP	80 55	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	Standard	32 LQFP	12 to 17	°C/W
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	QFN-32 QFN-32	31 27	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	2S2P	QFN-32	12	°C/W
T <sub>sol</sub>	Wave Solder (Pb-Free)			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

# MC100EP101

**Table 5. 100EP DC CHARACTERISTICS, PECL**  $V_{CC} = 3.3\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 2)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	40	55	75	40	58	75	45	60	85	mA
$V_{OH}$	Output HIGH Voltage (Note 3)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
$V_{OL}$	Output LOW Voltage (Note 3)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	2075		2420	2075		2420	2075		2420	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	1355		1675	1355		1675	1355		1675	mV
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	-150			-150			-150			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

2. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.3 V to -2.2 V.

3. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

**Table 6. 100EP DC CHARACTERISTICS, PECL**  $V_{CC} = 5.0\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 4)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	40	58	75	40	61	75	45	64	85	mA
$V_{OH}$	Output HIGH Voltage (Note 5)	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV
$V_{OL}$	Output LOW Voltage (Note 5)	3055	3180	3305	3055	3180	3305	3055	3180	3305	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	3775		4120	3775		4120	3775		4120	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	3055		3375	3055		3375	3055		3375	mV
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	-150			-150			-150			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

4. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +2.0 V to -0.5 V.

5. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

**Table 7. 100EP DC CHARACTERISTICS, NECL**  $V_{CC} = 0\text{ V}$ ,  $V_{EE} = -5.5\text{ V}$  to  $-3.0\text{ V}$  (Note 6)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current $V_{CC} = -3.3\text{ V}$ $V_{CC} = -5.0\text{ V}$	40	55	75	40	58	75	45	60	85	mA
		40	58	75	40	61	75	45	64	85	
$I_{EE}$	Power Supply Current	50	63	80	55	67	85	60	70	88	mA
$V_{OH}$	Output HIGH Voltage (Note 7)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
$V_{OL}$	Output LOW Voltage (Note 7)	-1945	-1820	-1695	-1945	-1820	-1695	-1945	-1820	-1695	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	-1225		-880	-1225		-880	-1225		-880	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	-1945		-1625	-1945		-1625	-1945		-1625	mV
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	-150			-150			-150			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

6. Input and output parameters vary 1:1 with  $V_{CC}$ .

7. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

# MC100EP101

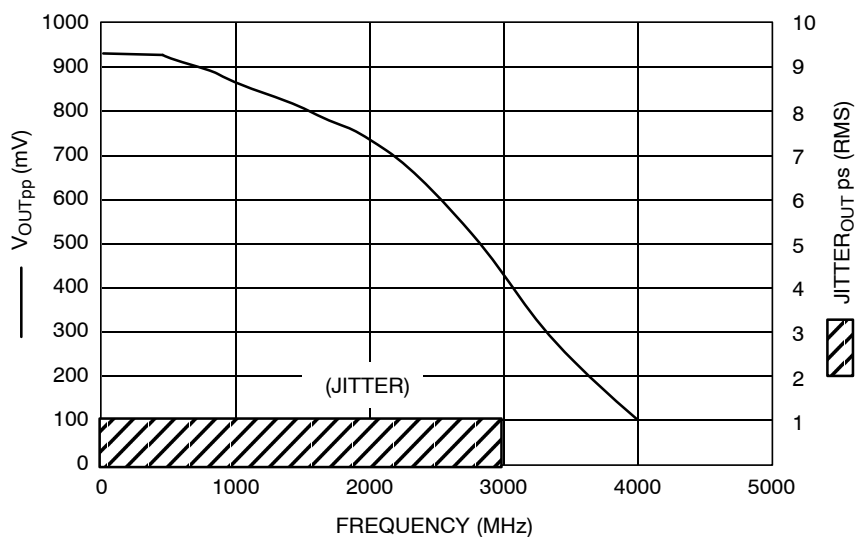
**Table 8. AC CHARACTERISTICS**  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.0\text{ V}$  to  $-5.5\text{ V}$  or  $V_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 8)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\max}$	Maximum Frequency (See Figure 4. $F_{\max}/\text{JITTER}$ )		> 3			> 3			> 3		GHz
$t_{PLH}$ , $t_{PHL}$	Propagation Delay D to Q, $\bar{Q}$ 10 100	125 180	225 280	325 380	150 200	250 300	370 400	170 250	300 320	420 450	ps
$t_{\text{SKEW}}$	Within Device Skew Q, $\bar{Q}$ Device to Device Skew (Note 9)		15	50 200		20	50 200		20	50 200	ps
$t_{\text{JITTER}}$	Cycle-to-Cycle Jitter (See Figure 4. $F_{\max}/\text{JITTER}$ )		0.2	< 1		0.2	< 1		0.2	< 1	ps
$t_r$ , $t_f$	Output Rise/Fall Times Q, $\bar{Q}$ (20% – 80%)	100	150	200	120	170	220	150	190	250	ps

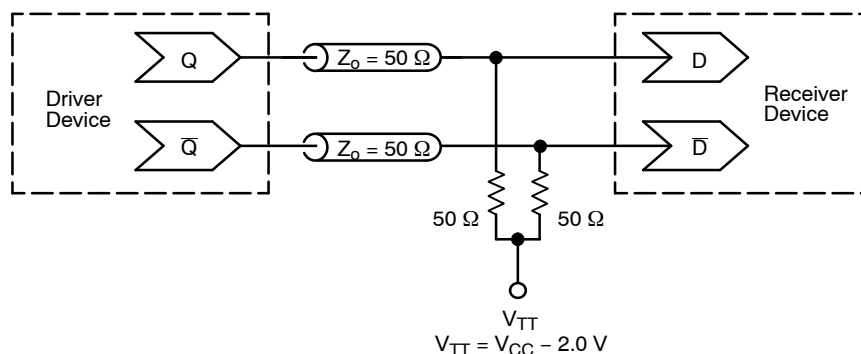
NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

8. Measured using a 750 mV source, 50% duty cycle clock source. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .

9. Skew is measured between outputs under identical transitions.



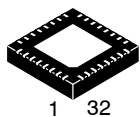
**Figure 4.  $F_{\max}/\text{Jitter}$**



**Figure 5. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices.)

## Resource Reference of Application Notes

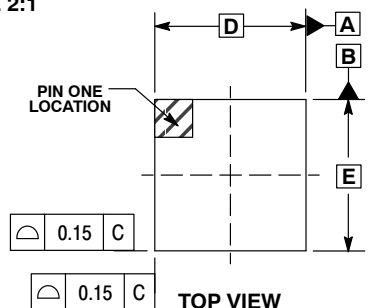
- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices



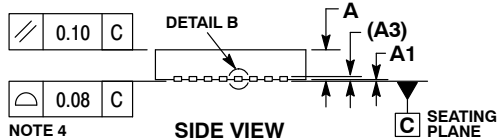
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SCALE 2:1

**QFN32 5x5, 0.5P**  
**CASE 488AM**  
**ISSUE A**

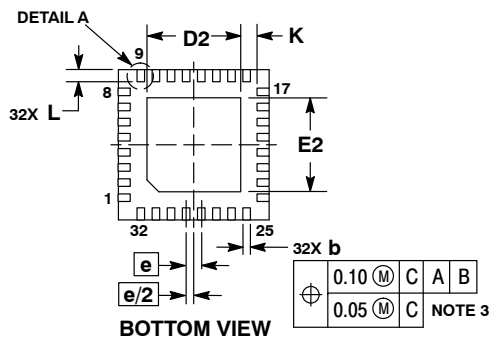
DATE 23 OCT 2013



**TOP VIEW**

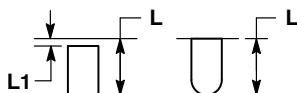
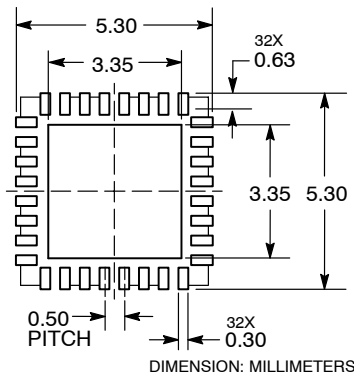


**SIDE VIEW**

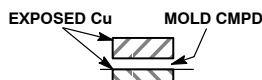


**BOTTOM VIEW**

**RECOMMENDED  
SOLDERING FOOTPRINT\***



**DETAIL A**  
**ALTERNATE TERMINAL**  
**CONSTRUCTIONS**



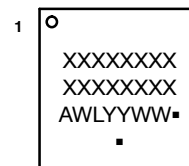
**DETAIL B**  
**ALTERNATE**  
**CONSTRUCTION**

**NOTES:**

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1		0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	2.95	3.25
E	5.00 BSC	
E2	2.95	3.25
e	0.50 BSC	
K	0.20	
L	0.30	0.50
L1		0.15

**GENERIC  
MARKING DIAGRAM\***



XXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking.  
Pb-Free indicator, "G" or microdot "▪", may or may not be present.

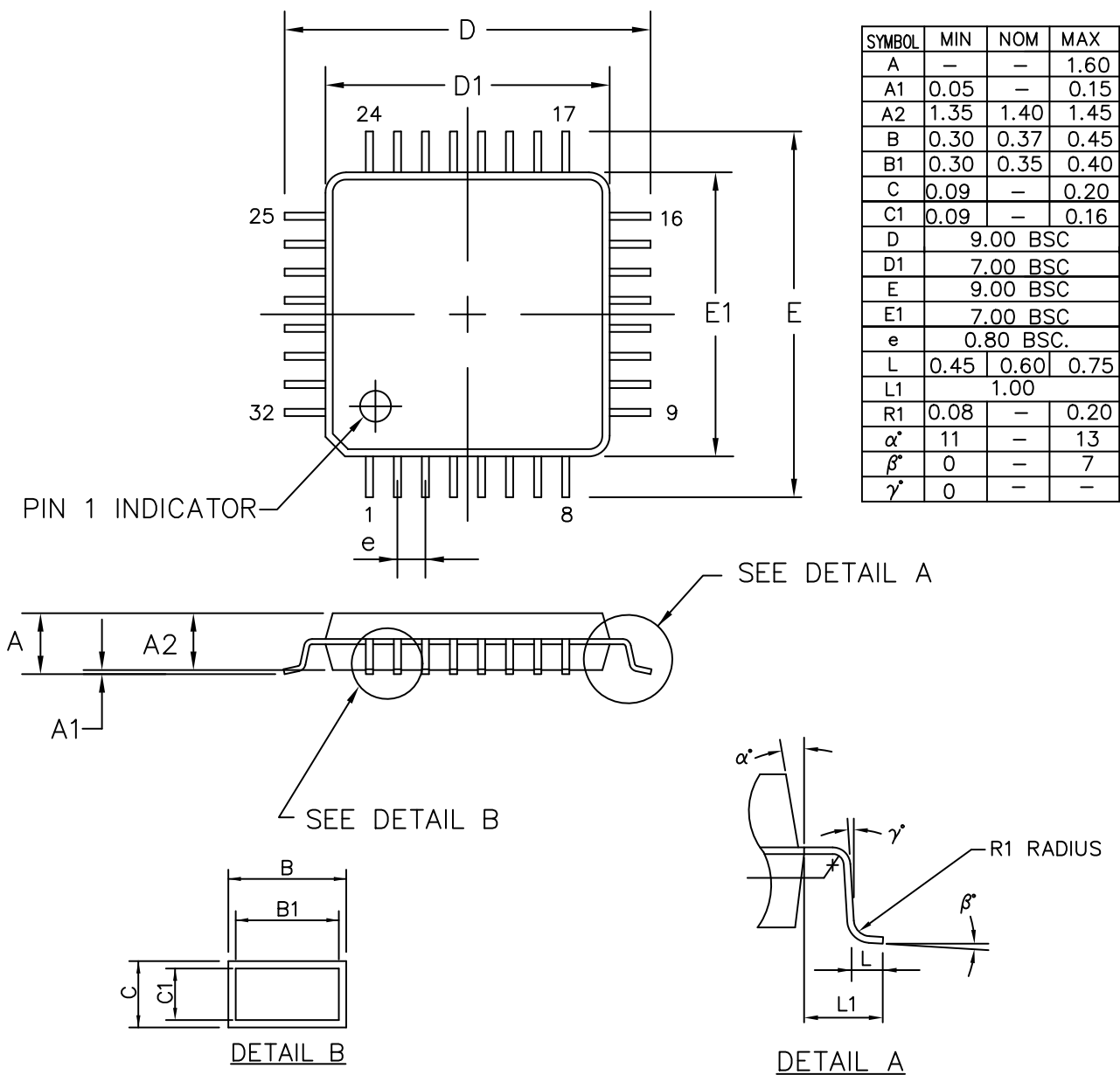
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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**LQFP-32, 7x7**  
**CASE 561AB**  
**ISSUE O**

DATE 19 JUN 2008



ALL DIMENSIONS IN MM

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