

3.3 V LVTTL/LVCMOS to **Differential LVECL Translator**

MC100EPT24



The MC100EPT24 is a LVTTL/LVCMOS to differential LVECL translator. Because LVECL levels and LVTTL/LVCMOS levels are used, a -3.3 V, +3.3 V and ground are required. The small outline 8-lead package and the single gate of the EPT24 makes it ideal for those applications where space, performance, and low power are at a premium.

Features

- 350 ps Typical Propagation Delay
- Maximum Input Clock Frequency = > 1.0 GHz Typical
- The 100 Series Contains Temperature Compensation
- Operating Range: $V_{CC} = 3.0 \text{ V}$ to 3.6 V; $V_{EE} = -3.6 \text{ V}$ to -3.0 V; GND = 0 V
- PNP LVTTL Input for Minimal Loading
- Q Output will Default HIGH with Input Open
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant







SOIC-8 NB **D SUFFIX**

TSSOP-8 **DT SUFFIX**

MN SUFFIX CASE 751-07 CASE 948R-02 CASE 506AA

MARKING DIAGRAMS*







SOIC-8 NB

DFN8

Α = Assembly Location

= Wafer Lot Υ = Year W = Work Week = Date Code = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

Device	Package	Shipping†
MC100EPT24DTG	TSSOP-8 (Pb-Free)	100 Units / Tube
MC100EPT24MNR4G	DFN8 (Pb-Free)	1000 Tape & Reel

DISCONTINUED (Note 1)

MC100EPT24DG	SOIC-8 NB (Pb-Free)	98 Units / Tube
MC100EPT24DR2G	SOIC-8 NB (Pb-Free)	2500 Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1. DISCONTINUED: These devices are not recommended for new design. Please contact your onsemi representative for information. The most current information on these devices may be available on www.onsemi.com.

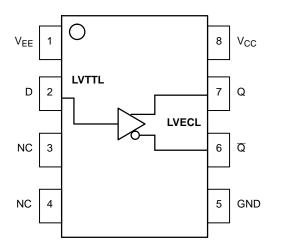


Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

Table 1. PIN DESCRIPTION

PIN	FUNCTION
Q, Q	Differential LVECL Outputs
D	LVTTL Input
V _{CC}	Positive Supply
GND	Ground
V _{EE}	Negative Supply
NC	No Connect
EP	(DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.

Table 2. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	N/A
Internal Input Pullup Resistor	N/A
ESD Protection Human Body Model Machine Model Charged Device Model	> 4 kV > 200 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb-Free Pkg
SOIC-8 NB TSSOP-8 DFN8	Level 1 Level 3 Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	181 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

^{1.} For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	Positive Power Supply	GND = 0 V	V _{EE} = −3.3V	3.8	V
V _{EE}	Negative Power Supply	GND = 0 V	V _{CC} = 3.3V	-3.8	V
V _{IN}	Input Voltage	GND = 0 V	$V_{I} \leq V_{CC}$	0 to V _{CC}	V
I _{out}	Output Current	Continuous Surge		50 100	mA
T _A	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 50 lfpm	SOIC-8 NB SOIC-8 NB	190 130	°C/W
$\theta_{\sf JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-8 NB	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 50 lfpm	TSSOP-8 TSSOP-8	185 140	°C/W
θJC	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-8	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 50 lfpm	DFN8 DFN8	129 84	°C/W
T _{sol}	Wave Solder (Pb-Free)			265	°C
$\theta_{\sf JC}$	Thermal Resistance (Junction-to-Case)	(Note 1)	DFN8	35 to 40	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

 $\textbf{Table 4. LVTTL INPUT DC CHARACTERISTICS} \ (V_{CC} = \ 3.3 \ V, \ V_{EE} = -3.6 \ V \ to \ -3.0 \ V, \ GND = 0.0 \ V; \ T_A = -40 ^{\circ}C \ to \ 85 ^{\circ}C)$

Symbol	Characteristic	Condition	Min	Тур	Max	Unit
I _{IH}	Input HIGH Current	V _{IN} = 2.7 V			20	μΑ
I _{IHH}	Input HIGH Current HIGH Voltage	$V_{CC} = V_{IN} = 3.8 \text{ V}$			100	μΑ
I _{IL}	Input LOW Current	V _{IN} = 0.5 V			-0.6	mA
V _{IK}	Input Clamp Voltage	I _{IN} = -18 mA			-1.0	V
V _{IH}	Input HIGH Voltage		2.0			V
V _{IL}	Input LOW Voltage				0.8	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

Table 5. NECL OUTPUT DC CHARACTERISTICS ($V_{CC} = 3.3 \text{ V}, V_{EE} = -3.3 \text{ V}, \text{GND} = 0.0 \text{ V} \text{ (Note 1))}$

		-40°C		25°C			85°C				
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
V _{OH}	Output HIGH Voltage (Note 2)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1030	-895	mV
V _{OL}	Output LOW Voltage (Note 2)	-1945	-1820	-1695	-1945	-1820	-1695	-1945	-1820	-1695	mV
I _{CC}	Positive Power Supply Current		2.0	4.0		2.0	4.0		2.0	4.0	mA
I _{EE}	Negative Power Supply Current	20	30	38	20	30	38	20	30	38	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

- 1. Output levels will vary 1:1 with GND. V_{EE} can vary \pm 0.3 V.
- 2. Outputs are terminated through a 50 Ω resistor to GND 2 V.

^{1.} JEDEC standard multilayer board - 2S2P (2 signal, 2 power)

Table 6. AC CHARACTERISTICS ($V_{CC} = 0 \text{ V}$; $V_{EE} = -3.0 \text{ V}$ to -5.5 V or $V_{CC} = 3.0 \text{ V}$ to 5.5 V; $V_{EE} = 0 \text{ V}$ (Note 1))

		-40°C		25°C		85°C					
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
f _{max}	Maximum Input Clock Frequency (Figure 2)		> 1			> 1			> 1		GHz
t _{PLH} , t _{PHL}	Propagation Delay to Output Differential (Note 2)	300	500	800	300	530	800	300	560	800	ps
t _{JITTER}	RMS Random Clock Jitter (Figure 2)		0.2	< 1		0.2	< 1		0.2	< 1	ps
t _r t _f	Output Rise/Fall Times Q, \overline{Q} (20% – 80%) @ 50 MHz	70	125	170	80	130	180	100	150	200	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

- 1. Measured using a LVTTL source, 50% duty cycle clock source. All loading with 50 Ω to GND 2.0 V. 2. Specifications for standard TTL input signal.

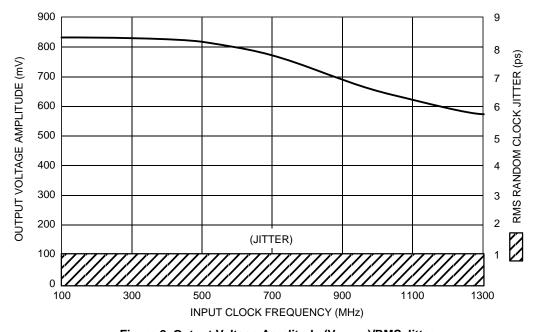


Figure 2. Output Voltage Amplitude (V_{OUTpp})/RMS Jitter vs. Input Clock Frequency at Ambient Temperature

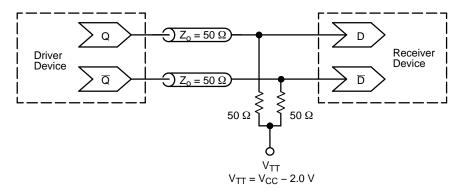


Figure 3. Typical Termination for Output Driver and Device Evaluation (See Application Note <u>AND8020/D</u> – Termination of ECL Logic Devices)

Resource Reference of Application Notes

AN1405/D - ECL Clock Distribution Techniques

AN1406/D - Designing with PECL (ECL at +5.0 V)

AN1503/D - ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D - Metastability and the ECLinPS Family

AN1568/D - Interfacing Between LVDS and ECL

AND8001/D - The ECL Translator Guide

AND8001/D - Odd Number Counters Design

AND8002/D - Marking and Date Codes

AND8020/D - Termination of ECL Logic Devices

AND8066/D - Interfacing with ECLinPS

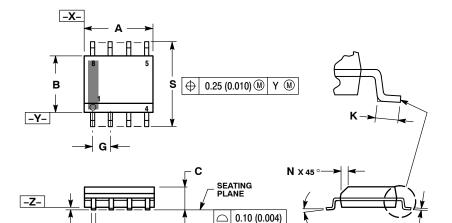
AND8090/D - AC Characteristics of ECL Devices





SOIC-8 NB CASE 751-07 **ISSUE AK**

DATE 16 FEB 2011



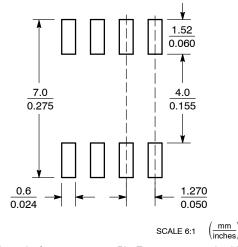
XS

- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
- 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

	MILLIMETERS		INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	4.80	5.00	0.189	0.197	
В	3.80	4.00	0.150	0.157	
С	1.35	1.75	0.053	0.069	
D	0.33	0.51	0.013	0.020	
G	1.27	7 BSC	0.050 BSC		
Н	0.10	0.25	0.004	0.010	
J	0.19	0.25	0.007	0.010	
K	0.40	1.27	0.016	0.050	
М	0 °	8 °	0 °	8 °	
N	0.25	0.50	0.010	0.020	
S	5.80	6.20	0.228	0.244	

SOLDERING FOOTPRINT*

0.25 (0.010) M Z Y S



^{*}For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code = Assembly Location = Wafer Lot

= Year = Work Week W = Pb-Free Package

XXXXXX XXXXXX AYWW AYWW H \mathbb{H} Discrete **Discrete** (Pb-Free)

XXXXXX = Specific Device Code = Assembly Location Α

ww = Work Week

= Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC-8 NB CASE 751-07 ISSUE AK

DATE 16 FEB 2011

STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER	STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1	STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1	STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE
STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE	STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE	STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd STYLE 11:	STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2
STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON	STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND	PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1	PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN	STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN	STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON	STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1
STYLE 17: PIN 1. VCC 2. V2OUT 3. V10UT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC	STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE	STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2	STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN
5. RXE 6. VEE 7. GND 8. ACC STYLE 21: PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6	8. CATHODE STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND	7. DHAIN 1 8. MIRROR 1 STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT	STYLE 24: PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE
STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT	STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC	STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN	STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN
STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1	STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1		

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DIMENSIONING AND TOLERANCING PER

PAD AS WELL AS THE TERMINALS. MILLIMETERS

> 1.00 0.00 0.05

MIN MAX

0.20 REF

0.80

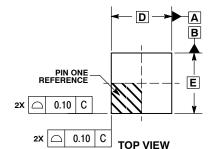
ASME Y14.5M, 1994 . CONTROLLING DIMENSION: MILLIMETERS. DIMENSION & APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP. COPLANARITY APPLIES TO THE EXPOSED

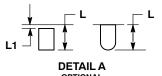


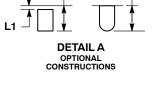


DFN8 2x2, 0.5P CASE 506AA **ISSUE F**

DATE 04 MAY 2016

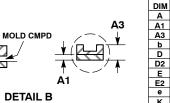


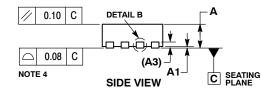


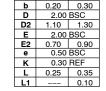


ALTERNATE CONSTRUCTIONS

EXPOSED Cu

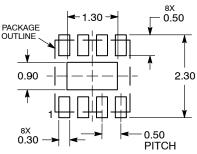




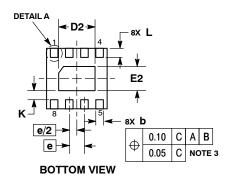


NOTES

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS



GENERIC MARKING DIAGRAM*



XX = Specific Device Code

= Date Code

= Pb-Free Device

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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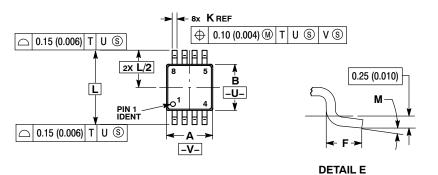
^{*}This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

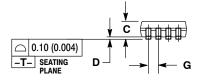


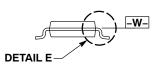


TSSOP-8 3.00x3.00x0.95 CASE 948R-02 **ISSUE A**

DATE 07 APR 2000







NOTES:

- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: MILLIMETER.

 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15

 (0.006) PER SIDE.
- DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- 6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIN	IETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	2.90	3.10	0.114	0.122	
В	2.90	3.10	0.114	0.122	
С	0.80	1.10	0.031	0.043	
D	0.05	0.15	0.002	0.006	
F	0.40	0.70	0.016	0.028	
G	0.65 BSC		0.026 BSC		
K	0.25	0.40	0.010	0.016	
L	4.90 BSC		0.193 BSC		
M	0°	6 °	0°	6°	

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