

## 3.3 V ECL Differential Clock D Flip-Flop

### MC100LVEL51

#### Description

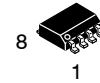
The MC100LVEL51 is a differential clock D flip-flop with reset. The device is functionally equivalent to the EL51 device, but operates from a 3.3 V supply. With propagation delays and output transition times essentially equal to the EL51, the LVEL51 is ideally suited for those applications which require the ultimate in AC performance at 3.3 V  $V_{CC}$ .

The reset input is an asynchronous, level triggered signal. Data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The differential clock inputs of the LVEL51 allow the device to be used as a negative edge triggered flip-flop.

The differential input employs clamp circuitry to maintain stability under open input conditions. When left open, the CLK input will be pulled down to  $V_{EE}$  and the  $\overline{CLK}$  input will be biased at  $V_{CC}/2$ .

#### Features

- 475 ps Propagation Delay
- 2.8 GHz Toggle Frequency
- ESD Protection: > 4 kV Human Body Model, > 200 V Machine Model
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range:  $V_{CC} = 3.0$  V to 3.8 V with  $V_{EE} = 0$  V
- NECL Mode Operating Range:  $V_{CC} = 0$  V with  $V_{EE} = -3.0$  V to  $-3.8$  V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level
  - ◆ Level 1 for SOIC-8 NB
  - ◆ Level 3 for TSSOP-8
  - ◆ For Additional Information, see Application Note [AND8003/D](#)
- Flammability Rating: UL 94 V-0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 114 devices
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

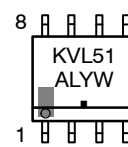


SOIC-8 NB  
D SUFFIX  
CASE 751

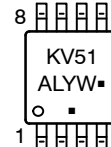


TSSOP-8  
DT SUFFIX  
CASE 948R

#### MARKING DIAGRAMS\*



SOIC-8



TSSOP-8

A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
■ = Pb-Free Package

(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note [AND8002/D](#).

#### ORDERING INFORMATION

| Device           | Package             | Shipping <sup>†</sup> |
|------------------|---------------------|-----------------------|
| MC100LVEL51DG    | SOIC-8 NB (Pb-Free) | 98 Units/Tube         |
| MC100LVEL51DTR2G | TSSOP-8 (Pb-Free)   | 2500 / Tape & Reel    |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

# MC100LVEL51

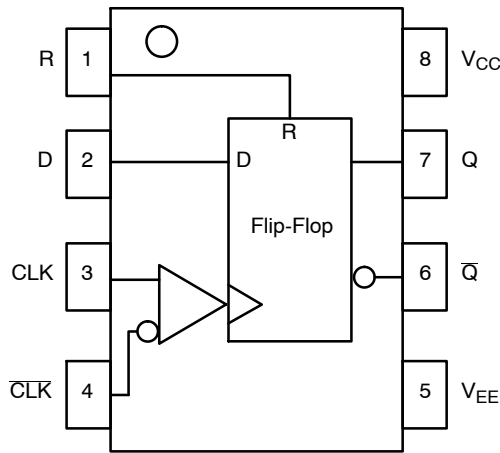


Figure 1. Logic Diagram and Pinout Assignment

Table 1. PIN DESCRIPTION

| PIN                          | FUNCTION                     |
|------------------------------|------------------------------|
| CLK, $\overline{\text{CLK}}$ | ECL Differential Clock Input |
| Q, $\overline{\text{Q}}$     | ECL Differential Output      |
| D                            | ECL D Input                  |
| R                            | ECL Reset Input              |
| V <sub>CC</sub>              | Positive Supply              |
| V <sub>EE</sub>              | Negative Supply              |

Table 2. TRUTH TABLE

| D | R | CLK | Q |
|---|---|-----|---|
| L | L | Z   | L |
| H | L | Z   | H |
| X | H | X   | L |

Z = LOW to HIGH Transition  
X = Don't Care

Table 3. MAXIMUM RATINGS

| Symbol           | Parameter                                          | Condition 1                                    | Condition 2                                                          | Rating            | Unit |
|------------------|----------------------------------------------------|------------------------------------------------|----------------------------------------------------------------------|-------------------|------|
| V <sub>CC</sub>  | PECL Mode Power Supply                             | V <sub>EE</sub> = 0 V                          |                                                                      | 8 to 0            | V    |
| V <sub>EE</sub>  | NECL Mode Power Supply                             | V <sub>CC</sub> = 0 V                          |                                                                      | -8 to 0           | V    |
| V <sub>I</sub>   | PECL Mode Input Voltage<br>NECL Mode Input Voltage | V <sub>EE</sub> = 0 V<br>V <sub>CC</sub> = 0 V | V <sub>I</sub> ≤ V <sub>CC</sub><br>V <sub>I</sub> ≥ V <sub>EE</sub> | 6 to 0<br>-6 to 0 | V    |
| I <sub>out</sub> | Output Current                                     | Continuous<br>Surge                            |                                                                      | 50<br>100         | mA   |
| T <sub>A</sub>   | Operating Temperature Range                        |                                                |                                                                      | -40 to +85        | °C   |
| T <sub>stg</sub> | Storage Temperature Range                          |                                                |                                                                      | -65 to +150       | °C   |
| θ <sub>JA</sub>  | Thermal Resistance (Junction-to-Ambient)           | 0 lfpm<br>500 lfpm                             | SOIC-8 NB                                                            | 190<br>130        | °C/W |
| θ <sub>JC</sub>  | Thermal Resistance (Junction-to-Case)              | Standard Board                                 | SOIC-8 NB                                                            | 41 to 44 ±5%      | °C/W |
| θ <sub>JA</sub>  | Thermal Resistance (Junction-to-Ambient)           | 0 lfpm<br>500 lfpm                             | TSSOP-8                                                              | 185<br>140        | °C/W |
| θ <sub>JC</sub>  | Thermal Resistance (Junction-to-Case)              | Standard Board                                 | TSSOP-8                                                              | 41 to 44 ±5%      | °C/W |
| T <sub>sol</sub> | Wave Solder (Pb-Free)                              | < 2 to 3 sec @ 260°C                           |                                                                      | 265               | °C   |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. JEDEC standard multilayer board – 2S2P (2 signal, 2 power).

# MC100LVEL51

**Table 4. LVPECL DC CHARACTERISTICS** ( $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  (Note 2))

| Symbol      | Characteristic                                                                                                          | -40°C       |      |            | 25°C        |      |            | 85°C        |      |            | Unit          |
|-------------|-------------------------------------------------------------------------------------------------------------------------|-------------|------|------------|-------------|------|------------|-------------|------|------------|---------------|
|             |                                                                                                                         | Min         | Typ  | Max        | Min         | Typ  | Max        | Min         | Typ  | Max        |               |
| $I_{EE}$    | Power Supply Current                                                                                                    |             | 30   | 35         |             | 30   | 35         |             | 32   | 37         | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 3)                                                                                            | 2215        | 2295 | 2420       | 2275        | 2345 | 2420       | 2275        | 2345 | 2420       | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 3)                                                                                             | 1470        | 1605 | 1745       | 1490        | 1595 | 1680       | 1490        | 1595 | 1680       | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)                                                                                       | 2135        |      | 2420       | 2135        |      | 2420       | 2135        |      | 2420       | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)                                                                                        | 1490        |      | 1825       | 1490        |      | 1825       | 1490        |      | 1825       | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 7)<br>$V_{PP} < 500\text{ mV}$<br>$V_{PP} \geq 500\text{ mV}$ | 1.2<br>1.4  |      | 3.0<br>3.0 | 1.1<br>1.3  |      | 3.0<br>3.0 | 1.1<br>1.3  |      | 3.0<br>3.0 | V             |
| $I_{IH}$    | Input HIGH Current                                                                                                      |             |      | 150        |             |      | 150        |             |      | 150        | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current<br>Others<br>CLK                                                                                      | 0.5<br>-600 |      |            | 0.5<br>-600 |      |            | 0.5<br>-600 |      |            | $\mu\text{A}$ |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

2. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .

3. Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .

4.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{PPmin}$  and  $1\text{ V}$ .

**Table 5. LVNECL DC CHARACTERISTICS** ( $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -3.3\text{ V}$  (Note 5))

| Symbol      | Characteristic                                                                                                          | -40°C        |       |              | 25°C         |       |              | 85°C         |       |              | Unit          |
|-------------|-------------------------------------------------------------------------------------------------------------------------|--------------|-------|--------------|--------------|-------|--------------|--------------|-------|--------------|---------------|
|             |                                                                                                                         | Min          | Typ   | Max          | Min          | Typ   | Max          | Min          | Typ   | Max          |               |
| $I_{EE}$    | Power Supply Current                                                                                                    |              | 30    | 35           |              | 30    | 35           |              | 32    | 37           | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 6)                                                                                            | -1085        | -1005 | -880         | -1025        | -955  | -880         | -1025        | -955  | -880         | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 6)                                                                                             | -1830        | -1695 | -1555        | -1810        | -1705 | -1620        | -1810        | -1705 | -1620        | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)                                                                                       | -1165        |       | -880         | -1165        |       | -880         | -1165        |       | -880         | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)                                                                                        | -1810        |       | -1475        | -1810        |       | -1475        | -1810        |       | -1475        | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 7)<br>$V_{PP} < 500\text{ mV}$<br>$V_{PP} \geq 500\text{ mV}$ | -2.1<br>-1.9 |       | -0.3<br>-0.3 | -2.2<br>-2.0 |       | -0.3<br>-0.3 | -2.2<br>-2.0 |       | -0.3<br>-0.3 | V             |
| $I_{IH}$    | Input HIGH Current                                                                                                      |              |       | 150          |              |       | 150          |              |       | 150          | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current<br>Others<br>CLK                                                                                      | 0.5<br>-600  |       |              | 0.5<br>-600  |       |              | 0.5<br>-600  |       |              | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

5. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .

6. Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .

7.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{PPmin}$  and  $1\text{ V}$ .

# MC100LVEL51

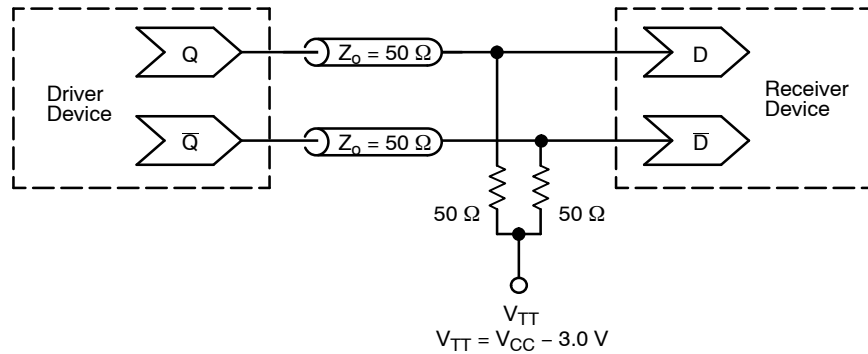
**Table 6. AC CHARACTERISTICS** ( $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  or  $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -3.3\text{ V}$  (Note 8))

| Symbol                 | Characteristic                             | -40°C      |            |            | 25°C       |            |            | 85°C       |            |            | Unit |
|------------------------|--------------------------------------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------|
|                        |                                            | Min        | Typ        | Max        | Min        | Typ        | Max        | Min        | Typ        | Max        |      |
| $f_{\max}$             | Maximum Toggle Frequency                   | 2.7        |            |            | 2.8        |            |            | 2.9        |            |            | GHz  |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>to Output<br>CLK<br>R | 330<br>340 | 465<br>455 | 510<br>540 | 340<br>350 | 475<br>465 | 520<br>550 | 370<br>390 | 530<br>510 | 550<br>590 | ps   |
| $t_S$                  | Setup Time                                 | 150        | 0          |            | 150        | 0          |            | 150        | 0          |            | ps   |
| $t_H$                  | Hold Time                                  | 200        | 100        |            | 200        | 100        |            | 200        | 100        |            | ps   |
| $t_{RR}$               | Reset Recovery                             | 350        | 200        |            | 350        | 200        |            | 350        | 200        |            | ps   |
| $t_{PW}$               | Minimum Pulse<br>CLK<br>Width<br>Reset     | 400<br>500 |            |            | 400<br>500 |            |            | 400<br>500 |            |            | ps   |
| $t_{JITTER}$           | Cycle-to-Cycle Jitter                      |            | 6.9        |            |            | 7.0        |            |            | 7.1        |            | ps   |
| $V_{PP}$               | Input Swing (Note 9)                       | 150        |            | 1000       | 150        |            | 1000       | 150        |            | 1000       | mV   |
| $t_r$<br>$t_f$         | Output Rise/Fall Times Q<br>(20% – 80%)    | 120        |            | 320        | 120        |            | 320        | 120        |            | 320        | ps   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

8.  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .

9.  $V_{PP}$  (min) is minimum input swing for which AC parameters are guaranteed.



**Figure 2. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices.)

## MC100LVEL51

### Resource Reference of Application Notes

|                                  |   |                                      |
|----------------------------------|---|--------------------------------------|
| <a href="#"><u>AN1405/D</u></a>  | - | ECL Clock Distribution Techniques    |
| <a href="#"><u>AN1406/D</u></a>  | - | Designing with PECL (ECL at +5.0 V)  |
| <a href="#"><u>AN1503/D</u></a>  | - | ECLinPS™ I/O SPiCE Modeling Kit      |
| <a href="#"><u>AN1504/D</u></a>  | - | Metastability and the ECLinPS Family |
| <a href="#"><u>AN1568/D</u></a>  | - | Interfacing Between LVDS and ECL     |
| <a href="#"><u>AN1672/D</u></a>  | - | The ECL Translator Guide             |
| <a href="#"><u>AND8001/D</u></a> | - | Odd Number Counters Design           |
| <a href="#"><u>AND8002/D</u></a> | - | Marking and Date Codes               |
| <a href="#"><u>AND8020/D</u></a> | - | Termination of ECL Logic Devices     |
| <a href="#"><u>AND8066/D</u></a> | - | Interfacing with ECLinPS             |
| <a href="#"><u>AND8090/D</u></a> | - | AC Characteristics of ECL Devices    |

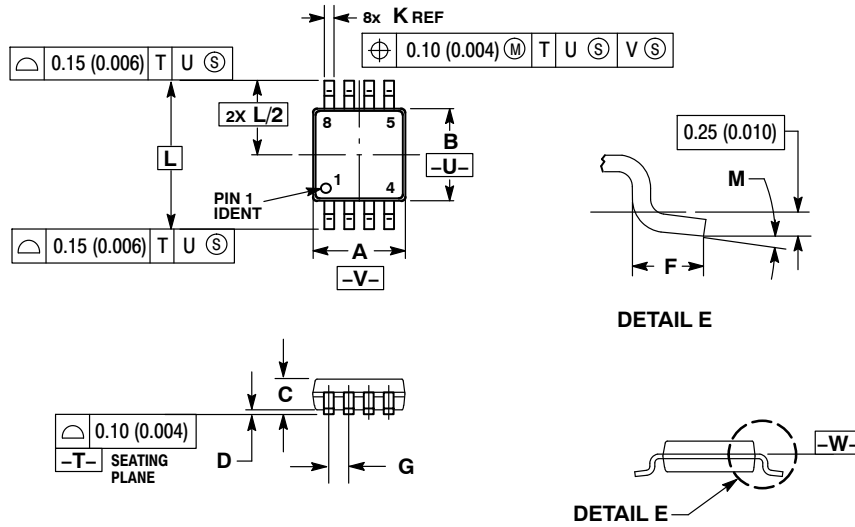
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SCALE 2:1

**TSSOP-8 3.00x3.00x0.95**  
CASE 948R-02  
ISSUE A

DATE 07 APR 2000



## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 2.90        | 3.10 | 0.114     | 0.122 |
| B   | 2.90        | 3.10 | 0.114     | 0.122 |
| C   | 0.80        | 1.10 | 0.031     | 0.043 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.40        | 0.70 | 0.016     | 0.028 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| K   | 0.25        | 0.40 | 0.010     | 0.016 |
| L   | 4.90 BSC    |      | 0.193 BSC |       |
| M   | 0°          | 6°   | 0°        | 6°    |

|                  |                        |                                                                                                                                                                                  |
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