

# 3.3 V / 5 V ECL 8-Bit Synchronous Binary Up Counter

## MC10EP016

### Description

The MC10EP016 is a high-speed synchronous, presettable, cascadeable 8-bit binary counter. Architecture and operation are the same as the MC10E016 in the ECLinPS™ family.

The counter features internal feedback to  $\overline{TC}$  gated by the TCLD (Terminal Count Load) pin. When TCLD is LOW (or left open, in which case it is pulled LOW by the internal pulldowns), the  $\overline{TC}$  feedback is disabled, and counting proceeds continuously, with  $\overline{TC}$  going LOW to indicate an all-one state. When TCLD is HIGH, the TC feedback causes the counter to automatically reload upon TC = LOW, thus functioning as a programmable counter. The Qn outputs do not need to be terminated for the count function to operate properly. To minimize noise and power, unused Q outputs should be left unterminated.

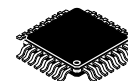
COUT and  $\overline{COUT}$  provide differential outputs from a single, non-cascaded counter or divider application. COUT and  $\overline{COUT}$  should not be used in cascade configuration. Only  $\overline{TC}$  should be used for a counter or divider cascade chain output.

A differential clock input has also been added to improve performance.

### Features

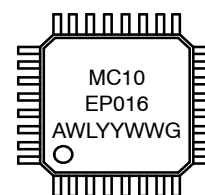
- 500 ps Typical Propagation Delay
- PECL Mode Operating Range:  $V_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$  with  $V_{EE} = 0\text{ V}$
- NECL Mode Operating Range:  $V_{CC} = 0\text{ V}$  with  $V_{EE} = -3.0\text{ V}$  to  $-5.5\text{ V}$
- Open Input Default State
- Safety Clamp on Inputs
- Internal  $\overline{TC}$  Feedback (Gated)
- Addition of COUT and  $\overline{COUT}$
- 8-Bit
- Differential Clock Input
- $V_{BB}$  Output
- Fully Synchronous Counting and  $\overline{TC}$  Generation
- Asynchronous Master Reset
- Pb-Free Packages are Available\*

\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



LQFP-32  
FA SUFFIX  
CASE 561AB

### MARKING DIAGRAM



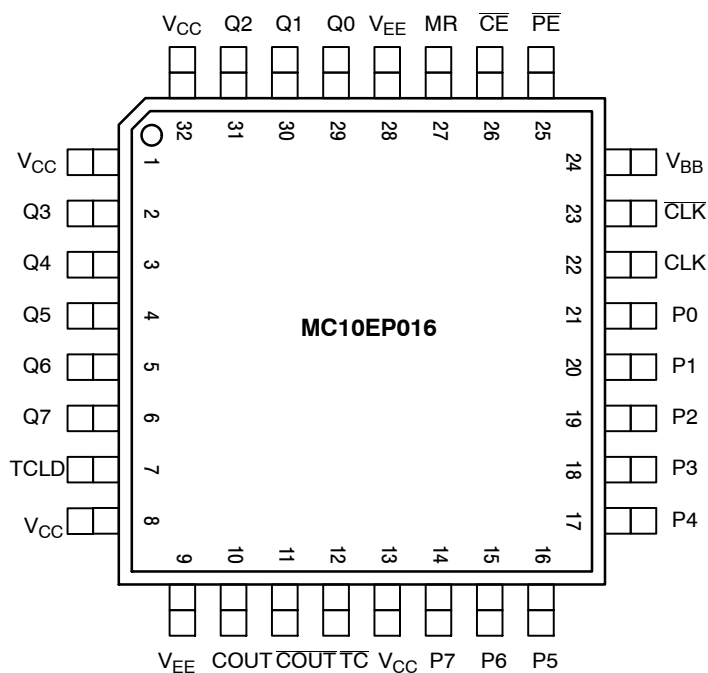
MC10EP016	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb-Free Package

\*For additional marking information, refer to Application Note [AND8002/D](#).

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

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Warning: All  $V_{CC}$  and  $V_{EE}$  pins must be externally connected to Power Supply to guarantee proper operation.

**Figure 1. LQFP-32 Pinout (Top View)**

**Table 1. PIN DESCRIPTION**

Pin	Function
P0–P7*	ECL Parallel Data (Preset) Inputs
Q0–Q7	ECL Data Outputs
$\overline{CE}^*$	ECL Count Enable Control Input
$\overline{PE}^*$	ECL Parallel Load Enable Control Input
$\overline{MR}^*$	ECL Master Reset
CLK*, $\overline{CLK}^*$	ECL Differential Clock
TC	ECL Terminal Count Output
TCLD*	ECL TC–Load Control Input
COUT, $\overline{COUT}$	ECL Differential Output
$V_{CC}$	Positive Supply
$V_{EE}$	Negative Supply
$V_{BB}$	Reference Voltage Output

\* Pins will default LOW when left open.

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**Table 2. FUNCTION TABLES**

$\overline{CE}$	$\overline{PE}$	TCLD	MR	CLK	FUNCTION
X	L	X	L	Z	Load Parallel (Pn to Qn)
L	H	L	L	Z	Continuous Count
L	H	H	L	Z	Count; Load Parallel on $\overline{TC}$ = LOW
H	H	X	L	Z	Hold
X	X	X	L	ZZ	Masters Respond, Slaves Hold
X	X	X	H	X	Reset (Qn : = LOW, $\overline{TC}$ : = HIGH)

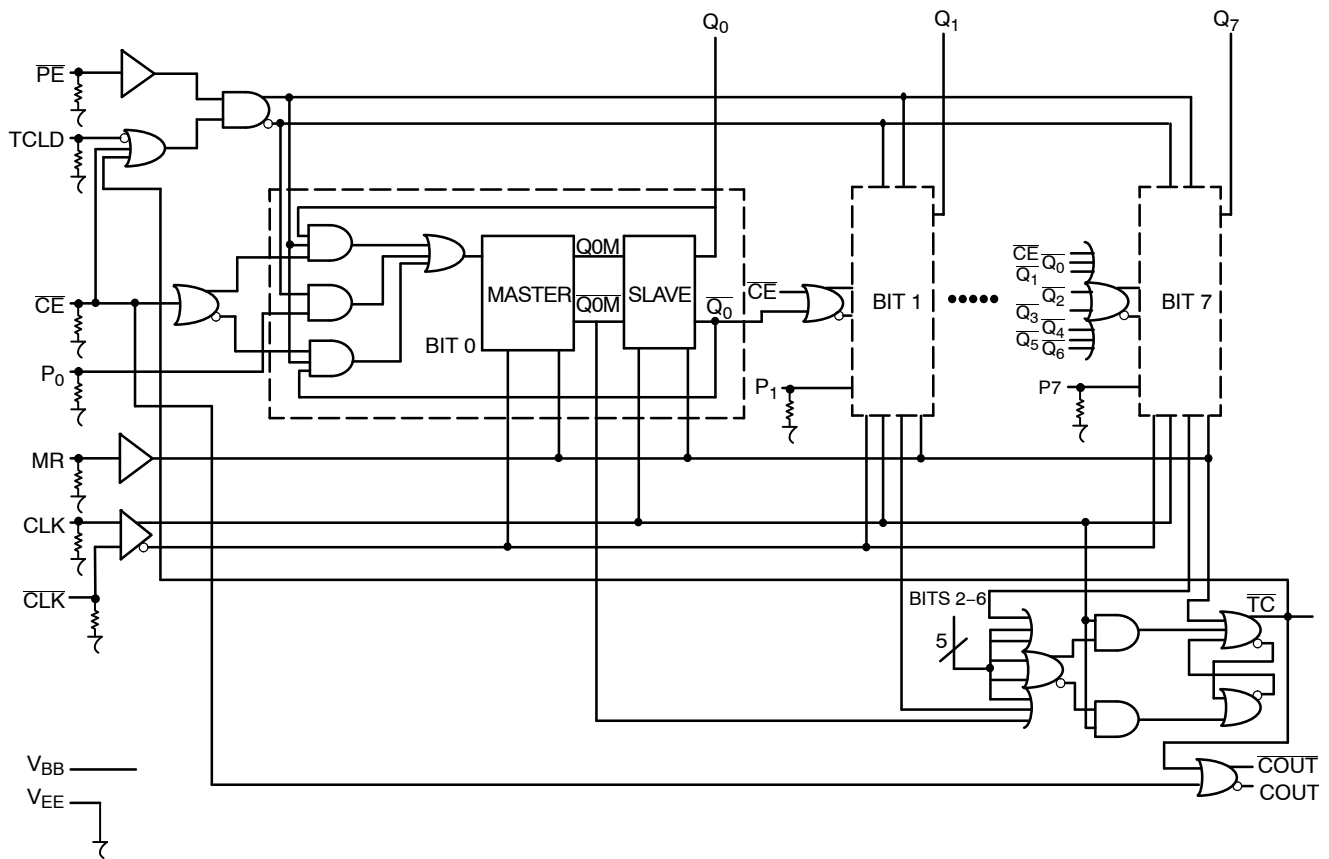
ZZ = Clock Pulse (High-to-Low)

Z = Clock Pulse (Low-to-High)

**Table 3. FUNCTION TABLE**

Function	$\overline{PE}$	$\overline{CE}$	MR	TCLD	CLK	P7-P4	P3	P2	P1	P0	Q7-Q4	Q3	Q2	Q1	Q0	$\overline{TC}$	$\overline{COUT}$	COUT
Load Count	L	X	L	X	Z	H	H	H	L	L	H	H	H	L	L	H	H	L
	H	L	L	L	Z	X	X	X	X	X	H	H	H	L	H	H	H	L
	H	L	L	L	Z	X	X	X	X	X	H	H	H	H	H	L	L	H
	H	L	L	L	Z	X	X	X	X	X	L	L	L	L	L	H	H	L
	H	L	L	L	Z	X	X	X	X	X	L	L	L	L	L	H	H	L
Load Hold	L	X	L	X	Z	H	H	H	L	L	H	H	H	L	L	H	H	L
	H	H	L	X	Z	X	X	X	X	X	H	H	H	L	L	H	H	L
	H	H	L	X	Z	X	X	X	X	X	H	H	H	L	L	H	H	L
	H	H	L	X	Z	X	X	X	X	X	H	H	H	L	L	H	H	L
	H	H	L	X	Z	X	X	X	X	X	H	H	H	L	L	H	H	L
Load on Terminal Count	H	L	L	H	Z	H	L	H	H	L	H	H	H	L	H	H	H	L
	H	L	L	H	Z	H	L	H	H	L	H	H	H	H	L	H	H	L
	H	L	L	H	Z	H	L	H	H	L	H	H	H	H	L	H	H	L
	H	L	L	H	Z	H	L	H	H	L	H	H	H	H	L	H	H	L
	H	L	L	H	Z	H	L	H	H	L	H	H	H	L	L	H	H	L
Reset	X	X	H	X	X	X	X	X	X	X	L	L	L	L	L	H	H	L

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Note that this diagram is provided for understanding of logic operation only.  
It should not be used for propagation delays as many gate functions are achieved internally without incurring a full gate delay.

**Figure 2. 8-BIT Binary Counter Logic Diagram**

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**Table 4. ATTRIBUTES**

Characteristics	Value
Internal Input Pulldown Resistor	75 k $\Omega$
Internal Input Pullup Resistor	N/A
ESD Protection Human Body Model Machine Model Charged Device Model	> 2 kV > 100 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb-Free Pkg Level 2
LQFP-32	
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	897 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note [AND8003/D](#).

**Table 5. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	PECL Mode Power Supply	V <sub>EE</sub> = 0 V		6	V
V <sub>EE</sub>	NECL Mode Power Supply	V <sub>CC</sub> = 0 V		-6	V
V <sub>I</sub>	PECL Mode Input Voltage	V <sub>EE</sub> = 0 V	V <sub>I</sub> ≤ V <sub>CC</sub>	6	V
	NECL Mode Input Voltage	V <sub>CC</sub> = 0 V	V <sub>I</sub> ≥ V <sub>EE</sub>	-6	V
I <sub>out</sub>	Output Current	Continuous Surge		50	mA
				100	mA
I <sub>BB</sub>	V <sub>BB</sub> Sink/Source			± 0.5	mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm	32 LQFP	80	°C/W
		500 lfpm	32 LQFP	55	°C/W
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	32 LQFP	12 to 17	°C/W
T <sub>sol</sub>	Wave Solder Pb Pb-Free			265	°C
				265	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with y8 filled thermal vias under exposed pad.

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**Table 6. 10EP DC CHARACTERISTICS, PECL  $V_{CC} = 3.3\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 3)**

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	120	160	200	120	160	200	120	160	200	mA
$V_{OH}$	Output HIGH Voltage (Note 4)	2165	2290	2415	2230	2355	2480	2290	2415	2540	mV
$V_{OL}$	Output LOW Voltage (Note 4)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	2090		2415	2155		2480	2215		2540	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	1365		1690	1460		1755	1490		1815	mV
$V_{BB}$	Output Voltage Reference	1790	1890	1990	1855	1955	2055	1915	2015	2115	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 5)	2.0		3.3	2.0		3.3	2.0		3.3	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

3. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.3 V to -2.2 V.

4. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

5.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**Table 7. 10EP DC CHARACTERISTICS, PECL  $V_{CC} = 5.0\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 6)**

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current (Note 7)	120	160	200	120	160	200	120	160	200	mA
$V_{OH}$	Output HIGH Voltage (Note 8)	3865	3990	4115	3930	4055	4180	3990	4115	4240	mV
$V_{OL}$	Output LOW Voltage (Note 8)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	3790		4115	3855		4180	3915		4240	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	3065		3390	3130		3455	3190		3515	mV
$V_{BB}$	Output Voltage Reference	3490	3590	3690	3555	3655	3755	3615	3715	3815	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 9)	2.0		5.0	2.0		5.0	2.0		5.0	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

6. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +2.0 V to -0.5 V.

7. Required 500 lfm air flow when using +5 V power supply. For  $(V_{CC} - V_{EE}) > 3.3\text{ V}$ , 5  $\Omega$  to 10  $\Omega$  in line with  $V_{EE}$  required for maximum thermal protection at elevated temperatures. Recommend  $V_{CC} - V_{EE}$  operation at  $\leq 3.3\text{ V}$ .

8. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

9.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

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**Table 8. 10EP DC CHARACTERISTICS, NECL**  $V_{CC} = 0\text{ V}$ ,  $V_{EE} = -5.5\text{ V}$  to  $-3.0\text{ V}$  (Note 10)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current (Note 11)	120	160	200	120	160	200	120	160	200	mA
$V_{OH}$	Output HIGH Voltage (Note 12)	-1135	-1010	-885	-1070	-945	-820	-1010	-885	-760	mV
$V_{OL}$	Output LOW Voltage (Note 12)	-1935	-1810	-1685	-1870	-1745	-1620	-1810	-1685	-1560	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	-1210		-885	-1145		-820	-1085		-760	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	-1935		-1610	-1870		-1545	-1810		-1485	mV
$V_{BB}$	Output Voltage Reference	-1510	-1410	-1310	-1445	-1345	-1245	-1385	-1285	-1185	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 13)	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

10. Input and output parameters vary 1:1 with  $V_{CC}$ .

11. Required 500 lfm air flow when using -5 V power supply. For  $(V_{CC} - V_{EE}) > 3.3\text{ V}$ ,  $5\ \Omega$  to  $10\ \Omega$  in line with  $V_{EE}$  required for maximum thermal protection at elevated temperatures. Recommend  $V_{CC}-V_{EE}$  operation at  $\leq 3.3\text{ V}$ .

12. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .

13.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

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**Table 9. AC CHARACTERISTICS**  $V_{EE} = -3.0\text{ V to }-5.5\text{ V}$ ;  $V_{CC} = 0\text{ V or }V_{CC} = 3.0\text{ V to }5.5\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 14)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f <sub>COUNT</sub>	Maximum Frequency Q, $\overline{\text{TC}}$ COUT/ $\overline{\text{COUT}}$		> 1 > 800			> 1 > 800			> 1 > 800		GHz MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay (10) CLK to Q (10) MR to Q (10) CLK to $\overline{\text{TC}}$ (10) MR to $\overline{\text{TC}}$ (10) CLK to COUT (10) MR to COUT (100) CLK to Q (100) MR to Q (100) CLK to $\overline{\text{TC}}$ (100) MR to $\overline{\text{TC}}$ (100) CLK to COUT (100) MR to COUT	300 300 350 250 400 300 350 400 350 400 400 450	460 400 420 350 470 400 500 550 500 550 550 600	600 500 550 450 650 550 650 700 650 700 750 800	350 400 400 350 450 400 400 450 400 450 450 500	500 500 500 450 550 500 550 590 550 590 600 640	650 600 600 550 700 650 700 750 700 750 800 850	400 450 400 400 450 450 480 520 480 520 530 570	560 580 550 510 600 560 630 670 630 670 680 720	700 700 700 600 800 700 780 820 780 820 880 920	ps
t <sub>S</sub>	Setup Time Pn $\overline{\text{CE}}$ $\overline{\text{PE}}$ TCLD	100 500 500 500	-50 300 300 300		100 500 500 500	-50 300 300 300		100 500 500 500	-50 300 300 300		ps
t <sub>H</sub>	Hold Time Pn $\overline{\text{CE}}$ $\overline{\text{PE}}$ TCLD	100 500 500 500	-50 300 300 300		100 500 500 500	-50 300 300 300		100 500 500 500	-50 300 300 300		ps
t <sub>JITTER</sub>	Clock Random Jitter (RMS >1000 Waveforms)		2.6	8.5		2.5	8.0		2.5	8.0	ps
t <sub>RR</sub>	Reset Recovery Time	200	80		200	80		200	80		ps
t <sub>PW</sub>	Minimum Pulse Width CLK, MR	550	300		550	300		550	300		ps
t <sub>r</sub> t <sub>f</sub>	Output Rise/Fall Times 20% – 80%	120	210	320	120	220	320	150	250	450	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

14. Measured using a 750 mV source, 50% duty cycle clock source. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .



For applications which call for larger than 8-bit counters multiple EP016s can be tied together to achieve very wide bit width counters. The active low terminal count ( $\overline{\text{TC}}$ ) output and count enable input ( $\overline{\text{CE}}$ ) greatly facilitate the cascading of EP016 devices. Two EP016s can be cascaded without the need for external gating, however for counters wider than 16 bits external OR gates are necessary for cascade implementations.

one bit thus sending their terminal count outputs back to a high state disabling the count operation of the more significant counters and placing them back into hold modes. Therefore, for an EP016 in the chain to count, all of the lower order terminal count outputs must be in the low state. The bit width of the counter can be increased or decreased by simply adding or subtracting EP016 devices from Figure 3 and maintaining the logic pattern illustrated in the same figure.

The maximum frequency of operation for a cascaded counter chain is set by the propagation delay of the  $\overline{\text{TC}}$  output, the necessary setup time of the  $\overline{\text{CE}}$  input, and the propagation delay through the OR gate controlling it (for 16-bit counters the limitation is only the  $\overline{\text{TC}}$  propagation delay and the  $\overline{\text{CE}}$  setup time). Figure 3 shows EP01 gates used to control the count enable inputs, however, if the frequency of operation is slow enough, a LVECL OR gate can be used. Using the worst case guarantees for these parameters.



## Programmable Divider

The EP016 has been designed with a control pin which makes it ideal for use as an 8-bit programmable divider. The TCLD pin (load on terminal count) when asserted reloads the data present at the parallel input pin (Pn's) upon reaching terminal count (an all 1s state on the outputs). Because this feedback is built internal to the chip, the programmable division operation will run at very nearly the same frequency as the maximum counting frequency of the device. Figure 4 below illustrates the input conditions necessary for utilizing the EP016 as a programmable divider set up to divide by 113.

## APPLICATIONS INFORMATION (CONTINUED)

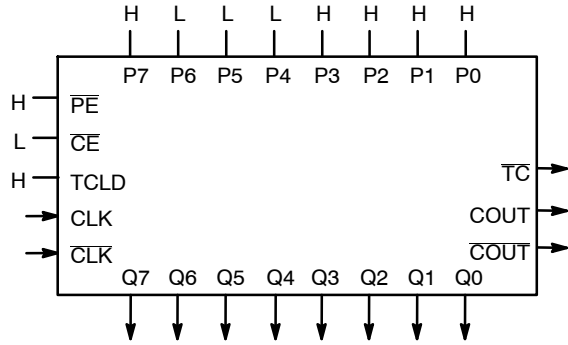


Figure 4. Mod 2 to 256 Programmable Divider

To determine what value to load into the device to accomplish the desired division, the designer simply subtracts the binary equivalent of the desired divide ratio from the binary value for 256. As an example for a divide ratio of 113:

$$Pn's = 256 - 113 = 8F_{16} = 1000\ 1111$$

where:

P0 = LSB and P7 = MSB

Forcing this input condition as per the setup in Figure 4 will result in the waveforms of Figure 5. Note that the  $\overline{TC}$  output is used as the divide output and the pulse duration is equal to a full clock period. For even divide ratios, twice the desired divide ratio can be loaded into the EP016 and the  $\overline{TC}$  output can feed the clock input of a toggle flip flop to create a signal divided as desired with a 50% duty cycle.

Table 10. PRESET VALUES FOR VARIOUS DIVIDE RATIOS

Divide Ratio	Preset Data Inputs							
	P7	P6	P5	P4	P3	P2	P1	P0
2	H	H	H	H	H	H	H	L
3	H	H	H	H	H	H	L	H
4	H	H	H	H	H	H	L	L
5	H	H	H	H	H	L	H	H
w	w	•	•	•	•	•	•	•
w	•	•	•	•	•	•	•	•
112	H	L	L	H	L	L	L	L
113	H	L	L	L	H	H	H	H
114	H	L	L	L	H	H	H	L
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
254	L	L	L	L	L	L	H	L
255	L	L	L	L	L	L	L	H
256	L	L	L	L	L	L	L	L

A single EP016 can be used to divide by any ratio from 2 to 256 inclusive. If divide ratios of greater than 256 are needed multiple EP016s can be cascaded in a manner similar to that already discussed. When EP016s are cascaded to build larger dividers the TCLD pin will no longer provide a means for loading on terminal count. Because one does not want to reload the counters until all of the devices in the chain have reached terminal count, external gating of the  $\overline{TC}$  pins must be used for multiple EP016 divider chains.

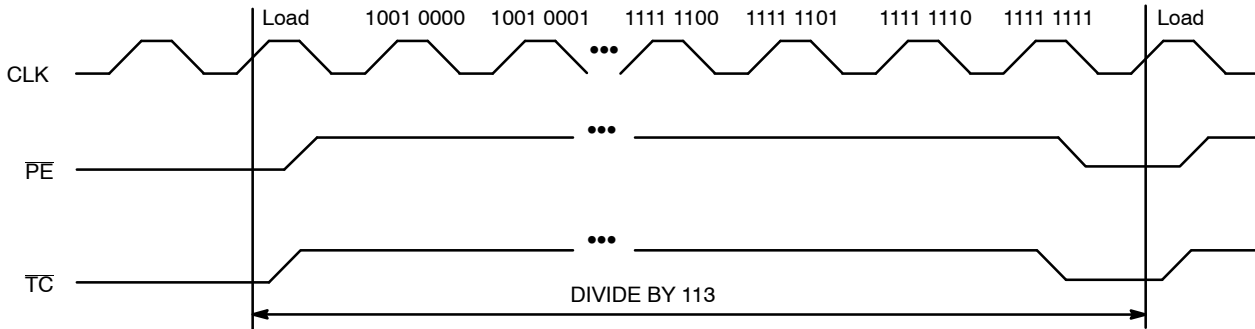


Figure 5. Divide by 113 EP016 Programmable Divider Waveforms

## APPLICATIONS INFORMATION (CONTINUED)

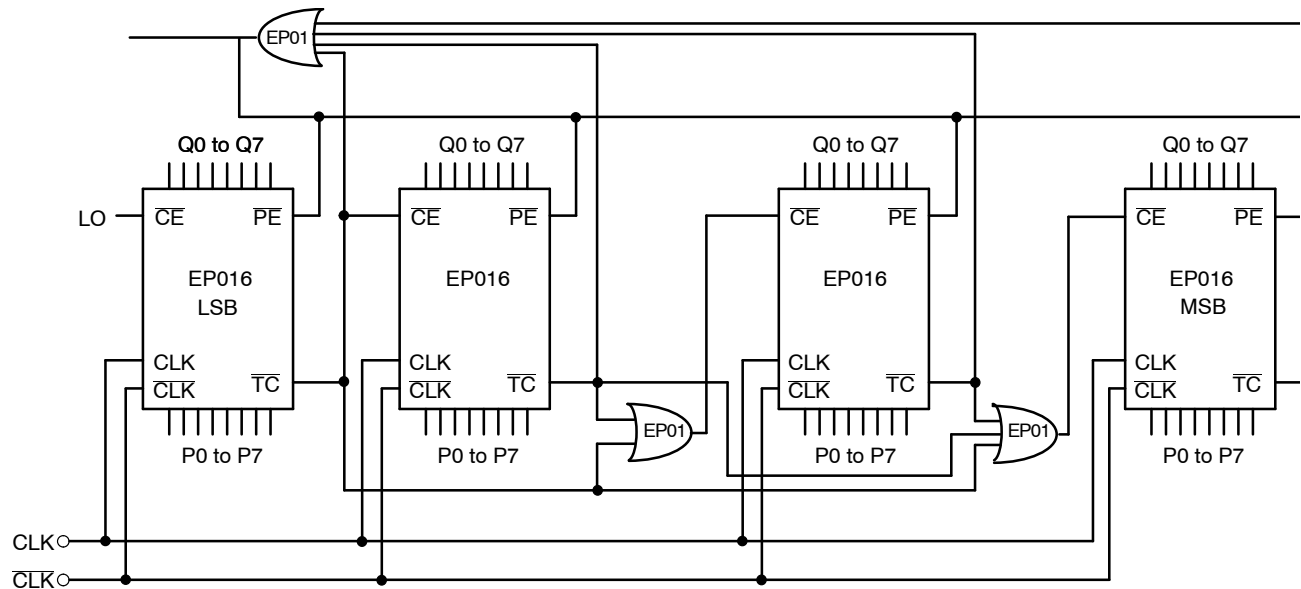


Figure 6. 32-Bit Cascaded EP016 Programmable Divider

Figure 6 shows a typical block diagram of a 32-bit divider chain. Once again to maximize the frequency of operation EP01 OR gates were used. For lower frequency applications a slower OR gate could replace the EP01. Note that for a 16-bit divider the OR function feeding the  $\overline{PE}$  (program enable) input CANNOT be replaced by a wire OR tie as the  $\overline{TC}$  output of the least significant EP016 must also feed the  $\overline{CE}$  input of the most significant EP016. If the two  $\overline{TC}$  outputs were OR tied the cascaded count operation would not operate properly. Because in the cascaded form the  $\overline{PE}$  feedback is external and requires external gating, the maximum frequency of operation will be significantly less than the same operation in a single device.

**Maximizing EP016 Count Frequency**

The EP016 device produces 9 fast transitioning single-ended outputs, thus  $V_{CC}$  noise can become significant in situations where all of the outputs switch simultaneously in the same direction. This  $V_{CC}$  noise can negatively impact the maximum frequency of operation of the device. Since the device does not need to have the Q outputs terminated to count properly, it is recommended that if the outputs are not going to be used in the rest of the system they should be left unterminated. In addition, if only a subset of the Q outputs are used in the system only those outputs should be terminated. Not terminating the unused outputs will not only cut down the  $V_{CC}$  noise generated but will also save in total system power dissipation. Following these guidelines will allow designers to either be more aggressive in their designs or provide them with an extra margin to the published data book specifications.

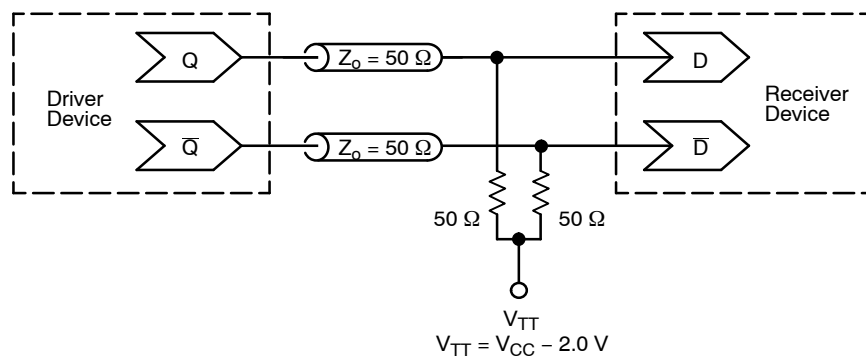


Figure 7. Typical Termination for Output Driver and Device Evaluation  
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices.)

## MC10EP016

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC10EP016FAG	LQFP-32 (Pb-Free)	250 Units / Tray
MC10EP016FAR2G	LQFP-32 (Pb-Free)	2,000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

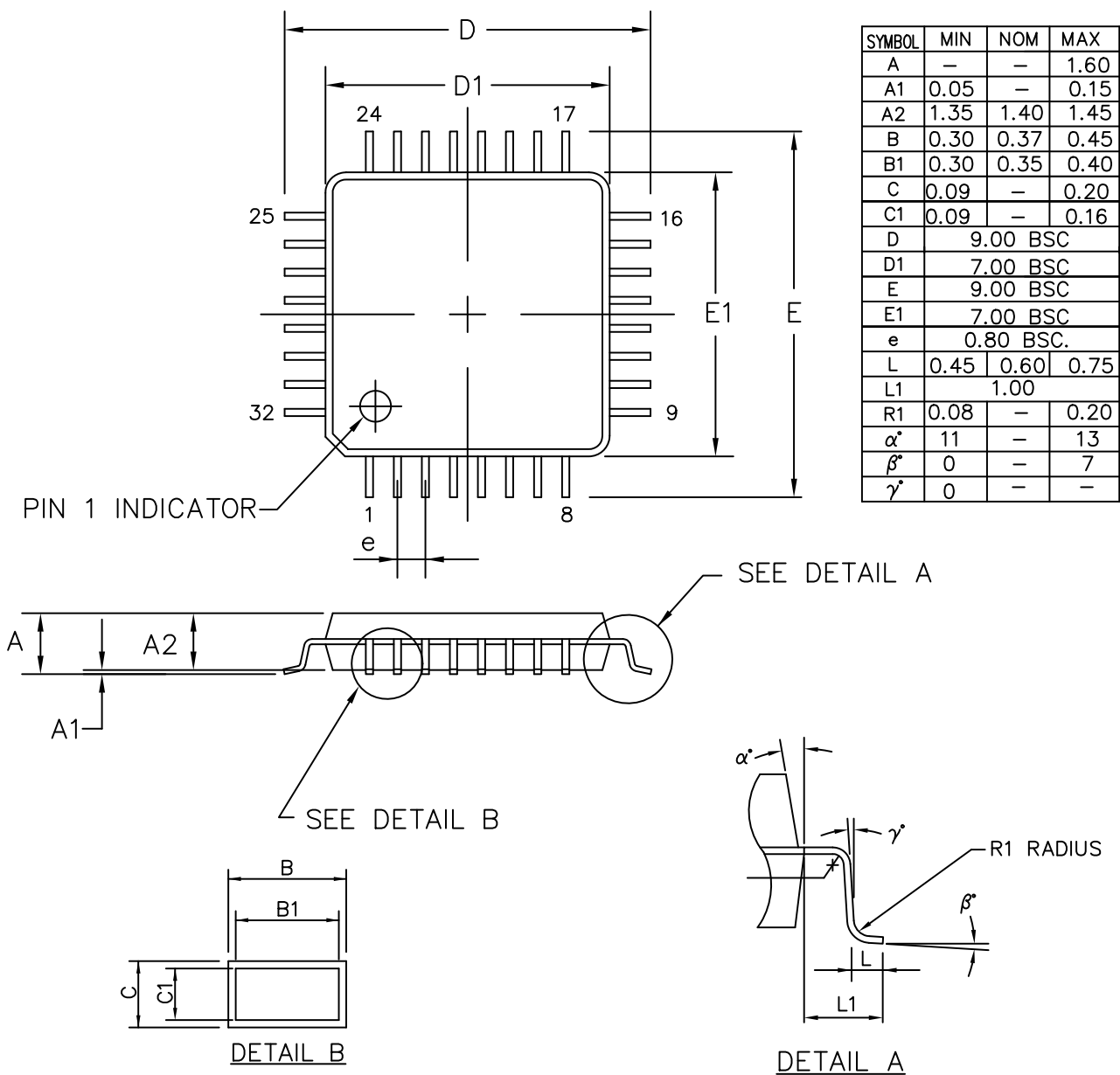
### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

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**CASE 561AB**  
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