# Undervoltage Sensing Circuit

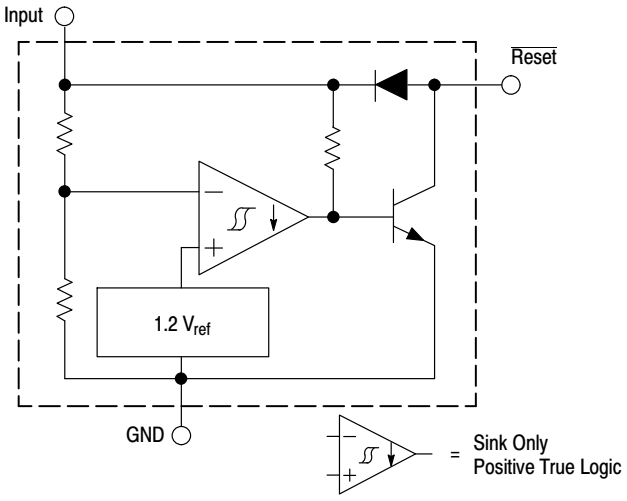
# MC34064, MC33064, NCV33064

The MC34064 is an undervoltage sensing circuit specifically designed for use as a reset controller in microprocessor−based systems. It offers the designer an economical solution for low voltage detection with a single external resistor. The MC34064 features a trimmed−in−package bandgap reference, and a comparator with precise thresholds and built-in hysteresis to prevent erratic reset operation. The open collector reset output is capable of sinking in excess of 10 mA, and operation is guaranteed down to 1.0 V input with low standby current. The MC devices are packaged in 3−pin TO-92, micro size TSOP−5, 8−pin SOIC−8 and Micro8 surface mount packages. The NCV device is packaged in SOIC−8 and TO−92.

Applications include direct monitoring of the 5.0 V MPU/logic power supply used in appliance, automotive, consumer and industrial equipment.

**Features**

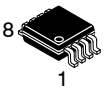
- Trimmed−In−Package Temperature Compensated Reference
- Comparator Threshold of 4.6 V at 25°C
- Precise Comparator Thresholds Guaranteed Over Temperature
- Comparator Hysteresis Prevents Erratic Reset
- Reset Output Capable of Sinking in Excess of 10 mA
- Internal Clamp Diode for Discharging Delay Capacitor
- Guaranteed Reset Operation with 1.0 V Input
- Low Standby Current
- Economical TO−92, TSOP−5, SOIC−8 and Micro8 Surface Mount Packages
- NCV Prefix for Automotive and Other Applications Requiring Site and Control Changes
- These Devices are Pb−Free and are RoHS Compliant



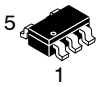

This device contains 21 active transistors.

**Figure 1. Representative Block Diagram**


**SOIC−8**
**D SUFFIX**
**CASE 751**

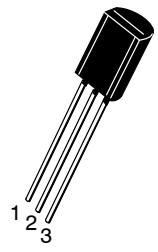



**Micro8**
**DM SUFFIX**
**CASE 846A**

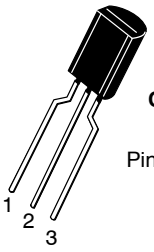



**TSOP−5**
**SN SUFFIX**
**CASE 483**

Pin 1. Ground
2. Input
3. Reset
4. NC
5. NC




STRAIGHT LEAD

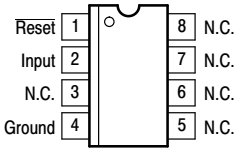



BENT LEAD

**TO−92**
**CASE 29−10**

Pin: 1. Reset
2. Input
3. Ground

## PIN CONNECTIONS




(Top View)

## ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

## DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 7 of this data sheet.

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Input Supply Voltage | $V_{in}$ | −1.0 to 10 | V |
| $\overline{\text{Reset}}$ Output Voltage | $V_O$ | 10 | V |
| $\overline{\text{Reset}}$ Output Sink Current (Note 2) | $I_{Sink}$ | Internally Limited | mA |
| Clamp Diode Forward Current, Reset to Input Pin (Note 2) | $I_F$ | 100 | mA |
| Power Dissipation and Thermal Characteristics<br>P Suffix, Plastic Package<br>Maximum Power Dissipation @ $T_A$ = 25°C<br>Thermal Resistance, Junction−to−Air<br>D Suffix, Plastic Package<br>Maximum Power Dissipation @ $T_A$ = 25°C<br>Thermal Resistance, Junction−to−Air<br>DM Suffix, Plastic Package<br>Maximum Power Dissipation @ $T_A$ = 25°C<br>Thermal Resistance, Junction−to−Air | <br><br>$P_D$<br>$R_{\theta JA}$<br><br>$P_D$<br>$R_{\theta JA}$<br><br>$P_D$<br>$R_{\theta JA}$ | <br><br>625<br>200<br><br>625<br>200<br><br>520<br>240 | <br><br>mW<br>°C/W<br><br>mW<br>°C/W<br><br>mW<br>°C/W |
| Operating Junction Temperature | $T_J$ | +150 | °C |
| Operating Ambient Temperature<br>MC34064<br>MC33064<br>NCV33064 | $T_A$ | <br>0 to +70<br>−40 to +85<br>−40 to +125 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. ESD data available upon request.

## ELECTRICAL CHARACTERISTICS (For typical values $T_A$ = 25°C, for min/max values $T_A$ is the operating ambient temperature range that applies [Notes 3 and 4] unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **COMPARATOR** | | | | | |
| Threshold Voltage<br>High State Output ($V_{in}$ Increasing)<br>Low State Output ($V_{in}$ Decreasing)<br>Hysteresis | <br>$V_{IH}$<br>$V_{IL}$<br>$V_H$ | <br>4.5<br>4.5<br>0.01 | <br>4.61<br>4.59<br>0.02 | <br>4.7<br>4.7<br>0.05 | V |
| **$\overline{\text{RESET}}$ OUTPUT** | | | | | |
| Output Sink Saturation<br>($V_{in}$ = 4.0 V, $I_{Sink}$ = 8.0 mA)<br>($V_{in}$ = 4.0 V, $I_{Sink}$ = 2.0 mA)<br>($V_{in}$ = 1.0 V, $I_{Sink}$ = 0.1 mA) | $V_{OL}$ | <br>−<br>−<br>− | <br>0.46<br>0.15<br>− | <br>1.0<br>0.4<br>0.1 | V |
| Output Sink Current ($V_{in}$, $\overline{\text{Reset}}$ = 4.0 V) | $I_{Sink}$ | 10 | 27 | 60 | mA |
| Output Off-State Leakage ($V_{in}$, $\overline{\text{Reset}}$ = 5.0 V) | $I_{OH}$ | − | 0.02 | 0.5 | μA |
| Clamp Diode Forward Voltage, Reset to Input Pin ($I_F$ = 10 mA) | $V_F$ | 0.6 | 0.9 | 1.2 | V |
| **TOTAL DEVICE** | | | | | |
| Operating Input Voltage Range | $V_{in}$ | 1.0 to 6.5 | − | − | V |
| Quiescent Input Current ($V_{in}$ = 5.0 V) | $I_{in}$ | − | 390 | 500 | μA |

2. Maximum package power dissipation limits must be observed.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
4. $T_{low}$ = 0°C for MC34064 $T_{high}$ = +70°C for MC34064
   −40°C for MC33064 +85°C for MC33064
   −40°C for NCV33064 +125°C for NCV33064
5. NCV prefix is for automotive and other applications requiring site and change control.

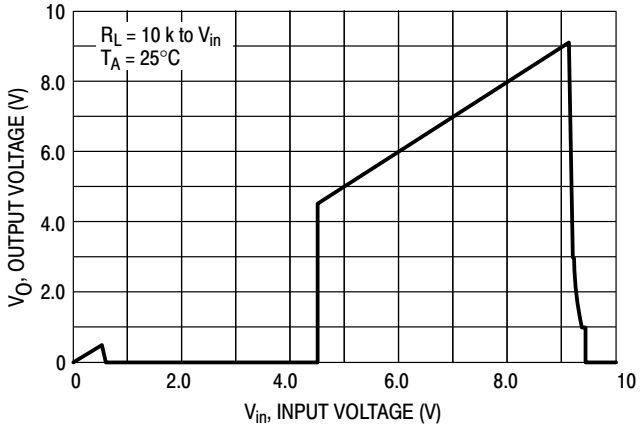



**Figure 2. $\overline{\text{Reset}}$ Output Voltage versus Input Voltage**

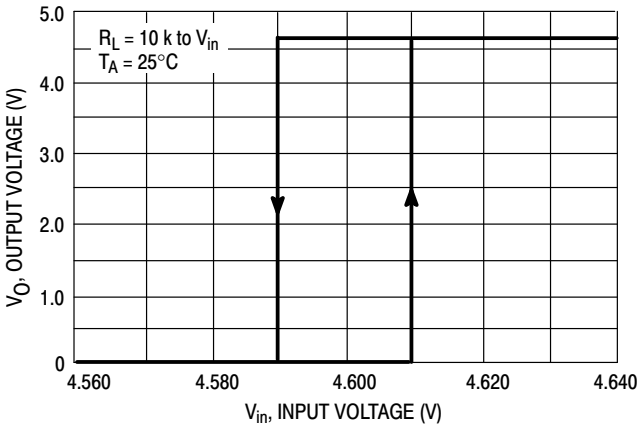



**Figure 3. $\overline{\text{Reset}}$ Output Voltage versus Input Voltage**

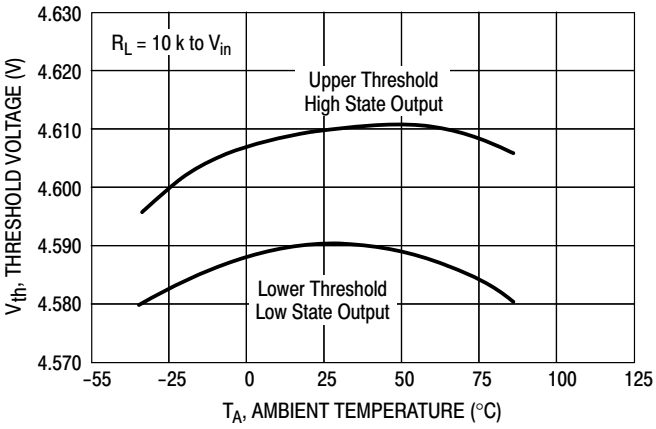



**Figure 4. Comparator Threshold Voltage versus Temperature**

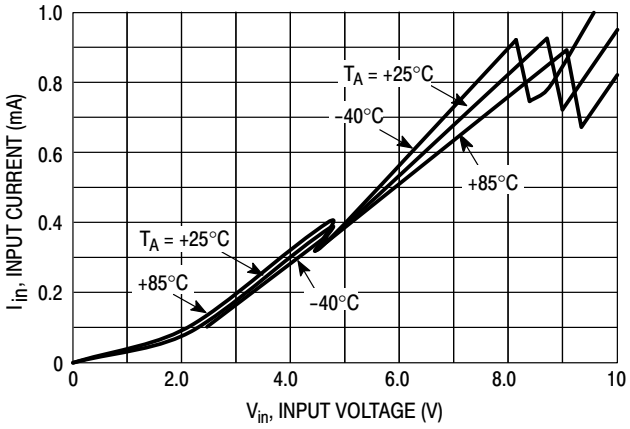



**Figure 5. Input Current versus Input Voltage**

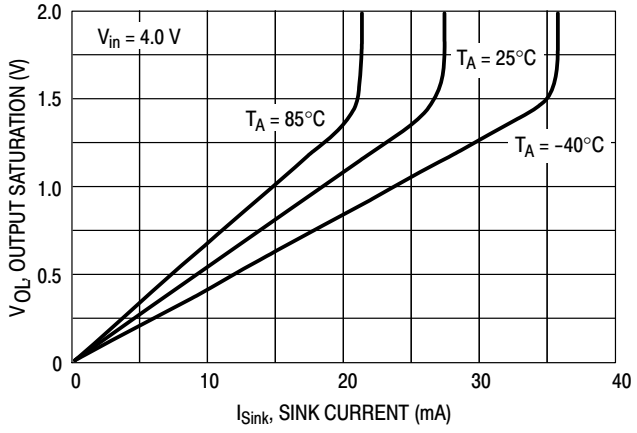



**Figure 6. $\overline{\text{Reset}}$ Output Saturation versus Sink Current**

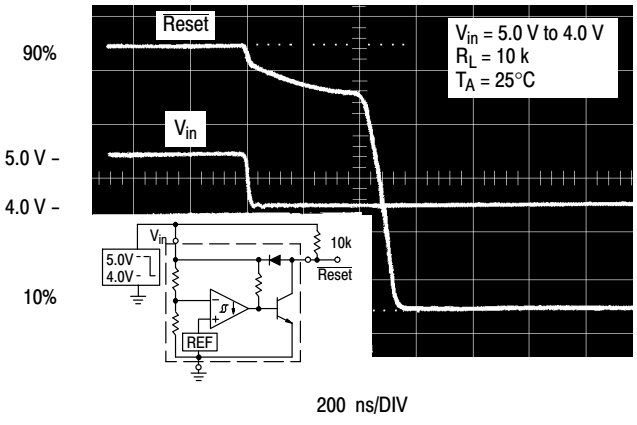



**Figure 7. $\overline{\text{Reset}}$ Delay Time**

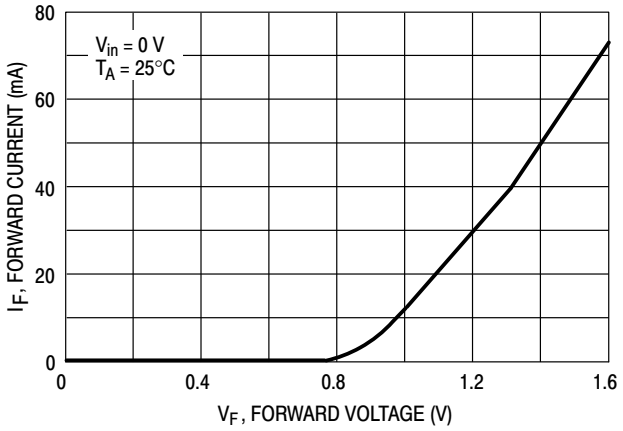



**Figure 8. Clamp Diode Forward Current versus Voltage**

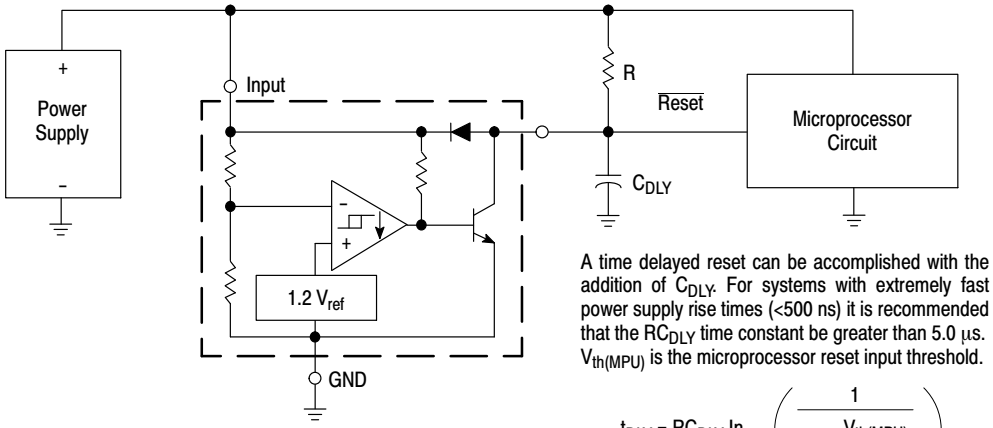
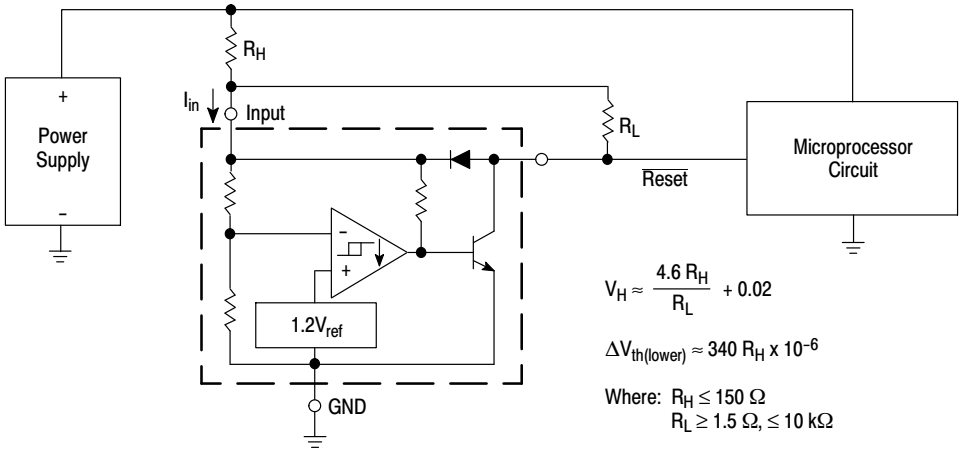



**Figure 9. Low Voltage Microprocessor Reset**




**TEST DATA**

| $V_H$ (mV) | $\Delta V_{th}$ (mV) | $R_H$ (Ω) | $R_L$ (kΩ) |
|---|---|---|---|
| 20 | 0 | 0 | 0 |
| 51 | 3.4 | 10 | 1.5 |
| 40 | 6.8 | 20 | 4.7 |
| 81 | 6.8 | 20 | 1.5 |
| 71 | 10 | 30 | 2.7 |
| 112 | 10 | 30 | 1.5 |
| 100 | 16 | 47 | 2.7 |
| 164 | 16 | 47 | 1.5 |
| 190 | 34 | 100 | 2.7 |
| 327 | 34 | 100 | 1.5 |
| 276 | 51 | 150 | 2.7 |
| 480 | 51 | 150 | 1.5 |

Comparator hysteresis can be increased with the addition of resistor $R_H$. The hysteresis equation has been simplified and does not account for the change of input current $I_{in}$ as $V_{CC}$ crosses the comparator threshold (Figure 4). An increase of the lower threshold $\Delta V_{th(lower)}$ will be observed due to $I_{in}$ which is typically 340 μA at 4.59 V. The equations are accurate to ±10% with $R_H$ less than 150 Ω and $R_L$ between 1.5 kΩ and 10 kΩ.

**Figure 10. Low Voltage Microprocessor Reset with Additional Hysteresis**

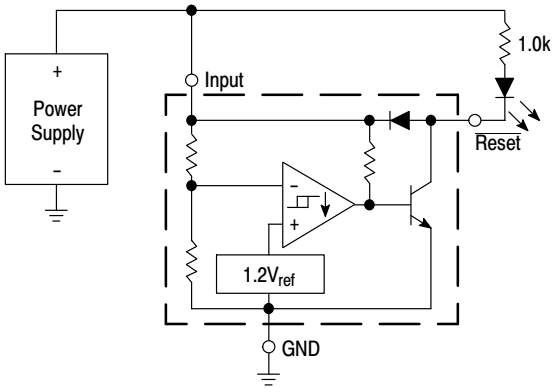



Figure 11. Voltage Monitor

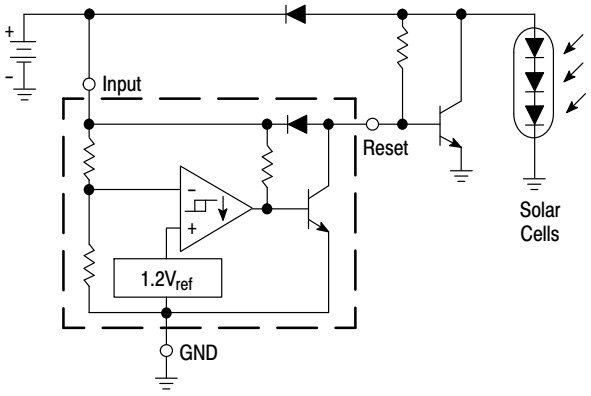
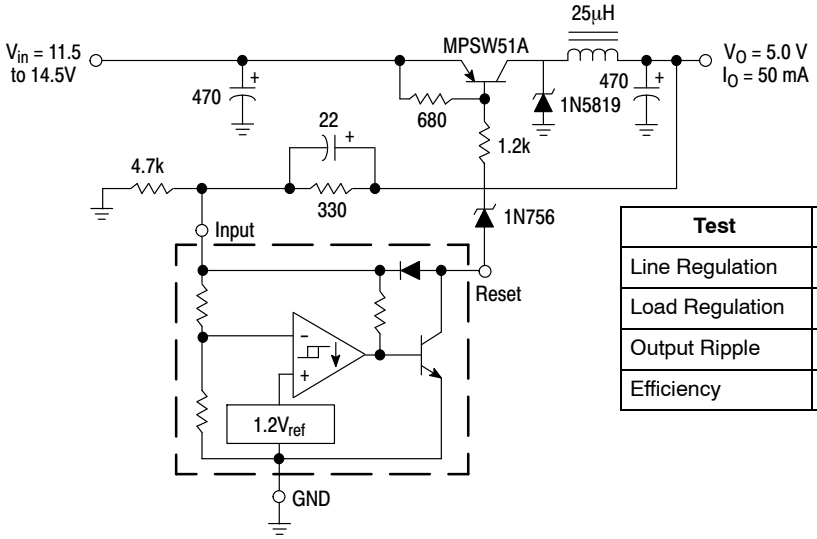
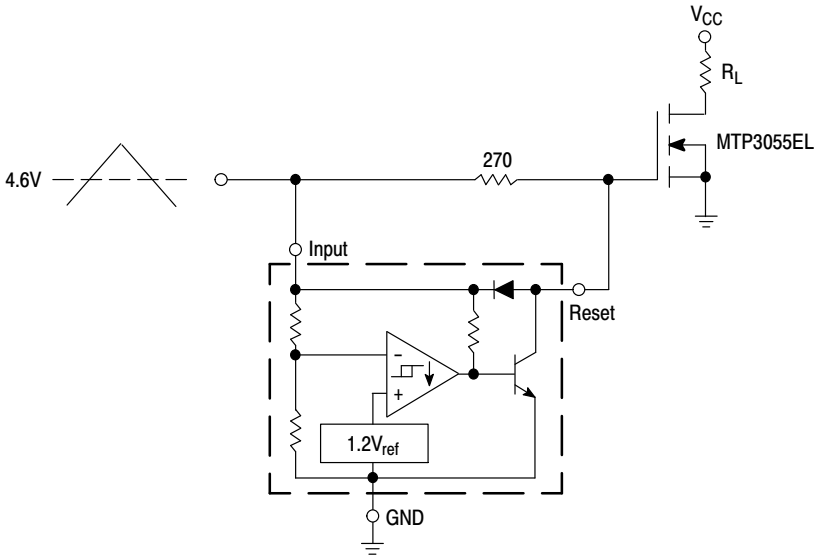



Figure 12. Solar Powered Battery Charger




| Test | Conditions | Results |
|---|---|---|
| Line Regulation | $V_{in}$ = 11.5 V to 14.5 V, $I_O$ = 50 mA | 35 mV |
| Load Regulation | $V_{in}$ = 12.6 V, $I_O$ = 0 mA to 50 mA | 12 mV |
| Output Ripple | $V_{in}$ = 12.6 V, $I_O$ = 50 mA | 60 mVpp |
| Efficiency | $V_{in}$ = 12.6 V, $I_O$ = 50 mA | 77% |

Figure 13. Low Power Switching Regulator




Overheating of the logic level power MOSFET due to insufficient gate voltage can be prevented with the above circuit. When the input signal is below the 4.6 V threshold of the MC34064, its output grounds the gate of the $L^2$ MOSFET.

Figure 14. MOSFET Low Voltage Gate Drive Protection

## ORDERING INFORMATION

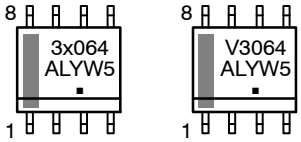
| Device | Operating Temperature Range | Package | Shipping† |
|---|---|---|---|
| MC34064D−5G | $T_A$ = 0°C to +70°C | SOIC−8 (Pb−Free) | 98 Units / Rail |
| MC34064D−5R2G | | SOIC−8 (Pb−Free) | 2500 Units/ Tape & Reel |
| MC34064DM−5R2G | | Micro8 (Pb−Free) | 4000 Units / Tape & Reel |
| MC34064P−5G | | TO−92 (Pb−Free) | 2000 Units / Bag |
| MC34064P−5RAG | | TO−92 (Pb−Free) | 2000 Units / Tape & Reel |
| MC34064P−5RPG | | TO−92 (Pb−Free) | 2000 Units / Ammo Pack |
| MC34064P−5RMG | | TO−92 (Pb−Free) | |
| MC34064SN−5T1G | | TSOP−5 (Pb−Free) | 3000 Units / Tape & Reel |
| MC33064D−5G | $T_A$ = −40°C to +85°C | SOIC−8 (Pb−Free) | 98 Units / Rail |
| MC33064D−5R2G | | SOIC−8 (Pb−Free) | 2500 Units / Tape & Reel |
| MC33064DM−5R2G | | Micro8 (Pb−Free) | 4000 Units / Tape & Reel |
| MC33064P−5G | | TO−92 (Pb−Free) | 2000 Units / Bag |
| MC33064P−5RAG | | TO−92 (Pb−Free) | 2000 Units / Tape & Reel |
| MC33064P−5RPG | | TO−92 (Pb−Free) | 2000 Units / Ammo Pack |
| MC33064SN−5T1G | | TSOP−5 (Pb−Free) | 3000 Units / Tape & Reel |
| NCV33064D−5R2G* | $T_A$ = −40°C to +125°C | SOIC−8 (Pb−Free) | 2500 Units / Tape & Reel |
| NCV33064P−5RAG* | | TO−92 (Pb−Free) | 2000 Units / Tape & Reel |
| NCV33064P−5RPG* | | TO−92 (Pb−Free) | 2000 Units / Ammo Pack |
| NCV33064DM−5R2G* | | Micro8 (Pb−Free) | 4000 Units / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, pleaserefer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

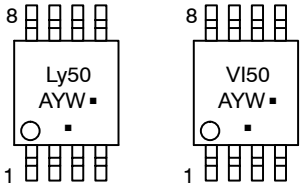
*NCV33064: $T_{low}$ = −40°C, $T_{high}$ = +125°C. Guaranteed by design. NCV prefix is for automotive and other applications requiring site and change control.

## MARKING DIAGRAMS

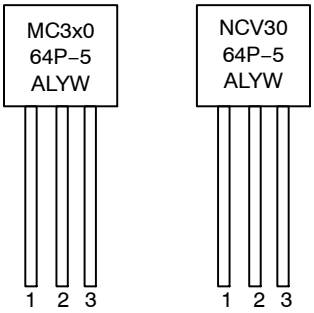
**SOIC−8**
**D SUFFIX**
**CASE 751**



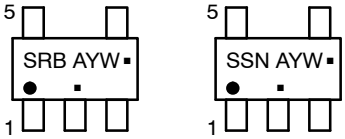

**Micro8**
**DM SUFFIX**
**CASE 846A**




**TO−92**
**P SUFFIX**
**CASE 029**




**TSOP−5**
**SN SUFFIX**
**CASE 483**




**MC34064** **MC33064**

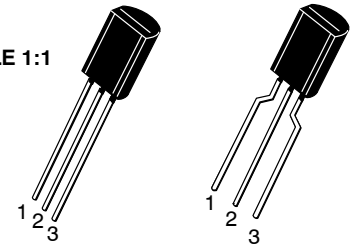
x = 3 or 4
y = C or I
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

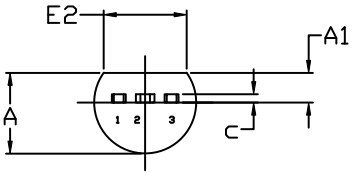
**TO−92 (TO−226) 1 WATT**
CASE 29−10
ISSUE D

DATE 05 MAR 2021

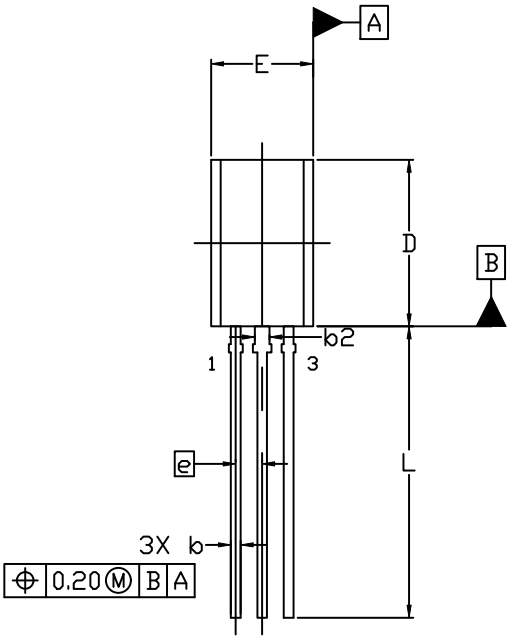
SCALE 1:1




## STRAIGHT LEAD




END VIEW




TOP VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS.
4. DIMENSION b AND b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 0.20. DIMENSION b2 LOCATED ABOVE THE DAMBAR PORTION OF MIDDLE LEAD.

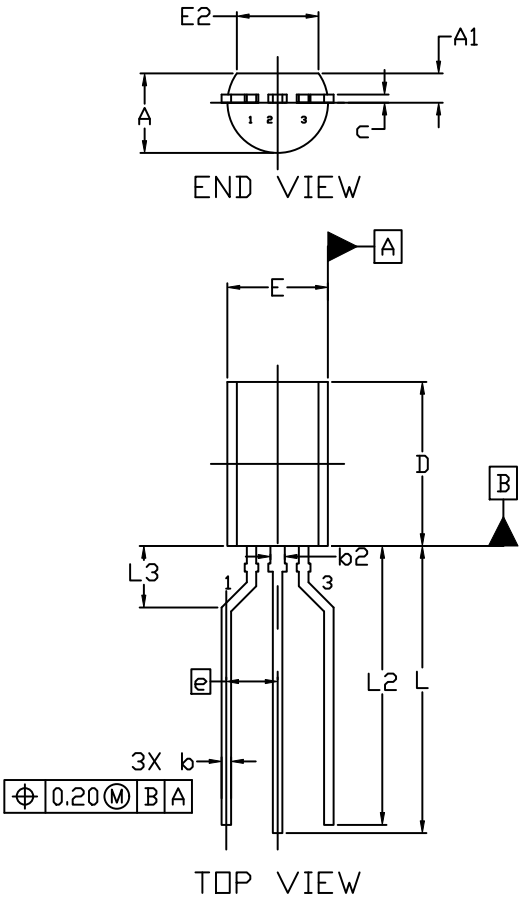
| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN. | NOM. | MAX. |
| A | 3.75 | 3.90 | 4.05 |
| A1 | 1.28 | 1.43 | 1.58 |
| b | 0.38 | 0.465 | 0.55 |
| b2 | 0.62 | 0.70 | 0.78 |
| c | 0.35 | 0.40 | 0.45 |
| D | 7.85 | 8.00 | 8.15 |
| E | 4.75 | 4.90 | 5.05 |
| E2 | 3.90 | --- | --- |
| e | 1.27 BSC | | |
| L | 13.80 | 14.00 | 14.20 |

**STYLES AND MARKING ON PAGE 3**

**TO−92 (TO−226) 1 WATT**
CASE 29−10
ISSUE D

DATE 05 MAR 2021

FORMED LEAD

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| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN. | NOM. | MAX. |
| A | 3.75 | 3.90 | 4.05 |
| A1 | 1.28 | 1.43 | 1.58 |
| b | 0.38 | 0.465 | 0.55 |
| b2 | 0.62 | 0.70 | 0.78 |
| c | 0.35 | 0.40 | 0.45 |
| D | 7.85 | 8.00 | 8.15 |
| E | 4.75 | 4.90 | 5.05 |
| E2 | 3.90 | --- | --- |
| e | 2.50 BSC | | |
| L | 13.80 | 14.00 | 14.20 |
| L2 | 13.20 | 13.60 | 14.00 |
| L3 | 3.00 REF | | |

**STYLES AND MARKING ON PAGE 3**

**TO−92 (TO−226) 1 WATT**
CASE 29−10
ISSUE D

DATE 05 MAR 2021

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN

STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE

STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2

STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

STYLE 13:
PIN 1. ANODE 1
2. GATE
3. CATHODE 2

STYLE 14:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2

STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE

STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

STYLE 18:
PIN 1. ANODE
2. CATHODE
3. NOT CONNECTED

STYLE 19:
PIN 1. GATE
2. ANODE
3. CATHODE

STYLE 20:
PIN 1. NOT CONNECTED
2. CATHODE
3. ANODE

STYLE 21:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

STYLE 23:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 24:
PIN 1. EMITTER
2. COLLECTOR/ANODE
3. CATHODE

STYLE 25:
PIN 1. MT 1
2. GATE
3. MT 2

STYLE 26:
PIN 1. $V_{CC}$
2. GROUND 2
3. OUTPUT

STYLE 27:
PIN 1. MT
2. SUBSTRATE
3. MT

STYLE 28:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 29:
PIN 1. NOT CONNECTED
2. ANODE
3. CATHODE

STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE

STYLE 31:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 32:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 33:
PIN 1. RETURN
2. INPUT
3. OUTPUT

STYLE 34:
PIN 1. INPUT
2. GROUND
3. LOGIC

STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

## GENERIC MARKING DIAGRAM*


XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

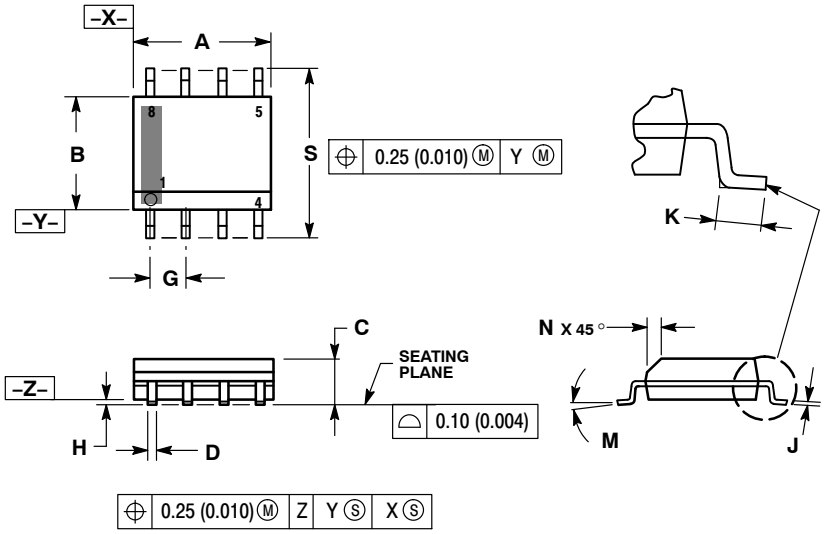
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

**SCALE 1:1**

**SOIC−8 NB**
CASE 751−07
ISSUE AK

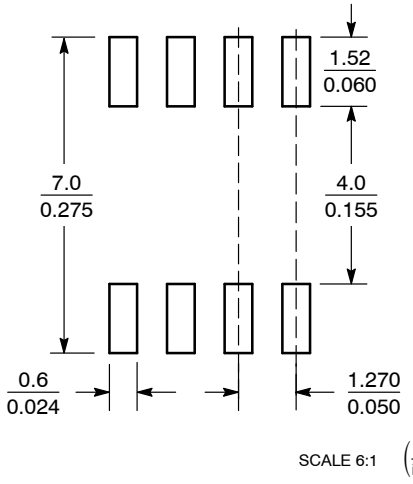
DATE 16 FEB 2011




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

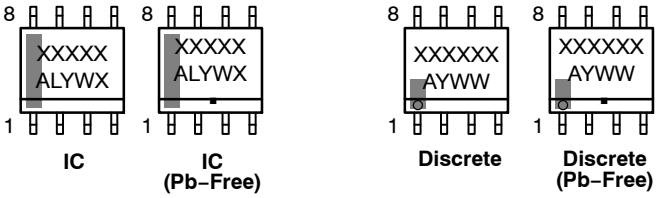
## SOLDERING FOOTPRINT*




SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**STYLES ON PAGE 2**

| | | | |
|---|---|---|---|
| **DOCUMENT NUMBER:** | **98ASB42564B** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. | |
| **DESCRIPTION:** | **SOIC−8 NB** | | **PAGE 1 OF 2** |

**SOIC−8 NB**
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

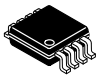
STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

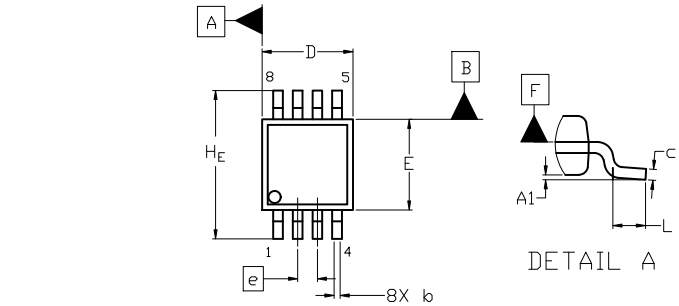
| | | | |
|---|---|---|---|
| **DOCUMENT NUMBER:** | **98ASB42564B** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. | |
| **DESCRIPTION:** | **SOIC−8 NB** | | **PAGE 2 OF 2** |

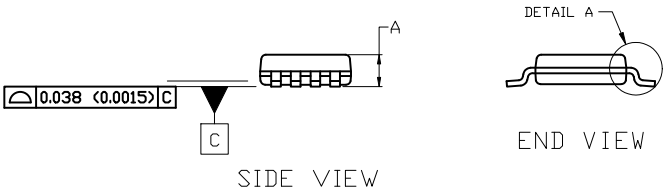


**SCALE 2:1**

**Micro8**
CASE 846A–02
ISSUE K

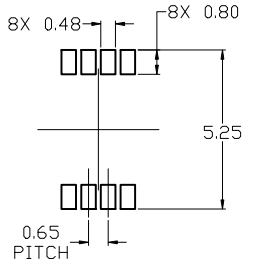
DATE 16 JUL 2020




NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

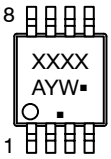



RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | --- | --- | 1.10 |
| A1 | 0.05 | 0.08 | 0.15 |
| b | 0.25 | 0.33 | 0.40 |
| c | 0.13 | 0.18 | 0.23 |
| D | 2.90 | 3.00 | 3.10 |
| E | 2.90 | 3.00 | 3.10 |
| e | 0.65 BSC | | |
| $H_E$ | 4.75 | 4.90 | 5.05 |
| L | 0.40 | 0.55 | 0.70 |

## GENERIC MARKING DIAGRAM*




XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb–Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:
PIN 1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98ASB14087C** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
| **DESCRIPTION:** | **MICRO8** | **PAGE 1 OF 1** |

## ADDITIONAL INFORMATION

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**Technical Library:** www.onsemi.com/design/resources/technical−documentation
**onsemi Website:** www.onsemi.com

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**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales