## Microcontroller Subsystem (MSS) (Ask a Question)

- Hard 100 MHz 32-bit ARM® Cortex®-M3 Processor
  - 1.25 DMIPS/MHz Throughput from Zero Wait State Memory
  - Memory Protection Unit (MPU)
  - Single Cycle Multiplication, Hardware Divide
  - JTAG Debug (4 wires), Serial Wire Debug (SWD, 2 wires), and Single Wire Viewer (SWV) Interfaces
- Internal Memory
  - Embedded Nonvolatile Flash Memory (eNVM), 128 Kbytes to 512 Kbytes
  - Embedded High-Speed SRAM (eSRAM), 16 Kbytes to 64 Kbytes, Implemented in 2 Physical Blocks to Enable Simultaneous Access from 2 Different Masters
- Multi-Layer AHB Communications Matrix
  - Provides up to 16 Gbps of On-Chip Memory Bandwidth [1] , Allowing Multi-Master Schemes
- 10/100 Ethernet MAC with RMII Interface [2]
- Programmable External Memory Controller, Which Supports:
  - Asynchronous Memories
  - NOR Flash, SRAM, PSRAM
  - Synchronous SRAMs
- Two $I^2C$ Peripherals
- Two 16550 Compatible UARTs
- Two SPI Peripherals
- Two 32-bit Timers
- 32-bit Watchdog Timer
- 8-channel DMA Controller to Offload the Cortex-M3 from Data Transactions
- Clock Sources
  - 32 KHz to 20 MHz Main Oscillator
  - Battery-Backed 32 KHz Low Power Oscillator with Real-Time Counter (RTC)
  - 100 MHz Embedded RC Oscillator; 1% Accurate
  - Embedded Analog PLL with 4 Output Phases (0, 90, 180, 270)

**Notes:**

1. Theoretical maximum
2. A2F200 and larger devices

## High-Performance FPGA (Ask a Question)

- Based on proven ProASIC® 3 FPGA Fabric
- Low Power, Firm-Error Immune 130-nm, 7-Layer Metal, Flash-Based CMOS Process

- Nonvolatile, Instant On, Retains Program When Powered Off
- 350 MHz System Performance
- Embedded SRAMs and FIFOs
  - Variable Aspect Ratio 4,608-Bit SRAM Blocks
  - x1, x2, x4, x9, and x18 Organizations
  - True Dual-Port SRAM (excluding x18)
  - Programmable Embedded FIFO Control Logic
- Secure ISP with 128-bit AES via JTAG
- FlashLock® to Secure FPGA Contents
- Five Clock Conditioning Circuits (CCCs) with up to 2 Integrated Analog PLLs
  - Phase Shift, Multiply/Divide, and Delay Capabilities
  - Frequency: Input 1.5–350 MHz, Output 0.75 to 350 MHz

## Programmable Analog (Ask a Question)

### Analog Front-End (AFE)

- Up to Three 12-Bit SAR ADCs
  - 500 Ksps in 12-Bit Mode
  - 550 Ksps in 10-Bit Mode
  - 600 Ksps in 8-Bit Mode
- Internal 2.56V Reference or Optional External Reference
- One First-Order ΣΔ DAC (sigma-delta) per ADC
  - 8-Bit, 16-Bit, or 24-Bit 500 Ksps Update Rate
- Up to 5 High-Performance Analog Signal Conditioning Blocks (SCB) per Device, Each Including:
  - Two High-Voltage Bipolar Voltage Monitors (with 4 input ranges from ±2.5V to –11.5/+14V) with 1% Accuracy
  - High Gain Current Monitor, Differential Gain = 50, up to 14V Common Mode
  - Temperature Monitor (Resolution = ¼ °C in 12-Bit Mode; Accurate from –55 °C to 150 °C)
- Up to Ten High-Speed Voltage Comparators (tpd = 15 ns)

### Analog Compute Engine (ACE)

- Offloads Cortex-M3–Based MSS from Analog Initialization and Processing of ADC, DAC, and SCBs
- Sample Sequence Engine for ADC and DAC Parameter Set-Up
- Post-Processing Engine for Functions such as Low-Pass Filtering and Linear Transformation
- Easily Configured via GUI in Libero® System-on-Chip (SoC) Software

## I/Os and Operating Voltage (Ask a Question)

- FPGA I/Os
  - LVDS, PCI, PCI-X, up to 24 mA IOH/IOL
  - Up to 350 MHz
- MSS I/Os
  - Schmitt Trigger, up to 6 mA IOH, 8 mA IOL
  - Up to 180 MHz
- Single 3.3V Power Supply with On-Chip 1.5V Regulator

- External 1.5V Is Allowed by Bypassing Regulator (digital VCC = 1.5V for FPGA and MSS, analog VCC = 3.3V and 1.5V)

## SmartFusion cSoC Family Product Table (Ask a Question)

**Table 1.** SmartFusion cSoC Family Product Table

| FPGA Fabric | A2F060[1] | | | A2F200 | | | | A2F500 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | TQ144 | CS288 | FG256 | PQ208 | CS288 | FG256 | FG484 | PQ208 | CS288 | FG256 | FG484 |
| System Gates | 60,000 | | | 200,000 | | | | 500,000 | | | |
| Tiles (D-flip-flops) | 1,536 | | | 4,608 | | | | 11,520 | | | |
| RAM Blocks (4,608 bits) | 8 | | | 8 | | | | 24 | | | |
| **Microcontroller Subsystem (MSS)** | **A2F060** | | | **A2F200** | | | | **A2F500** | | | |
| | **TQ144** | **CS288** | **FG256** | **PQ208** | **CS288** | **FG256** | **FG484** | **PQ208** | **CS288** | **FG256** | **FG484** |
| Flash (Kbytes) | 128 | | | 256 | | | | 512 | | | |
| SRAM (Kbytes) | 16 | | | 64 | | | | 64 | | | |
| Cortex®-M3 processor with MPU | Yes | | | Yes | | | | Yes | | | |
| 10/100 Ethernet MAC | No | | | Yes | | | | Yes | | | |
| External Memory Controller (EMC) | — | 26-/16-bit address/data | | 26-bit address,16-bit data | | | | — | 26-/16-bit address/data | | |
| DMA | 8 Ch | | | 8 Ch | | | | 8 Ch | | | |
| $I^2C$ | 2 | | | 2 | | | | 2 | | | |
| SPI | 1 | 2 | | 1 | 2 | | | 1 | 2 | | |
| 16550 UART | 2 | | | 2 | | | | 2 | | | |
| 32-Bit Timer | 2 | | | 2 | | | | 2 | | | |
| PLL | 1 | | | 1 | | | | 1 | 2 | 1 | 2 |
| 32 KHz Low Power Oscillator | 1 | | | 1 | | | | 1 | | | |
| 100 MHz On-Chip RC Oscillator | 1 | | | 1 | | | | 1 | | | |
| Main Oscillator (32 KHz to 20 MHz) | 1 | | | 1 | | | | 1 | | | |
| **Programmable Analog** | **A2F060[1]** | | | **A2F200** | | | | **A2F500** | | | |
| | **TQ144** | **CS288** | **FG256** | **PQ208** | **CS288** | **FG256** | **FG484** | **PQ208** | **CS288** | **FG256** | **FG484** |
| ADCs (8-/10-/12-bit SAR) | 1 | | | 2 | | | | 2 | | | 3 |
| DACs (8-/16-/24-bit sigma-delta) | 1 | | | 2 | | | | 2 | | | 3 |
| Signal Conditioning Blocks (SCBs) | 1 | | | 4 | | | | 4 | | | 5 |
| Comparator[2] | 2 | | | 8 | | | | 8 | | | 10 |
| Current Monitors[2] | 1 | | | 4 | | | | 4 | | | 5 |
| Temperature Monitors[2] | 1 | | | 4 | | | | 4 | | | 5 |
| Bipolar High Voltage Monitors[2] | 2 | | | 8 | | | | 8 | | | 10 |

**Notes:**

1. Part No A2F060 is discontinued.
2. These functions share I/O pins and may not all be available at the same time. See the “Analog Front-End Overview” section in the UG0251: SmartFusion Analog User Guide for details.

## Package I/Os: MSS + FPGA I/Os (Ask a Question)

**Table 2.** Package I/Os: MSS + FPGA I/Os

| Device | A2F060[1] | | | A2F200[2] | | | | A2F500[2] | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Package | TQ144 | CS288 | FG256 | PQ208 | CS288 | FG256 | FG484 | PQ208 | CS288 | FG256 | FG484 |
| Direct Analog Inputs | 11 | 11 | 11 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 12 |
| Shared Analog Inputs | 4 | 4 | 4 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 20 |
| Total Analog Inputs | 15 | 15 | 15 | 24 | 24 | 24 | 24 | 24 | 24 | 24 | 32 |
| Analog Outputs | 1 | 1 | 1 | 1 | 2 | 2 | 2 | 1 | 2 | 2 | 3 |
| MSS I/Os[3, 4] | 21[5] | 28[5] | 26[5] | 22 | 31 | 25 | 41 | 22 | 31 | 25 | 41 |
| FPGA I/Os | 33[6] | 68 | 66 | 66 | 78 | 66 | 94 | 66[6] | 78 | 66 | 128 |
| Total I/Os | 70 | 112 | 108 | 113 | 135 | 117 | 161 | 113 | 135 | 117 | 204 |

**Notes:**

1. Part No A2F060 is discontinued.
2. These pins are shared between direct analog inputs to the ADCs and voltage/current/temperature monitors.
3. 16 MSS I/Os are multiplexed and can be used as FPGA I/Os, if not needed for MSS. These I/Os support Schmitt triggers and support only LVTTL and LVCMOS (1.5/1.8/2.5, 3.3V) standards.
4. 9 MSS I/Os are primarily for 10/100 Ethernet MAC and are also multiplexed and can be used as FPGA I/Os if Ethernet MAC is not used in a design. These I/Os support Schmitt triggers and support only LVTTL and LVCMOS (1.5/1.8/2.5, 3.3V standards.
5. 10/100 Ethernet MAC is not available on A2F060.
6. EMC is not available on the A2F500 PQ208 and A2F060 TQ144 package.

**Table 3.** SmartFusion cSoC Package Sizes Dimensions

| Package | TQ144 | PQ208 | CS288 | FG256 | FG484 |
|---|---|---|---|---|---|
| Length × Width (mm \ mm) | 20 × 20 | 28 × 28 | 11 × 11 | 17 × 17 | 23 × 23 |
| Nominal Area ($mm^2$) | 400 | 784 | 121 | 289 | 529 |
| Pitch (mm) | 0.5 | 0.5 | 0.5 | 1.0 | 1.0 |
| Height (mm) | 1.40 | 3.40 | 1.05 | 1.60 | 2.23 |

## SmartFusion cSoC Device Status (Ask a Question)

**Table 4.** SmartFusion cSoC Device Status

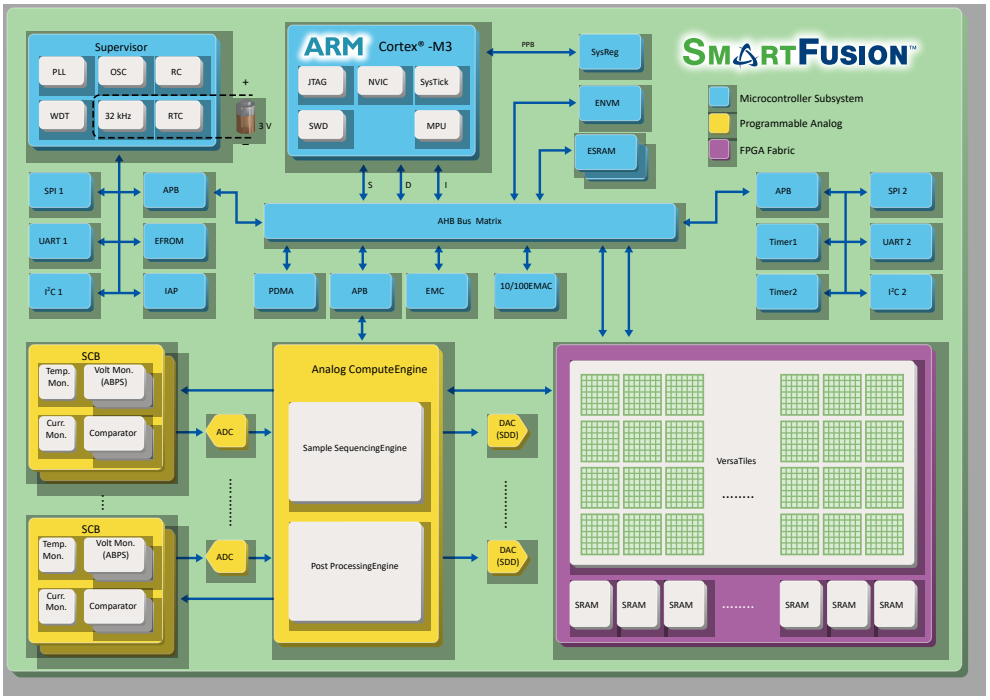
| Device | Status |
|---|---|
| A2F060 [1] | Preliminary: CS288, FG256, TQ144 |
| A2F200 | Production: CS288, FG256, FG484, PQ208 |
| A2F500 | Production: CS288, FG256, FG484, PQ208 |

**Note:**

1. Part No A2F060 is discontinued.

## SmartFusion cSoC Block Diagram (Ask a Question)

**Figure 1.** SmartFusion cSoC Block Diagram

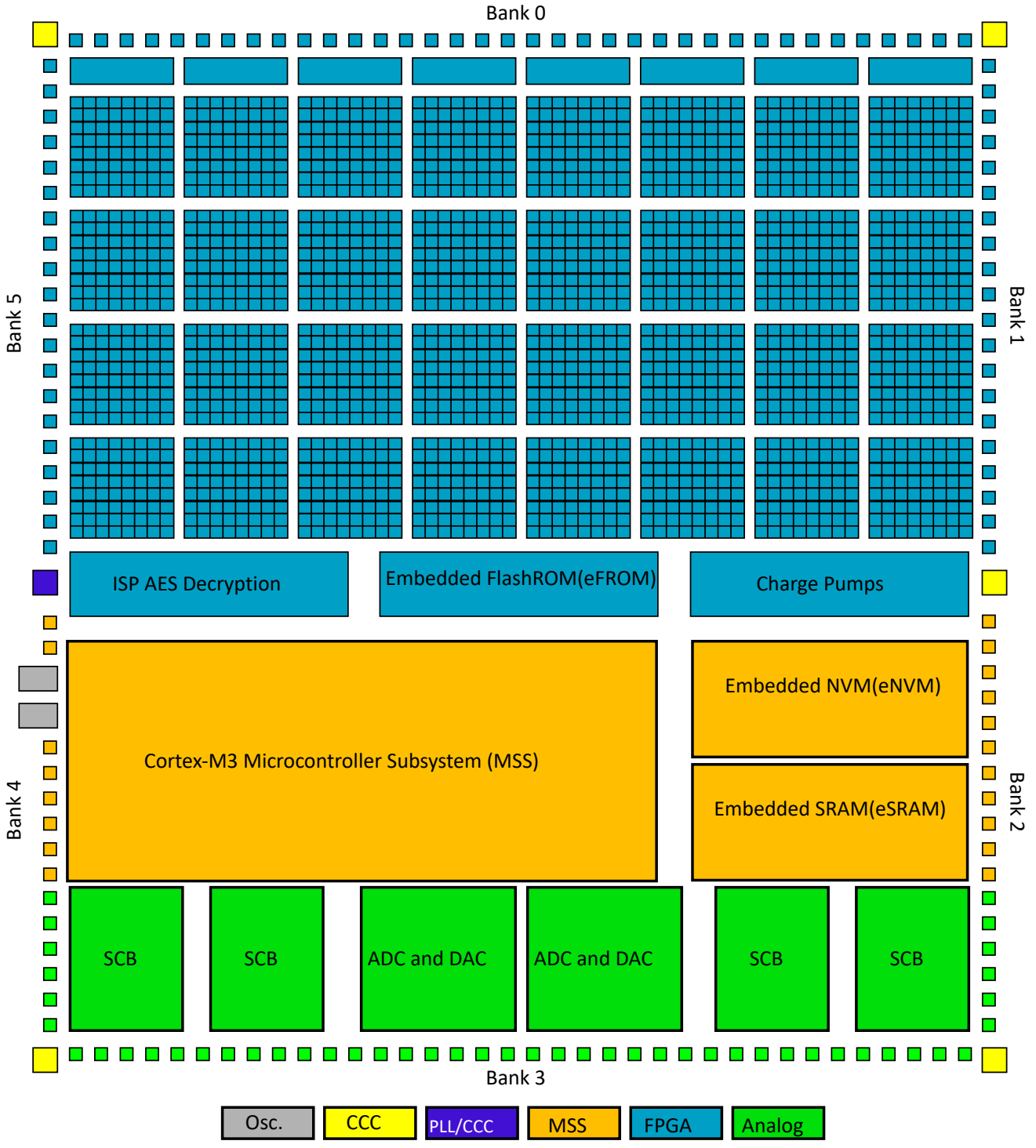



**Legend:**

- SDD – Sigma-delta DAC
- SCB – Signal conditioning block
- PDMA – Peripheral DMA
- IAP – In-application programming
- ABPS – Active bipolar prescaler
- WDT – Watchdog Timer
- SWD – Serial Wire Debug

## SmartFusion cSoC System Architecture (Ask a Question)

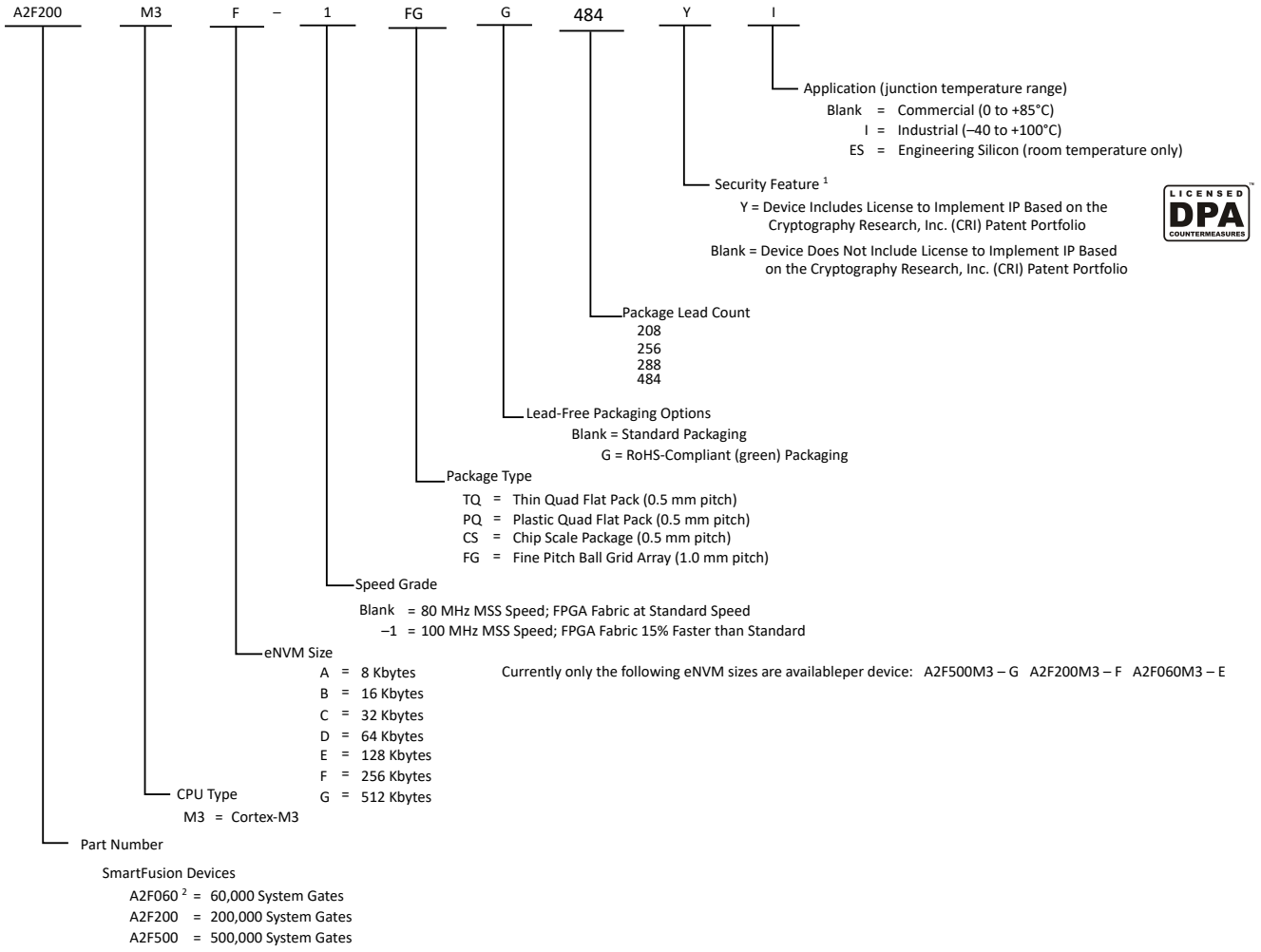
**Figure 2.** SmartFusion cSoC System Architecture




**Note:** Architecture for A2F200.

# Product Ordering Codes (Ask a Question)

**Figure 3.** Product Ordering Codes




**Notes:**

1. Most devices in the SmartFusion cSoC family can be ordered with the Y suffix. Devices with a package size greater or equal to 5 x 5 mm are supported. Contact your local Microchip sales representative for more information.
2. Part No A2F060 is discontinued.

# Temperature Grade Offerings (Ask a Question)

**Table 5.** Temperature Grade Offerings

| SmartFusion® cSoC | A2F060[3] | A2F200 | A2F500 |
|---|---|---|---|
| TQ144 | C, I | — | — |
| PQ208 | — | C, I | C, I |
| CS288 | C, I | C, I | C, I |
| FG256 | C, I | C, I | C, I |

| .....continued | | | |
|---|---|---|---|
| SmartFusion® cSoC | A2F060[3] | A2F200 | A2F500 |
| FG484 | — | C, I | C, I |

**Notes:**

1. C = Commercial Temperature Range: 0 °C to 85 °C Junction
2. I = Industrial Temperature Range: –40 °C to 100 °C Junction
3. Part No A2F060 is discontinued.

# Table of Contents

# 1. Introduction (Ask a Question)

The SmartFusion® family of cSoCs builds on the technology first introduced with the Fusion mixed signal FPGAs. SmartFusion cSoCs are made possible by integrating FPGA technology with programmable high-performance analog and hardened ARM Cortex-M3 microcontroller blocks on a flash semiconductor process. The SmartFusion cSoC takes its name from the fact that these three discrete technologies are integrated on a single chip, enabling the lowest cost of ownership and smallest footprint solution to you.

# 2. General Description (Ask a Question)

## 2.1 Microcontroller Subsystem (MSS) (Ask a Question)

The MSS is composed of a 100 MHz Cortex-M3 processor and integrated peripherals, which are interconnected via a multi-layer AHB bus matrix (ABM). This matrix allows the Cortex-M3 processor, FPGA fabric master, Ethernet media access controller (MAC), when available, and peripheral DMA (PDMA) controller to act as masters to the integrated peripherals, FPGA fabric, embedded nonvolatile memory (eNVM), embedded synchronous RAM (eSRAM), external memory controller (EMC), and analog compute engine (ACE) blocks.

SmartFusion cSoCs of different densities offer various sets of integrated peripherals. Available peripherals include SPI, $I^2C$, and UART serial ports, embedded FlashROM (EFROM), 10/100 Ethernet MAC, timers, phase-locked loops (PLLs), oscillators, real-time counters (RTC), and peripheral DMA controller (PDMA).

## 2.2 Programmable Analog (Ask a Question)

### Analog Front-End (AFE)

SmartFusion cSoCs offer an enhanced analog front-end compared to Fusion devices. The successive approximation register analog-to-digital converters (SAR ADC) are similar to those found on Fusion devices. SmartFusion cSoC also adds first order sigma-delta digital-to-analog converters (SDD DAC).

SmartFusion cSoCs can handle multiple analog signals simultaneously with its signal conditioning blocks (SCBs). SCBs are made of a combination of active bipolar prescalers (ABPS), comparators, current monitors and temperature monitors. ABPS modules allow larger bipolar voltages to be fed to the ADC. Current monitors take the voltage across an external sense resistor and convert it to a voltage suitable for the ADC input range. Similarly, the temperature monitor reads the current through an external PN-junction (diode or transistor) and converts it internally for the ADC. The SCB also includes comparators to monitor fast signal thresholds without using the ADC. The output of the comparators can be fed to the analog compute engine or the ADC.

### Analog Compute Engine (ACE)

The mixed signal blocks found in SmartFusion cSoCs are controlled and connected to the rest of the system via a dedicated processor called the analog compute engine (ACE). The role of the ACE is to offload control of the analog blocks from the Cortex-M3, thus offering faster throughput or better power consumption compared to a system where the main processor is in charge of monitoring the analog resources. The ACE is built to handle sampling, sequencing, and post-processing of the ADCs, DACs, and SCBs.

## 2.3 ProASIC3 FPGA Fabric (Ask a Question)

The SmartFusion cSoC family, based on the proven, low power, firm-error immune ProASIC®3 flash FPGA architecture, benefits from the advantages only flash-based devices offer:

### Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, high performance, and ease of use. Flash-based SmartFusion cSoCs are Instant On and do not need to be loaded from an external boot PROM at each power-up. On-board security mechanisms prevent access to the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system programming (ISP) to support future design iterations and critical field upgrades, with confidence that valuable IP cannot be compromised or copied. Secure ISP can be performed using the industry standard AES algorithm with MAC data authentication on the device.

### Low Power

Flash-based SmartFusion cSoCs exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. With SmartFusion cSoCs, there is no power-on current and no high current transition, both of which are common with SRAM-based FPGAs.

SmartFusion cSoCs also have low dynamic power consumption and support very low power time-keeping mode, offering further power savings.

### Security

As the nonvolatile, flash-based SmartFusion cSoC family requires no boot PROM, there is no vulnerable external bitstream. SmartFusion cSoCs incorporate FlashLock®, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only a device with nonvolatile flash programming can offer.

SmartFusion cSoCs utilize a 128-bit flash-based key lock and a separate AES key to provide security for programmed IP and configuration data. The FlashROM data in Fusion devices can also be encrypted prior to loading. Additionally, the flash memory blocks can be programmed during runtime using the AES-128 block cipher encryption standard (FIPS Publication 192).

SmartFusion cSoCs with AES-based security are designed to provide protection for remote field updates over public networks, such as the Internet, and help to ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. As an additional security measure, the FPGA configuration data of a programmed Fusion device cannot be read back, although secure design verification is possible. During design, the user controls and defines both internal and external access to the flash memory blocks.

Security, built into the FPGA fabric, is an inherent component of the SmartFusion cSoC family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. SmartFusion cSoCs, with FlashLock and AES security, are unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with industry standard security measures, making remote ISP feasible. A SmartFusion cSoC provides the highest security available for programmable logic designs.

### Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based SmartFusion cSoCs do not require system configuration components such as electrically erasable programmable read-only memories (EEPROMs) or microcontrollers to load device configuration data during power-up. This reduces bill-of-materials costs and PCB area, and increases system security and reliability.

### Instant On

Flash-based SmartFusion cSoCs are Instant On. Instant On SmartFusion cSoCs greatly simplify total system design and reduce total system cost by eliminating the need for complex programmable logic devices (CPLDs). SmartFusion Instant On clocking (PLLs) replace off-chip clocking resources. In addition, glitches and brownouts in system power will not corrupt the SmartFusion flash configuration. Unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored.

This enables reduction or complete removal of expensive voltage monitor and brownout detection devices from the PCB design. Flash-based SmartFusion cSoCs simplify total system design and reduce cost and design risk, while increasing system reliability.

### Immunity to Firm Errors

Firm errors occur most commonly when high-energy neutrons, generated in the atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O configuration behavior in an unpredictable way.

Another source of radiation-induced firm errors is alpha particles. For alpha radiation to cause a soft or firm error, its source must be in very close proximity to the affected circuit. The alpha source must be in the package molding compound or in the die itself. While low-alpha molding compounds

are being used increasingly, this helps reduce but does not entirely eliminate alpha-induced firm errors.

Firm errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not occur in SmartFusion cSoCs. Once it is programmed, the flash cell configuration element of SmartFusion cSoCs cannot be altered by high energy neutrons and is therefore immune to errors from them. Recoverable (or soft) errors occur in the user data SRAMs of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

## 2.4 Specifying I/O States During Programming (Ask a Question)

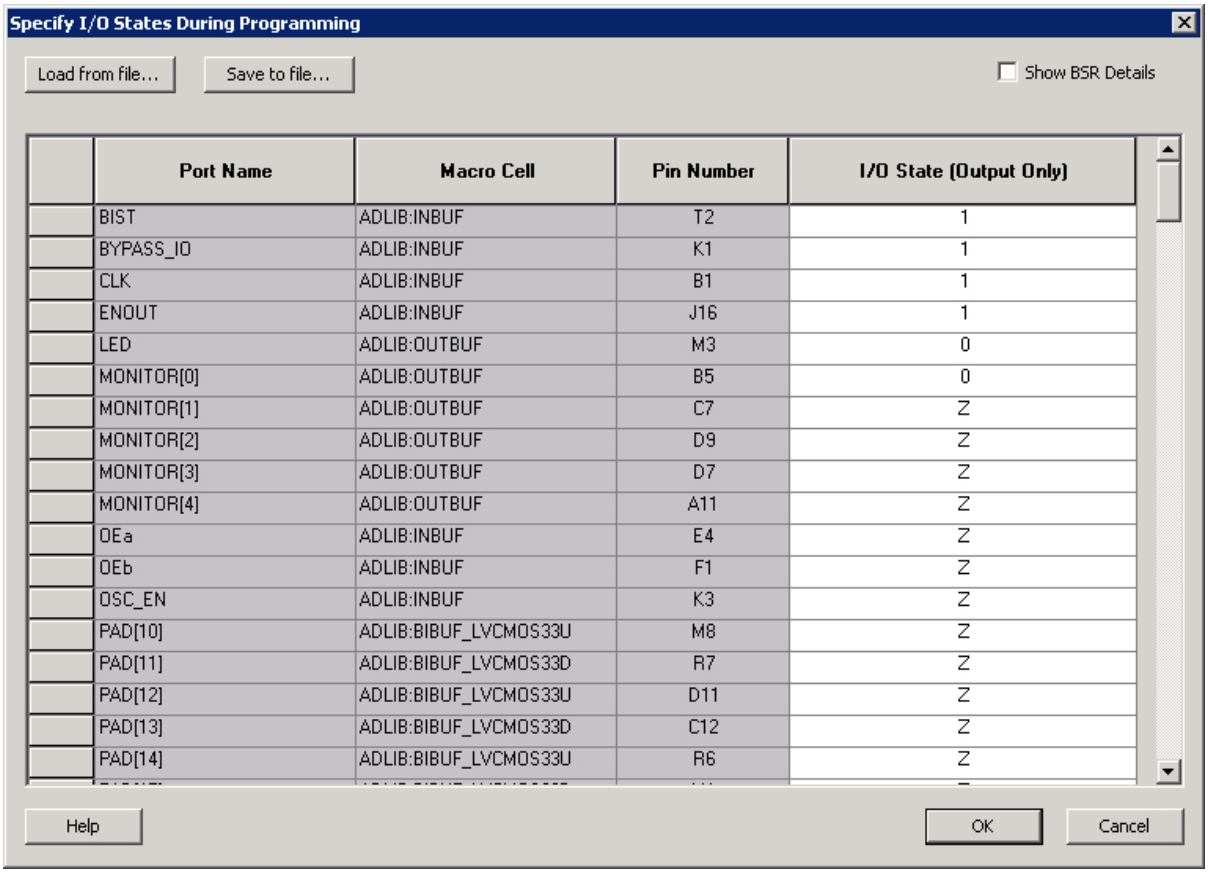
You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the FlashPro User's Guide for more information.

**Note:** PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

The I/Os are controlled by the JTAG Boundary Scan register during programming, except for the analog pins (AC, AT and AV). The Boundary Scan register of the AG pin can be used to enable/disable the gate driver in software v9.0.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the **Specify I/O States During Programming** dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 2-1).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:
   - 1 – I/O is set to drive out logic High.
   - 0 – I/O is set to drive out logic Low.
   - Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming.
   - Z -Tri-State – I/O is tristated.

**Figure 2-1.** I/O States During Programming Window




6. Click **OK** to return to the FlashPoint – Programming File Generator window.

**Note:** I/O States during programming are saved to the ADB and resulting programming files after completing programming file generation.

# 3. General Specifications (Ask a Question)

## 3.1 Operating Conditions (Ask a Question)

Stresses beyond the operating conditions listed in Table 3-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 3-3 is not implied.

**Table 3-1.** Absolute Maximum Ratings

| Symbol | Parameter | Limits | Units |
|---|---|---|---|
| VCC | DC core supply voltage | –0.3 to 1.65 | V |
| VJTAG | JTAG DC voltage | –0.3 to 3.75 | V |
| VPP | Programming voltage | –0.3 to 3.75 | V |
| VCCPLLx | Analog power supply (PLL) | –0.3 to 1.65 | V |
| VCCFPGAIOBx | DC FPGA I/O buffer supply voltage | –0.3 to 3.75 | V |
| VCCMSSIOBx | DC MSS I/O buffer supply voltage | –0.3 to 3.75 | V |
| VI | I/O input voltage | –0.3V to 3.6V<br>(when I/O hot insertion mode is enabled)<br>–0.3V to (VCCxxxxIOBx + 1V) or 3.6V, whichever voltage is lower (when I/O hot-insertion mode is disabled) | V |
| VCC33A | Analog clean 3.3V supply to the analog circuitry | –0.3 to 3.75 | V |
| VCC33ADCx | Analog 3.3V supply to ADC | –0.3 to 3.75 | V |
| VCC33AP | Analog clean 3.3V supply to the charge pump | –0.3 to 3.75 | V |
| VCC33SDDx | Analog 3.3V supply to the sigma-delta DAC | –0.3 to 3.75 | V |
| VAREFx | Voltage reference for ADC | 1.0 to 3.75 | V |
| VCCRCOSC | Analog supply to the integrated RC oscillator | –0.3 to 3.75 | V |
| VDDBAT | External battery supply | –0.3 to 3.75 | V |
| VCCMAINXTAL | Analog supply to the main crystal oscillator | –0.3 to 3.75 | V |
| VCCLPXTAL | Analog supply to the low power 32 kHz crystal oscillator | –0.3 to 3.75 | V |
| VCCENVM | Embedded nonvolatile memory supply | –0.3 to 1.65 | V |
| VCCESRAM | Embedded SRAM supply | –0.3 to 1.65 | V |
| VCC15A | Analog 1.5V supply to the analog circuitry | –0.3 to 1.65 | V |
| VCC15ADCx | Analog 1.5V supply to the ADC | –0.3 to 1.65 | V |
| $T_{STG}$[1] | Storage temperature | –65 to +150 | °C |
| $T_J$[1] | Junction temperature | 125 | °C |

**Notes:**

1. For flash programming and retention maximum limits, refer to Table 3-4. For recommended operating conditions, refer to Table 3-3.
2. The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 3-5.

**Table 3-2.** Analog Maximum Ratings

| Parameter | Conditions | Min. | Max. | Units |
|---|---|---|---|---|
| ABPS[n] pad voltage (relative to ground) | GDEC[1:0] = 00 (±15.36V range) | | | |
| | Absolute maximum | –11.5 | 14.4 | V |
| | Recommended | –11 | 14 | V |
| | GDEC[1:0] = 01 (±10.24V range) | –11.5 | 12 | V |
| | GDEC[1:0] = 10 (±5.12V range) | –6 | 6 | V |
| | GDEC[1:0] = 11 (±2.56V range) | –3 | 3 | V |
| CM[n] pad voltage relative to ground) | CMB_DI_ON = 0 (ADC isolated)<br>COMP_EN = 0 (comparator off, for the associated even-numbered comparator) | | | |
| | Absolute maximum | –0.3 | 14.4 | V |
| | Recommended | –0.3 | 14 | V |
| | CMB_DI_ON = 0 (ADC isolated)<br>COMP_EN = 1 (comparator on) | –0.3 | 3 | V |
| | TMB_DI_ON = 1 (direct ADC in) | –0.3 | 3 | V |
| TM[n] pad voltage (relative to ground) | TMB_DI_ON = 0 (ADC isolated)<br>COMP_EN = 1(comparator on) | –0.3 | 3 | V |
| | TMB_DI_ON = 1 (direct ADC in) | –0.3 | 3 | V |
| ADC[n] pad voltage (relative to ground) | — | –0.3 | 3.6 | V |

**Table 3-3.** Recommended Operating Conditions[5, 6]

| Symbol | Parameter [1] | | Commercial | Industrial | Units |
|---|---|---|---|---|---|
| $T_J$ | Junction temperature | | 0 to +85 | –40 to +100 | °C |
| VCC [2] | 1.5V DC core supply voltage | | 1.425 to 1.575 | 1.425 to 1.575 | V |
| VJTAG | JTAG DC voltage | | 1.425 to 3.6 | 1.425 to 3.6 | V |
| VPP | Programming voltage | Programming mode [3] | 3.15 to 3.45 | 3.15 to 3.45 | V |
| | | Operation[4] | 0 to 3.6 | 0 to 3.6 | V |
| VCCPLLx | Analog power supply (PLL) | | 1.425 to 1.575 | 1.425 to 1.575 | V |
| VCCFPGAIOBx/ VCCMSSIOBx[5] | 1.5V DC supply voltage | | 1.425 to 1.575 | 1.425 to 1.575 | V |
| | 1.8V DC supply voltage | | 1.7 to 1.9 | 1.7 to 1.9 | V |
| | 2.5V DC supply voltage | | 2.3 to 2.7 | 2.3 to 2.7 | V |
| | 3.3V DC supply voltage | | 3.0 to 3.6 | 3.0 to 3.6 | V |
| | LVDS differential I/O | | 2.375 to 2.625 | 2.375 to 2.625 | V |
| | LVPECL differential I/O | | 3.0 to 3.6 | 3.0 to 3.6 | V |
| VCC33A[6] | Analog clean 3.3V supply to the analog circuitry | | 3.15 to 3.45 | 3.15 to 3.45 | V |
| VCC33ADCx[6] | Analog 3.3V supply to ADC | | 3.15 to 3.45 | 3.15 to 3.45 | V |
| VCC33AP[6] | Analog clean 3.3V supply to the charge pump | | 3.15 to 3.45 | 3.15 to 3.45 | V |
| VCC33SDDx[6] | Analog 3.3V supply to sigma-delta DAC | | 3.15 to 3.45 | 3.15 to 3.45 | V |
| VAREFx | Voltage reference for ADC | | 2.527 to 3.3 | 2.527 to 3.3 | V |
| VCCRCOSC | Analog supply to the integrated RC oscillator | | 3.15 to 3.45 | 3.15 to 3.45 | V |
| VDDBAT | External battery supply | | 2.7 to 3.63 | 2.7 to 3.63 | V |
| VCCMAINXTAL[6] | Analog supply to the main crystal oscillator | | 3.15 to 3.45 | 3.15 to 3.45 | V |
| VCCLPXTAL[6] | Analog supply to the low power 32 KHz crystal oscillator | | 3.15 to 3.45 | 3.15 to 3.45 | V |
| VCCENVM | Embedded nonvolatile memory supply | | 1.425 to 1.575 | 1.425 to 1.575 | V |
| VCCESRAM | Embedded SRAM supply | | 1.425 to 1.575 | 1.425 to 1.575 | V |
| VCC15A[2] | Analog 1.5V supply to the analog circuitry | | 1.425 to 1.575 | 1.425 to 1.575 | V |

| .....continued | | | | |
|---|---|---|---|---|
| Symbol | Parameter [1] | Commercial | Industrial | Units |
| VCC15ADCx[2] | Analog 1.5V supply to the ADC | 1.425 to 1.575 | 1.425 to 1.575 | V |

**Notes:**

1. All parameters representing voltages are measured with respect to GND unless otherwise specified.
2. The following 1.5V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.
3. The Programming temperature range supported is $T_{ambient}$ = 0 °C to 85 °C.
4. VPP can be left floating during operation (not programming mode).
5. The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 5-1. VCCxxxxIOBx should be at the same voltage within a given I/O bank.
6. The following 3.3V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.

**Table 3-4.** FPGA and Embedded Flash Programming, Storage and Operating Limits

| Product Grade | Storage Temperature | Element | Grade Programming Cycles | Retention |
|---|---|---|---|---|
| Commercial | Min. $T_J$ = 0 °C | FPGA/FlashROM | 500 | 20 years |
| | Max. $T_J$ = 85 °C | Embedded Flash | < 1,000 | 20 years |
| | | | < 10,000 | 10 years |
| | | | < 15,000 | 5 years |
| Industrial | Min. $T_J$ = –40 °C | FPGA/FlashROM | 500 | 20 years |
| | Max. $T_J$ = 100 °C | Embedded Flash | < 1,000 | 20 years |
| | | | < 10,000 | 10 years |
| | | | < 15,000 | 5 years |

**Table 3-5.** Overshoot and Undershoot Limits [1]

| VCCxxxxIOBx | Average VCCxxxxIOBx–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2] | Maximum Overshoot/ Undershoot[2] |
|---|---|---|
| 2.7V or less | 10% | 1.4V |
| | 5% | 1.49V |
| 3V | 10% | 1.1V |
| | 5% | 1.19V |
| 3.3V | 10% | 0.79V |
| | 5% | 0.88V |
| 3.6V | 10% | 0.45V |
| | 5% | 0.54 V |

**Notes:**

1. Based on reliability requirements at 85 °C.
2. The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15V.
3. This table does not provide PCI overshoot/undershoot limits.

## 3.2 Power Supply Sequencing Requirement (Ask a Question)

SmartFusion cSoCs have an on-chip 1.5V regulator, but usage of an external 1.5V supply is also allowed while the on-chip regulator is disabled. In that case, the 3.3V supplies (VCC33A, etc.) should be powered before 1.5V (VCC, etc.) supplies. The 1.5V supplies should be enabled only after 3.3V supplies reach a value higher than 2.7V.

## 3.3 I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial) (Ask a Question)

Sophisticated power-up management circuitry is designed into every SmartFusion cSoC. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 3-1.

There are five regions to consider during power-up.

SmartFusion I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCxxxxIOBx are above the minimum specified trip points (Figure 3-1).
2. VCCxxxxIOBx > VCC – 0.75V (typical)
3. Chip is in the SoC Mode.

**VCCxxxxIOBx Trip Point:**

- Ramping up: 0.6V < trip_point_up < 1.2V
- Ramping down: 0.5V < trip_point_down < 1.1V

**VCC Trip Point:**

- Ramping up: 0.6V < trip_point_up < 1.1V
- Ramping down: 0.5V < trip_point_down < 1V

VCC and VCCxxxxIOBx ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- By default, during programming I/Os become tristated and weakly pulled up to VCCxxxxIOBx. You can modify the I/O states during programming in FlashPro. For more details, refer to 2.4. Specifying I/O States During Programming.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

**PLL Behavior at Brownout Condition**

The Microchip Group recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLLx exceed brownout activation levels. The VCC activation level is specified as 1.1V worst-case (see Figure 3-1 for more details).

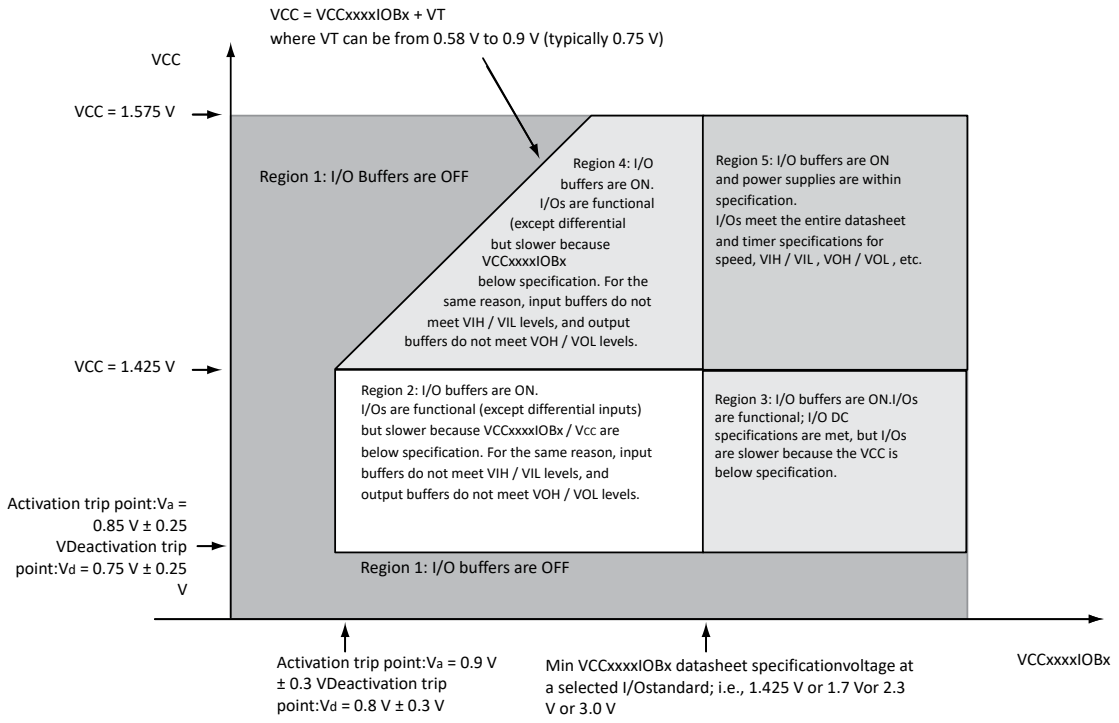
When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels (0.75V ± 0.25V), the PLL output lock signal goes low and/or the output clock is lost. Refer to the “Power-Up/-Down Behavior of Low Power Flash Devices” chapter of the ProASIC3 FPGA Fabric User’s Guide for information on clock and lock recovery.

**Internal Power-Up Activation Sequence**

1. Core
2. Input buffers

Output buffers, after 200 ns delay from input buffer activation

**Figure 3-1.** I/O State as a Function of VCCxxxxIOBx and VCC Voltage Levels




## 3.4 Thermal Characteristics (Ask a Question)

### Introduction

The temperature variable in the SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures. The following equations give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - \theta_A}{P} \qquad EQ\ 1$$

$$\theta_{JB} = \frac{T_J - T_B}{P} \qquad EQ\ 2$$

$$\theta_{JC} = \frac{T_J - T_C}{P} \qquad EQ\ 3$$

where

$\theta_{JA}$ = Junction-to-air thermal resistance

$\theta_{JB}$ = Junction-to-board thermal resistance

$\theta_{JC}$ = Junction-to-case thermal resistance

$T_J$ = Junction temperature

$T_A$ = Ambient temperature

$T_B$ = Board temperature (measured 1.0 mm away from the package edge)

$T_C$ = Case temperature

P = Total power dissipated by the device

**Table 3-6.** Package Thermal Resistance

| Product | $\theta_{JA}$ | | | $\theta_{JC}$ | $\theta_{JB}$ | Units |
|---|---|---|---|---|---|---|
| | Still Air | 1.0 m/s | 2.5 m/s | | | |
| A2F200M3F-FG256 | 33.7 | 30.0 | 28.3 | 9.3 | 24.8 | °C/W |
| A2F200M3F-FG484 | 21.8 | 18.2 | 16.7 | 7.7 | 16.8 | °C/W |
| A2F200M3F-CS288 | 26.6 | 20.2 | 18.1 | 7.3 | 9.4 | °C/W |
| A2F200M3F-PQG208I | 38.5 | 34.6 | 33.1 | 0.7 | 31.6 | °C/W |

### Theta-JA

Junction-to-ambient thermal resistance ($\theta_{JA}$) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation showing the maximum power dissipation allowed for the A2F200-FG484 package under forced convection of 1.0 m/s and 75 °C ambient temperature is as follows:

$$\text{Maximum Power Allowed} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

*EQ 4*

where

$\theta_{JA}$ = 19.00 °C/W (taken from Table 3-6).

$T_A$ = 75.00 °C

$$\text{Maximum Power Allowed} = \frac{100.00°C - 75.00°C}{19.00°C/W} = 1.3\ W$$

*EQ 5*

The power consumption of a device can be calculated using the Microchip's power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package. If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

### Theta-JB

Junction-to-board thermal resistance ($\theta_{JB}$) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

### Theta-JC

Junction-to-case thermal resistance ($\theta_{JC}$) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used

with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition. This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

**Calculation for Heat Sink**

For example, in a design implemented in an A2F200-FG484 package with 2.5 m/s airflow, the power consumption value using the power calculator is 3.00W. The user-dependent $T_a$ and $T_j$ are given as follows:

$T_J$ = 100.00 °C

$T_A$ = 70.00 °C

From the datasheet:

$\theta_{JA}$ = 17.00 °C/W

$\theta_{JC}$ = 8.28 °C/W

$$P = \frac{T_J - T_A}{\theta_{JA}} = \frac{100°C - 70°C}{17.00\ W} = 1.76\ W$$

*EQ 6*

The 1.76W power is less than the required 3.00W. The design therefore requires a heat sink, or the airflow where the device is mounted should be increased. The design's total junction-to-air thermal resistance requirement can be estimated by the following equation.

$$\theta_{JA(total)} = \frac{T_J - T_A}{P} = \frac{100°C - 70°C}{3.00\ W} = 10.00°C/W$$

*EQ 7*

Determining the heat sink's thermal performance proceeds as follows:

$$\theta_{JA(TOTAL)} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

*EQ 8*

where

$\theta_{JA}$ = 0.37 °C/W

= Thermal resistance of the interface material between the case and the heat sink, usually provided by the thermal interface manufacturer

$\theta_{SA}$ = Thermal resistance of the heat sink in °C/W

$$\theta_{SA} = \theta_{JA(TOTAL)} - \theta_{JC} - \theta_{CS}$$

*EQ 9*

$$\theta_{SA} = 13.33°C/W - 8.28°C/W - 0.37°C/W = 5.01°C/W$$

A heat sink with a thermal resistance of 5.01 °C/W or better should be used. Thermal resistance of heat sinks is a function of airflow. The heat sink performance can be significantly improved with increased airflow.

Carefully estimating thermal resistance is important in the long-term reliability of an FPGA. Design engineers should always correlate the power consumption of the device with the maximum allowable power dissipation of the package selected for that device.

**Note:**
The junction-to-air and junction-to-board thermal resistances are based on JEDEC standard (JESD-51) and assumptions made in building the model. It may not be realized in actual application and therefore should be used with a degree of caution. Junction-to-case thermal resistance assumes that all power is dissipated through the case.

### Temperature and Voltage Derating Factors

**Table 3-7.** Temperature and Voltage Derating Factors for Timing Delays (Normalized to $T_J$ = 85 °C, Worst-Case VCC = 1.425V)

| Array Voltage VCC (V) | Junction Temperature (°C) | | | | | |
|---|---|---|---|---|---|---|
| | –40 °C | 0 °C | 25 °C | 70 °C | 85 °C | 100 °C |
| 1.425 | 0.86 | 0.91 | 0.93 | 0.98 | 1.00 | 1.02 |
| 1.500 | 0.81 | 0.86 | 0.88 | 0.93 | 0.95 | 0.96 |
| 1.575 | 0.78 | 0.83 | 0.85 | 0.90 | 0.91 | 0.93 |

# 4. Calculating Power Dissipation (Ask a Question)

## 4.1 Quiescent Supply Current (Ask a Question)

**Table 4-1.** Power Supplies Configuration

| Modes and Power Supplies | VCCxxxxIOBx VCCFPGAIOBx VCCMSSIOBx | VCC33A / VCC33ADCx VCC33AP / VCC33SDDx VCCMAINXTAL / VCCLPXTAL | VCC / VCC15A / VCC15ADCx VCCPLLx, VCCENVM, VCCESRAM | VDDBAT | VCCRCOSC | VJTAG | VPP | eNVM (reset/off) | LPXTAL (enable/disable) | MAINXTAL (enable/disable) |
|---|---|---|---|---|---|---|---|---|---|---|
| Time Keeping mode | 0V | 0V | 0V | 3.3V | 0V | 0V | 0V | OFF | Enable | Disable |
| Standby mode | ON[1] | 3.3V | 1.5V | N/A | 3.3V | N/A | N/A | Reset | Enable | Disable |
| SoC mode | ON[1] | 3.3V | 1.5V | N/A | 3.3V | N/A | N/A | ON | Enable | Enable |

**Note:**

1. ON means proper voltage is applied. Refer to Table 3-3 for recommended operating conditions.

**Table 4-2.** Quiescent Supply Current Characteristics

| Parameter | Modes | A2F060[1] | | A2F200 | | A2F500 | |
|---|---|---|---|---|---|---|---|
| | | 1.5V Domain | 3.3V Domain | 1.5V Domain | 3.3V Domain | 1.5V Domain | 3.3V Domain |
| IDC1 | SoC mode | 3 mA | 2 mA | 7 mA | 4 mA | 16.5 mA | 4 mA |
| IDC2 | Standby mode | 3 mA | 2 mA | 7 mA | 4 mA | 16.5 mA | 4 mA |
| IDC3 | Time Keeping mode | N/A | 10 µA | N/A | 10 µA | N/A | 10 µA |

**Note:**

1. Part No A2F060 is discontinued.

## 4.2 Power per I/O Pin (Ask a Question)

**Table 4-3.** Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

| | VCCFPGAIOBx (V) | Static Power PDC7 (mW) | Dynamic Power PAC9 (µW/MHz) |
|---|---|---|---|
| **Single-Ended** | | | |
| 3.3V LVTTL / 3.3V LVCMOS | 3.3 | — | 17.55 |
| 2.5V LVCMOS | 2.5 | — | 5.97 |
| 1.8V LVCMOS | 1.8 | — | 2.88 |
| 1.5V LVCMOS (JESD8-11) | 1.5 | — | 2.33 |
| 3.3V PCI | 3.3 | — | 19.21 |
| 3.3V PCI-X | 3.3 | — | 19.21 |
| **Differential** | | | |
| LVDS | 2.5 | 2.26 | 0.82 |
| LVPECL | 3.3 | 5.72 | 1.16 |

**Table 4-4.** Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings – Applicable to MSS I/O Banks

| | VCCMSSIOBx (V) | Static Power PDC7 (mW) | Dynamic Power PAC9 (µW/MHz) |
|---|---|---|---|
| **Single-Ended** | | | |
| 3.3V LVTTL / 3.3V LVCMOS | 3.3 | — | 17.21 |
| 3.3V LVCMOS / 3.3V LVCMOS – Schmitt trigger | 3.3 | — | 20.00 |
| 2.5V LVCMOS | 2.5 | — | 5.55 |
| 2.5V LVCMOS – Schmitt trigger | 2.5 | — | 7.03 |
| 1.8V LVCMOS | 1.8 | — | 2.61 |
| 1.8V LVCMOS – Schmitt trigger | 1.8 | — | 2.72 |
| 1.5V LVCMOS (JESD8-11) | 1.5 | — | 1.98 |
| 1.5V LVCMOS (JESD8-11) – Schmitt trigger | 1.5 | — | 1.93 |

**Table 4-5.** Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1] Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

| | $C_{LOAD}$ (pF) | VCCFPGAIOBx (V) | Static Power **PDC8 (mW)** | Dynamic Power **PAC10 (µW/MHz)** |
|---|---|---|---|---|
| **Single-Ended** | | | | |
| 3.3V LVTTL / 3.3 V LVCMOS | 35 | 3.3 | — | 475.66 |
| 2.5V LVCMOS | 35 | 2.5 | — | 270.50 |
| 1.8V LVCMOS | 35 | 1.8 | — | 152.17 |
| 1.5V LVCMOS (JESD8-11) | 35 | 1.5 | — | 104.44 |
| 3.3V PCI | 10 | 3.3 | — | 202.69 |
| 3.3V PCI-X | 10 | 3.3 | — | 202.69 |
| **Differential** | | | | |
| LVDS | — | 2.5 | 7.74 | 88.26 |
| LVPECL | — | 3.3 | 19.54 | 164.99 |

**Note:**

1. Dynamic power consumption is given for standard load and software default drive strength and output slew.

**Table 4-6.** Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings– Applicable to MSS I/O Banks

| | $C_{LOAD}$ (pF) | VCCMSSIOBx (V) | Static Power **PDC8 (mW)**[2] | Dynamic Power **PAC10 (µW/MHz)**[3] |
|---|---|---|---|---|
| **Single-Ended** | | | | |
| 3.3V LVTTL / 3.3V LVCMOS | 10 | 3.3 | — | 155.65 |
| 2.5V LVCMOS | 10 | 2.5 | — | 88.23 |
| 1.8V LVCMOS | 10 | 1.8 | — | 45.03 |
| 1.5V LVCMOS (JESD8-11) | 10 | 1.5 | — | 31.01 |

## 4.3 Power Consumption of Various Internal Resources (Ask a Question)

**Table 4-7.** Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs

| Parameter | Definition | Power Supply | | Device | | | Units |
|---|---|---|---|---|---|---|---|
| | | Name | Domain | A2F060 [1] | A2F200 | A2F500 | |
| PAC1 | Clock contribution of a Global Rib | VCC | 1.5V | 3.39 | 3.40 | 5.05 | µW/MHz |
| PAC2 | Clock contribution of a Global Spine | VCC | 1.5V | 1.14 | 1.83 | 2.50 | µW/MHz |
| PAC3 | Clock contribution of a VersaTile row | VCC | 1.5V | 1.15 | 1.15 | 1.15 | µW/MHz |
| PAC4 | Clock contribution of a VersaTile used as a sequential module | VCC | 1.5V | 0.12 | 0.12 | 0.12 | µW/MHz |
| PAC5 | First contribution of a VersaTile used as a sequential module | VCC | 1.5V | 0.07 | 0.07 | 0.07 | µW/MHz |
| PAC6 | Second contribution of a VersaTile used as a sequential module | VCC | 1.5V | 0.29 | 0.29 | 0.29 | µW/MHz |
| PAC7 | Contribution of a VersaTile used as a combinatorial module | VCC | 1.5V | 0.29 | 0.29 | 0.29 | µW/MHz |
| PAC8 | Average contribution of a routing net | VCC | 1.5V | 1.04 | 0.79 | 0.79 | µW/MHz |
| PAC9 | Contribution of an I/O input pin (standard dependent) | VCCxxxxIOBx/ VCC | See Table 4-3 and Table 4-4 | | | | |
| PAC10 | Contribution of an I/O output pin (standard dependent) | VCCxxxxIOBx/ VCC | See Table 4-5 and Table 4-6 | | | | |
| PAC11 | Average contribution of a RAM block during a read operation | VCC | 1.5V | 25.00 | | | µW/MHz |

**.....continued**

| Parameter | Definition | Power Supply | | Device | | | Units |
|---|---|---|---|---|---|---|---|
| | | Name | Domain | A2F060 [1] | A2F200 | A2F500 | |
| PAC12 | Average contribution of a RAM block during a write operation | VCC | 1.5V | 30.00 | | | µW/MHz |
| PAC13 | Dynamic Contribution for PLL | VCC | 1.5V | 2.60 | | | µW/MHz |
| PAC15 | Contribution of NVM block during a read operation (F < 33 MHz) | VCC | 1.5V | 358.00 | | | µW/MHz |
| PAC16 | 1st contribution of NVM block during a read operation (F > 33 MHz) | VCC | 1.5V | 12.88 | | | mW |
| PAC17 | 2nd contribution of NVM block during a read operation (F > 33 MHz) | VCC | 1.5V | 4.80 | | | µW/MHz |
| PAC18 | Main Crystal Oscillator contribution | VCCMAINXTAL | 3.3V | 1.98 | | | mW |
| PAC19a | RC Oscillator contribution | VCCRCOSC | 3.3V | 3.30 | | | mW |
| PAC19b | RC Oscillator contribution | VCC | 1.5V | 3.00 | | | mW |
| PAC20a | Analog Block Dynamic Power Contribution of the ADC | VCC33ADCx | 3.3V | 8.25 | | | mW |
| PAC20b | Analog Block Dynamic Power Contribution of the ADC | VCC15ADCx | 1.5V | 3.00 | | | mW |
| PAC21 | Low Power Crystal Oscillator contribution | VCCLPXTAL | 3.3V | 33.00 | | | µW |
| PAC22 | MSS Dynamic Power Contribution – Running Drysthone at 100 MHz[2] | VCC | 1.5V | 67.50 | | | mW |
| PAC23 | Temperature Monitor Power Contribution | See Table 15-2 | — | 1.23 | | | mW |

| .....continued | | | | | | | |
|---|---|---|---|---|---|---|---|
| Parameter | Definition | Power Supply | | Device | | | Units |
| | | Name | Domain | A2F060 [1] | A2F200 | A2F500 | |
| PAC24 | Current Monitor Power Contribution | See Table 15-1 | — | 1.03 | | | mW |
| PAC25 | ABPS Power Contribution | See Table 15-4 | — | 0.70 | | | mW |
| PAC26 | Sigma-Delta DAC Power Contribution[3] | See Table 15-6 | — | 0.58 | | | mW |
| PAC27 | Comparator Power Contribution | See Table 15-5 | — | 1.02 | | | mW |
| PAC28 | Voltage Regulator Power Contribution[4] | See Table 15-7 | — | 36.30 | | | mW |

**Notes:**

1. Part No A2F060 is discontinued.
2. For a different use of MSS peripherals and resources, refer to SmartPower.
3. Assumes Input = Half Scale Operation mode.
4. Assumes 100 mA load on 1.5V domain.

**Table 4-8.** Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs

| Parameter | Definition | Power Supply | | Device | | | Units |
|---|---|---|---|---|---|---|---|
| | | Name | Domain | A2F060 [1] | A2F200 | A2F200 | |
| PDC1 | Core static power contribution in SoC mode | VCC | 1.5V | 11.10 | 23.70 | 37.95 | mW |
| PDC2 | Device static power contribution in Standby Mode | See Table 4-1 | — | 11.10 | 23.70 | 37.95 | mW |
| PDC3 | Device static power contribution in Time Keeping mode | See Table 4-1 | 3.3V | 33.00 | 33.00 | 33.00 | µW |
| PDC7 | Static contribution per input pin (standard dependent contribution) | VCCxxxxIOBx/VCC | See Table 4-3 and Table 4-4 . | | | | |
| PDC8 | Static contribution per output pin (standard dependent contribution) | VCCxxxxIOBx/VCC | See Table 4-5 and Table 4-6. | | | | |
| PDC9 | Static contribution per PLL | VCC | 1.5V | 2.55 | 2.55 | 2.55 | mW |

**Note:**

1. Part No A2F060 is discontinued.

**Table 4-9.** eNVM Dynamic Power Consumption

| Parameter | Description | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| eNVM System | eNVM array operating power | Idle | — | 795 | — | µA |
| | | Read operation | See Table 4-7. | | | |
| | | Erase | — | 900 | — | µA |
| | | Write | — | 900 | — | µA |
| PNVMCTRL | eNVM controller operating power | — | — | 20 | — | µW/MHz |

## 4.4 Power Calculation Methodology (Ask a Question)

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in the Libero SoC software. The power calculation methodology described below uses the following variables:

- The number of PLLs/CCCs as well as the number and the frequency of each output clock generated.
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- The number of eNVM blocks used in the design
- The analog block used in the design, including the temperature monitor, current monitor, ABPS, sigma-delta DAC, comparator, low power crystal oscillator, RC oscillator and the main crystal oscillator
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 4-10
- Enable rates of output buffers—guidelines are provided for typical applications in Table 4-11
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 4-11
- Read rate to the eNVM blocks

The calculation should be repeated for each clock domain defined in the design.

### Methodology

#### Total Power Consumption—$P_{TOTAL}$

#### SoC Mode, Standby Mode, and Time Keeping Mode

$P_{TOTAL} = P_{STAT} + P_{DYN}$

$P_{STAT}$ is the total static power consumption.

$P_{DYN}$ is the total dynamic power consumption.

#### Total Static Power Consumption—$P_{STAT}$

#### SoC Mode

$P_{STAT} = P_{DC1} + (N_{INPUTS} * P_{DC7}) + (N_{OUTPUTS} * P_{DC8}) + (N_{PLLS} * P_{DC9})$

$N_{INPUTS}$ is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

$N_{PLLS}$ is the number of PLLs available in the device.

#### Standby Mode

$P_{STAT} = P_{DC2}$

#### Time Keeping Mode

$P_{STAT} = P_{DC3}$

#### Total Dynamic Power Consumption—$P_{DYN}$

#### SoC Mode

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL} + P_{eNVM} + P_{XTL\text{-}OSC} + P_{RC\text{-}OSC} + P_{AB} + P_{LPXTAL\text{-}OSC} + P_{MSS}$

#### Standby Mode

$P_{DYN} = P_{RC-OSC} + P_{LPXTAL-OSC}$

**Time Keeping Mode**

$P_{DYN} = P_{LPXTAL-OSC}$

**Global Clock Dynamic Contribution—$P_{CLOCK}$**

**SoC Mode**

$P_{CLOCK} = (P_{AC1} + N_{SPINE} * P_{AC2} + N_{ROW} * P_{AC3} + N_{S-CELL} * P_{AC4}) * F_{CLK}$

$N_{SPINE}$ is the number of global spines used in the user design—guidelines are provided in the "Device Architecture" chapter of the SmartFusion FPGA Fabric User's Guide.

$N_{ROW}$ is the number of VersaTile rows used in the design—guidelines are provided in the "Device Architecture" chapter of the SmartFusion FPGA Fabric User's Guide.

$F_{CLK}$ is the global clock signal frequency.

$N_{S-CELL}$ is the number of VersaTiles used as sequential modules in the design.

**Standby Mode and Time Keeping Mode**

$P_{CLOCK} = 0W$

**Sequential Cells Dynamic Contribution—$P_{S-CELL}$**

**SoC Mode**

$P_{S-CELL} = N_{S-CELL} * (P_{AC5} + (\alpha_1 / 2) * P_{AC6}) * F_{CLK}$

$N_{S-CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

$\alpha_1$ is the toggle rate of VersaTile outputs—guidelines are provided in Table 4-10.

$F_{CLK}$ is the global clock signal frequency.

**Standby Mode and Time Keeping Mode**

$P_{S-CELL} = 0W$

**Combinatorial Cells Dynamic Contribution—$P_{C-CELL}$**

**SoC Mode**

$P_{C-CELL} = N_{C-CELL} * (\alpha_1 / 2) * P_{AC7} * F_{CLK}$

$N_{C-CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

$\alpha_1$ is the toggle rate of VersaTile outputs—guidelines are provided in Table 4-10.

$F_{CLK}$ is the global clock signal frequency.

**Standby Mode and Time Keeping Mode**

$P_{C-CELL} = 0W$

**Routing Net Dynamic Contribution—$P_{NET}$**

**SoC Mode**

$P_{NET} = (N_{S-CELL} + N_{C-CELL}) * (\alpha_1 / 2) * P_{AC8} * F_{CLK}$

$N_{S-CELL}$ is the number VersaTiles used as sequential modules in the design.

$N_{C-CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

$\alpha_1$ is the toggle rate of VersaTile outputs—guidelines are provided in Table 4-10.

$F_{CLK}$ is the frequency of the clock driving the logic including these nets.

**Standby Mode and Time Keeping Mode**

$P_{NET}$ = 0W

**I/O Input Buffer Dynamic Contribution—$P_{INPUTS}$**

**SoC Mode**

$P_{INPUTS} = N_{INPUTS} * (\alpha_2 / 2) * P_{AC9} * F_{CLK}$

Where:

$N_{INPUTS}$ is the number of I/O input buffers used in the design.

$\alpha_2$ is the I/O buffer toggle rate—guidelines are provided in Table 4-10.

$F_{CLK}$ is the global clock signal frequency.

**Standby Mode and Time Keeping Mode**

$P_{INPUTS}$ = 0W

**I/O Output Buffer Dynamic Contribution—$P_{OUTPUTS}$**

**SoC Mode**

$P_{OUTPUTS} = N_{OUTPUTS} * (\alpha_2 / 2) * \beta_1 * P_{AC10} * F_{CLK}$

Where:

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

$\alpha_2$ is the I/O buffer toggle rate—guidelines are provided in Table 4-10.

β1 is the I/O buffer enable rate—guidelines are provided in Table 4-11.

$F_{CLK}$ is the global clock signal frequency.

**Standby Mode and Time Keeping Mode**

$P_{OUTPUTS}$ = 0W

FPGA Fabric SRAM Dynamic Contribution—$P_{MEMORY}$

**SoC Mode**

$P_{MEMORY} = (N_{BLOCKS} * P_{AC11} * \beta_2 * F_{READ\text{-}CLOCK}) + (N_{BLOCKS} * P_{AC12} * \beta_3 * F_{WRITE\text{-}CLOCK})$

Where:

$N_{BLOCKS}$ is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

$\beta_2$ is the RAM enable rate for read operations—guidelines are provided in Table 4-11.

$\beta_3$ the RAM enable rate for write operations—guidelines are provided in Table 4-11.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

**Standby Mode and Time Keeping Mode**

$P_{MEMORY}$ = 0W

**PLL/CCC Dynamic Contribution—$P_{PLL}$**

**SoC Mode**

$P_{PLL} = P_{AC13} * F_{CLKOUT}$

$F_{CLKIN}$ is the input clock frequency.

$F_{CLKOUT}$ is the output clock frequency.[1]

**Note:**

1. The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula output clock by adding its corresponding contribution ($P_{AC14}$ * $F_{CLKOUT}$ product) to the total PLL contribution.

**Standby Mode and Time Keeping Mode**

$P_{PLL}$ = 0W

**Embedded Nonvolatile Memory Dynamic Contribution—$P_{eNVM}$**

**SoC Mode**

The eNVM dynamic power consumption is a piecewise linear function of frequency.

$P_{eNVM} = N_{eNVM\text{-}BLOCKS} * \beta_4 * P_{AC15} * F_{READ\text{-}eNVM}$ when $F_{READ\text{-}eNVM} \leq 33$ MHz,

$P_{eNVM} = N_{eNVM\text{-}BLOCKS} * \beta_4 * (P_{AC16} + P_{AC17} * F_{READ\text{-}eNVM})$ when $F_{READ\text{-}eNVM} > 33$ MHz

Where:

$N_{eNVM\text{-}BLOCKS}$ is the number of eNVM blocks used in the design.

$\beta_4$ is the eNVM enable rate for read operations. Default is 0 (eNVM mainly in idle state).

$F_{READ\text{-}eNVM}$ is the eNVM read clock frequency.

**Standby Mode and Time Keeping Mode**

$P_{eNVM}$ = 0W

**Main Crystal Oscillator Dynamic Contribution—$P_{XTL\text{-}OSC}$**

**SoC Mode**

$P_{XTL\text{-}OSC} = P_{AC18}$

**Standby Mode**

$P_{XTL\text{-}OSC}$ = 0W

**Time Keeping Mode**

$P_{XTL\text{-}OSC}$ = 0W

**Low Power Oscillator Crystal Dynamic Contribution—$P_{LPXTAL\text{-}OSC}$**

**Operating, Standby, and Time Keeping Mode**

$P_{LPXTAL\text{-}OSC} = P_{AC21}$

**RC Oscillator Dynamic Contribution—$P_{RC\text{-}OSC}$**

**SoC Mode**

$P_{RC\text{-}OSC} = P_{AC19A} + P_{AC19B}$

**Standby Mode and Time Keeping Mode**

$P_{RC\text{-}OSC}$ = 0W

**Analog System Dynamic Contribution—$P_{AB}$**

**SoC Mode**

$P_{AB} = P_{AC23} * N_{TM} + P_{AC24} * N_{CM} + P_{AC25} * N_{ABPS} + P_{AC26} * N_{SDD} + P_{AC27} * N_{COMP} + P_{ADC} * N_{ADC} + P_{VR}$

Where:

$N_{CM}$ is the number of current monitor blocks

$N_{TM}$ is the number of temperature monitor blocks

$N_{SDD}$ is the number of sigma-delta DAC blocks

$N_{ABPS}$ is the number of ABPS blocks

$N_{ADC}$ is the number of ADC blocks

$N_{COMP}$ is the number of comparator blocks

$P_{VR} = P_{AC28}$

$P_{ADC} = P_{AC20A} + P_{AC20B}$

### Microcontroller Subsystem Dynamic Contribution—$P_{MSS}$

#### SoC Mode

$P_{MSS} = P_{AC22}$

## Guidelines

### Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that the net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100%, as all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  Bit 0 (LSB) = 100%
  Bit 1 = 50%
  Bit 2 = 25%
  ...
  Bit 7 (MSB) = 0.78125%
  Average toggle rate = (100% + 50% + 25% + 12.5% + . . . 0.78125%) / 8.

### Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When non-tristate output buffers are used, the enable rate should be 100%.

**Table 4-10.** Toggle Rate Guidelines Recommended for Power Calculation

| Component | Definition | Guideline |
|---|---|---|
| $\alpha_1$ | Toggle rate of VersaTile outputs | 10% |
| $\alpha_2$ | I/O buffer toggle rate | 10% |

**Table 4-11.** Enable Rate Guidelines Recommended for Power Calculation

| Component | Definition | Guideline |
|---|---|---|
| $\beta_1$ | I/O output buffer enable rate | Toggle rate of the logic driving the output buffer |
| $\beta_2$ | FPGA fabric SRAM enable rate for read operations | 12.5% |
| β3 | FPGA fabric SRAM enable rate for write operations | 12.5% |
| $\beta_4$ | eNVM enable rate for read operations | < 5% |

# 5. User I/O Characteristics (Ask a Question)

## 5.1 Timing Model (Ask a Question)

**Figure 5-1.** Timing Model Operating Conditions: –1 Speed, Commercial Temperature Range ($T_J$ = 85 °C), Worst Case VCC = 1.425V

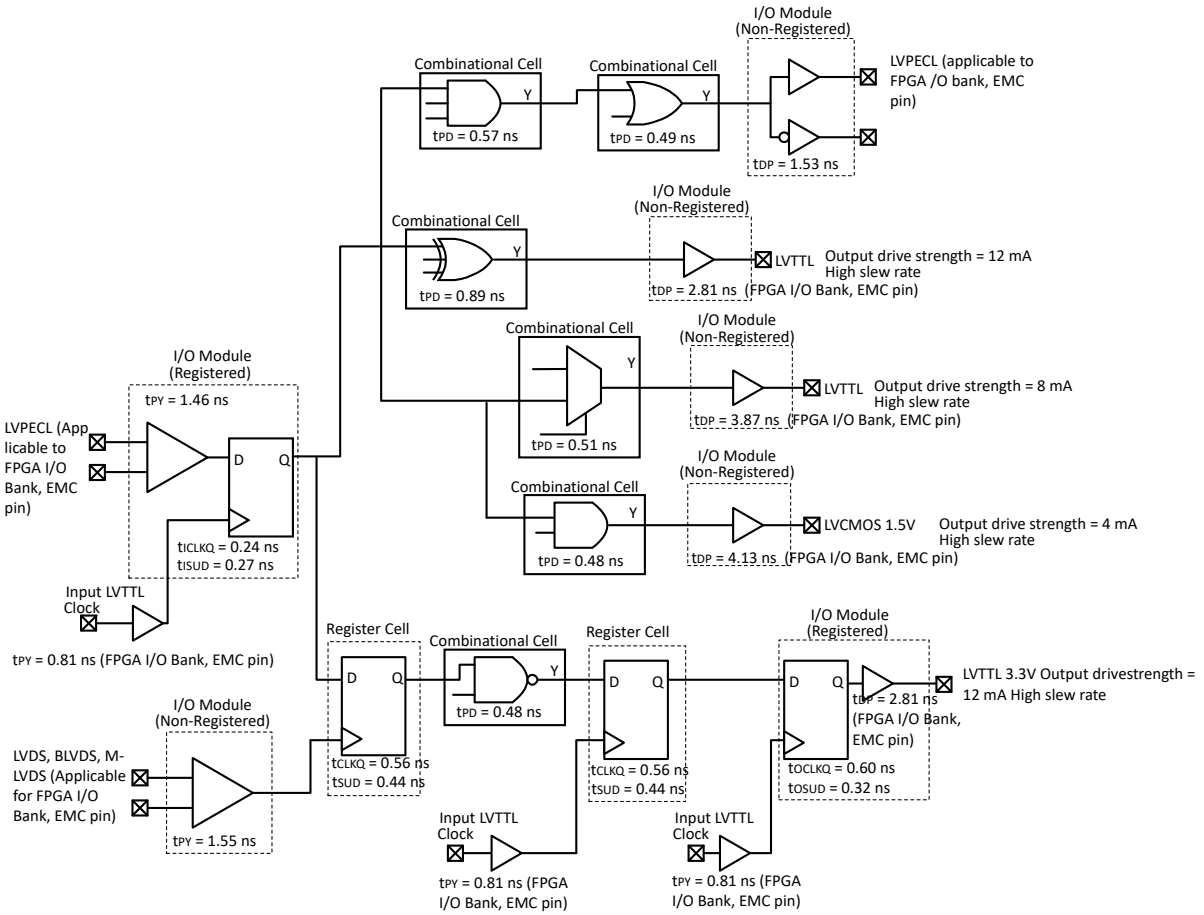
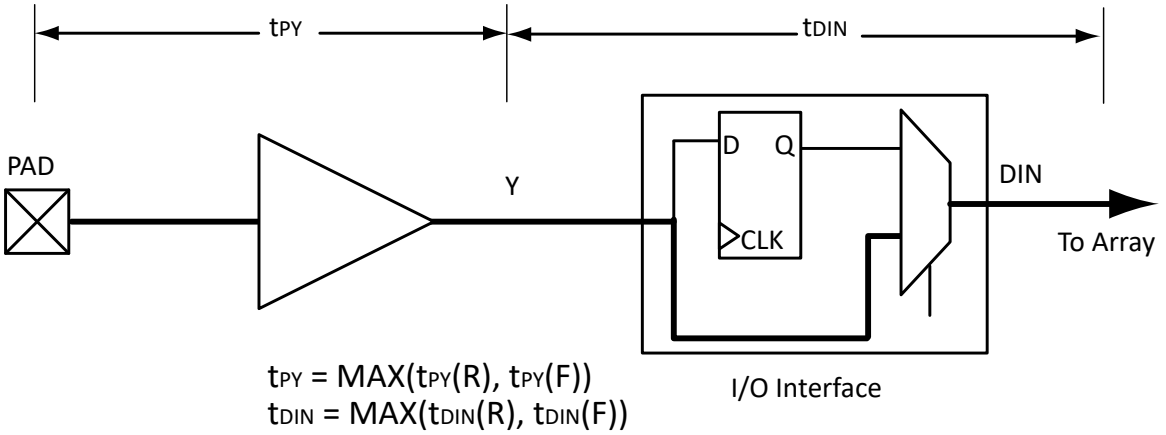


**Figure 5-2.** Input Buffer Timing Model and Delays (Example)



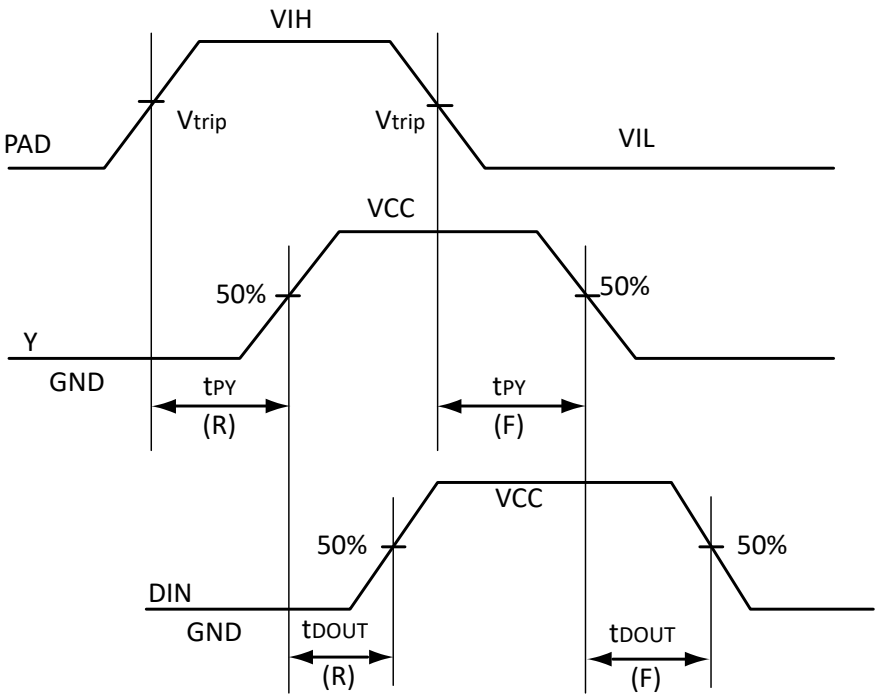



**Figure 5-3.** Output Buffer Model and Delays (Example)

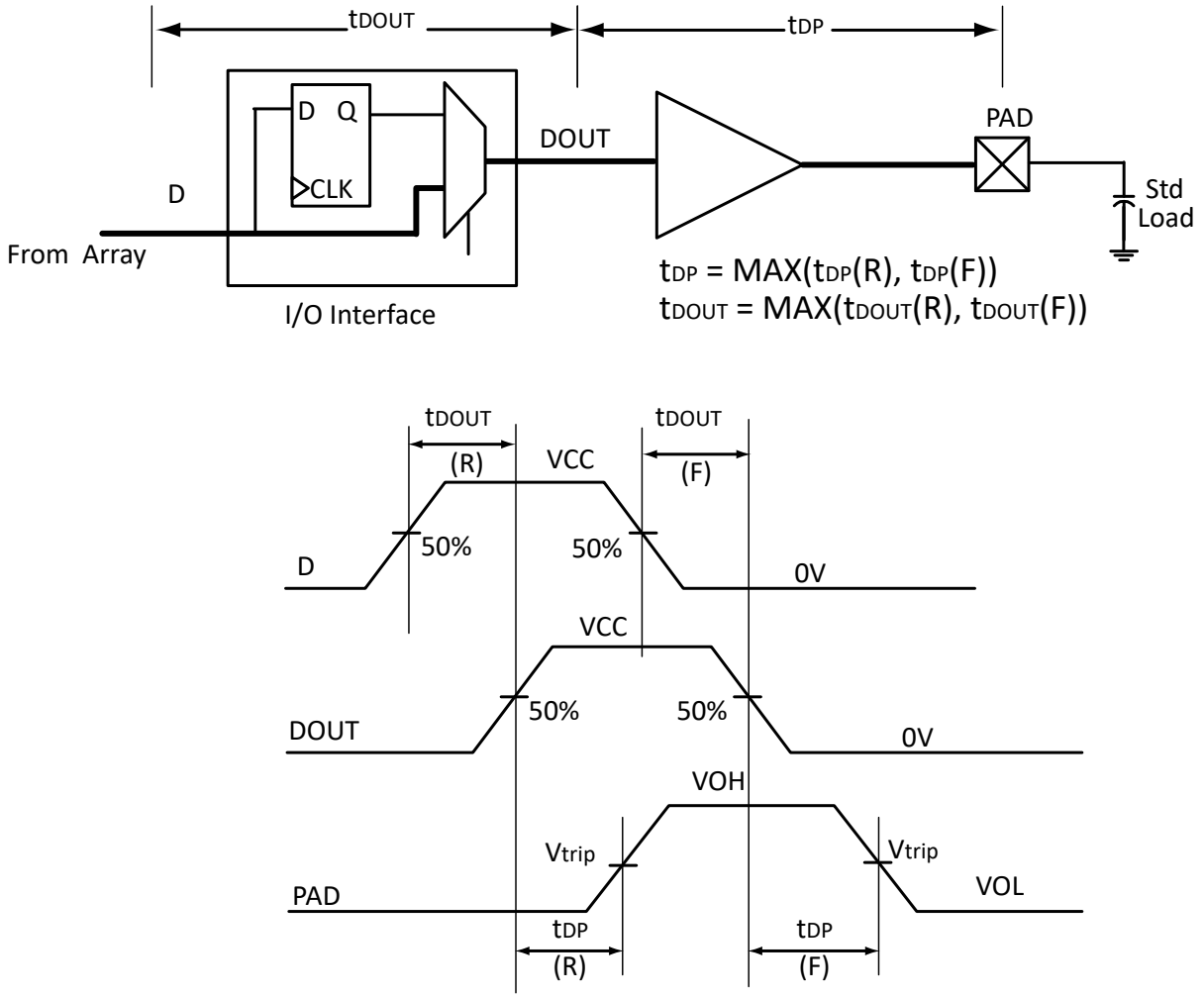
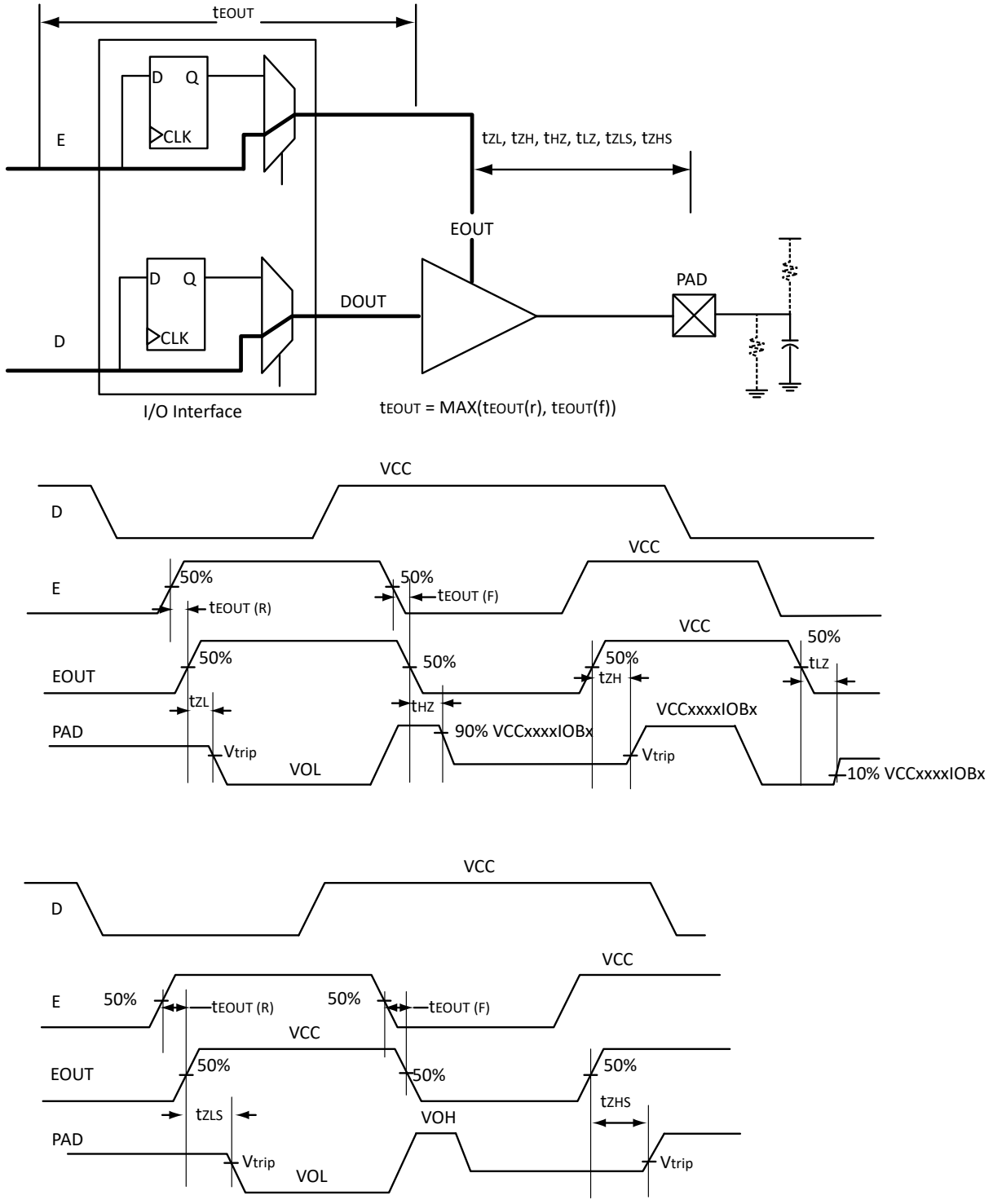


**Figure 5-4.** Tristate Output Buffer Timing Model and Delays (Example)



## 5.2 Overview of I/O Performance (Ask a Question)

### Summary of I/O DC Input and Output Levels – Default I/O Software Settings

**Table 5-1.** Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial Conditions —Software Default Settings Applicable to FPGA I/O Banks

| I/O Standard | Drive Strgth. | Slew Rate | VIL | | VIH | | VOL | VOH | $I_{OL}$[1] | $I_{OH}$[1] |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA |
| 3.3V LVTTL / 3.3V LVCMOS | 12 mA | High | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 12 | 12 |
| 2.5V LVCMOS | 12 mA | High | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 12 | 12 |
| 1.8V LVCMOS | 12 mA | High | –0.3 | 0.35 * VCCxxxxIOBx | 0.65 * VCCxxxxIOBx | 3.6 | 0.45 | VCCxxxxIOBx – 0.45 | 12 | 12 |
| 1.5V LVCMOS | 12 mA | High | –0.3 | 0.35 * VCCxxxxIOBx | 0.65 * VCCxxxxIOBx | 3.6 | 0.25 * VCCxxxxIOBx | 0.75 * VCCxxxxIOBx | 12 | 12 |
| 3.3V PCI | Per PCI specifications | | | | | | | | | |
| 3.3V PCI-X | Per PCI-X specifications | | | | | | | | | |

**Notes:**

1. Currents are measured at 85 °C junction temperature.
2. Output slew rate can be extracted by the IBIS Models.

**Table 5-2.** Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial Conditions —Software Default Settings Applicable to MSS I/O Banks

| I/O Standard | Drive Strgth. | Slew Rate | VIL | | VIH | | VOL | VOH | $I_{OL}$[1] | $I_{OH}$[1] |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA |
| 3.3V LVTTL / 3.3V LVCMOS | 8 mA | High | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 8 | 8 |
| 2.5V LVCMOS | 8 mA | High | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 8 | 8 |
| 1.8V LVCMOS | 4 mA | High | –0.3 | 0.35 * VCCxxxxIOBx | 0.65 * VCCxxxxIOBx | 3.6 | 0.45 | VCCxxxxIOBx – 0.45 | 4 | 4 |
| 1.5V LVCMOS | 2 mA | High | –0.3 | 0.35 * VCCxxxxIOBx | 0.65 * VCCxxxxIOBx | 3.6 | 0.25 * VCCxxxxIOBx | 0.75 * VCCxxxxIOBx | 2 | 2 |

**Notes:**

1. Currents are measured at 85 °C junction temperature.
2. Output slew rate can be extracted by the IBIS Models.

**Table 5-3.** Summary of Maximum and Minimum DC Input Levels Applicable to Commercial Conditions in all I/O Bank Types

| DC I/O Standards | Commercial | |
|---|---|---|
| | $I_{IL}$ | $I_{IH}$ |
| | µA | µA |
| 3.3V LVTTL / 3.3V LVCMOS | 15 | 15 |
| 2.5V LVCMOS | 15 | 15 |
| 1.8V LVCMOS | 15 | 15 |
| 1.5V LVCMOS | 15 | 15 |
| 3.3V PCI | 15 | 15 |

| .....continued | | |
|---|---|---|
| DC I/O Standards | Commercial | |
| | $I_{IL}$ | $I_{IH}$ |
| | µA | µA |
| 3.3V PCI-X | 15 | 15 |

## Summary of I/O Timing Characteristics – Default I/O Software Settings

**Table 5-4.** Summary of AC Measuring Points Applicable to All I/O Bank Types

| Standard | Measuring Trip Point ($V_{trip}$) |
|---|---|
| 3.3V LVTTL / 3.3V LVCMOS | 1.4V |
| 2.5V LVCMOS | 1.2V |
| 1.8V LVCMOS | 0.90V |
| 1.5V LVCMOS | 0.75V |
| 3.3V PCI | 0.285 * VCCxxxxIOBx (RR) |
| | 0.615 * VCCxxxxIOBx (FF) |
| 3.3V PCI-X | 0.285 * VCCxxxxIOBx (RR) |
| | 0.615 * VCCxxxxIOBx (FF) |
| LVDS | Cross point |
| LVPECL | Cross point |

**Table 5-5.** I/O AC Parameter Definitions

| Parameter | Parameter Definition |
|---|---|
| $t_{DP}$ | Data to pad delay through the output buffer |
| $t_{PY}$ | Pad to data delay through the input buffer |
| $t_{DOUT}$ | Data to output buffer delay through the I/O interface |
| $t_{EOUT}$ | Enable to output buffer tristate control delay through the I/O interface |
| $t_{DIN}$ | Input buffer to data delay through the I/O interface |
| $t_{HZ}$ | Enable to pad delay through the output buffer—High to Z |
| $t_{ZH}$ | Enable to pad delay through the output buffer—Z to High |
| $t_{LZ}$ | Enable to pad delay through the output buffer—Low to Z |
| $t_{ZL}$ | Enable to pad delay through the output buffer—Z to Low |
| $t_{ZHS}$ | Enable to pad delay through the output buffer with delayed enable—Z to High |
| $t_{ZLS}$ | Enable to pad delay through the output buffer with delayed enable—Z to Low |

**Table 5-6.** Summary of I/O Timing Characteristics—Software Default Settings –1 Speed Grade, Worst Commercial-Case Conditions: $T_J$ = 85 °C, Worst Case VCC = 1.425V, Worst-Case VCCxxxxIOBx (per standard) Applicable to FPGA I/O Banks, Assigned to EMC I/O Pins

| I/O Standard | Drive Strength | Slew Rate | Capacitive Load (pF) | External Resistor (Ω) | $t_{DOUT}$ (ns) | $t_{DP}$ (ns) | $t_{DIN}$ (ns) | $t_{PY}$ (ns) | $t_{EOUT}$ (ns) | $t_{ZL}$ (ns) | $t_{ZH}$ (ns) | $t_{LZ}$ (ns) | $t_{HZ}$ (ns) | $t_{ZLS}$ (ns) | $t_{ZHS}$ (ns) | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3.3V LVTTL / 3.3V LVCMOS | 12 mA | High | 35 | — | 0.50 | 2.81 | 0.03 | 0.81 | 0.32 | 2.86 | 2.23 | 2.55 | 2.82 | 4.58 | 3.94 | ns |
| 2.5V LVCMOS | 12 mA | High | 35 | — | 0.50 | 2.73 | 0.03 | 1.03 | 0.32 | 2.88 | 2.69 | 2.62 | 2.70 | 4.60 | 4.41 | ns |
| 1.8V LVCMOS | 12 mA | High | 35 | — | 0.50 | 2.81 | 0.03 | 0.95 | 0.32 | 2.87 | 2.38 | 2.92 | 3.18 | 4.58 | 4.10 | ns |

| .....continued | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| I/O Standard | Drive Strength | Slew Rate | Capacitive Load (pF) | External Resistor (Ω) | $t_{DOUT}$ (ns) | $t_{DP}$ (ns) | $t_{DIN}$ (ns) | $t_{PY}$ (ns) | $t_{EOUT}$ (ns) | $t_{ZL}$ (ns) | $t_{ZH}$ (ns) | $t_{LZ}$ (ns) | $t_{HZ}$ (ns) | $t_{ZLS}$ (ns) | $t_{ZHS}$ (ns) | Units |
| 1.5V LVCMOS | 12 mA | High | 35 | — | 0.50 | 3.24 | 0.03 | 1.12 | 0.32 | 3.30 | 2.79 | 3.10 | 3.27 | 5.02 | 4.50 | ns |
| 3.3V PCI | Per PCI spec | High | 10 | 25[1] | 0.50 | 2.11 | 0.03 | 0.68 | 0.32 | 2.15 | 1.57 | 2.55 | 2.82 | 3.87 | 3.28 | ns |
| 3.3V PCI-X | Per PCI-X spec | High | 10 | 25[1] | 0.50 | 2.11 | 0.03 | 0.64 | 0.32 | 2.15 | 1.57 | 2.55 | 2.82 | 3.87 | 3.28 | ns |
| LVDS | 24 mA | High | — | — | 0.50 | 1.53 | 0.03 | 1.55 | — | — | — | — | — | — | — | ns |
| LVPECL | 24 mA | High | — | — | 0.50 | 1.46 | 0.03 | 1.46 | — | — | — | — | — | — | — | ns |

**Notes:**

1. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 5-9 for connectivity. This resistor is not required during normal operation.
2. For specific junction temperature and voltage supply levels, refer to Table 3-7 for derating values.

**Table 5-7.** Summary of I/O Timing Characteristics—Software Default Settings –1 Speed Grade, Worst Commercial-Case Conditions: $T_J$ = 85 °C, Worst Case VCC = 1.425V, Worst-Case VCCxxxxIOBx (per standard) Applicable to MSS I/O Banks

| I/O Standard | Drive Strength | Slew Rate | Capacitive Load (pF) | External Resistor | $t_{DOUT}$ (ns) | $t_{DP}$ (ns) | $t_{DIN}$ (ns) | $t_{PY}$ (ns) | $t_{PYS}$ (ns) | $t_{EOUT}$ (ns) | $t_{ZL}$ (ns) | $t_{ZH}$ (ns) | $t_{LZ}$ (ns) | $t_{HZ}$ (ns) | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3.3V LVTTL / 3.3V LVCMOS | 8 mA | High | 10 | — | 0.18 | 1.92 | 0.07 | 0.78 | 1.09 | 0.18 | 1.96 | 1.55 | 1.83 | 2.04 | ns |
| 2.5V LVCMOS | 8 mA | High | 10 | — | 0.18 | 1.96 | 0.07 | 0.99 | 1.16 | 0.18 | 2.00 | 1.82 | 1.82 | 1.93 | ns |
| 1.8V LVCMOS | 4 mA | High | 10 | — | 0.18 | 2.31 | 0.07 | 0.91 | 1.37 | 0.18 | 2.35 | 2.27 | 1.84 | 1.87 | ns |
| 1.5V LVCMOS | 2 mA | High | 10 | — | 0.18 | 2.70 | 0.07 | 1.07 | 1.55 | 0.18 | 2.75 | 2.67 | 1.87 | 1.85 | ns |

**Notes:**

1. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 5-9 for connectivity. This resistor is not required during normal operation.
2. For specific junction temperature and voltage supply levels, refer to Table 3-7 for derating values.

## 5.3 Detailed I/O DC Characteristics (Ask a Question)

**Table 5-8.** Input Capacitance

| Symbol | Definition | Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0, f = 1.0 MHz | — | 8 | pF |
| $C_{INCLK}$ | Input capacitance on the clock pin | $V_{IN}$ = 0, f = 1.0 MHz | — | 8 | pF |

**Table 5-9.** I/O Output Buffer Maximum Resistances [1] Applicable to FPGA I/O Banks

| Standard | Drive Strength | $R_{PULL\text{-}DOWN}$ (Ω)[2] | $R_{PULL\text{-}UP}$ (Ω)[3] |
|---|---|---|---|
| 3.3V LVTTL / 3.3V LVCMOS | 2 mA | 100 | 300 |
| | 4 mA | 100 | 300 |
| | 6 mA | 50 | 150 |
| | 8 mA | 50 | 150 |
| | 12 mA | 25 | 75 |
| | 16 mA | 17 | 50 |
| | 24 mA | 11 | 33 |
| 2.5V LVCMOS | 2 mA | 100 | 200 |
| | 4 mA | 100 | 200 |
| | 6 mA | 50 | 100 |
| | 8 mA | 50 | 100 |
| | 12 mA | 25 | 50 |
| | 16 mA | 20 | 40 |
| | 24 mA | 11 | 22 |
| 1.8V LVCMOS | 2 mA | 200 | 225 |
| | 4 mA | 100 | 112 |
| | 6 mA | 50 | 56 |
| | 8 mA | 50 | 56 |
| | 12 mA | 20 | 22 |
| | 16 mA | 20 | 22 |
| 1.5V LVCMOS | 2 mA | 200 | 224 |
| | 4 mA | 100 | 112 |
| | 6 mA | 67 | 75 |
| | 8 mA | 33 | 37 |
| | 12 mA | 33 | 37 |
| 3.3V PCI/PCI-X | Per PCI/PCI-X specification | 25 | 75 |

**Notes:**

1. These maximum values are provided for information only. Minimum output buffer resistance values depend on VCCxxxxIOBx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microchip website (also generated by the SoC Products Group Libero SoC toolset).
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R(_{PULL\text{-}UP\text{-}MAX}) = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$

**Table 5-10.** I/O Output Buffer Maximum Resistances[1] Applicable to MSS I/O Banks

| Standard | Drive Strength | $R_{PULL\text{-}DOWN}$ (Ω)[2] | $R_{PULL\text{-}UP}$ (Ω)[3] |
|---|---|---|---|
| 3.3V LVTTL/3.3V LVCMOS | 8 mA | 50 | 150 |
| 2.5V LVCMOS | 8 mA | 50 | 100 |
| 1.8V LVCMOS | 4 mA | 100 | 112 |
| 1.5V LVCMOS | 2 mA | 200 | 224 |

**Notes:**

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCxxxxIOBx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microchip website.
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$

**Table 5-11.** I/O Weak Pull-Up/Pull-Down Resistances—Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

| VCCxxxxIOBx | $R_{(WEAK\ PULL\text{-}UP)}$[1] (Ω) | | $R_{(WEAK\ PULL\text{-}DOWN)}$[2] (Ω) | |
|---|---|---|---|---|
| | Min. | Max. | Min. | Max. |
| 3.3V | 10k | 45k | 10k | 45k |
| 2.5V | 11k | 55k | 12k | 74k |
| 1.8V | 18k | 70k | 17k | 110k |
| 1.5V | 19k | 90k | 19k | 140k |

**Notes:**

1. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)} = (V_{CCImax} - V_{OHspec}) / I_{(WEAK\ PULL\text{-}UP\text{-}MIN)}$
2. $R_{(WEAK\ PULL\text{-}DOWN\text{-}MAX)} = (V_{OLspec}) / I_{(WEAK\ PULL\text{-}DOWN\text{-}MIN)}$

**Table 5-12.** I/O Short Currents $I_{OSH}/I_{OSL}$ Applicable to FPGA I/O Banks

| | Drive Strength | $I_{OSL}$ (mA)[1] | $I_{OSH}$ (mA)[1] |
|---|---|---|---|
| 3.3V LVTTL / 3.3V LVCMOS | 2 mA | 27 | 25 |
| | 4 mA | 27 | 25 |
| | 6 mA | 54 | 51 |
| | 8 mA | 54 | 51 |
| | 12 mA | 109 | 103 |
| | 16 mA | 127 | 132 |
| | 24 mA | 181 | 268 |
| 2.5V LVCMOS | 2 mA | 18 | 16 |
| | 4 mA | 18 | 16 |
| | 6 mA | 37 | 32 |
| | 8 mA | 37 | 32 |
| | 12 mA | 74 | 65 |
| | 16 mA | 87 | 83 |
| | 24 mA | 124 | 169 |
| 1.8V LVCMOS | 2 mA | 11 | 9 |
| | 4 mA | 22 | 17 |
| | 6 mA | 44 | 35 |
| | 8 mA | 51 | 45 |
| | 12 mA | 74 | 91 |
| | 16 mA | 74 | 91 |

| .....continued | | | |
|---|---|---|---|
| | Drive Strength | $I_{OSL}$ (mA)[1] | $I_{OSH}$ (mA)[1] |
| 1.5V LVCMOS | 2 mA | 16 | 13 |
| | 4 mA | 33 | 25 |
| | 6 mA | 39 | 32 |
| | 8 mA | 55 | 66 |
| | 12 mA | 55 | 66 |
| 3.3V PCI/PCI-X | Per PCI/PCI-X specification | 109 | 103 |

**Note:**

1. $T_J$ = 85 °C.

**Table 5-13.** I/O Short Currents $I_{OSH}/I_{OSL}$ Applicable to MSS I/O Banks

| | Drive Strength | $I_{OSL}$ (mA)[1] | $I_{OSH}$ (mA)[1] |
|---|---|---|---|
| 3.3V LVTTL / 3.3V LVCMOS | 8 mA | 54 | 51 |
| 2.5V LVCMOS | 8 mA | 37 | 32 |
| 1.8V LVCMOS | 4 mA | 22 | 17 |
| 1.5V LVCMOS | 2 mA | 16 | 13 |

**Note:**

1. $T_J$ = 85 °C

The length of time an I/O can withstand $I_{OSH}/I_{OSL}$ events depends on the junction temperature. The reliability data below is based on a 3.3V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100 °C, the short current condition would have to be sustained for more than 2200 operation hours to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

**Table 5-14.** Duration of Short Circuit Event before Failure

| Temperature | Time before Failure |
|---|---|
| –40 °C | > 20 years |
| 0 °C | > 20 years |
| 25 °C | > 20 years |
| 70 °C | 5 years |
| 85 °C | 2 years |
| 100 °C | 6 months |

**Table 5-15.** Schmitt Trigger Input Hysteresis— Hysteresis Voltage Value (typical) for Schmitt Mode Input Buffers

| Input Buffer Configuration | Hysteresis Value (typical) |
|---|---|
| 3.3V LVTTL / LVCMOS / PCI / PCI-X (Schmitt trigger mode) | 240 mV |
| 2.5V LVCMOS (Schmitt trigger mode) | 140 mV |
| 1.8V LVCMOS (Schmitt trigger mode) | 80 mV |
| 1.5V LVCMOS (Schmitt trigger mode) | 60 mV |

**Table 5-16.** I/O Input Rise Time, Fall Time, and Related I/O Reliability

| Input Buffer | Input Rise/Fall Time (min.) | Input Rise/Fall Time (max.) | Reliability |
|---|---|---|---|
| LVTTL/LVCMOS | No requirement | 10 ns 1 | 20 years (100 °C) |
| LVDS/B-LVDS/ M-LVDS/LVPECL | No requirement | 10 ns 1 | 10 years (100 °C) |

**Note:**

1. The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microchip recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals. See www.microchip.com/en-us/products/fpgas-and-plds/system-on-chip-fpgas/smartfusion-fpgas#ibis.

## 5.4 Single-Ended I/O Characteristics (Ask a Question)

### 3.3V LVTTL/3.3V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTL) is a general-purpose standard (EIA/JESD) for 3.3V applications. It uses an LVTTL input buffer and push-pull output buffer.

**Table 5-17.** Minimum and Maximum DC Input and Output Levels Applicable to FPGA I/O Banks

| 3.3V LVTTL / 3.3V LVCMOS | VIL | | VIH | | VOL | VOH | $I_{OL}$ | $I_{OH}$ | $I_{OSL}$ | $I_{OSH}$ | $I_{IL}$ | $I_{IH}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[1] | Max. mA[1] | µA[2] | µA[2] |
| 2 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 2 | 2 | 27 | 25 | 15 | 15 |
| 4 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 4 | 4 | 27 | 25 | 15 | 15 |
| 6 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 6 | 6 | 54 | 51 | 15 | 15 |
| 8 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 8 | 8 | 54 | 51 | 15 | 15 |
| 12 mA[3] | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 12 | 12 | 109 | 103 | 15 | 15 |
| 16 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 16 | 16 | 127 | 132 | 15 | 15 |
| 24 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 24 | 24 | 181 | 268 | 10 | 10 |

**Notes:**

1. Currents are measured at 100 °C junction temperature and maximum voltage.
2. Currents are measured at 85 °C junction temperature.
3. Denotes the software default selection. This note is applicable for the entire row.

**Table 5-18.** Minimum and Maximum DC Input and Output Levels Applicable to MSS I/O Banks

| 3.3V LVTTL / 3.3V LVCMOS | VIL | | VIH | | VOL | VOH | $I_{OL}$ | $I_{OH}$ | $I_{OSL}$ | $I_{OSH}$ | $I_{IL}$ | $I_{IH}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[1] | Max. mA[1] | µA[2] | µA[2] |
| 8 mA[3] | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 8 | 8 | 54 | 51 | 15 | 15 |

**Notes:**

1. Currents are measured at 100 °C junction temperature and maximum voltage.
2. Currents are measured at 85 °C junction temperature.
3. Denotes the software default selection. This note is applicable for the entire row.

**Figure 5-5.** AC Loading

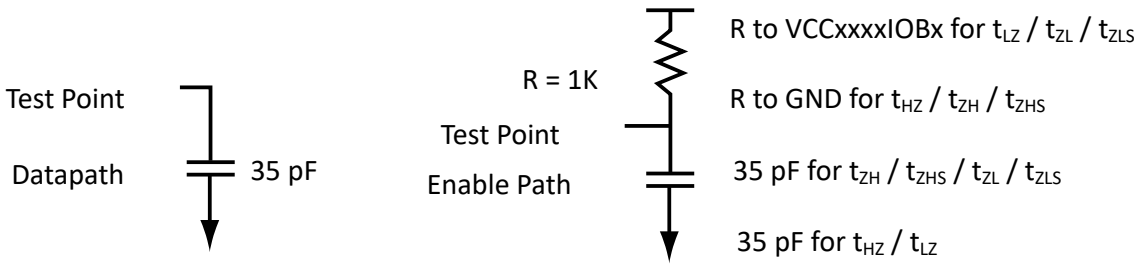



**Table 5-19.** AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|
| 0 | 3.3 | 1.4 | — | 35 |

**Note:** *Measuring point = $V_{trip}$. See Table 5-4 for a complete table of trip points.

## Timing Characteristics

**Table 5-20.** 3.3V LVTTL/3.3V LVCMOS High Slew Worst Commercial-Case Conditions: $T_J$ = 85 °C, Worst-Case VCC = 1.425V, Worst-Case VCCxxxxIOBx = 3.0V—Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 mA | Std. | 0.60 | 7.20 | 0.04 | 0.97 | 0.39 | 7.34 | 6.18 | 2.52 | 2.46 | 9.39 | 8.23 | ns |
| | –1 | 0.50 | 6.00 | 0.03 | 0.81 | 0.32 | 6.11 | 5.15 | 2.10 | 2.05 | 7.83 | 6.86 | ns |
| 8 mA | Std. | 0.60 | 4.64 | 0.04 | 0.97 | 0.39 | 4.73 | 3.84 | 2.85 | 3.02 | 6.79 | 5.90 | ns |
| | –1 | 0.50 | 3.87 | 0.03 | 0.81 | 0.32 | 3.94 | 3.20 | 2.37 | 2.52 | 5.65 | 4.91 | ns |
| 12 mA[1] | Std. | 0.60 | 3.37 | 0.04 | 0.97 | 0.39 | 3.43 | 2.67 | 3.07 | 3.39 | 5.49 | 4.73 | ns |
| | –1 | 0.50 | 2.81 | 0.03 | 0.81 | 0.32 | 2.86 | 2.23 | 2.55 | 2.82 | 4.58 | 3.94 | ns |
| 16 mA | Std. | 0.60 | 3.18 | 0.04 | 0.97 | 0.39 | 3.24 | 2.43 | 3.11 | 3.48 | 5.30 | 4.49 | ns |
| | –1 | 0.50 | 2.65 | 0.03 | 0.81 | 0.32 | 2.70 | 2.03 | 2.59 | 2.90 | 4.42 | 3.74 | ns |
| 24 mA | Std. | 0.60 | 2.93 | 0.04 | 0.97 | 0.39 | 2.99 | 2.03 | 3.17 | 3.83 | 5.05 | 4.09 | ns |
| | –1 | 0.50 | 2.45 | 0.03 | 0.81 | 0.32 | 2.49 | 1.69 | 2.64 | 3.19 | 4.21 | 3.41 | ns |

**Notes:**

1. Denotes the software default selection. This note is applicable for the entire row.
2. For specific junction temperature and voltage supply levels, refer to Table 3-7 for derating values.

**Table 5-21.** 3.3V LVTTL/3.3V LVCMOS Low Slew Worst Commercial-Case Conditions: $T_J$ = 85 °C, Worst-Case VCC = 1.425V, Worst-Case VCCxxxxIOBx = 3.0V—Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 mA | Std. | 0.60 | 9.75 | 0.04 | 0.97 | 0.39 | 9.93 | 8.22 | 2.52 | 2.31 | 11.99 | 10.28 | ns |
| | –1 | 0.50 | 8.12 | 0.03 | 0.81 | 0.32 | 8.27 | 6.85 | 2.10 | 1.93 | 9.99 | 8.57 | ns |
| 8 mA | Std. | 0.60 | 6.96 | 0.04 | 0.97 | 0.39 | 7.09 | 5.85 | 2.84 | 2.87 | 9.15 | 7.91 | ns |
| | –1 | 0.50 | 5.80 | 0.03 | 0.81 | 0.32 | 5.91 | 4.88 | 2.37 | 2.39 | 7.62 | 6.59 | ns |
| 12 mA | Std. | 0.60 | 5.35 | 0.04 | 0.97 | 0.39 | 5.45 | 4.58 | 3.06 | 3.23 | 7.51 | 6.64 | ns |
| | –1 | 0.50 | 4.46 | 0.03 | 0.81 | 0.32 | 4.54 | 3.82 | 2.55 | 2.69 | 6.26 | 5.53 | ns |
| 16 mA | Std. | 0.60 | 5.01 | 0.04 | 0.97 | 0.39 | 5.10 | 4.30 | 3.11 | 3.32 | 7.16 | 6.36 | ns |
| | –1 | 0.50 | 4.17 | 0.03 | 0.81 | 0.32 | 4.25 | 3.58 | 2.59 | 2.77 | 5.97 | 5.30 | ns |

| .....continued | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
| 24 mA | Std. | 0.60 | 4.67 | 0.04 | 0.97 | 0.39 | 4.75 | 4.28 | 3.16 | 3.66 | 6.81 | 6.34 | ns |
| | –1 | 0.50 | 3.89 | 0.03 | 0.81 | 0.32 | 3.96 | 3.57 | 2.64 | 3.05 | 5.68 | 5.28 | ns |

**Note:**

1. For specific junction temperature and voltage supply levels, refer to Table 3-7 for derating values.

**Table 5-22.** 3.3V LVTTL/3.3V LVCMOS High Slew Worst Commercial-Case Conditions: $T_J$ = 85 °C, Worst-Case VCC = 1.425V, Worst-Case VCCxxxxIOBx = 3.0V—Applicable to MSS I/O Banks

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 8 mA[1] | Std. | 0.22 | 2.31 | 0.09 | 0.94 | 1.30 | 0.22 | 2.35 | 1.86 | 2.20 | 2.45 | ns |
| | –1 | 0.18 | 1.92 | 0.07 | 0.78 | 1.09 | 0.18 | 1.96 | 1.55 | 1.83 | 2.04 | ns |

**Notes:**

1. Denotes the software default selection. This note is applicable for the entire row.
2. For specific junction temperature and voltage supply levels, refer to Table 3-7 for derating values.

### 2.5V LVCMOS

Low-Voltage CMOS for 2.5V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5V applications.

**Table 5-23.** Minimum and Maximum DC Input and Output Levels Applicable to FPGA I/O Banks

| 2.5V LVCMOS | VIL | | VIH | | VOL | VOH | $I_{OL}$ | $I_{OH}$ | $I_{OSL}$ | $I_{OSH}$ | $I_{IL}$ | $I_{IH}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[1] | Max. mA[1] | µA[2] | µA[2] |
| 2 mA | –0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 2 | 2 | 18 | 16 | 15 | 15 |
| 4 mA | –0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 4 | 4 | 18 | 16 | 15 | 15 |
| 6 mA | –0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 6 | 6 | 37 | 32 | 15 | 15 |
| 8 mA | –0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 8 | 8 | 37 | 32 | 15 | 15 |
| 12 mA[3] | –0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 12 | 12 | 74 | 65 | 15 | 15 |
| 16 mA | –0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 16 | 16 | 87 | 83 | 15 | 15 |
| 24 mA | –0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 24 | 24 | 124 | 169 | 15 | 15 |

**Notes:**

1. Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.
2. Currents are measured at 85 °C junction temperature.
3. Denotes the software default selection. This note is applicable for the entire row.

**Table 5-24.** Minimum and Maximum DC Input and Output Levels Applicable to MSS I/O Banks

| 2.5V LVCMOS | VIL | | VIH | | VOL | VOH | $I_{OL}$ | $I_{OH}$ | $I_{OSL}$ | $I_{OSH}$ | $I_{IL}$ | $I_{IH}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[1] | Max., mA[1] | µA[2] | µA[2] |
| 8 mA[3] | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 8 | 8 | 37 | 32 | 15 | 15 |

**Notes:**

1. Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.
2. Currents are measured at 85 °C junction temperature.
3. Denotes the software default selection. This note is applicable for the entire row.

**Figure 5-6.** AC Loading

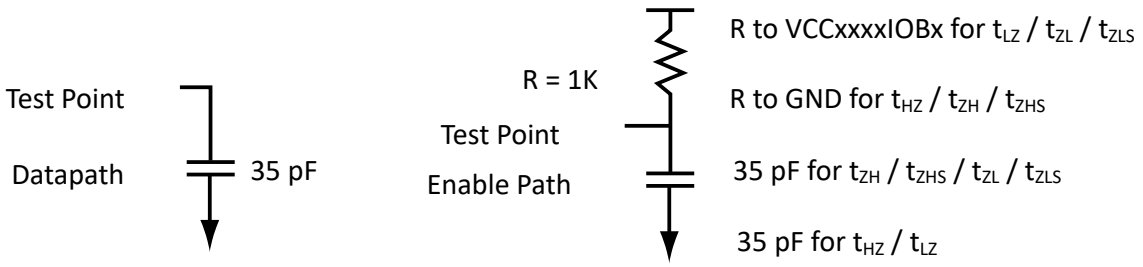



**Table 5-25.** AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|
| 0 | 2.5 | 1.2 | — | 35 |

**Note:** Measuring point = $V_{trip}$. See Table 5-4 for a complete table of trip points.

### Timing Characteristics

**Table 5-26.** 2.5V LVCMOS High Slew Worst Commercial-Case Conditions: $T_J$ = 85 °C, Worst-Case VCC = 1.425V, Worst-Case VCCxxxxIOBx = 2.3V—Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 mA | Std. | 0.55 | 8.10 | 0.04 | 1.23 | 0.39 | 7.37 | 8.10 | 2.54 | 2.17 | 9.43 | 10.15 | ns |
| | –1 | 0.46 | 6.75 | 0.03 | 1.03 | 0.32 | 6.14 | 6.75 | 2.12 | 1.81 | 7.85 | 8.46 | ns |
| 8 mA | Std. | 0.55 | 4.85 | 0.04 | 1.23 | 0.39 | 4.76 | 4.85 | 2.90 | 2.83 | 6.82 | 6.91 | ns |
| | –1 | 0.46 | 4.04 | 0.03 | 1.03 | 0.32 | 3.97 | 4.04 | 2.42 | 2.36 | 5.68 | 5.76 | ns |
| 12 mA[1] | Std. | 0.60 | 3.28 | 0.04 | 1.23 | 0.39 | 3.46 | 3.23 | 3.15 | 3.24 | 5.52 | 5.29 | ns |
| | –1 | 0.50 | 2.73 | 0.03 | 1.03 | 0.32 | 2.88 | 2.69 | 2.62 | 2.70 | 4.60 | 4.41 | ns |
| 16 mA | Std. | 0.60 | 3.09 | 0.04 | 1.23 | 0.39 | 3.27 | 2.88 | 3.20 | 3.35 | 5.33 | 4.94 | ns |
| | –1 | 0.50 | 2.57 | 0.03 | 1.03 | 0.32 | 2.72 | 2.40 | 2.67 | 2.79 | 4.44 | 4.12 | ns |
| 24 mA | Std. | 0.60 | 2.95 | 0.04 | 1.23 | 0.39 | 3.01 | 2.31 | 3.27 | 3.76 | 5.07 | 4.37 | ns |
| | –1 | 0.50 | 2.46 | 0.03 | 1.03 | 0.32 | 2.51 | 1.93 | 2.73 | 3.13 | 4.22 | 3.64 | ns |

**Notes:**

1. Denotes the software default selection. This note is applicable for the entire row.
2. For specific junction temperature and voltage supply levels, refer to Table 3-7 for derating values.

**Table 5-27.** 2.5V LVCMOS Low Slew Worst Commercial-Case Conditions: $T_J$ = 85 °C, Worst-Case VCC = 1.425V, Worst-Case VCCxxxxIOBx = 2.3V—Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 mA | Std. | 0.55 | 10.50 | 0.04 | 1.23 | 0.39 | 10.69 | 10.50 | 2.54 | 2.07 | 12.75 | 12.56 | ns |
| | –1 | 0.46 | 8.75 | 0.03 | 1.03 | 0.32 | 8.91 | 8.75 | 2.12 | 1.73 | 10.62 | 10.47 | ns |

| .....continued | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
| 8 mA | Std. | 0.55 | 7.61 | 0.04 | 1.23 | 0.39 | 7.46 | 7.19 | 2.81 | 2.66 | 9.52 | 9.25 | ns |
| | –1 | 0.46 | 6.34 | 0.03 | 1.03 | 0.32 | 6.22 | 5.99 | 2.34 | 2.22 | 7.93 | 7.71 | ns |
| 12 mA | Std. | 0.60 | 5.92 | 0.04 | 1.23 | 0.39 | 5.79 | 5.45 | 3.04 | 3.06 | 7.85 | 7.51 | ns |
| | –1 | 0.50 | 4.93 | 0.03 | 1.03 | 0.32 | 4.83 | 4.54 | 2.53 | 2.55 | 6.54 | 6.26 | ns |
| 16 mA | Std. | 0.60 | 5.53 | 0.04 | 1.23 | 0.39 | 5.40 | 5.09 | 3.09 | 3.16 | 7.46 | 7.14 | ns |
| | –1 | 0.50 | 4.61 | 0.03 | 1.03 | 0.32 | 4.50 | 4.24 | 2.58 | 2.64 | 6.22 | 5.95 | ns |
| 24 mA | Std. | 0.60 | 5.18 | 0.04 | 1.23 | 0.39 | 5.28 | 5.14 | 3.27 | 3.64 | 7.34 | 7.20 | ns |
| | –1 | 0.50 | 4.32 | 0.03 | 1.03 | 0.32 | 4.40 | 4.29 | 2.72 | 3.03 | 6.11 | 6.00 | ns |

**Note:**

1. For specific junction temperature and voltage supply levels, refer to Table 3-7 for derating values.

**Table 5-28.** 2.5V LVCMOS High Slew Worst Commercial-Case Conditions: $T_J$ = 85 °C, Worst-Case VCC = 1.425V Worst-Case VCCxxxxIOBx = 3.0V—Applicable to MSS I/O Banks

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 8 mA[1] | Std. | 0.22 | 2.35 | 0.09 | 1.18 | 1.39 | 0.22 | 2.40 | 2.18 | 2.19 | 2.32 | ns |
| | –1 | 0.18 | 1.96 | 0.07 | 0.99 | 1.16 | 0.18 | 2.00 | 1.82 | 1.82 | 1.93 | ns |

**Notes:**

1. Denotes the software default selection. This note is applicable for the entire row.
2. For specific junction temperature and voltage supply levels, refer to Table 3-7 for derating values.

### 1.8V LVCMOS

Low-voltage CMOS for 1.8V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8V applications. It uses a 1.8V input buffer and a push-pull output buffer.

**Table 5-29.** Minimum and Maximum DC Input and Output Levels—Applicable to FPGA I/O Banks

| 1.8V LVCMOS | VIL | | VIH | | VOL | VOH | $I_{OL}$ | $I_{OH}$ | $I_{OSL}$ | $I_{OSH}$ | $I_{IL}$ | $I_{IH}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[1] | Max. mA[1] | µA[2] | µA[2] |
| 2 mA | –0.3 | 0.35 * VCCxxxxIOBx | 0.65 * VCCxxxxIOBx | 1.9 | 0.45 | VCCxxxxIOBx – 0.45 | 2 | 2 | 11 | 9 | 15 | 15 |
| 4 mA | –0.3 | 0.35 * VCCxxxxIOBx | 0.65 * VCCxxxxIOBx | 1.9 | 0.45 | VCCxxxxIOBx – 0.45 | 4 | 4 | 22 | 17 | 15 | 15 |
| 6 mA | –0.3 | 0.35 * VCCxxxxIOBx | 0.65 * VCCxxxxIOBx | 1.9 | 0.45 | VCCxxxxIOBx – 0.45 | 6 | 6 | 44 | 35 | 15 | 15 |
| 8 mA | –0.3 | 0.35 * VCCxxxxIOBx | 0.65 * VCCxxxxIOBx | 1.9 | 0.45 | VCCxxxxIOBx – 0.45 | 8 | 8 | 51 | 45 | 15 | 15 |
| 12 mA [3] | –0.3 | 0.35 * VCCxxxxIOBx | 0.65 * VCCxxxxIOBx | 1.9 | 0.45 | VCCxxxxIOBx – 0.45 | 12 | 12 | 74 | 91 | 15 | 15 |
| 16 mA | –0.3 | 0.35 * VCCxxxxIOBx | 0.65 * VCCxxxxIOBx | 1.9 | 0.45 | VCCxxxxIOBx – 0.45 | 16 | 16 | 74 | 91 | 15 | 15 |

**Notes:**

1. Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.
2. Currents are measured at 85 °C junction temperature.
3. Denotes the software default selection. This note is applicable for the entire row.

**Table 5-30.** Minimum and Maximum DC Input and Output Levels—Applicable to MSS I/O Banks

| 1.8 V LVCMOS | VIL | | VIH | | VOL | VOH | $I_{OL}$ | $I_{OH}$ | $I_{OSL}$ | $I_{OSH}$ | $I_{IL}$ | $I_{IH}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[1] | Max. mA[1] | µA[2] | µA[2] |
| 4 mA [3] | –0.3 | 0.35 * VCCxxxxIOBx | 0.65 * VCCxxxxIOBx | 3.6 | 0.45 | VCCxxxxIOBx – 0.45 | 4 | 4 | 22 | 17 | 15 | 15 |

**Notes:**

1. Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.
2. Currents are measured at 85 °C junction temperature.
3. Denotes the software default selection. This note is applicable for the entire row.

**Figure 5-7.** AC Loading

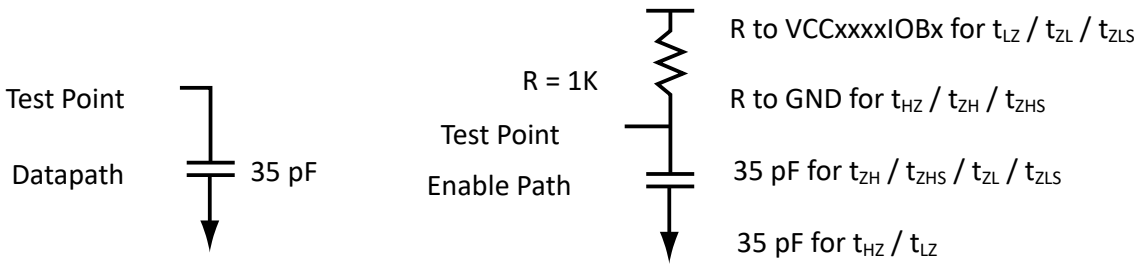



**Table 5-31.** AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|
| 0 | 1.8 | 0.9 | — | 35 |

**Note:**
*Measuring point = $V_{trip}$. See Table 5-4 for a complete table of trip points.

### Timing Characteristics

**Table 5-32.** 1.8V LVCMOS High Slew Worst Commercial-Case Conditions: $T_J$ = 85 °C, Worst-Case VCC = 1.425V,Worst-Case VCCxxxxIOBx = 1.7V—Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.60 | 11.06 | 0.04 | 1.14 | 0.39 | 8.61 | 11.06 | 2.61 | 1.59 | 10.67 | 13.12 | ns |
| | –1 | 0.50 | 9.22 | 0.03 | 0.95 | 0.32 | 7.17 | 9.22 | 2.18 | 1.33 | 8.89 | 10.93 | ns |
| 4 mA | Std. | 0.60 | 6.46 | 0.04 | 1.14 | 0.39 | 5.53 | 6.46 | 3.04 | 2.66 | 7.59 | 8.51 | ns |
| | –1 | 0.50 | 5.38 | 0.03 | 0.95 | 0.32 | 4.61 | 5.38 | 2.54 | 2.22 | 6.33 | 7.10 | ns |
| 6 mA | Std. | 0.60 | 4.16 | 0.04 | 1.14 | 0.39 | 3.99 | 4.16 | 3.34 | 3.18 | 6.05 | 6.22 | ns |
| | –1 | 0.50 | 3.47 | 0.03 | 0.95 | 0.32 | 3.32 | 3.47 | 2.78 | 2.65 | 5.04 | 5.18 | ns |

| .....continued | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
| 8 mA | Std. | 0.60 | 3.69 | 0.04 | 1.14 | 0.39 | 3.76 | 3.67 | 3.40 | 3.31 | 5.81 | 5.73 | ns |
| | –1 | 0.50 | 3.07 | 0.03 | 0.95 | 0.32 | 3.13 | 3.06 | 2.84 | 2.76 | 4.85 | 4.78 | ns |
| 12 mA [1] | Std. | 0.60 | 3.38 | 0.04 | 1.14 | 0.39 | 3.44 | 2.86 | 3.50 | 3.82 | 5.50 | 4.91 | ns |
| | –1 | 0.50 | 2.81 | 0.03 | 0.95 | 0.32 | 2.87 | 2.38 | 2.92 | 3.18 | 4.58 | 4.10 | ns |
| 16 mA | Std. | 0.60 | 3.38 | 0.04 | 1.14 | 0.39 | 3.44 | 2.86 | 3.50 | 3.82 | 5.50 | 4.91 | ns |
| | –1 | 0.50 | 2.81 | 0.03 | 0.95 | 0.32 | 2.87 | 2.38 | 2.92 | 3.18 | 4.58 | 4.10 | ns |

**Notes:**

1. Denotes the software default selection. This note is applicable for the entire row.
2. For specific junction temperature and voltage supply levels, refer to Table 3-7 for derating values.

**Table 5-33.** 1.8V LVCMOS Low Slew—Worst Commercial-Case Conditions: $T_J$ = 85 °C, Worst-Case VCC = 1.425V, Worst-Case VCCxxxxIOBx = 1.7V Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.60 | 14.24 | 0.04 | 1.14 | 0.39 | 13.47 | 14.24 | 2.62 | 1.54 | 15.53 | 16.30 | ns |
| | –1 | 0.50 | 11.87 | 0.03 | 0.95 | 0.32 | 11.23 | 11.87 | 2.18 | 1.28 | 12.94 | 13.59 | ns |
| 4 mA | Std. | 0.60 | 9.74 | 0.04 | 1.14 | 0.39 | 9.92 | 9.62 | 3.05 | 2.57 | 11.98 | 11.68 | ns |
| | –1 | 0.50 | 8.11 | 0.03 | 0.95 | 0.32 | 8.26 | 8.02 | 2.54 | 2.14 | 9.98 | 9.74 | ns |
| 6 mA | Std. | 0.60 | 7.67 | 0.04 | 1.14 | 0.39 | 7.81 | 7.24 | 3.34 | 3.08 | 9.87 | 9.30 | ns |
| | –1 | 0.50 | 6.39 | 0.03 | 0.95 | 0.32 | 6.51 | 6.03 | 2.79 | 2.56 | 8.23 | 7.75 | ns |
| 8 mA | Std. | 0.60 | 7.15 | 0.04 | 1.14 | 0.39 | 7.29 | 6.75 | 3.41 | 3.21 | 9.34 | 8.80 | ns |
| | –1 | 0.50 | 5.96 | 0.03 | 0.95 | 0.32 | 6.07 | 5.62 | 2.84 | 2.68 | 7.79 | 7.34 | ns |
| 12 mA | Std. | 0.60 | 6.76 | 0.04 | 1.14 | 0.39 | 6.89 | 6.75 | 3.50 | 3.70 | 8.95 | 8.81 | ns |
| | –1 | 0.50 | 5.64 | 0.03 | 0.95 | 0.32 | 5.74 | 5.62 | 2.92 | 3.08 | 7.46 | 7.34 | ns |
| 16 mA | Std. | 0.60 | 6.76 | 0.04 | 1.14 | 0.39 | 6.89 | 6.75 | 3.50 | 3.70 | 8.95 | 8.81 | ns |
| | –1 | 0.50 | 5.64 | 0.03 | 0.95 | 0.32 | 5.74 | 5.62 | 2.92 | 3.08 | 7.46 | 7.34 | ns |

**Note:** For specific junction temperature and voltage supply levels, refer to Table 3-7 for derating values.

**Table 5-34.** 1.8V LVCMOS High Slew Worst Commercial-Case Conditions: $T_J$ = 85 °C, Worst-Case VCC = 1.425V Worst-Case VCCxxxxIOBx = 1.7V—Applicable to MSS I/O Banks

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 mA [1] | Std. | 0.22 | 2.77 | 0.09 | 1.09 | 1.64 | 0.22 | 2.82 | 2.72 | 2.21 | 2.25 | ns |
| | –1 | 0.18 | 2.31 | 0.07 | 0.91 | 1.37 | 0.18 | 2.35 | 2.27 | 1.84 | 1.87 | ns |

**Notes:**

1. Denotes the software default selection. This note is applicable for the entire row.
2. For specific junction temperature and voltage supply levels, refer to Table 3-7 for derating values.

### 1.5V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5V applications. It uses a 1.5V input buffer and a push-pull output buffer.

**Table 5-35.** Minimum and Maximum DC Input and Output Levels Applicable to FPGA I/O Banks

| 1.5V LVCMOS | VIL | | VIH | | VOL | VOH | $I_{OL}$ | $I_{OH}$ | $I_{OSL}$ | $I_{OSH}$ | $I_{IL}$ | $I_{IH}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[1] | Max. mA[1] | µA[2] | µA[2] |
| 2 mA | –0.3 | 0.35 * VCCxxxxIOBx | 0.65 * VCCxxxxIOBx | 1.575 | 0.25 * VCCxxxxIOBx | 0.75 * VCCxxxxIOBx | 2 | 2 | 16 | 13 | 15 | 15 |
| 4 mA | –0.3 | 0.35 * VCCxxxxIOBx | 0.65 * VCCxxxxIOBx | 1.575 | 0.25 * VCCxxxxIOBx | 0.75 * VCCxxxxIOBx | 4 | 4 | 33 | 25 | 15 | 15 |
| 6 mA | –0.3 | 0.35 * VCCxxxxIOBx | 0.65 * VCCxxxxIOBx | 1.575 | 0.25 * VCCxxxxIOBx | 0.75 * VCCxxxxIOBx | 6 | 6 | 39 | 32 | 15 | 15 |
| 8 mA | –0.3 | 0.35 * VCCxxxxIOBx | 0.65 * VCCxxxxIOBx | 1.575 | 0.25 * VCC | 0.75 * VCCxxxxIOBx | 8 | 8 | 55 | 66 | 15 | 15 |
| 12 mA [3] | –0.3 | 0.35 * VCCxxxxIOBx | 0.65 * VCCxxxxIOBx | 1.575 | 0.25 * VCCxxxxIOBx | 0.75 * VCCxxxxIOBx | 12 | 12 | 55 | 66 | 15 | 15 |

**Notes:**

1. Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.
2. Currents are measured at 85 °C junction temperature.
3. Denotes the software default selection. This note is applicable for the entire row.

**Table 5-36.** Minimum and Maximum DC Input and Output Levels Applicable to MSS I/O Banks

| 1.5V LVCMOS | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ | $I_{OSL}$ | $I_{OSH}$ | $I_{IL}$ | $I_{IH}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[1] | Max. mA[1] | µA[2] | µA[2] |
| 2 mA [3] | –0.3 | 0.35 * VCCxxxxIOBx | 0.65 * VCCxxxxIOBx | 1.575 | 0.25 * VCCxxxxIOBx | 0.75 * VCCxxxxIOBx | 2 | 2 | 16 | 13 | 15 | 15 |

**Notes:**

1. Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.
2. Currents are measured at 85 °C junction temperature.
3. Denotes the software default selection. This note is applicable for the entire row.

**Figure 5-8.** AC Loading

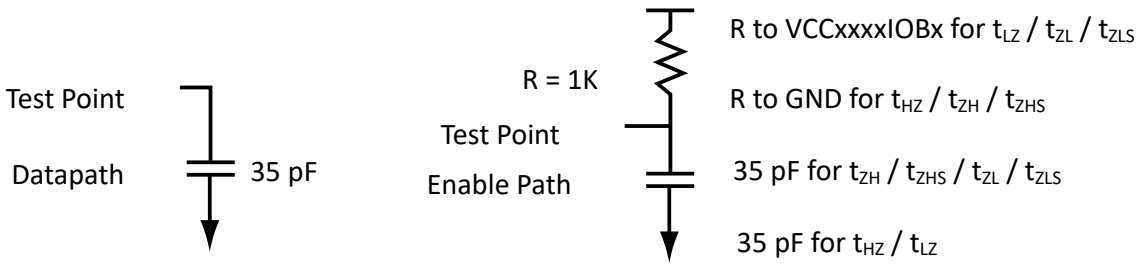



**Table 5-37.** AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|
| 0 | 1.5 | 0.75 | — | 35 |

**Note:**

1. Measuring point = $V_{trip}$. See Table 5-4 for a complete table of trip points.

### Timing Characteristics

**Table 5-38.** 1.5V LVCMOS High Slew—Worst Commercial-Case Conditions: $T_J$ = 85 °C, Worst-Case VCC = 1.425V, Worst-Case VCCxxxxIOBx = 1.425V Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.60 | 7.79 | 0.04 | 1.34 | 0.39 | 6.43 | 7.79 | 3.19 | 2.59 | 8.49 | 9.85 | ns |
| | –1 | 0.50 | 6.49 | 0.03 | 1.12 | 0.32 | 5.36 | 6.49 | 2.66 | 2.16 | 7.08 | 8.21 | ns |
| 4 mA | Std. | 0.60 | 4.95 | 0.04 | 1.34 | 0.39 | 4.61 | 4.96 | 3.53 | 3.19 | 6.67 | 7.02 | ns |
| | –1 | 0.50 | 4.13 | 0.03 | 1.12 | 0.32 | 3.85 | 4.13 | 2.94 | 2.66 | 5.56 | 5.85 | ns |
| 6 mA | Std. | 0.60 | 4.36 | 0.04 | 1.34 | 0.39 | 4.34 | 4.36 | 3.60 | 3.34 | 6.40 | 6.42 | ns |
| | –1 | 0.50 | 3.64 | 0.03 | 1.12 | 0.32 | 3.62 | 3.64 | 3.00 | 2.78 | 5.33 | 5.35 | ns |
| 8 mA | Std. | 0.60 | 3.89 | 0.04 | 1.34 | 0.39 | 3.96 | 3.34 | 3.72 | 3.92 | 6.02 | 5.40 | ns |
| | –1 | 0.50 | 3.24 | 0.03 | 1.12 | 0.32 | 3.30 | 2.79 | 3.10 | 3.27 | 5.02 | 4.50 | ns |
| 12 mA[1] | Std. | 0.60 | 3.89 | 0.04 | 1.34 | 0.39 | 3.96 | 3.34 | 3.72 | 3.92 | 6.02 | 5.40 | ns |
| | –1 | 0.50 | 3.24 | 0.03 | 1.12 | 0.32 | 3.30 | 2.79 | 3.10 | 3.27 | 5.02 | 4.50 | ns |

**Notes:**

1. Denotes the software default selection. This note is applicable for the entire row.
2. For specific junction temperature and voltage supply levels, refer to Table 3-7 for derating values.

**Table 5-39.** 1.5V LVCMOS Low Slew—Worst Commercial-Case Conditions: $T_J$ = 85 °C, Worst-Case VCC = 1.425V, Worst-Case VCCxxxxIOBx = 1.4V Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.60 | 11.96 | 0.04 | 1.34 | 0.39 | 12.18 | 11.70 | 3.20 | 2.47 | 14.24 | 13.76 | ns |
| | –1 | 0.50 | 9.96 | 0.03 | 1.12 | 0.32 | 10.15 | 9.75 | 2.67 | 2.06 | 11.86 | 11.46 | ns |
| 4 mA | Std. | 0.60 | 9.51 | 0.04 | 1.34 | 0.39 | 9.68 | 8.76 | 3.54 | 3.07 | 11.74 | 10.82 | ns |
| | –1 | 0.50 | 7.92 | 0.03 | 1.12 | 0.32 | 8.07 | 7.30 | 2.95 | 2.56 | 9.79 | 9.02 | ns |
| 6 mA | Std. | 0.60 | 8.86 | 0.04 | 1.34 | 0.39 | 9.03 | 8.17 | 3.61 | 3.22 | 11.08 | 10.23 | ns |
| | –1 | 0.50 | 7.39 | 0.03 | 1.12 | 0.32 | 7.52 | 6.81 | 3.01 | 2.68 | 9.24 | 8.52 | ns |
| 8 mA | Std. | 0.60 | 8.44 | 0.04 | 1.34 | 0.39 | 8.60 | 8.18 | 3.73 | 3.78 | 10.66 | 10.24 | ns |
| | –1 | 0.50 | 7.04 | 0.03 | 1.12 | 0.32 | 7.17 | 6.82 | 3.11 | 3.15 | 8.88 | 8.53 | ns |
| 12 mA | Std. | 0.60 | 8.44 | 0.04 | 1.34 | 0.39 | 8.60 | 8.18 | 3.73 | 3.78 | 10.66 | 10.24 | ns |
| | –1 | 0.50 | 7.04 | 0.03 | 1.12 | 0.32 | 7.17 | 6.82 | 3.11 | 3.15 | 8.88 | 8.53 | ns |

**Note:**

1. For specific junction temperature and voltage supply levels, refer to Table 3-7 for derating values.

**Table 5-40.** 1.5 V LVCMOS High Slew—Worst Commercial-Case Conditions: $T_J$ = 85 °C, Worst-Case VCC = 1.425V, Worst-Case VCCxxxxIOBx = 3.0V Applicable to MSS I/O Banks

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA [1] | Std. | 0.22 | 3.24 | 0.09 | 1.28 | 1.86 | 0.22 | 3.30 | 3.20 | 2.24 | 2.21 | ns |
| | –1 | 0.18 | 2.70 | 0.07 | 1.07 | 1.55 | 0.18 | 2.75 | 2.67 | 1.87 | 1.85 | ns |

**Notes:**

1. Denotes the software default selection. This note is applicable for the entire row.
2. For specific junction temperature and voltage supply levels, refer to Table 3-7 for derating values.

### 3.3V PCI, 3.3V PCI-X

Peripheral Component Interface for 3.3V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

**Table 5-41.** Minimum and Maximum DC Input and Output Levels

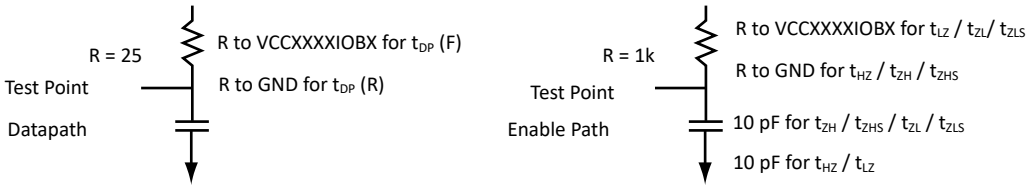
| 3.3V PCI/PCI-X | VIL | | VIH | | VOL | VOH | $I_{OL}$ | $I_{OH}$ | $I_{OSL}$ | $I_{OSH}$ | $I_{IL}$ | $I_{IH}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[1] | Max. mA[1] | µA[2] | µA[2] |
| Per PCI specification | Per PCI curves | | | | | | | | | | 15 | 15 |

**Notes:**

1. Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.
2. Currents are measured at 85 °C junction temperature.

AC loadings are defined per the PCI/PCI-X specifications for the datapath; SoC Products Group loadings for enable path characterization are described in the following figure.

**Figure 5-9.** AC Loading




AC loadings are defined per PCI/PCI-X specifications for the datapath; SoC Products Group loading for tristate is described in the following table.

**Table 5-42.** AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|
| 0 | 3.3 | 0.285 * VCCxxxxIOBx for $t_{DP(R)}$<br>0.615 * VCCxxxxIOBx for $t_{DP(F)}$ | — | 10 |

**Note:** Measuring point = $V_{trip}$. See Table 5-4 for a complete table of trip points.

### Timing Characteristics

**Table 5-43.** 3.3V PCI Worst Commercial-Case Conditions: $T_J$ = 85 °C, Worst-Case VCC = 1.425V, Worst-Case VCCxxxxIOBx = 3.0V—Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 0.60 | 2.54 | 0.04 | 0.82 | 0.39 | 2.58 | 1.88 | 3.06 | 3.39 | 4.64 | 3.94 | ns |
| –1 | 0.50 | 2.11 | 0.03 | 0.68 | 0.32 | 2.15 | 1.57 | 2.55 | 2.82 | 3.87 | 3.28 | ns |

**Note:** For specific junction temperature and voltage supply levels, refer to Table 3-7 for derating values.

**Table 5-44.** 3.3V PCI-X Worst Commercial-Case Conditions: $T_J$ = 85 °C, Worst-Case VCC = 1.425V, Worst-Case VCCxxxxIOBx = 3.0V—Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 0.60 | 2.54 | 0.04 | 0.77 | 0.39 | 2.58 | 1.88 | 3.06 | 3.39 | 4.64 | 3.94 | ns |
| –1 | 0.50 | 2.11 | 0.03 | 0.64 | 0.32 | 2.15 | 1.57 | 2.55 | 2.82 | 3.87 | 3.28 | ns |

**Note:** For specific junction temperature and voltage supply levels, refer to Table 3-7 for derating values.

## 5.5 Differential I/O Characteristics (Ask a Question)

### Physical Implementation

Configuration of the I/O modules as a differential pair is handled by SoC Products Group Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

### LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in the following figure. The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, SmartFusion cSoCs also support bus LVDS structure and multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

**Figure 5-10.** LVDS Circuit Diagram and Board-Level Implementation

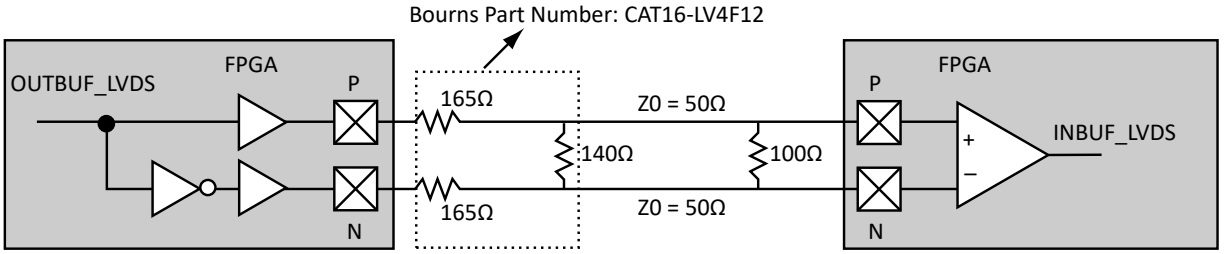



**Table 5-45.** LVDS Minimum and Maximum DC Input and Output Levels

| DC Parameter | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| VCCFPGAIOBx | Supply voltage | 2.375 | 2.5 | 2.625 | V |
| VOL | Output low voltage | 0.9 | 1.075 | 1.25 | V |
| VOH | Output high voltage | 1.25 | 1.425 | 1.6 | V |
| $I_{OL}$[1] | Output lower current | 0.65 | 0.91 | 1.16 | mA |
| $I_{OH}$[1] | Output high current | 0.65 | 0.91 | 1.16 | mA |
| VI | Input voltage | 0 | — | 2.925 | V |
| $I_{IH}$[2] | Input high leakage current | — | — | 15 | µA |

| .....continued | | | | | |
|---|---|---|---|---|---|
| DC Parameter | Description | Min. | Typ. | Max. | Units |
| $I_{IL}$[2] | Input low leakage current | — | — | 15 | µA |
| $V_{ODIFF}$ | Differential output voltage | 250 | 350 | 450 | mV |
| $V_{OCM}$ | Output common mode voltage | 1.125 | 1.25 | 1.375 | V |
| $V_{ICM}$ | Input common mode voltage | 0.05 | 1.25 | 2.35 | V |
| $V_{IDIFF}$ | Input differential voltage | 100 | 350 | — | mV |

**Notes:**

1. $I_{OL}$ / $I_{OH}$ defined by $V_{ODIFF}$ / (resistor network).
2. Currents are measured at 85 °C junction temperature.

**Table 5-46.** AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | $V_{REF}$ (typ.) (V) |
|---|---|---|---|
| 1.075 | 1.325 | Cross point | — |

**Note:** Measuring point = $V_{trip}$. See Table 5-4 for a complete table of trip points.

### Timing Characteristics

**Table 5-47.** LVDS Worst Commercial-Case Conditions: $T_J$ = 85 °C, Worst-Case VCC = 1.425V, Worst-Case VCCFPGAIOBx = 2.3V—Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | Units |
|---|---|---|---|---|---|
| Std. | 0.60 | 1.83 | 0.04 | 1.87 | ns |
| –1 | 0.50 | 1.53 | 0.03 | 1.55 | ns |

**Notes:**

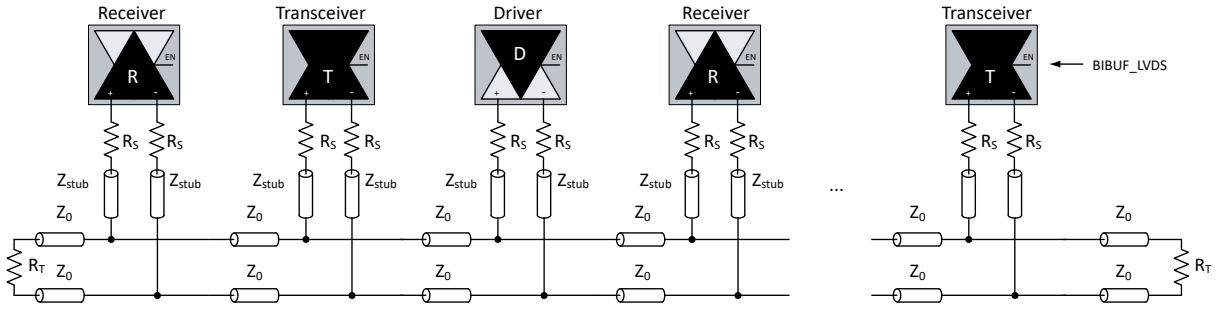
1. For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 for derating values.
2. The above mentioned timing parameters correspond to 24mA drive strength.

#### B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. SoC Products Group LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using SoC Products Group LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in the following figure. The input and output buffer delays are available in the LVDS section in Table 5-47.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case commercial operating conditions, at the farthest receiver: $R_S$ = 60Ω and $R_T$ = 70Ω, given $Z_0$ = 50Ω (2") and $Z_{stub}$ = 50Ω (~1.5").

**Figure 5-11.** B-LVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers




## LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in the following figure. The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

**Figure 5-12.** LVPECL Circuit Diagram and Board-Level Implementation

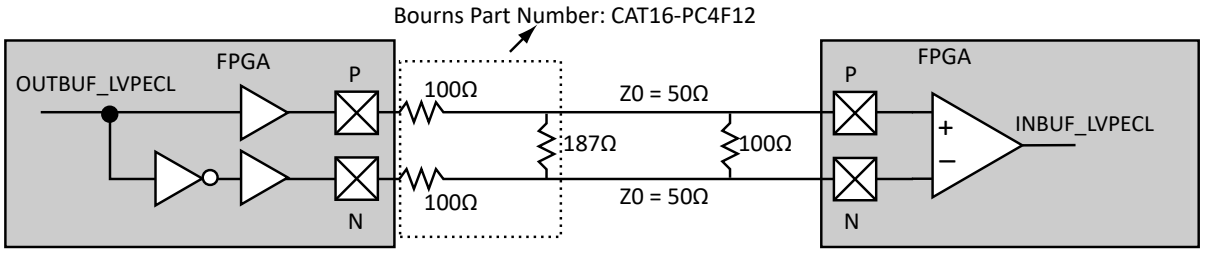



**Table 5-48.** Minimum and Maximum DC Input and Output Levels

| DC Parameter | Description | Min. | Max. | Min. | Max. | Min. | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| VCCFPGAIOBx | Supply Voltage | 3.0 | | 3.3 | | 3.6 | | V |
| VOL | Output Low Voltage | 0.96 | 1.27 | 1.06 | 1.43 | 1.30 | 1.57 | V |
| VOH | Output High Voltage | 1.8 | 2.11 | 1.92 | 2.28 | 2.13 | 2.41 | V |
| VIL, VIH | Input Low, Input High Voltages | 0 | 3.6 | 0 | 3.6 | 0 | 3.6 | V |
| VODIFF | Differential Output Voltage | 0.625 | 0.97 | 0.625 | 0.97 | 0.625 | 0.97 | V |
| VOCM | Output Common-Mode Voltage | 1.762 | 1.98 | 1.762 | 1.98 | 1.762 | 1.98 | V |
| VICM | Input Common-Mode Voltage | 1.01 | 2.57 | 1.01 | 2.57 | 1.01 | 2.57 | V |
| VIDIFF | Input Differential Voltage | 300 | — | 300 | — | 300 | — | mV |

**Table 5-49.** AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) |
|---|---|---|---|
| 1.64 | 1.94 | Cross point | — |

**Note:** Measuring point = $V_{trip}$. See Table 5-4 for a complete table of trip points.

### Timing Characteristics

**Table 5-50.** LVPECL Worst Commercial-Case Conditions: $T_J$ = 85 °C, Worst-Case VCC = 1.425V, Worst-Case VCCFPGAIOBx = 3.0V Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | Units |
|---|---|---|---|---|---|
| Std. | 0.60 | 1.76 | 0.04 | 1.76 | ns |
| –1 | 0.50 | 1.46 | 0.03 | 1.46 | ns |

**Notes:**

1. For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 for derating values.
2. The above mentioned timing parameters correspond to 24mA drive strength.

## 5.6 I/O Register Specifications (Ask a Question)

### Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

**Figure 5-13.** Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

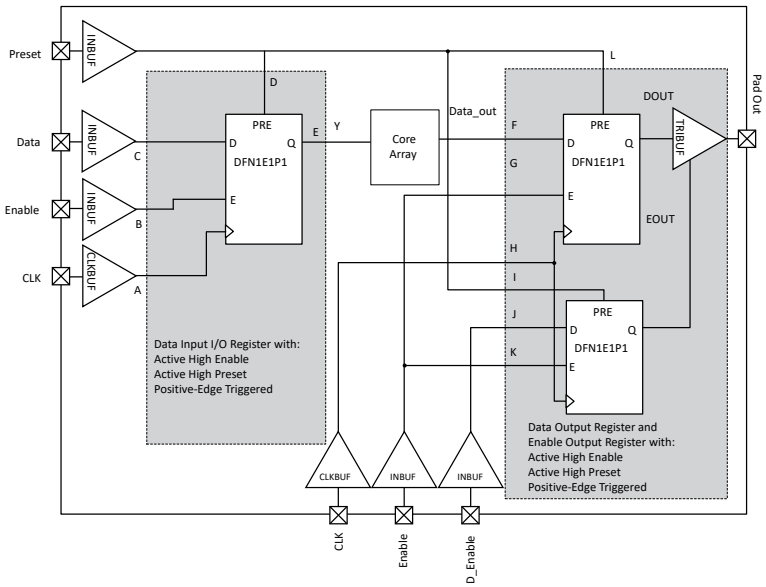



**Table 5-51.** Parameter Definition and Measuring Nodes

| Parameter Name | Parameter Definition | Measuring Nodes (from, to)[1] |
|---|---|---|
| $t_{OCLKQ}$ | Clock-to-Q of the Output Data Register | H, DOUT |
| $t_{OSUD}$ | Data Setup Time for the Output Data Register | F, H |
| $t_{OHD}$ | Data Hold Time for the Output Data Register | F, H |
| $t_{OSUE}$ | Enable Setup Time for the Output Data Register | G, H |
| $t_{OHE}$ | Enable Hold Time for the Output Data Register | G, H |
| $t_{OPRE2Q}$ | Asynchronous Preset-to-Q of the Output Data Register | L, DOUT |
| $t_{OREMPRE}$ | Asynchronous Preset Removal Time for the Output Data Register | L, H |
| $t_{ORECPRE}$ | Asynchronous Preset Recovery Time for the Output Data Register | L, H |
| $t_{OECLKQ}$ | Clock-to-Q of the Output Enable Register | H, EOUT |
| $t_{OESUD}$ | Data Setup Time for the Output Enable Register | J, H |

| .....continued | | |
|---|---|---|
| **Parameter Name** | **Parameter Definition** | **Measuring Nodes (from, to)[1]** |
| $t_{OEHD}$ | Data Hold Time for the Output Enable Register | J, H |
| $t_{OESUE}$ | Enable Setup Time for the Output Enable Register | K, H |
| $t_{OEHE}$ | Enable Hold Time for the Output Enable Register | K, H |
| $t_{OEPRE2Q}$ | Asynchronous Preset-to-Q of the Output Enable Register | I, EOUT |
| $t_{OEREMPRE}$ | Asynchronous Preset Removal Time for the Output Enable Register | I, H |
| $t_{OERECPRE}$ | Asynchronous Preset Recovery Time for the Output Enable Register | I, H |
| $t_{ICLKQ}$ | Clock-to-Q of the Input Data Register | A, E |
| $t_{ISUD}$ | Data Setup Time for the Input Data Register | C, A |
| $t_{IHD}$ | Data Hold Time for the Input Data Register | C, A |
| $t_{ISUE}$ | Enable Setup Time for the Input Data Register | B, A |
| $t_{IHE}$ | Enable Hold Time for the Input Data Register | B, A |
| $t_{IPRE2Q}$ | Asynchronous Preset-to-Q of the Input Data Register | D, E |
| $t_{IREMPRE}$ | Asynchronous Preset Removal Time for the Input Data Register | D, A |
| $t_{IRECPRE}$ | Asynchronous Preset Recovery Time for the Input Data Register | D, A |

**Note:**

1. See Figure 5-13 for more information.

### Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

**Figure 5-14.** Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

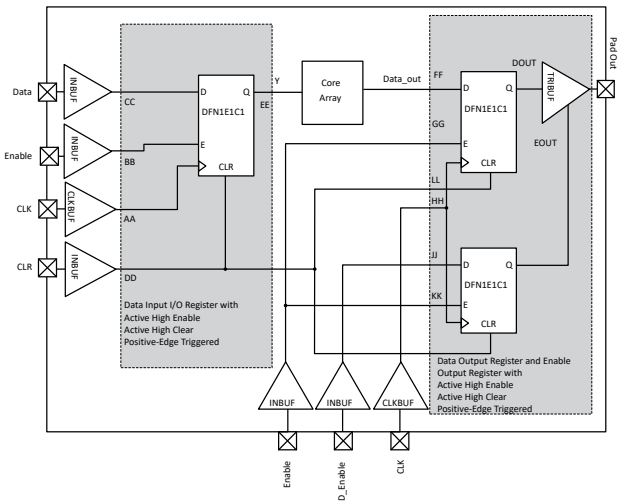



**Table 5-52.** Parameter Definition and Measuring Nodes

| Parameter Name | Parameter Definition | Measuring Nodes (from, to)[1] |
|---|---|---|
| $t_{OCLKQ}$ | Clock-to-Q of the Output Data Register | HH, DOUT |
| $t_{OSUD}$ | Data Setup Time for the Output Data Register | FF, HH |
| $t_{OHD}$ | Data Hold Time for the Output Data Register | FF, HH |
| $t_{OSUE}$ | Enable Setup Time for the Output Data Register | GG, HH |
| $t_{OHE}$ | Enable Hold Time for the Output Data Register | GG, HH |
| $t_{OCLR2Q}$ | Asynchronous Clear-to-Q of the Output Data Register | LL, DOUT |

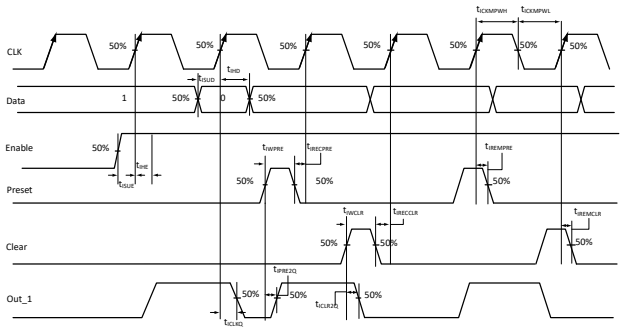
| .....continued | | |
|---|---|---|
| **Parameter Name** | **Parameter Definition** | **Measuring Nodes (from, to)[1]** |
| $t_{OREMCLR}$ | Asynchronous Clear Removal Time for the Output Data Register | LL, HH |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Data Register | LL, HH |
| $t_{OECLKQ}$ | Clock-to-Q of the Output Enable Register | HH, EOUT |
| $t_{OESUD}$ | Data Setup Time for the Output Enable Register | JJ, HH |
| $t_{OEHD}$ | Data Hold Time for the Output Enable Register | JJ, HH |
| $t_{OESUE}$ | Enable Setup Time for the Output Enable Register | KK, HH |
| $t_{OEHE}$ | Enable Hold Time for the Output Enable Register | KK, HH |
| $t_{OECLR2Q}$ | Asynchronous Clear-to-Q of the Output Enable Register | II, EOUT |
| $t_{OEREMCLR}$ | Asynchronous Clear Removal Time for the Output Enable Register | II, HH |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Enable Register | II, HH |
| $t_{ICLKQ}$ | Clock-to-Q of the Input Data Register | AA, EE |
| $t_{ISUD}$ | Data Setup Time for the Input Data Register | CC, AA |
| $t_{IHD}$ | Data Hold Time for the Input Data Register | CC, AA |
| $t_{ISUE}$ | Enable Setup Time for the Input Data Register | BB, AA |
| $t_{IHE}$ | Enable Hold Time for the Input Data Register | BB, AA |
| $t_{ICLR2Q}$ | Asynchronous Clear-to-Q of the Input Data Register | DD, EE |
| $t_{IREMCLR}$ | Asynchronous Clear Removal Time for the Input Data Register | DD, AA |
| $t_{IRECCLR}$ | Asynchronous Clear Recovery Time for the Input Data Register | DD, AA |

**Note:**

1. See Figure 5-14 for more information.

### Input Register

**Figure 5-15.** Input Register Timing Diagram




### Timing Characteristics

**Table 5-53.** Input Data Register Propagation Delays—Worst Commercial-Case Conditions: $T_J$ = 85 °C, Worst-Case VCC = 1.425V

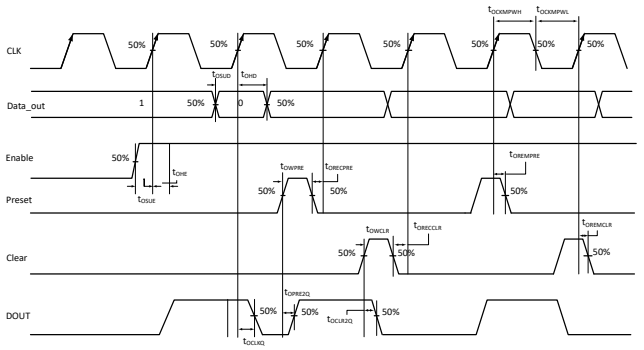
| Parameter | Description | –1 | Std. | Units |
|---|---|---|---|---|
| $t_{ICLKQ}$ | Clock-to-Q of the Input Data Register | 0.24 | 0.29 | ns |
| $t_{ISUD}$ | Data Setup Time for the Input Data Register | 0.27 | 0.32 | ns |
| $t_{IHD}$ | Data Hold Time for the Input Data Register | 0.00 | 0.00 | ns |
| $t_{ISUE}$ | Enable Setup Time for the Input Data Register | 0.38 | 0.45 | ns |
| $t_{IHE}$ | Enable Hold Time for the Input Data Register | 0.00 | 0.00 | ns |
| $t_{ICLR2Q}$ | Asynchronous Clear-to-Q of the Input Data Register | 0.46 | 0.55 | ns |

| .....continued | | | | |
|---|---|---|---|---|
| Parameter | Description | –1 | Std. | Units |
| $t_{IPRE2Q}$ | Asynchronous Preset-to-Q of the Input Data Register | 0.46 | 0.55 | ns |
| $t_{IREMCLR}$ | Asynchronous Clear Removal Time for the Input Data Register | 0.00 | 0.00 | ns |
| $t_{IRECCLR}$ | Asynchronous Clear Recovery Time for the Input Data Register | 0.23 | 0.27 | ns |
| $t_{IREMPRE}$ | Asynchronous Preset Removal Time for the Input Data Register | 0.00 | 0.00 | ns |
| $t_{IRECPRE}$ | Asynchronous Preset Recovery Time for the Input Data Register | 0.23 | 0.27 | ns |
| $t_{IWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Input Data Register | 0.22 | 0.22 | ns |
| $t_{IWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Input Data Register | 0.22 | 0.22 | ns |
| $t_{ICKMPWH}$ | Clock Minimum Pulse Width High for the Input Data Register | 0.36 | 0.36 | ns |
| $t_{ICKMPWL}$ | Clock Minimum Pulse Width Low for the Input Data Register | 0.32 | 0.32 | ns |

**Note:** For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 for derating values.

## Output Register

**Figure 5-16.** Output Register Timing Diagram




## Timing Characteristics

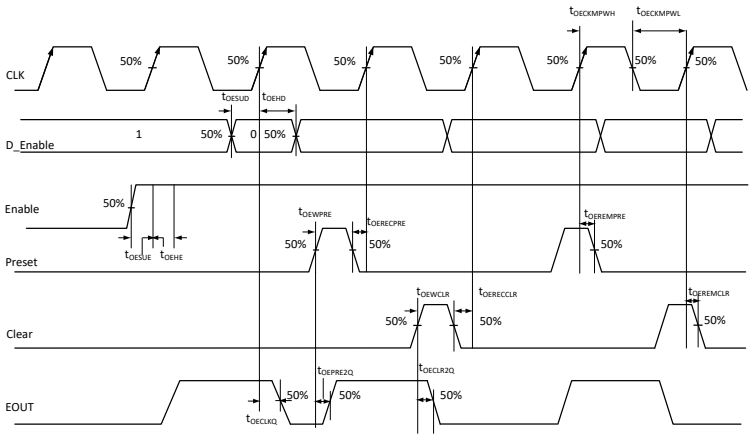
**Table 5-54.** Output Data Register Propagation Delays—Worst Commercial-Case Conditions: $T_J$ = 85 °C, Worst-Case VCC = 1.425V

| Parameter | Description | –1 | Std. | Units |
|---|---|---|---|---|
| $t_{OCLKQ}$ | Clock-to-Q of the Output Data Register | 0.60 | 0.72 | ns |
| $t_{OSUD}$ | Data Setup Time for the Output Data Register | 0.32 | 0.38 | ns |
| $t_{OHD}$ | Data Hold Time for the Output Data Register | 0.00 | 0.00 | ns |
| $t_{OSUE}$ | Enable Setup Time for the Output Data Register | 0.44 | 0.53 | ns |
| $t_{OHE}$ | Enable Hold Time for the Output Data Register | 0.00 | 0.00 | ns |
| $t_{OCLR2Q}$ | Asynchronous Clear-to-Q of the Output Data Register | 0.82 | 0.98 | ns |
| $t_{OPRE2Q}$ | Asynchronous Preset-to-Q of the Output Data Register | 0.82 | 0.98 | ns |
| $t_{OREMCLR}$ | Asynchronous Clear Removal Time for the Output Data Register | 0.00 | 0.00 | ns |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Data Register | 0.23 | 0.27 | ns |
| $t_{OREMPRE}$ | Asynchronous Preset Removal Time for the Output Data Register | 0.00 | 0.00 | ns |
| $t_{ORECPRE}$ | Asynchronous Preset Recovery Time for the Output Data Register | 0.23 | 0.27 | ns |
| $t_{OWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Output Data Register | 0.22 | 0.22 | ns |
| $t_{OWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Output Data Register | 0.22 | 0.22 | ns |
| $t_{OCKMPWH}$ | Clock Minimum Pulse Width High for the Output Data Register | 0.36 | 0.36 | ns |
| $t_{OCKMPWL}$ | Clock Minimum Pulse Width Low for the Output Data Register | 0.32 | 0.32 | ns |

**Note:** For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 for derating values.

## Output Enable Register

**Figure 5-17.** Output Enable Register Timing Diagram




## Timing Characteristics

**Table 5-55.** Output Enable Register Propagation Delays Worst Commercial-Case Conditions: $T_J$ = 85 °C, Worst-Case VCC = 1.425V

| Parameter | Description | –1 | Std. | Units |
|---|---|---|---|---|
| $t_{OECLKQ}$ | Clock-to-Q of the Output Enable Register | 0.45 | 0.54 | ns |
| $t_{OESUD}$ | Data Setup Time for the Output Enable Register | 0.32 | 0.38 | ns |
| $t_{OEHD}$ | Data Hold Time for the Output Enable Register | 0.00 | 0.00 | ns |
| $t_{OESUE}$ | Enable Setup Time for the Output Enable Register | 0.44 | 0.53 | ns |
| $t_{OEHE}$ | Enable Hold Time for the Output Enable Register | 0.00 | 0.00 | ns |
| $t_{OECLR2Q}$ | Asynchronous Clear-to-Q of the Output Enable Register | 0.68 | 0.81 | ns |
| $t_{OEPRE2Q}$ | Asynchronous Preset-to-Q of the Output Enable Register | 0.68 | 0.81 | ns |
| $t_{OEREMCLR}$ | Asynchronous Clear Removal Time for the Output Enable Register | 0.00 | 0.00 | ns |
| $t_{OERECCLR}$ | Asynchronous Clear Recovery Time for the Output Enable Register | 0.23 | 0.27 | ns |
| $t_{OEREMPRE}$ | Asynchronous Preset Removal Time for the Output Enable Register | 0.00 | 0.00 | ns |
| $t_{OERECPRE}$ | Asynchronous Preset Recovery Time for the Output Enable Register | 0.23 | 0.27 | ns |
| $t_{OEWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Output Enable Register | 0.22 | 0.22 | ns |
| $t_{OEWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Output Enable Register | 0.22 | 0.22 | ns |
| $t_{OECKMPWH}$ | Clock Minimum Pulse Width High for the Output Enable Register | 0.36 | 0.36 | ns |
| $t_{OECKMPWL}$ | Clock Minimum Pulse Width Low for the Output Enable Register | 0.32 | 0.32 | ns |

**Note:** For specific junction temperature and voltage supply levels, refer to Table 3-7 for derating values.

## 5.7 DDR Module Specifications (Ask a Question)

### Input DDR Module

**Figure 5-18.** Input DDR Timing Model

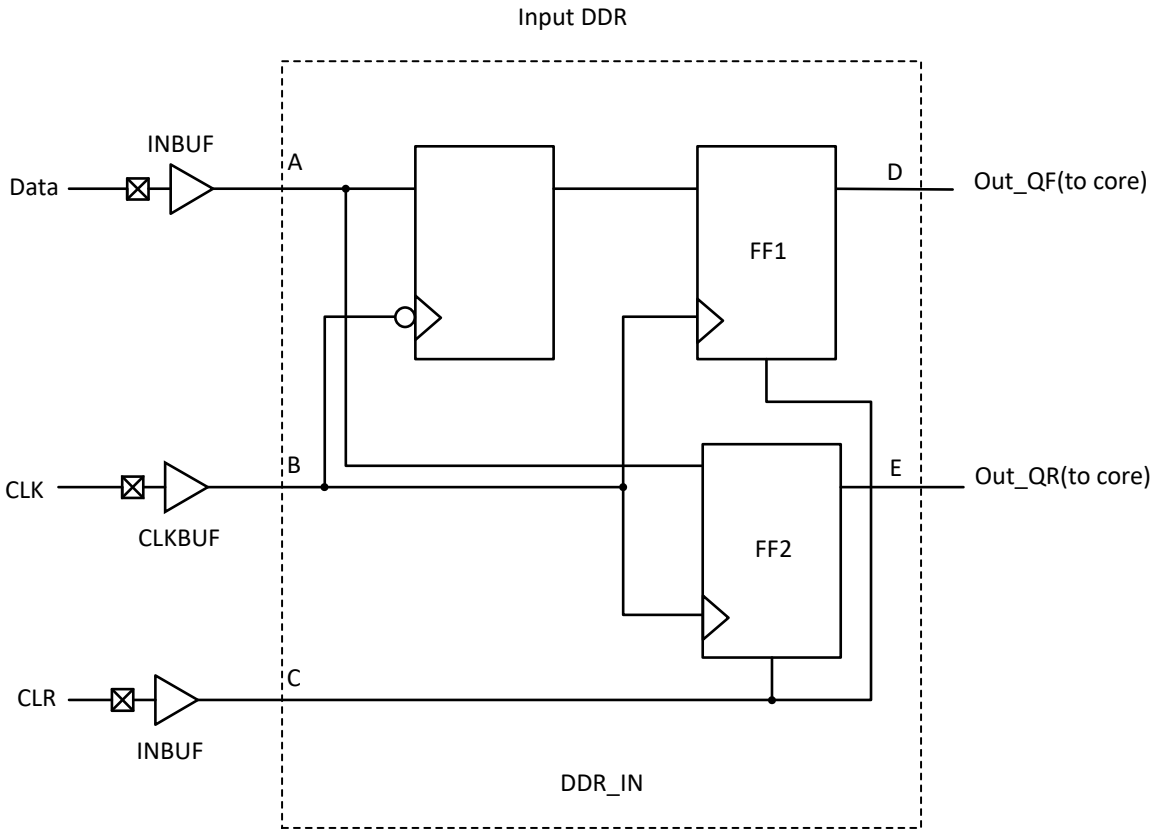
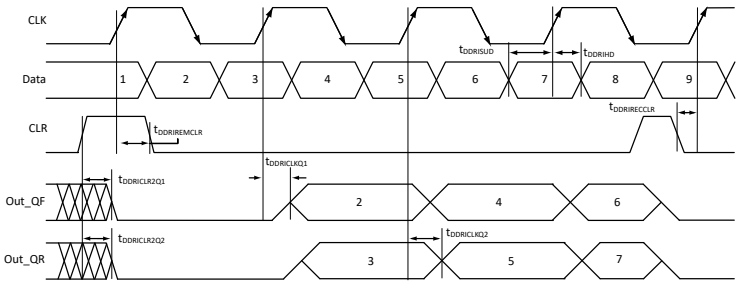



**Table 5-56.** Parameter Definitions

| Parameter Name | Parameter Definition | Measuring Nodes (from, to) |
|---|---|---|
| $t_{DDRICLKQ1}$ | Clock-to-Out Out_QR | B, D |
| $t_{DDRICLKQ2}$ | Clock-to-Out Out_QF | B, E |
| $t_{DDRISUD}$ | Data Setup Time of DDR input | A, B |
| $t_{DDRIHD}$ | Data Hold Time of DDR input | A, B |
| $t_{DDRICLR2Q1}$ | Clear-to-Out Out_QR | C, D |
| $t_{DDRICLR2Q2}$ | Clear-to-Out Out_QF | C, E |
| $t_{DDRIREMCLR}$ | Clear Removal | C, B |
| $t_{DDRIRECCLR}$ | Clear Recovery | C, B |

**Figure 5-19.** Input DDR Timing Diagram




## Timing Characteristics

**Table 5-57.** Input DDR Propagation Delays—Worst Commercial-Case Conditions: $T_J$ = 85 °C, Worst Case VCC = 1.425V

| Parameter | Description | –1 | Units |
|---|---|---|---|
| $t_{DDRICLKQ1}$ | Clock-to-Out Out_QR for Input DDR | 0.39 | ns |
| $t_{DDRICLKQ2}$ | Clock-to-Out Out_QF for Input DDR | 0.28 | ns |
| $t_{DDRISUD}$ | Data Setup for Input DDR | 0.29 | ns |
| $t_{DDRIHD}$ | Data Hold for Input DDR | 0.00 | ns |
| $t_{DDRICLR2Q1}$ | Asynchronous Clear-to-Out Out_QR for Input DDR | 0.58 | ns |
| $t_{DDRICLR2Q2}$ | Asynchronous Clear-to-Out Out_QF for Input DDR | 0.47 | ns |
| $t_{DDRIREMCLR}$ | Asynchronous Clear Removal time for Input DDR | 0.00 | ns |
| $t_{DDRIRECCLR}$ | Asynchronous Clear Recovery time for Input DDR | 0.23 | ns |
| $t_{DDRIWCLR}$ | Asynchronous Clear Minimum Pulse Width for Input DDR | 0.22 | ns |
| $t_{DDRICKMPWH}$ | Clock Minimum Pulse Width High for Input DDR | 0.36 | ns |
| $t_{DDRICKMPWL}$ | Clock Minimum Pulse Width Low for Input DDR | 0.32 | ns |
| $F_{DDRIMAX}$ | Maximum Frequency for Input DDR | 350 | MHz |

**Note:** For derating values at specific junction temperature and voltage-supply levels, refer to Table 3-7 for derating values.

## Output DDR Module

**Figure 5-20.** Output DDR Timing Module

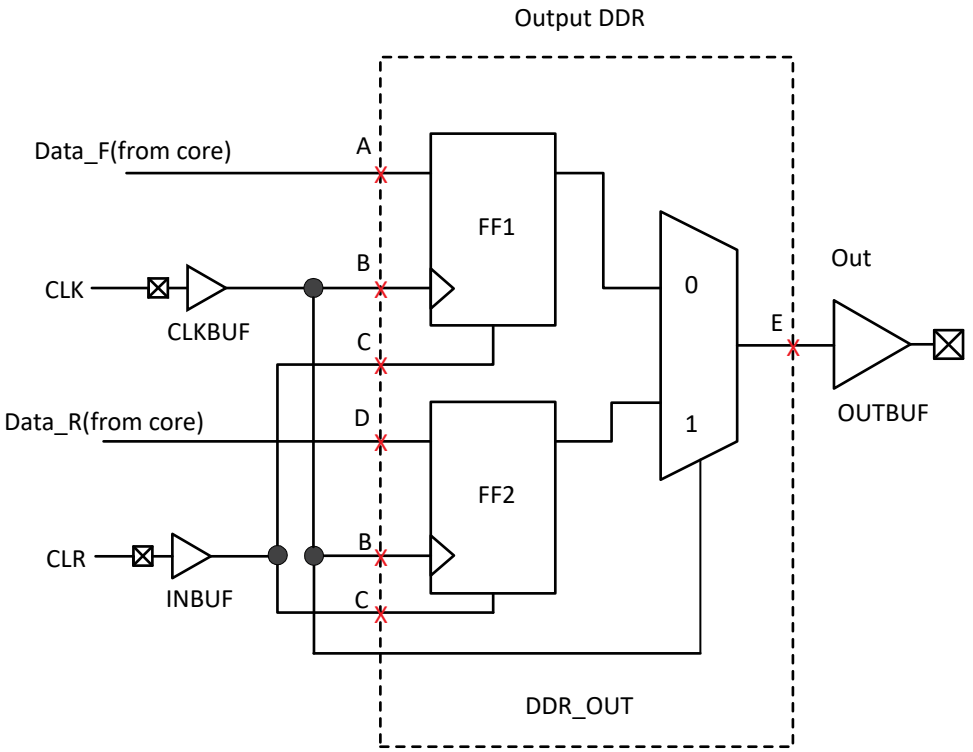
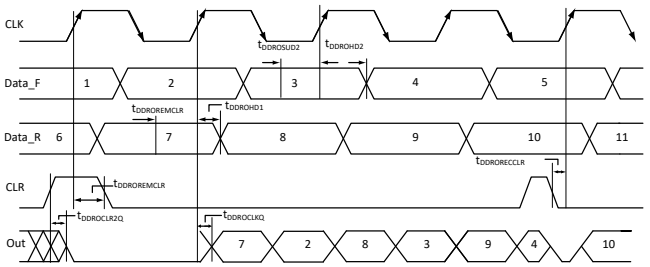



**Table 5-58.** Parameter Definitions

| Parameter Name | Parameter Definition | Measuring Nodes (from, to) |
|---|---|---|
| $t_{DDROCLKQ}$ | Clock-to-Out | B, E |
| $t_{DDROCLR2Q}$ | Asynchronous Clear-to-Out | C, E |
| $t_{DDROREMCLR}$ | Clear Removal | C, B |
| $t_{DDRORECCLR}$ | Clear Recovery | C, B |
| $t_{DDROSUD1}$ | Data Setup Data_F | A, B |
| $t_{DDROSUD2}$ | Data Setup Data_R | D, B |
| $t_{DDROHD1}$ | Data Hold Data_F | A, B |
| $t_{DDROHD2}$ | Data Hold Data_R | D, B |

**Figure 5-21.** Output DDR Timing Diagram




## Timing Characteristics

**Table 5-59.** Output DDR Propagation Delays—Worst Commercial-Case Conditions: $T_J$ = 85 °C, Worst Case VCC = 1.425V

| Parameter | Description | –1 | Units |
|---|---|---|---|
| $t_{DDROCLKQ}$ | Clock-to-Out of DDR for Output DDR | 0.71 | ns |
| $t_{DDROSUD1}$ | Data_F Data Setup for Output DDR | 0.38 | ns |
| $t_{DDROSUD2}$ | Data_R Data Setup for Output DDR | 0.38 | ns |
| $t_{DDROHD1}$ | Data_F Data Hold for Output DDR | 0.00 | ns |
| $t_{DDROHD2}$ | Data_R Data Hold for Output DDR | 0.00 | ns |
| $t_{DDROCLR2Q}$ | Asynchronous Clear-to-Out for Output DDR | 0.81 | ns |
| $t_{DDROREMCLR}$ | Asynchronous Clear Removal Time for Output DDR | 0.00 | ns |
| $t_{DDRORECCLR}$ | Asynchronous Clear Recovery Time for Output DDR | 0.23 | ns |
| $t_{DDROWCLR1}$ | Asynchronous Clear Minimum Pulse Width for Output DDR | 0.22 | ns |
| $t_{DDROCKMPWH}$ | Clock Minimum Pulse Width High for the Output DDR | 0.36 | ns |
| $t_{DDROCKMPWL}$ | Clock Minimum Pulse Width Low for the Output DDR | 0.32 | ns |
| $F_{DDOMAX}$ | Maximum Frequency for the Output DDR | 350 | MHz |

**Note:** For specific junction temperature and voltage supply levels, refer to Table 3-7 for derating values.

# 6. VersaTile Characteristics (Ask a Question)

## 6.1 VersaTile Specifications as a Combinatorial Module (Ask a Question)

The SmartFusion library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the IGLOO/e, Fusion, ProASIC3/E, and SmartFusion Macro Library Guide.

**Figure 6-1.** Sample of Combinatorial Cells

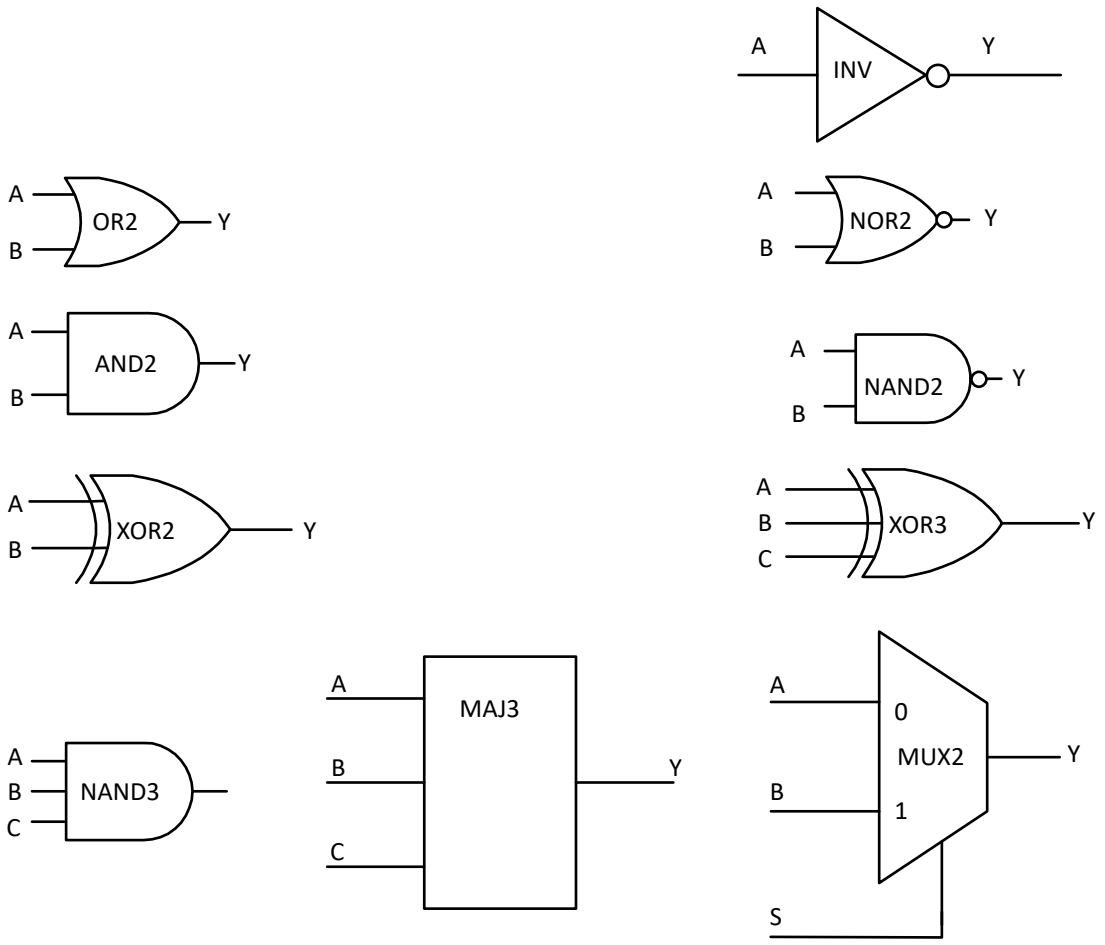
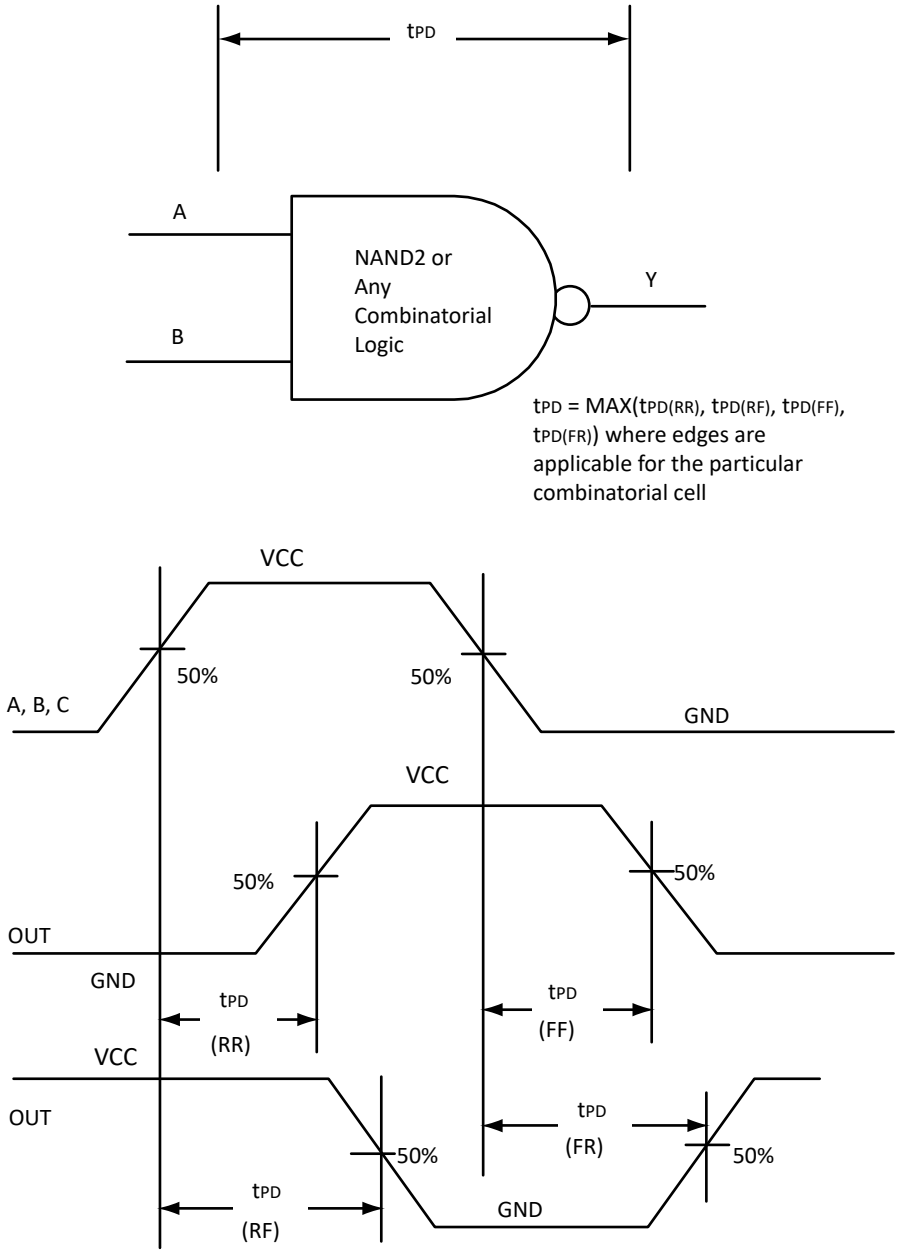


**Figure 6-2.** Timing Model and Waveforms




## Timing Characteristics

**Table 6-1.** Combinatorial Cell Propagation Delays Worst Commercial-Case Conditions: $T_J$ = 85 °C, Worst-Case VCC = 1.425V

| Combinatorial Cell | Equation | Parameter | –1 | Std. | Units |
|---|---|---|---|---|---|
| INV | Y = !A | $t_{PD}$ | 0.41 | 0.49 | ns |
| AND2 | Y = A · B | $t_{PD}$ | 0.48 | 0.57 | ns |
| NAND2 | Y = !(A · B) | $t_{PD}$ | 0.48 | 0.57 | ns |
| OR2 | Y = A + B | $t_{PD}$ | 0.49 | 0.59 | ns |

| .....continued | | | | | |
|---|---|---|---|---|---|
| Combinatorial Cell | Equation | Parameter | –1 | Std. | Units |
| NOR2 | Y = !(A + B) | $t_{PD}$ | 0.49 | 0.59 | ns |
| XOR2 | Y = A ⊕ B | $t_{PD}$ | 0.75 | 0.90 | ns |
| MAJ3 | Y = MAJ(A, B, C) | $t_{PD}$ | 0.71 | 0.85 | ns |
| XOR3 | Y = A ⊕ B ⊕ C | $t_{PD}$ | 0.89 | 1.07 | ns |
| MUX2 | Y = A !S + B S | $t_{PD}$ | 0.51 | 0.62 | ns |
| AND3 | Y = A · B · C | $t_{PD}$ | 0.57 | 0.68 | ns |

**Note:** For specific junction temperature and voltage supply levels, refer to Table 3-7 for derating values.

## 6.2 VersaTile Specifications as a Sequential Module (Ask a Question)

The SmartFusion library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the IGLOO/e, Fusion, ProASIC3/E, and SmartFusion Macro Library Guide.

**Figure 6-3.** Sample of Sequential Cells

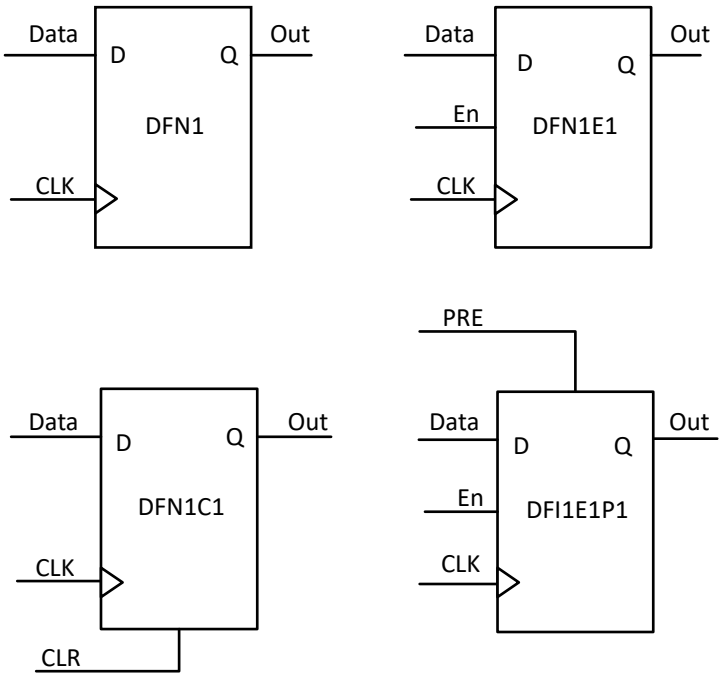
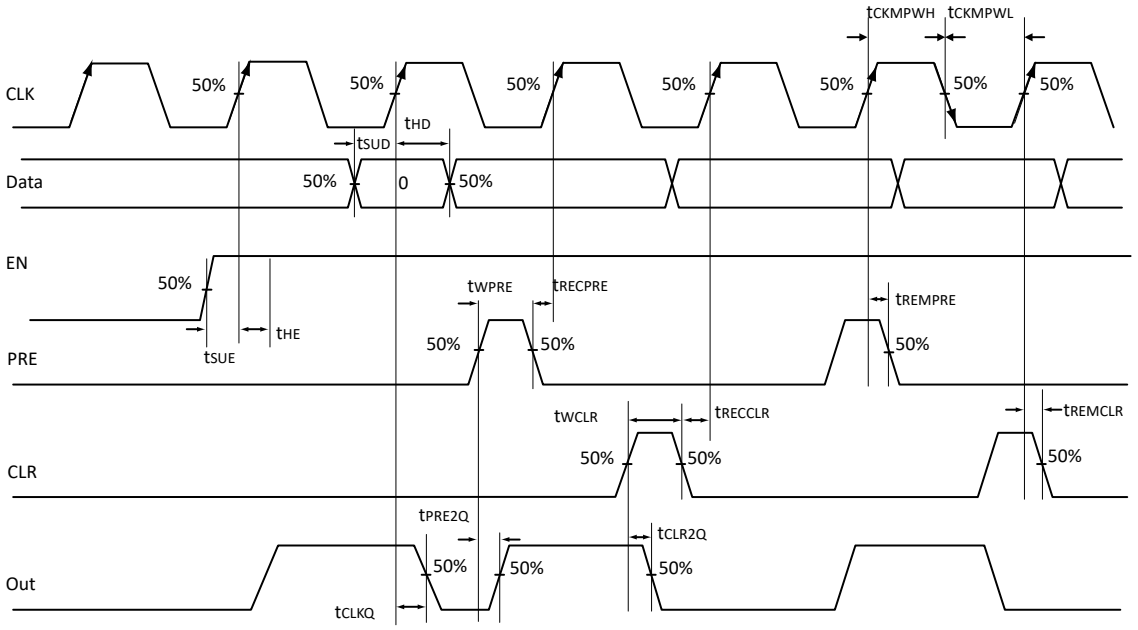


**Figure 6-4.** Timing Model and Waveforms




## Timing Characteristics

**Table 6-2.** Register Delays— Worst Commercial-Case Conditions: $T_J$ = 85 °C, Worst-Case VCC = 1.425V

| Parameter | Description | –1 | Std. | Units |
|---|---|---|---|---|
| $t_{CLKQ}$ | Clock-to-Q of the Core Register | 0.56 | 0.67 | ns |
| $t_{SUD}$ | Data Setup Time for the Core Register | 0.44 | 0.52 | ns |
| $t_{HD}$ | Data Hold Time for the Core Register | 0.00 | 0.00 | ns |
| $t_{SUE}$ | Enable Setup Time for the Core Register | 0.46 | 0.55 | ns |
| $t_{HE}$ | Enable Hold Time for the Core Register | 0.00 | 0.00 | ns |
| $t_{CLR2Q}$ | Asynchronous Clear-to-Q of the Core Register | 0.41 | 0.49 | ns |
| $t_{PRE2Q}$ | Asynchronous Preset-to-Q of the Core Register | 0.41 | 0.49 | ns |
| $t_{REMCLR}$ | Asynchronous Clear Removal Time for the Core Register | 0.00 | 0.00 | ns |
| $t_{RECCLR}$ | Asynchronous Clear Recovery Time for the Core Register | 0.23 | 0.27 | ns |
| $t_{REMPRE}$ | Asynchronous Preset Removal Time for the Core Register | 0.00 | 0.00 | ns |
| $t_{RECPRE}$ | Asynchronous Preset Recovery Time for the Core Register | 0.23 | 0.27 | ns |
| $t_{WCLR}$ | Asynchronous Clear Minimum Pulse Width for the Core Register | 0.22 | 0.22 | ns |
| $t_{WPRE}$ | Asynchronous Preset Minimum Pulse Width for the Core Register | 0.22 | 0.22 | ns |
| $t_{CKMPWH}$ | Clock Minimum Pulse Width High for the Core Register | 0.32 | 0.32 | ns |
| $t_{CKMPWL}$ | Clock Minimum Pulse Width Low for the Core Register | 0.36 | 0.36 | ns |

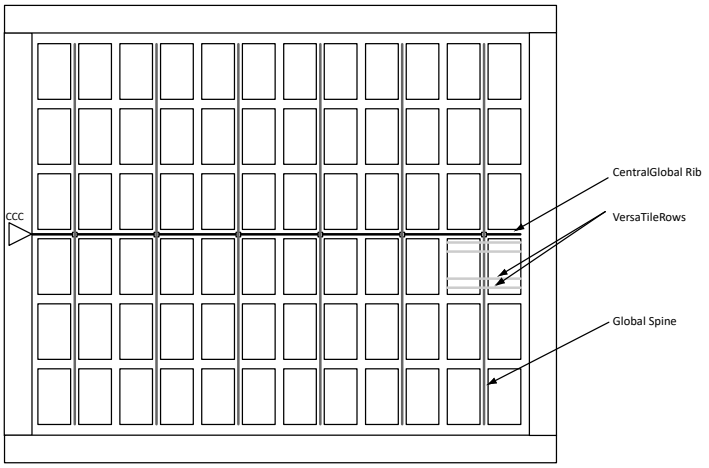
**Note:** For specific junction temperature and voltage supply levels, refer to Table 3-7 for derating values.

# 7. Global Resource Characteristics (Ask a Question)

## 7.1 A2F200 Clock Tree Topology (Ask a Question)

Clock delays are device-specific. The following figure is an example of a global tree used for clock routing. The global tree presented in the figure is driven by a CCC located on the west side of the A2F200 device. It is used to drive all D-flip-flops in the device.

**Figure 7-1.** Example of Global Tree Use in an A2F200 Device for Clock Routing




## 7.2 Global Tree Timing Characteristics (Ask a Question)

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the Clock Conditioning Circuits section. The following tables present minimum and maximum global clock delays for the SmartFusion cSoCs. Minimum and maximum delays are measured with minimum and maximum loading.

### Timing Characteristics

**Table 7-1.** A2F500 Global Resource Worst Commercial-Case Conditions: $T_J$ = 85 °C, VCC = 1.425V

| Parameter | Description | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|
| | | Min.[1] | Max.[2] | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 1.54 | 1.73 | 1.84 | 2.08 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 1.53 | 1.76 | 1.84 | 2.12 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 0.85 | — | 1.00 | — | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 0.85 | — | 1.00 | — | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | — | 0.23 | — | 0.28 | ns |

**Notes:**

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage-supply levels, refer to Table 3-7 for derating values.

**Table 7-2.** A2F200 Global Resource Worst Commercial-Case Conditions: $T_J$ = 85 °C, VCC = 1.425V

| Parameter | Description | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|
| | | Min.[1] | Max.[2] | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 0.74 | 0.99 | 0.88 | 1.19 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 0.76 | 1.05 | 0.91 | 1.26 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 0.85 | — | 1.00 | — | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 0.85 | — | 1.00 | — | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | — | 0.29 | — | 0.35 | ns |

**Notes:**

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage-supply levels, refer to Table 3-7 for derating values.

**Table 7-3.** A2F060 [1] Global Resource Worst Commercial-Case Conditions: $T_J$ = 85 °C, VCC = 1.425V

| Parameter | Description | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|
| | | Min. [2] | Max. [3] | Min.[2] | Max.[3] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 0.75 | 0.96 | 0.90 | 1.15 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 0.72 | 0.98 | 0.86 | 1.17 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 0.85 | — | 1.00 | — | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 0.85 | — | 1.00 | — | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | — | 0.26 | — | 0.31 | ns |

**Notes:**

1. Part No A2F060 is discontinued.
2. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
3. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
4. For specific junction temperature and voltage-supply levels, refer to Table 3-7 for derating values.

# 8. RC Oscillator (Ask a Question)

The table below describes the electrical characteristics of the RC oscillator.

**Table 8-1.** Electrical Characteristics of the RC Oscillator

| Parameter | Description | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| FRC | Operating frequency | — | — | 100 | — | MHz |
| | Accuracy | Temperature: –40 °C to 100 °C<br>Voltage: 3.3V ± 5% | — | 1 | — | % |
| | Output jitter | Period jitter (at 5K cycles) | — | 100 | — | ps RMS |
| | | Cycle-to-cycle jitter (at 5K cycles) | — | 100 | — | ps RMS |
| | | Period jitter (at 5K cycles) with 1 KHz / 300 mV peak-to-peak noise on power supply | — | 150 | — | ps RMS |
| | | Cycle-to-cycle jitter (at 5K cycles) with 1 KHz / 300 mV peak-to-peak noise on power supply | — | 150 | — | ps RMS |
| | Output duty cycle | — | — | 50 | — | % |
| IDYNRC | Operating current | 3.3V domain | — | 1 | — | mA |
| | | 1.5V domain | — | 2 | — | mA |

# 9. Main and Lower Power Crystal Oscillator (Ask a Question)

The tables below describes the electrical characteristics of the main and low power crystal oscillator.

**Table 9-1.** Electrical Characteristics of the Main Crystal Oscillator

| Parameter | Description | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| — | Operating frequency | Using external crystal | 0.032 | — | 20 | MHz |
| | | Using ceramic resonator | 0.5 | — | 8 | MHz |
| | | Using RC Network | 0.032 | — | 4 | MHz |
| — | Output duty cycle | — | — | 50 | — | % |
| — | Output jitter | With 10 MHz crystal | — | 1 | — | ns RMS |
| IDYNXTAL | Operating current | RC | — | 0.6 | — | mA |
| | | 0.032–0.2 | — | 0.6 | — | mA |
| | | 0.2–2.0 | — | 0.6 | — | mA |
| | | 2.0–20.0 | — | 0.6 | — | mA |
| ISTBXTAL | Standby current of crystal oscillator | — | — | 10 | — | µA |
| PSRRXTAL | Power supply noise tolerance | — | — | 0.5 | — | Vp-p |
| VIHXTAL | Input logic level High | — | 90% of VCC | — | — | V |
| VILXTAL | Input logic level Low | — | — | — | 10% of VCC | V |
| | Startup time | RC [Tested at 3.24 MHz] | — | 300 | 550 | µs |
| | — | 0.032–0.2 [Tested at 32 KHz] | — | 500 | 3,000 | µs |
| | — | 0.2–2.0 [Tested at 2 MHz] | — | 8 | 12 | µs |
| | — | 2.0–20.0 [Tested at 20 MHz] | — | 160 | 180 | µs |

**Table 9-2.** Electrical Characteristics of the Low Power Oscillator

| Parameter | Description | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| — | Operating frequency | — | — | 32 | — | KHz |
| — | Output duty cycle | — | — | 50 | — | % |
| — | Output jitter | — | — | 30 | — | ns RMS |
| IDYNXTAL | Operating current | 32 KHz | — | 10 | — | µA |
| ISTBXTAL | Standby current of crystal oscillator | — | — | 2 | — | µA |
| PSRRXTAL | Power supply noise tolerance | — | — | 0.5 | — | Vp-p |
| VIHXTAL | Input logic level High | — | 90% of VCC | — | — | V |
| VILXTAL | Input logic level Low | — | — | — | 10% of VCC | V |
| — | Startup time | Test load used: 20 pF | — | 2.5 | — | s |
| | | Test load used: 30 pF | — | 3.7 | 13 | s |

# 10. Clock Conditioning Circuits (Ask a Question)

## CCC Electrical Specifications

## Timing Characteristics

**Table 10-1.** SmartFusion® CCC/PLL Specification

| Parameter | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|
| Clock Conditioning Circuitry Input Frequency $f_{IN\_CCC}$ | 1.5 | — | 350 | MHz |
| Clock Conditioning Circuitry Output Frequency $f_{OUT\_CCC}$ | 0.75 | — | 350[1] | MHz |
| Delay Increments in Programmable Delay Blocks[2, 3,4] | — | 160 | — | ps |
| Number of Programmable Values in Each Programmable Delay Block | — | — | 32 | — |
| Input Period Jitter | — | — | 1.5 | ns |
| Acquisition Time | — | — | — | — |
| LockControl = 0 | — | — | 300 | µs |
| LockControl = 1 | — | — | 6.0 | ms |
| Tracking Jitter[5] | — | — | — | — |
| LockControl = 0 | — | — | 1.6 | ns |
| LockControl = 1 | — | — | 0.8 | ns |
| Output Duty Cycle | 48.5 | — | 5.15 | % |
| Delay Range in Block: Programmable Delay 1[2, 3] | 0.6 | — | 5.56 | ns |
| Delay Range in Block: Programmable Delay 2[2, 3] | 0.025 | — | 5.56 | ns |
| Delay Range in Block: Fixed Delay[2, 3] | — | 2.2 | — | ns |

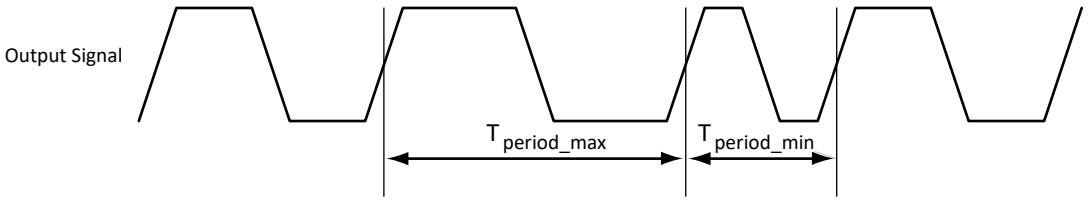
| CCC Output Peak-to-Peak Period Jitter $F_{CCC\_OUT}$ [6, 7] | Maximum Peak-to-Peak Period Jitter | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | **SSO ≤ 2** | | **SSO ≤ 4** | | **SSO ≤ 8** | | **SSO ≤ 16** | |
| — | **FG/CS** | **PQ** | **FG/CS** | **PQ** | **FG/CS** | **PQ** | **FG/CS** | **PQ** |
| 0.75 MHz to 50 MHz | 0.5% | 1.6% | 0.9% | 1.6% | 0.9% | 1.6% | 0.9% | 1.8% |
| 50 MHz to 250 MHz | 1.75% | 3.5% | 9.3% | 9.3% | 9.3% | 17.9% | 10.0% | 17.9% |
| 250 MHz to 350 MHz | 2.5% | 5.2% | 13.0% | 13.0% | 13.0% | 25.0% | 14.0% | 25.0% |

**Notes:**

1. One of the CCC outputs (GLA0) is used as an MSS clock and is limited to 100 MHz (maximum) by software. Details regarding CCC/PLL are in the “PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators” chapter of the SmartFusion Microcontroller Subsystem User’s Guide.
2. This delay is a function of voltage and temperature. See Table 3-7 for deratings.
3. $T_J$ = 25 °C, VCC = 1.5V
4. When the CCC/PLL core is generated by Microchip core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.
5. Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.
6. Measurement done with LVTTL 3.3V 12 mA I/O drive strength and High slew rate. VCC/VCCPLL = 1.425V, VCCI = 3.3V, 20 pF output load. All I/Os are placed outside of the PLL bank.
7. SSOs are outputs that are synchronous to a single clock domain and have their clock-to-out within ± 200 ps of each other.
8. VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the % jitter. The VCO jitter (in ps) applies to CCC_OUT

regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps.

**Figure 10-1.** Peak-to-Peak Jitter Definition

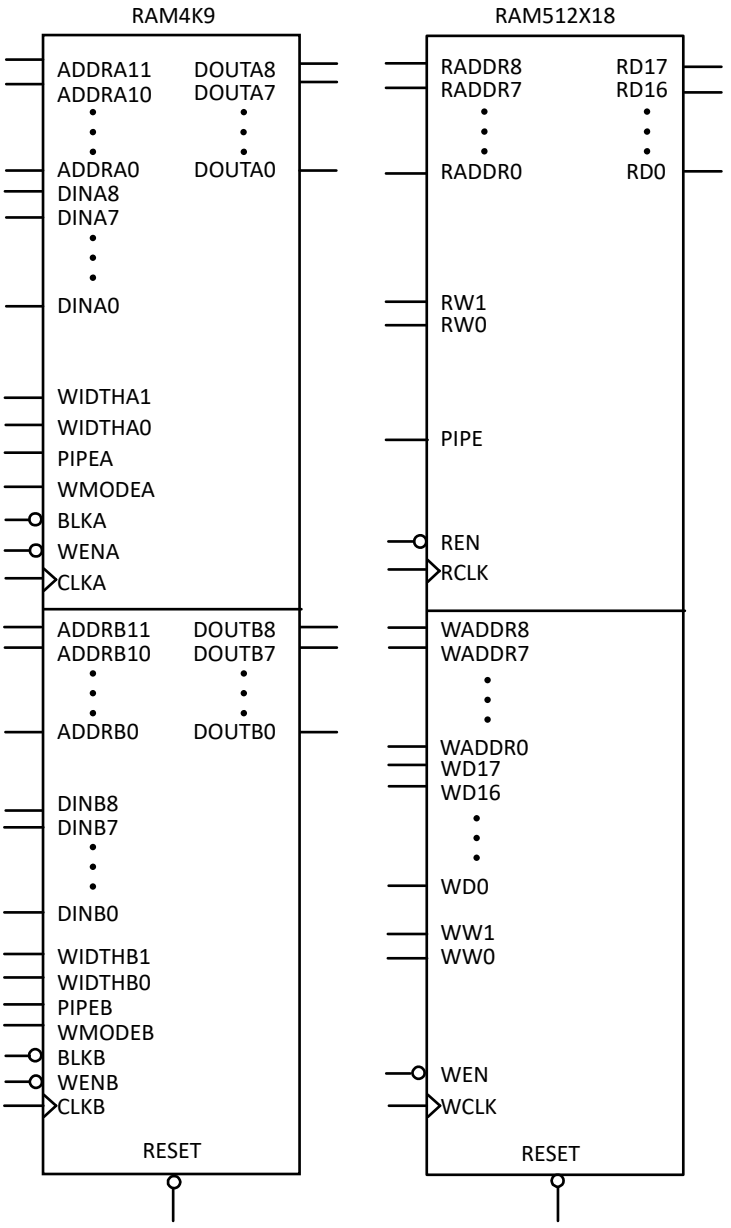



**Note:** Peak-to-peak jitter measurements are defined by $T_{peak\text{-}to\text{-}peak} = T_{period\_max} - T_{period\_min}$.

# 11. FPGA Fabric SRAM and FIFO Characteristics (Ask a Question)

## FPGA Fabric SRAM

**Figure 11-1.** RAM Models




### Timing Waveforms

**Figure 11-2.** RAM Read for Pass-Through Output. Applicable to both RAM4K9 and RAM512x18

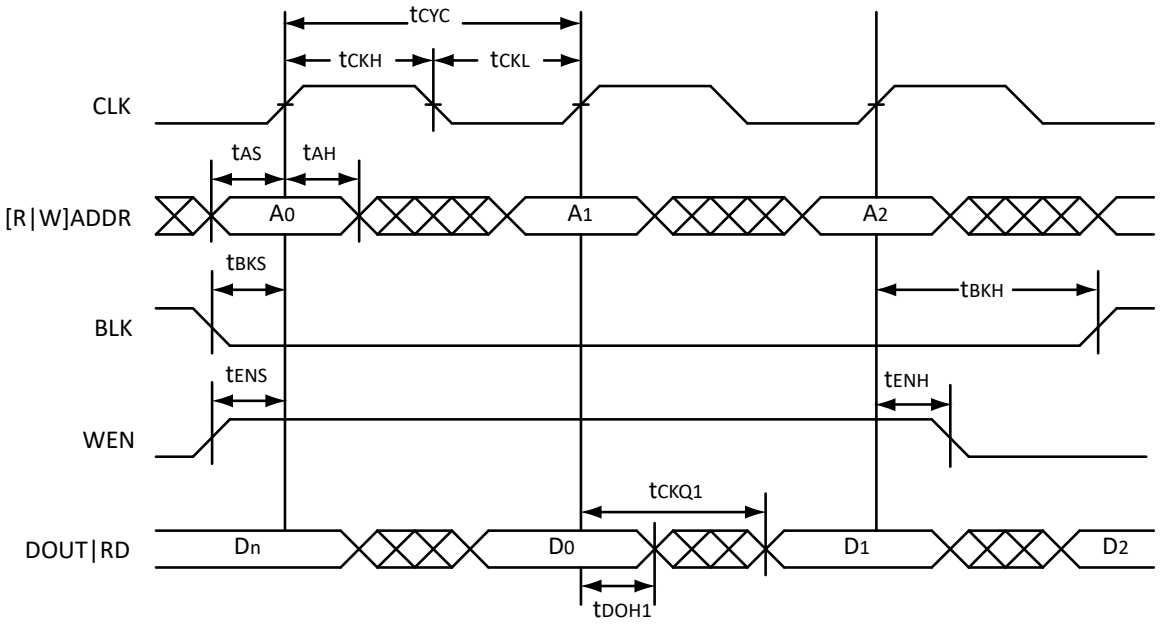



**Figure 11-3.** RAM Read for Pipelined Output Applicable to both RAM4K9 and RAM512x18

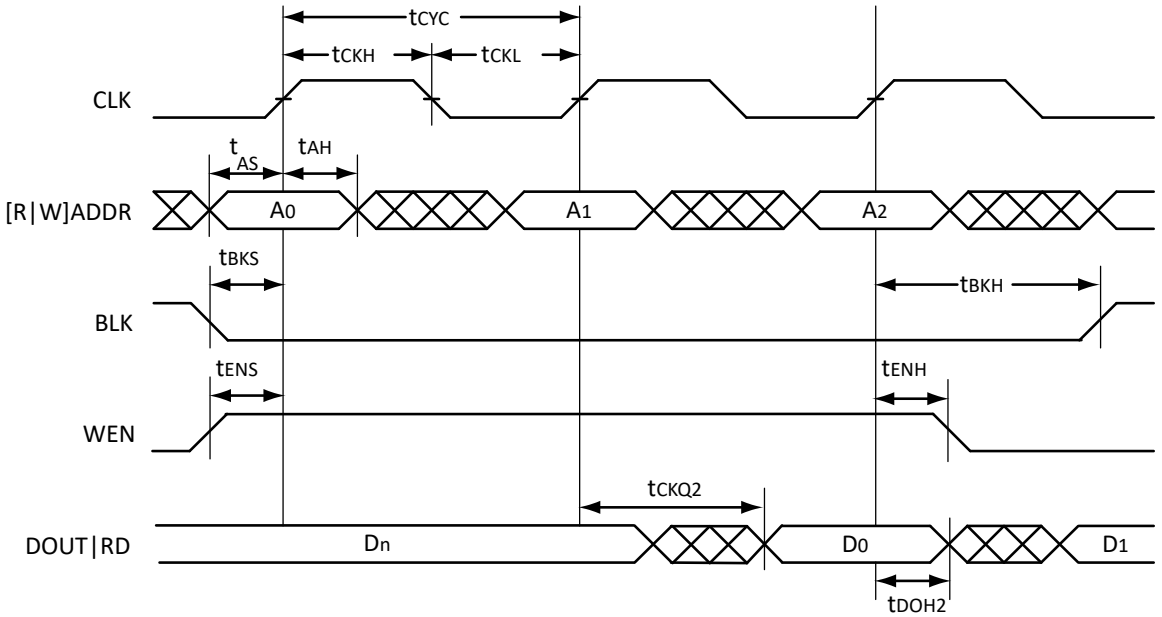


**Figure 11-4.** RAM Write, Output Retained. Applicable to both RAM4K9 and RAM512x18

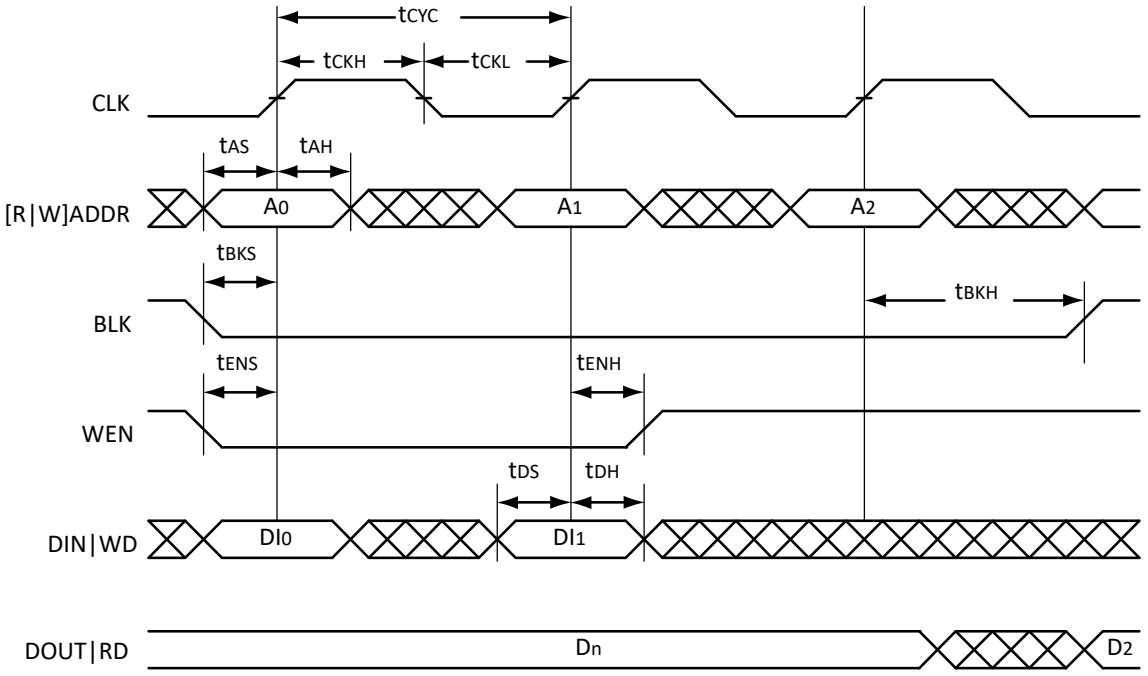


**Figure 11-5.** RAM Write, Output as Write Data (WMODE = 1). Applicable to RAM4K9 only

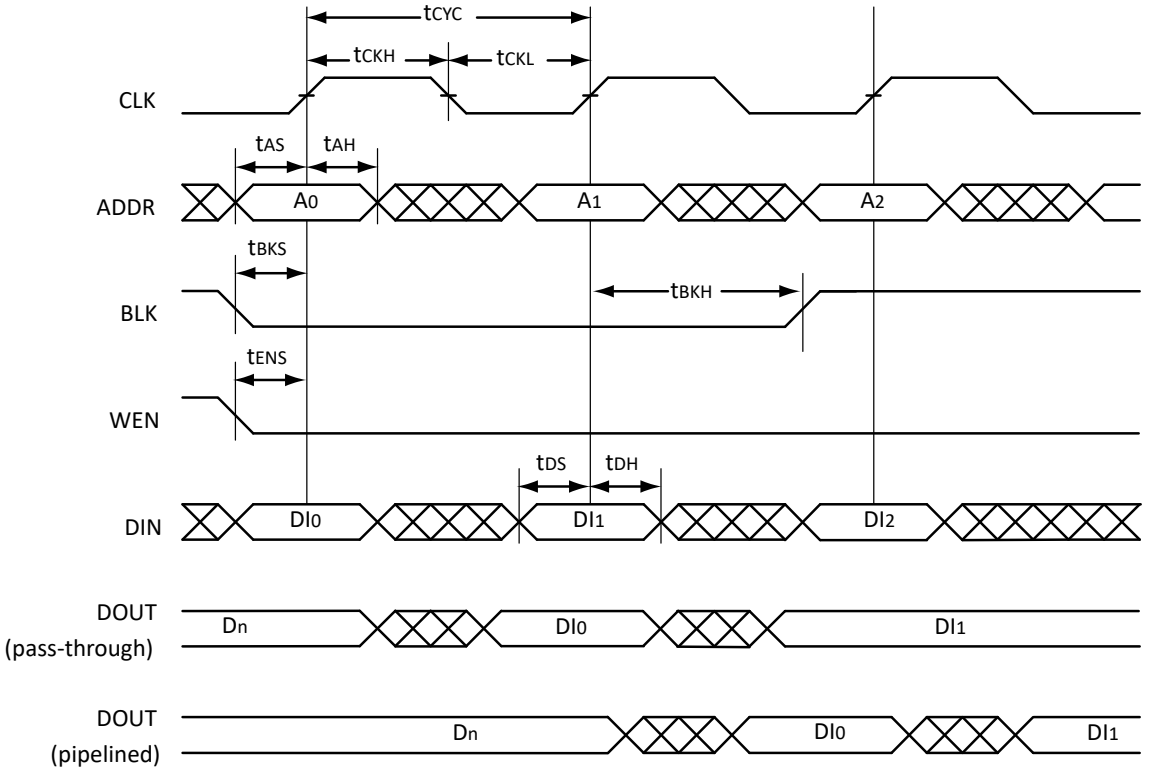
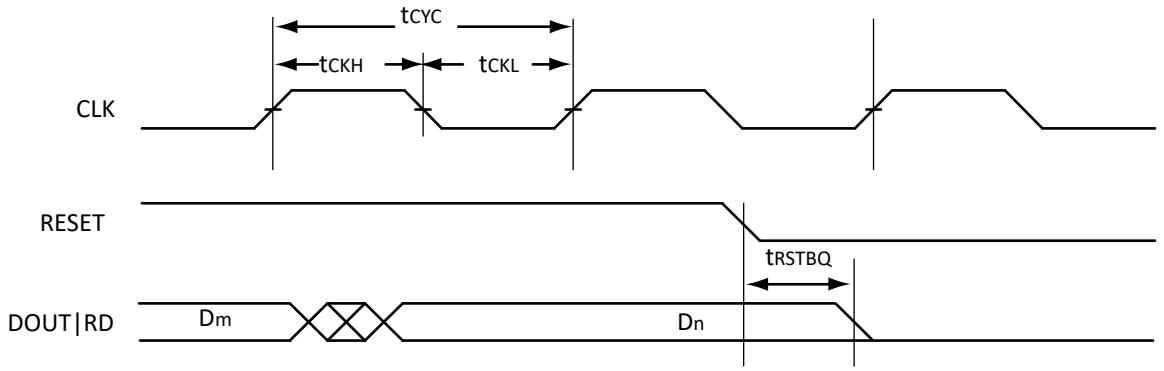



**Figure 11-6.** RAM Reset. Applicable to both RAM4K9 and RAM512x18




## Timing Characteristics

**Table 11-1.** RAM4K9 Worst Commercial-Case Conditions: $T_J$ = 85 °C, Worst-Case VCC = 1.425V

| Parameter | Description | –1 | Std. | Units |
|---|---|---|---|---|
| $t_{AS}$ | Address setup time | 0.25 | 0.30 | ns |
| $t_{AH}$ | Address hold time | 0.00 | 0.00 | ns |
| $t_{ENS}$ | REN, WEN setup time | 0.15 | 0.17 | ns |

| .....continued | | | | |
|---|---|---|---|---|
| Parameter | Description | –1 | Std. | Units |
| $t_{ENH}$ | REN, WEN hold time | 0.10 | 0.12 | ns |
| $t_{BKS}$ | BLK setup time | 0.24 | 0.28 | ns |
| $t_{BKH}$ | BLK hold time | 0.02 | 0.02 | ns |
| $t_{DS}$ | Input data (DIN) setup time | 0.19 | 0.22 | ns |
| $t_{DH}$ | Input data (DIN) hold time | 0.00 | 0.00 | ns |
| $t_{CKQ1}$ | Clock High to new data valid on DOUT (output retained, WMODE = 0) | 1.81 | 2.18 | ns |
| | Clock High to new data valid on DOUT (flow-through, WMODE = 1) | 2.39 | 2.87 | ns |
| $t_{CKQ2}$ | Clock High to new data valid on DOUT (pipelined) | 0.91 | 1.09 | ns |
| $t_{C2CWWH}$[1] | Address collision clk-to-clk delay for reliable write after write on same address—applicable to rising edge | 0.23 | 0.26 | ns |
| $t_{C2CRWH}$[1] | Address collision clk-to-clk delay for reliable read access after write on same address —applicable to opening edge | 0.34 | 0.38 | ns |
| $t_{C2CWRH}$[1] | Address collision clk-to-clk delay for reliable write access after read on same address — applicable to opening edge | 0.37 | 0.42 | ns |
| $t_{RSTBQ}$ | RESET Low to data out Low on DOUT (flow-through) | 0.94 | 1.12 | ns |
| | RESET Low to Data Out Low on DOUT (pipelined) | 0.94 | 1.12 | ns |
| $t_{REMRSTB}$ | RESET removal | 0.29 | 0.35 | ns |
| $t_{RECRSTB}$ | RESET recovery | 1.52 | 1.83 | ns |
| $t_{MPWRSTB}$ | RESET minimum pulse width | 0.22 | 0.22 | ns |
| $t_{CYC}$ | Clock cycle time | 3.28 | 3.28 | ns |
| $F_{MAX}$ | Maximum clock frequency | 305 | 305 | MHz |

**Notes:**

1. For more information, refer to the Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs application note.
2. For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 for derating values.

**Table 11-2.** RAM512X18 Worst Commercial-Case Conditions: $T_J$ = 85 °C, Worst-Case VCC = 1.425V

| Parameter | Description | –1 | Std. | Units |
|---|---|---|---|---|
| $t_{AS}$ | Address setup time | 0.25 | 0.30 | ns |
| $t_{AH}$ | Address hold time | 0.00 | 0.00 | ns |
| $t_{ENS}$ | REN, WEN setup time | 0.09 | 0.11 | ns |
| $t_{ENH}$ | REN, WEN hold time | 0.06 | 0.07 | ns |
| $t_{DS}$ | Input data (WD) setup time | 0.19 | 0.22 | ns |
| $t_{DH}$ | Input data (WD) hold time | 0.00 | 0.00 | ns |
| $t_{CKQ1}$ | Clock High to new data valid on RD (output retained, WMODE = 0) | 2.19 | 2.63 | ns |
| $t_{CKQ2}$ | Clock High to new data valid on RD (pipelined) | 0.91 | 1.09 | ns |
| $t_{C2CRWH}$[1] | Address collision clk-to-clk delay for reliable read access after write on same address—applicable to opening edge | 0.38 | 0.43 | ns |
| $t_{C2CWRH}$[1] | Address collision clk-to-clk delay for reliable write access after read on same address—applicable to opening edge | 0.44 | 0.50 | ns |
| $t_{RSTBQ}$ | RESET Low to data out Low on RD (flow-through) | 0.94 | 1.12 | ns |
| | RESET Low to data out Low on RD (pipelined) | 0.94 | 1.12 | ns |
| $t_{REMRSTB}$ | RESET removal | 0.29 | 0.35 | ns |
| $t_{RECRSTB}$ | RESET recovery | 1.52 | 1.83 | ns |
| $t_{MPWRSTB}$ | RESET minimum pulse width | 0.22 | 0.22 | ns |

**.....continued**

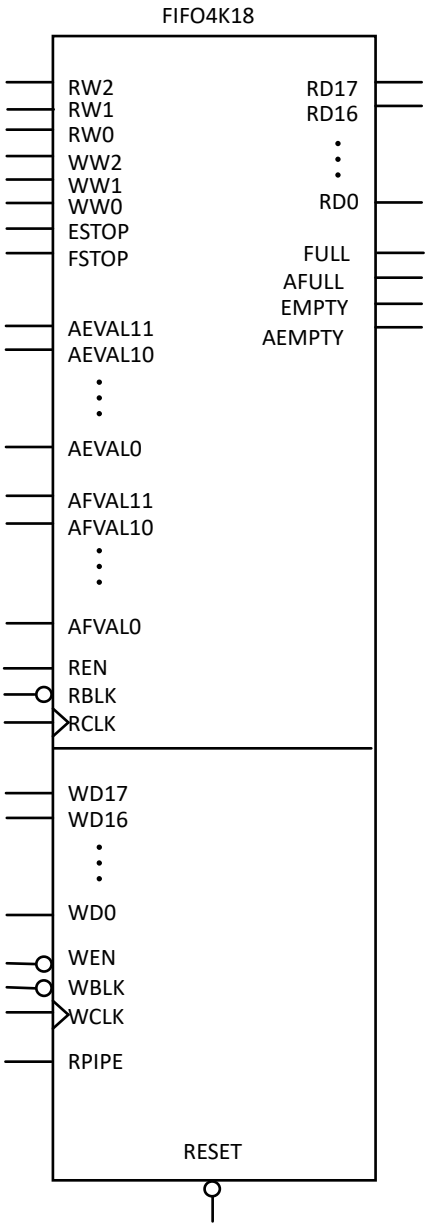
| Parameter | Description | –1 | Std. | Units |
|---|---|---|---|---|
| $t_{CYC}$ | Clock cycle time | 3.28 | 3.28 | ns |
| $F_{MAX}$ | Maximum clock frequency | 305 | 305 | MHz |

**Notes:**

1. For more information, refer to the Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs application note.
2. For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 for derating values.

## FIFO

**Figure 11-7.** FIFO Model




## Timing Waveforms

**Figure 11-8.** FIFO Read

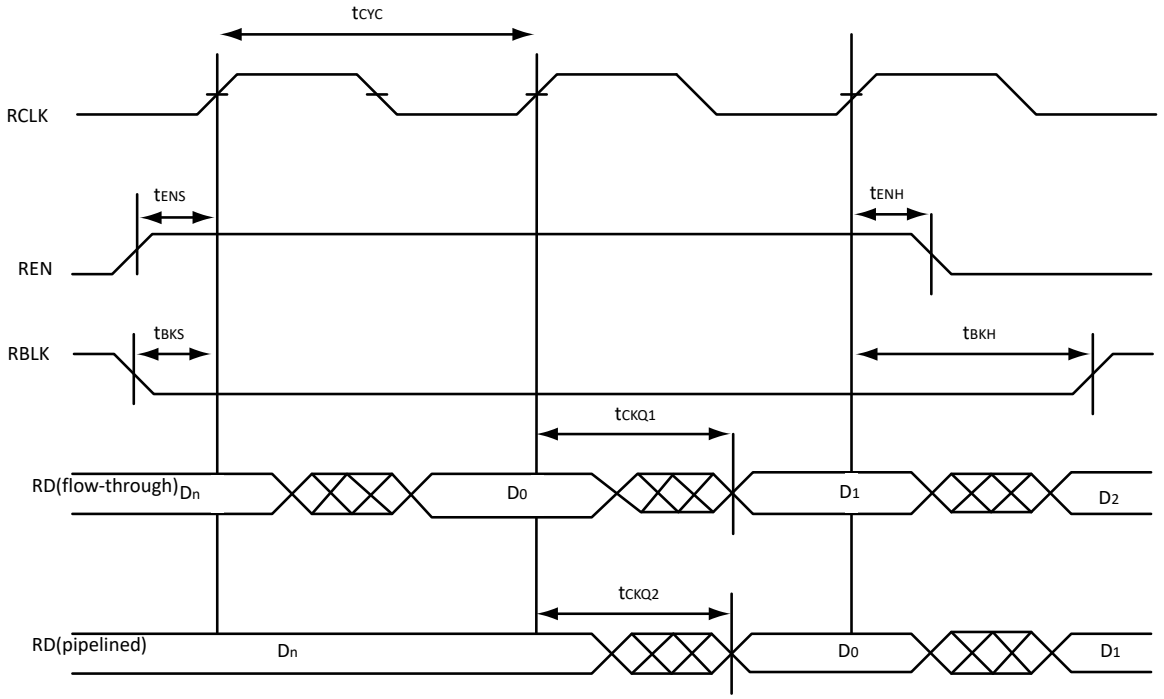



**Figure 11-9.** FIFO Write

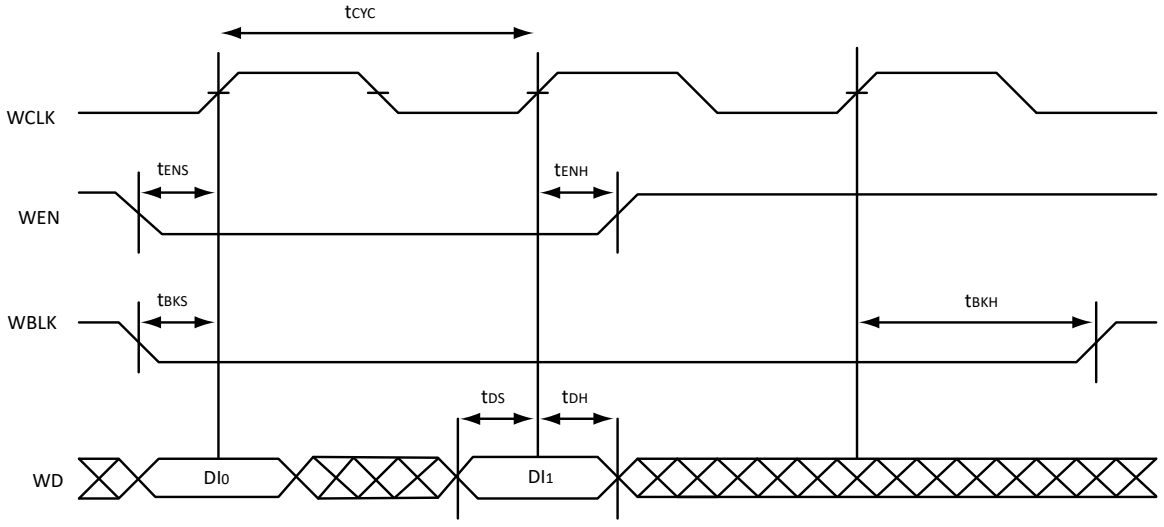


**Figure 11-10.** FIFO Reset

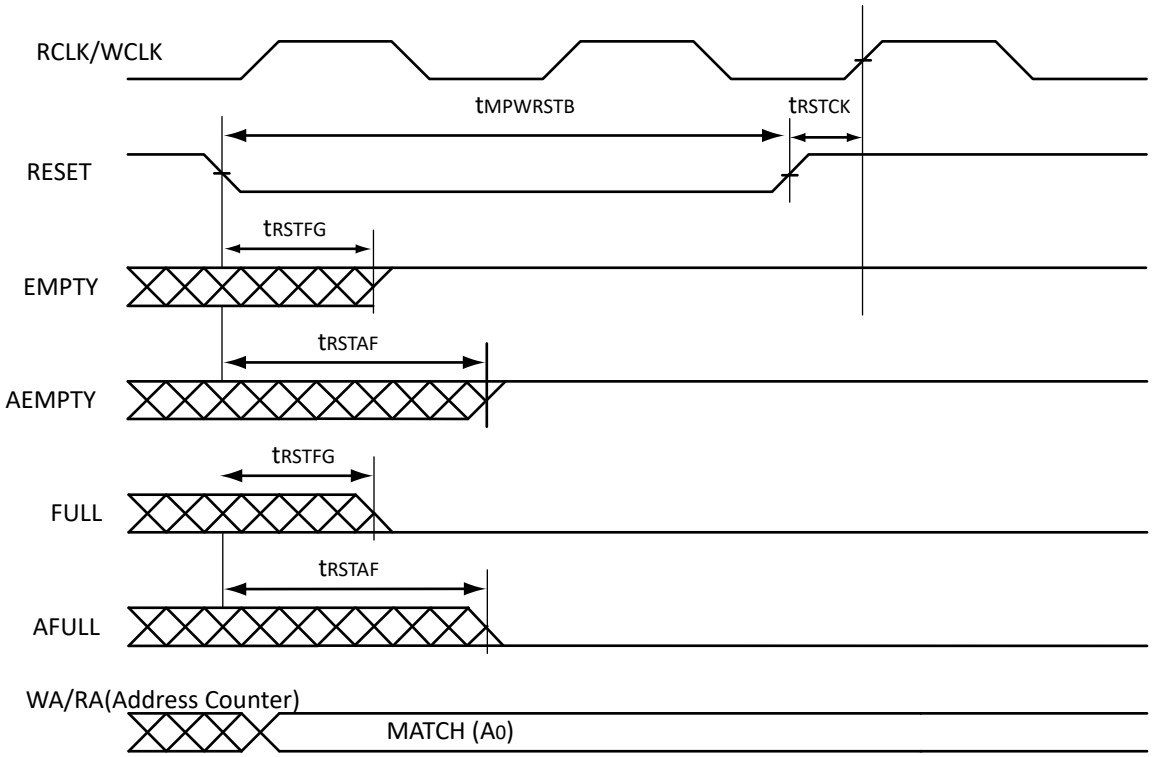



**Figure 11-11.** FIFO EMPTY Flag and AEMPTY Flag Assertion

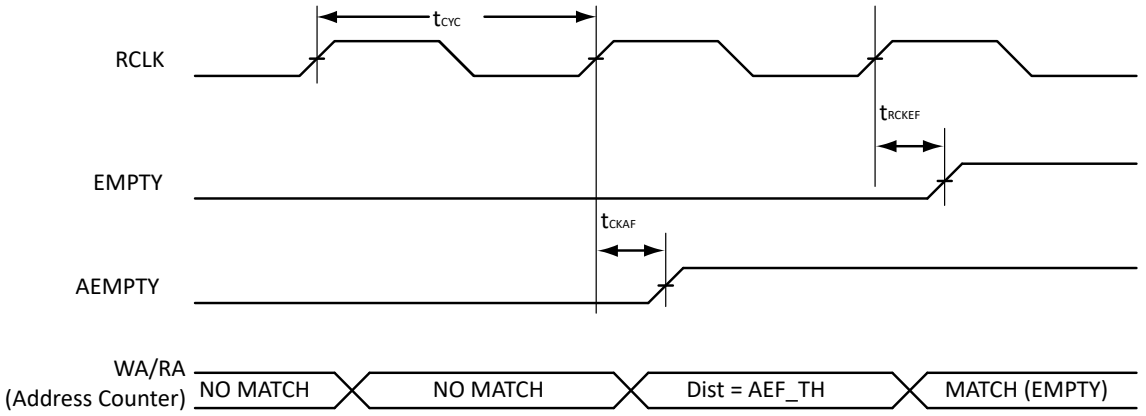


**Figure 11-12.** FIFO FULL Flag and AFULL Flag Assertion

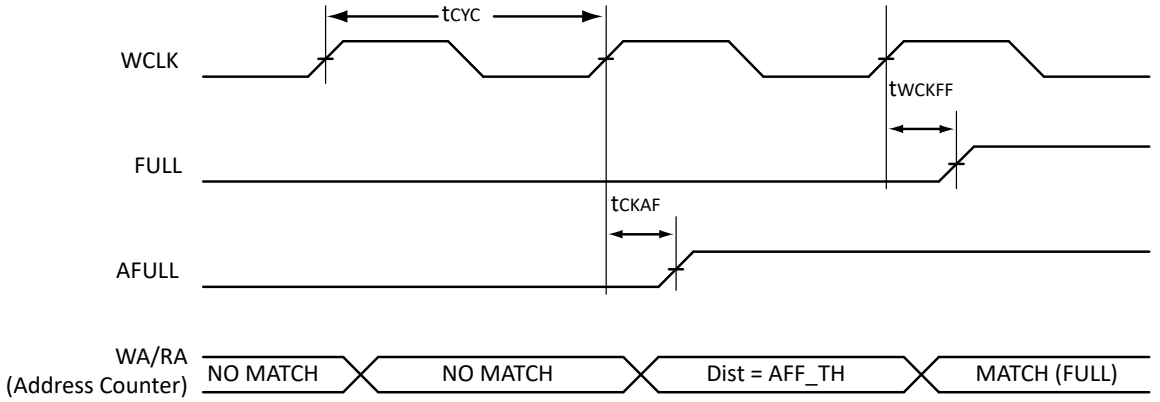



**Figure 11-13.** FIFO EMPTY Flag and AEMPTY Flag Deassertion

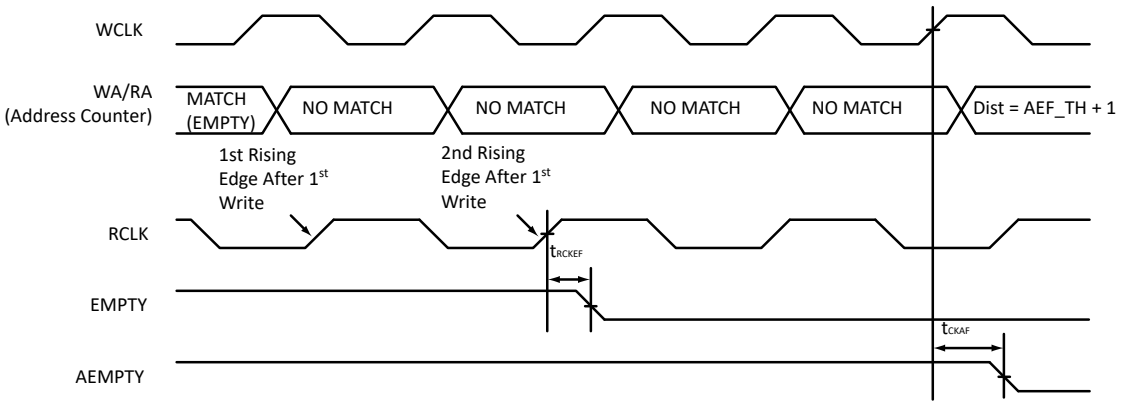
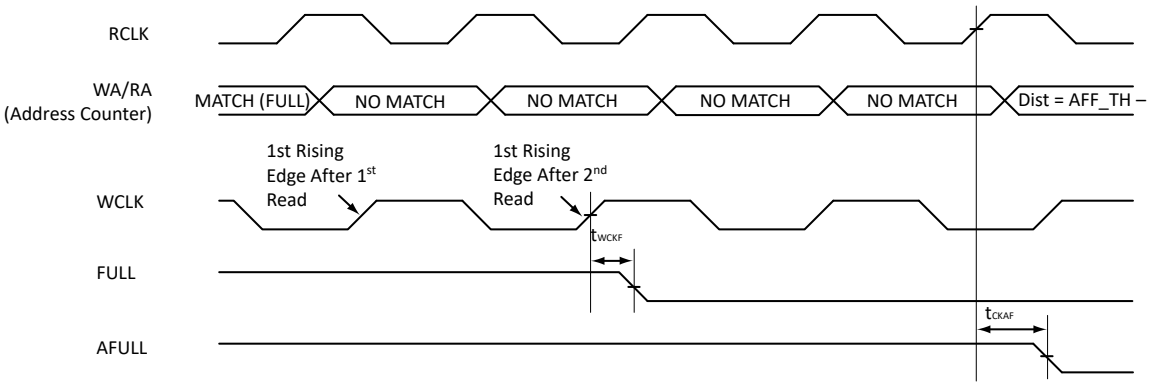



**Figure 11-14.** FIFO FULL Flag and AFULL Flag Deassertion




## Timing Characteristics

**Table 11-3.** FIFO Worst Commercial-Case Conditions: $T_J$ = 85 °C, VCC = 1.425V

| Parameter | Description | –1 | Std. | Units |
|---|---|---|---|---|
| $t_{ENS}$ | REN, WEN Setup Time | 1.40 | 1.68 | ns |
| $t_{ENH}$ | REN, WEN Hold Time | 0.02 | 0.02 | ns |
| $t_{BKS}$ | BLK Setup Time | 0.19 | 0.19 | ns |
| $t_{BKH}$ | BLK Hold Time | 0.00 | 0.00 | ns |
| $t_{DS}$ | Input Data (WD) Setup Time | 0.19 | 0.22 | ns |
| $t_{DH}$ | Input Data (WD) Hold Time | 0.00 | 0.00 | ns |
| $t_{CKQ1}$ | Clock High to New Data Valid on RD (flow-through) | 2.39 | 2.87 | ns |
| $t_{CKQ2}$ | Clock High to New Data Valid on RD (pipelined) | 0.91 | 1.09 | ns |
| $t_{RCKEF}$ | RCLK High to Empty Flag Valid | 1.74 | 2.09 | ns |
| $t_{WCKFF}$ | WCLK High to Full Flag Valid | 1.66 | 1.99 | ns |
| $t_{CKAF}$ | Clock HIGH to Almost Empty/Full Flag Valid | 6.29 | 7.54 | ns |
| $t_{RSTFG}$ | RESET Low to Empty/Full Flag Valid | 1.72 | 2.06 | ns |
| $t_{RSTAF}$ | RESET Low to Almost Empty/Full Flag Valid | 6.22 | 7.47 | ns |
| $t_{RSTBQ}$ | RESET Low to Data Out Low on RD (flow-through) | 0.94 | 1.12 | ns |
| | RESET Low to Data Out Low on RD (pipelined) | 0.94 | 1.12 | ns |
| $t_{REMRSTB}$ | RESET Removal | 0.29 | 0.35 | ns |
| $t_{RECRSTB}$ | RESET Recovery | 1.52 | 1.83 | ns |
| $t_{MPWRSTB}$ | RESET Minimum Pulse Width | 0.22 | 0.22 | ns |
| $t_{CYC}$ | Clock Cycle Time | 3.28 | 3.28 | ns |
| $F_{MAX}$ | Maximum Frequency for FIFO | 305 | 305 | MHz |

**Note:** For specific junction temperature and voltage supply levels, refer to Table 3-7 for derating values.

# 12. Embedded Nonvolatile Memory Block (eNVM) (Ask a Question)

## 12.1 Electrical Characteristics (Ask a Question)

The following table describes the eNVM maximum performance.

**Table 12-1.** eNVM Block Timing, Worst Commercial Case Conditions: $T_J$ = 85 °C, VCC = 1.425V

| Parameter | Description | A2F060 [1] | | A2F200 | | A2F500 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | –1 | Std. | –1 | Std. | –1 | Std. | |
| $t_{FMAXCLKeNVM}$ | Maximum frequency for clock for the control logic – 5 cycles (5:1:1:1 [2]) | 50 | 50 | 50 | 50 | 50 | 50 | MHz |
| $t_{FMAXCLKeNVM}$ | Maximum frequency for clock for the control logic – 6 cycles (6:1:1:1 [3]) | 100 | 80 | 100 | 80 | 100 | 80 | MHz |

**Notes:**

1. Part No A2F060 is discontinued.
2. 6:1:1:1 indicates 6 cycles for the first access and 1 each for the next three accesses. 5:1:1:1 indicates 5 cycles for the first access and 1 each for the next three accesses.
3. Moving from 5:1:1:1 mode to 6:1:1:1 mode results in throughput change that is dependent on the system functionality. When the Cortex-M3 code is executed from eNVM - with sequential firmware (sequential address reads), the throughput reduction can be around 10%.

# 13. Embedded FlashROM (eFROM) (Ask a Question)

## 13.1 Electrical Characteristics (Ask a Question)

The following table describes the eFROM maximum performance

**Table 13-1.** FlashROM Access Time, Worse Commercial Case Conditions: $T_J$ = 85 °C, VCC = 1.425V

| Parameter | Description | –1 | Std. | Units |
|---|---|---|---|---|
| $t_{CK2Q}$ | Clock to out per configuration* | 28.68 | 32.98 | ns |
| $F_{max}$ | Maximum Clock frequency | 15.00 | 15.00 | MHz |

# 14. JTAG 1532 Characteristics (Ask a Question)

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the 5. User I/O Characteristics for more details.

## Timing Characteristics

**Table 14-1.** JTAG 1532 Worst Commercial-Case Conditions: $T_J$ = 85 °C, Worst-Case VCC = 1.425V

| Parameter | Description | –1 | Std. | Units |
|---|---|---|---|---|
| $t_{DISU}$ | Test Data Input Setup Time | 0.67 | 0.77 | ns |
| $t_{DIHD}$ | Test Data Input Hold Time | 1.33 | 1.53 | ns |
| $t_{TMSSU}$ | Test Mode Select Setup Time | 0.67 | 0.77 | ns |
| $t_{TMDHD}$ | Test Mode Select Hold Time | 1.33 | 1.53 | ns |
| $t_{TCK2Q}$ | Clock to Q (data out) | 8.00 | 9.20 | ns |
| $t_{RSTB2Q}$ | Reset to Q (data out) | 26.67 | 30.67 | ns |
| $F_{TCKMAX}$ | TCK Maximum Frequency | 19.00 | 21.85 | MHz |
| $t_{TRSTREM}$ | ResetB Removal Time | 0.00 | 0.00 | ns |
| $t_{TRSTREC}$ | ResetB Recovery Time | 0.27 | 0.31 | ns |
| $t_{TRSTMPW}$ | ResetB Minimum Pulse | TBD | TBD | ns |

**Note:** For specific junction temperature and voltage supply levels, refer to Table 3-7 for derating values.

# 15. Programmable Analog Specifications (Ask a Question)

## 15.1 Current Monitor (Ask a Question)

Unless otherwise noted, current monitor performance is specified at 25 °C with nominal power supply voltages, with the output measured using the internal voltage reference with the internal ADC in 12-bit mode and 91 Ksps, after digital compensation. All results are based on averaging over 16 samples.

**Table 15-1.** Current Monitor Performance Specification

| Specification | Test Conditions | Min. | Typical | Max. | Units |
|---|---|---|---|---|---|
| Input voltage range (for driving ADC over full range) | — | 0–48 | 0–50 | 1–51 | mV |
| Analog gain | From the differential voltage across the input pads to the ADC input | — | 50 | — | V/V |
| Input referred offset voltage | Input referred offset voltage | 0 | 0.1 | 0.5 | mV |
| | –40 °C to +100 °C | 0 | 0.1 | 0.5 | mV |
| Gain error | Slope of BFSL vs. 50 V/V | — | ±0.1 | ±0.5 | % nom. |
| | –40 °C to +100 °C | — | — | ±0.5 | % nom. |
| Overall Accuracy | Peak error from ideal transfer function, 25 °C | — | ±(0.1 +0.25%) | ±(0.4 +1.5%) | mV plus % reading |
| Input referred noise | 0 VDC input (no output averaging) | 0.3 | 0.4 | 0.5 | mVrms |
| Common-mode rejection ratio | 0V to 12 VDC common-mode voltage | –86 | –87 | — | dB |
| Analog settling time | To 0.1% of final value (with ADC load) | — | | | |
| | From CM_STB (High) | 5 | — | — | µs |
| | From ADC_START (High) | 5 | — | 200 | µs |
| Input capacitance | — | — | 8 | — | pF |
| Input biased current | CM[n] or TM[n] pad, –40 °C to +100 °C over maximum input voltage range (plus is into pad) | — | — | — | — |
| | Strobe = 0; IBIAS on CM[n] | — | 0 | — | µA |
| | Strobe = 1; IBIAS on CM[n] | — | 1 | — | µA |
| | Strobe = 0; IBIAS on TM[n] | — | 2 | — | µA |
| | Strobe = 1; IBIAS on TM[n] | — | 1 | — | µA |
| Power supply rejection ratio | DC (0 – 10 KHz) | 41 | 42 | — | dB |
| Incremental operational current monitor power supply current requirements (per current monitor instance, not including ADC or VAREFx) | VCC33A | — | 150 | — | µA |
| | VCC33AP | — | 140 | — | µA |
| | VCC15A | — | 50 | — | µA |

**Note:** Under no condition should the TM pad ever be greater than 10 mV above the CM pad. This restriction is applicable only if current monitor is used.

## 15.2 Temperature Monitor (Ask a Question)

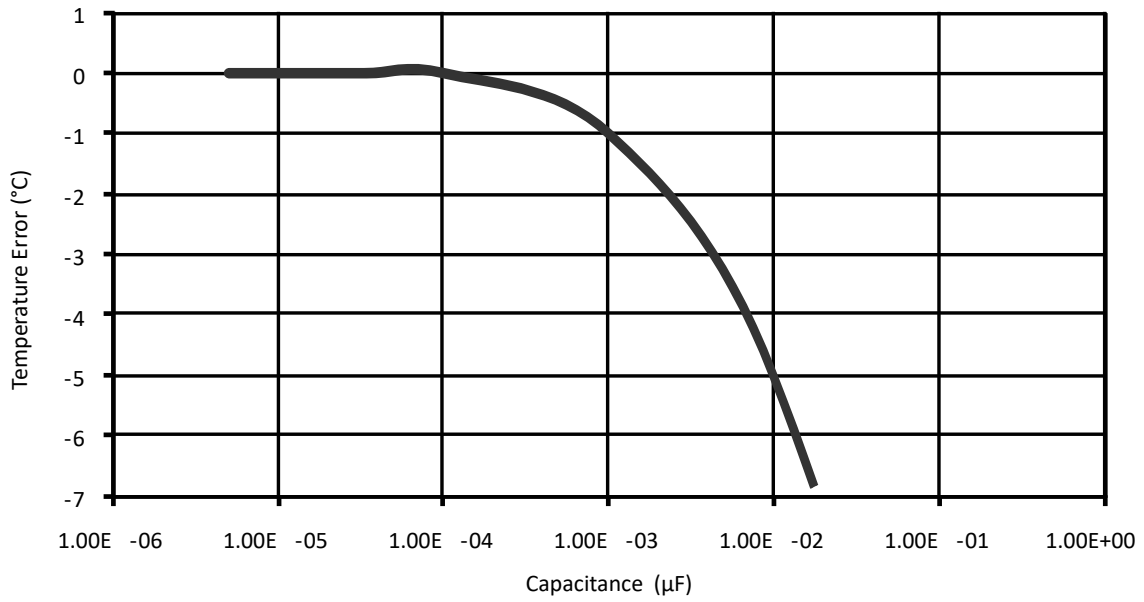
Unless otherwise noted, temperature monitor performance is specified with a 2N3904 diode-connected bipolar transistor from National Semiconductor or Infineon Technologies, nominal power supply voltages, with the output measured using the internal voltage reference with the internal ADC in 12-bit mode and 62.5 Ksps. After digital compensation. Unless otherwise noted, the specifications pertain to conditions where the SmartFusion cSoC and the sensing diode are at the same temperature.

**Table 15-2.** Temperature Monitor Performance Specifications

| Specification | Test Conditions | Min. | Typical | Max. | Units |
|---|---|---|---|---|---|
| Input diode temperature range | — | –55 | — | 150 | °C |
| | — | 233.2 | — | 378.15 | K |
| Temperature sensitivity | — | — | 2.5 | — | mV/K |
| Intercept | Extrapolated to 0K | — | 0 | — | V |
| Input referred temperature offset error | At 25 °C (298.15K) | — | ±1 | 1.5 | °C |
| Gain error | Slope of BFSL vs. 2.5 mV/K | — | ±1 | 2.5 | % nom. |
| Overall accuracy | Peak error from ideal transfer function | — | ±2 | ±3 | °C |
| Input referred noise | At 25 °C (298.15K) – no output averaging | — | 4 | — | °C rms |
| Output current | Idle mode | — | 100 | — | µA |
| | Final measurement phases | — | 10 | — | µA |
| Analog settling time | Measured to 0.1% of final value, (with ADC load) | — | | | |
| | From TM_STB (High) | 5 | — | — | µs |
| | From ADC_START (High) | 5 | — | 105 | µs |
| AT parasitic capacitance | — | — | — | 500 | pF |
| Power supply rejection ratio | DC (0–10 KHz) | 1.2 | 0.7 | — | °C/V |
| Input referred temperature sensitivity error | Variation due to device temperature (–40 °C to +100 °C). External temperature sensor held constant. | — | 0.005 | 0.008 | °C/°C |
| Temperature monitor (TM) operational power supply current requirements (per temperature monitor instance, not including ADC or VAREFx) | VCC33A | — | 200 | — | µA |
| | VCC33AP | — | 150 | — | µA |
| | VCC15A | — | 50 | — | µA |

**Note:** All results are based on averaging over 64 samples.

**Figure 15-1.** Temperature Error Versus External Capacitance



## 15.3 Analog-to-Digital Converter (ADC) (Ask a Question)

Unless otherwise noted, ADC direct input performance is specified at 25 °C with nominal power supply voltages, with the output measured using the external voltage reference with the internal ADC in 12-bit mode and 500 KHz sampling frequency, after trimming and digital compensation.

**Table 15-3.** ADC Specifications

| Specification | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Input voltage range (for driving ADC over its full range) | — | — | 2.56 | — | V |
| Gain error | — | — | ±0.4 | ±0.7 | % |
| | –40 °C to +100 °C | — | ±0.4 | ±0.7 | % |
| Input referred offset voltage | — | — | ±1 | ±2 | mV |
| | –40 °C to +100 °C | — | ±1 | ±2 | — |
| Integral non-linearity (INL) | RMS deviation from BFSL | — | | | |
| | 12-bit mode | — | 1.71 | | LSB |
| | 10-bit mode | — | 0.60 | 1.00 | LSB |
| | 8-bit mode | — | 0.2 | 0.33 | LSB |
| Differential non-linearity (DNL) | 12-bit mode | — | 2.4 | | LSB |
| | 10-bit mode | — | 0.80 | 0.94 | LSB |
| | 8-bit mode | — | 0.2 | 0.23 | LSB |
| Signal to noise ratio | — | 62 | 64 | — | dB |
| Effective number of bits | –1 dBFS input | — | | | |
| (ENOB) $ENOB = \frac{SINAD - 1.76\ dB}{6.02\ dB/bit}$ EQ 10 | 12-bit mode 10 KHz | 9.9 | 10 | — | Bits |
| | 12-bit mode 100 KHz | 9.9 | 10 | — | Bits |
| | 10-bit mode 10 KHz | 9.5 | 9.6 | — | Bits |
| | 10-bit mode 100 KHz | 9.5 | 9.6 | — | Bits |
| | 8-bit mode 10 KHz | 7.8 | 7.9 | — | Bits |
| | 8-bit mode 100 KHz | 7.8 | 7.9 | — | Bits |
| Full power bandwidth | At –3 dB; –1 dBFS input | 300 | — | — | KHz |
| Analog settling time | To 0.1% of final value (with 1 KΩ source impedance and with ADC load) | — | 2 | — | µs |
| Input capacitance | Switched capacitance (ADC sample capacitor) | — | 12 | 15 | pF |
| | Cs: Static capacitance (Figure 15-2) | | | | |
| | CM[n] input | — | 5 | 7 | pF |
| | TM[n] input | — | 5 | 7 | pF |
| | ADC[n] input | — | 5 | 7 | pF |
| Input resistance | Rin: Series resistance (Figure 15-2) | — | 2 | — | KΩ |
| | Rsh: Shunt resistance, exclusive of switched capacitance effects (Figure 15-2) | 10 | — | — | MΩ |
| Input leakage current | –40 °C to +100 °C | — | 1 | — | µA |
| Power supply rejection ratio | DC | 44 | 53 | — | dB |
| ADC power supply operational current requirements | VCC33ADCx | — | — | 2.5 | mA |
| | VCC15A | — | — | 2 | mA |

**Note:** All 3.3V supplies are tied together and varied from 3.0V to 3.6V. 1.5V supplies are held constant.

## 15.4 Analog Bipolar Prescaler (ABPS) (Ask a Question)

With the ABPS set to its high range setting (GDEC = 00), a hypothetical input voltage in the range –15.36V to +15.36V is scaled and offset by the ABPS input amplifier to match the ADC full range

of 0V to 2.56V using a nominal gain of –0.08333 V/V. However, due to reliability considerations, the voltage applied to the ABPS input should never be outside the range of –11.5V to +14.4V, restricting the usable ADC input voltage to 2.238V to 0.080V and the corresponding 12-bit output codes to the range of 3581 to 128 (decimal), respectively.

Unless otherwise noted, ABPS performance is specified at 25 °C with nominal power supply voltages, with the output measured using the internal voltage reference with the internal ADC in 12-bit mode and 100 KHz sampling frequency, after trimming and digital compensation; and applies to all ranges.

**Table 15-4.** ABPS Performance Specifications

| Specification | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Input voltage range (for driving ADC over its full range) | GDEC[1:0] = 11 | — | ±2.56 | — | V |
| | GDEC[1:0] = 10 | — | ±5.12 | — | V |
| | GDEC[1:0] = 01 | — | ±10.24 | — | V |
| | GDEC[1:0] = 00 (limited by maximum rating) | — | See note 1 | — | V |
| Analog gain (from input pad to ADC input) | GDEC[1:0] = 11 | — | –0.5 | — | V/V |
| | GDEC[1:0] = 10 | — | –0.25 | — | V/V |
| | GDEC[1:0] = 01 | — | –0.125 | — | V/V |
| | GDEC[1:0] = 00 | — | –0.0833 | — | V/V |
| Gain error | | –2.8 | –0.4 | 0.7 | % |
| | –40 °C to +100 °C | –2.8 | –0.4 | 0.7 | % |
| Input referred offset voltage | GDEC[1:0] = 11 | –0.31 | –0.07 | 0.31 | % FS* |
| | –40 °C to +100 °C | –1.00 | — | 1.47 | % FS* |
| | GDEC[1:0] = 10 | –0.34 | –0.07 | 0.34 | % FS* |
| | –40 °C to +100 °C | –0.90 | — | 1.37 | % FS* |
| | GDEC[1:0] = 01 | –0.61 | –0.07 | 0.35 | % FS* |
| | –40 °C to +100 °C | –1.05 | — | 1.35 | % FS* |
| | GDEC[1:0] = 00 | –0.39 | –0.07 | 0.35 | % FS* |
| | –40 °C to +100 °C | –1.06 | — | 1.38 | % FS* |
| SINAD | — | 53 | 56 | — | dB |
| Non-linearity | RMS deviation from BFSL | — | — | 0.5 | % FS* |
| Effective number of bits (ENOB) $ENOB = \frac{SINAD - 1.76\ dB}{6.02\ dB/bit}$ *EQ 11* | GDEC[1:0] = 11 (±2.56 range), –1 dBFS input | — | — | — | — |
| | 12-bit mode 10 KHz | 8.6 | 9.1 | — | Bits |
| | 12-bit mode 100 KHz | 8.6 | 9.1 | — | Bits |
| | 10-bit mode 10 KHz | 8.5 | 8.9 | — | Bits |
| | 10-bit mode 100 KHz | 8.5 | 8.9 | — | Bits |
| | 8-bit mode 10 KHz | 7.7 | 7.8 | — | Bits |
| | 8-bit mode 100 KHz | 7.7 | 7.8 | — | Bits |
| Large-signal bandwidth | –1 dBFS input | — | 1 | — | MHz |
| Analog settling time | To 0.1% of final value (with ADC load) | — | — | 10 | µs |
| Input resistance | — | — | 1 | — | MΩ |
| Power supply rejection ratio | DC (0–1 KHz) | 38 | 40 | — | dB |
| ABPS power supply current requirements (not including ADC or VAREFx) | ABPS_EN = 1 (operational mode) | | | | |
| | VCC33A | — | 123 | 134 | µA |
| | VCC33AP | — | 89 | 94 | µA |
| | VCC15A | — | 1 | — | µA |

**Note:** *FS is full-scale error, defined as the difference between the actual value that triggers the transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error. Refer to the Analog-to-Digital Converter chapter of the SmartFusion Programmable Analog User's Guide for more information.

## 15.5 Comparator (Ask a Question)

Unless otherwise specified, performance is specified at 25 °C with nominal power supply voltages.

**Table 15-5.** Comparator Performance Specifications

| Specification | Test Conditions | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Input voltage range | Minimum | | — | 0 | — | V |
| | Maximum | | — | 2.56 | — | V |
| Input offset voltage | HYS[1:0] = 00 (no hysteresis) | | — | ±1 | ±3 | mV |
| Input bias current | Comparator 1, 3, 5, 7, 9 (measured at 2.56V) | | — | 40 | 100 | nA |
| | Comparator 0, 2, 4, 6, 8 (measured at 2.56V) | | — | 150 | 300 | nA |
| Input resistance | — | | 10 | — | — | MΩ |
| Power supply rejection ratio | DC (0 – 10 KHz) | | 50 | 60 | — | dB |
| Propagation delay | 100 mV overdrive | | — | — | — | — |
| | HYS[1:0] = 00 | | — | — | — | — |
| | (no hysteresis) | | — | 15 | 18 | ns |
| | 100 mV overdrive | | — | — | — | — |
| | HYS[1:0] = 10 | | — | — | — | — |
| | (with hysteresis) | | — | 25 | 30 | ns |
| Hysteresis (± refers to rising and falling threshold shifts, respectively) | HYS[1:0] = 00 | Typical (25 °C) | 0 | 0 | ±5 | mV |
| | | Across all corners (–40 °C to +100 °C) | 0 | — | ±5 | mV |
| | HYS[1:0] = 01 | Typical (25 °C) | ±3 | ± 16 | ±30 | mV |
| | | Across all corners (–40 °C to +100 °C) | 0 | — | ±36 | mV |
| | HYS[1:0] = 10 | Typical (25 °C) | ±19 | ± 31 | ±48 | mV |
| | | Across all corners (–40 °C to +100 °C) | ±12 | — | ±54 | mV |
| | HYS[1:0] = 11 | Typical (25 °C) | ±80 | ± 105 | ±190 | mV |
| | | Across all corners (–40 °C to +100 °C) | ±80 | — | ±194 | mV |
| Comparator current requirements (per comparator) | VCC33A = 3.3V (operational mode); COMP_EN = 1 | | | | | |
| | VCC33A | | — | 150 | 165 | µA |
| | VCC33AP | | — | 140 | 165 | µA |
| | VCC15A | | — | 1 | 3 | µA |

## 15.6 Analog Sigma-Delta Digital to Analog Converter (DAC) (Ask a Question)

Unless otherwise noted, sigma-delta DAC performance is specified at 25 °C with nominal power supply voltages, using the internal sigma-delta modulators with 16-bit inputs, HCLK = 100 MHz, modulator inputs updated at a 100 KHz rate, in voltage output mode with an external 160 pF capacitor to ground, after trimming and digital [pre-]compensation.

**Table 15-6.** Analog Sigma-Delta DAC

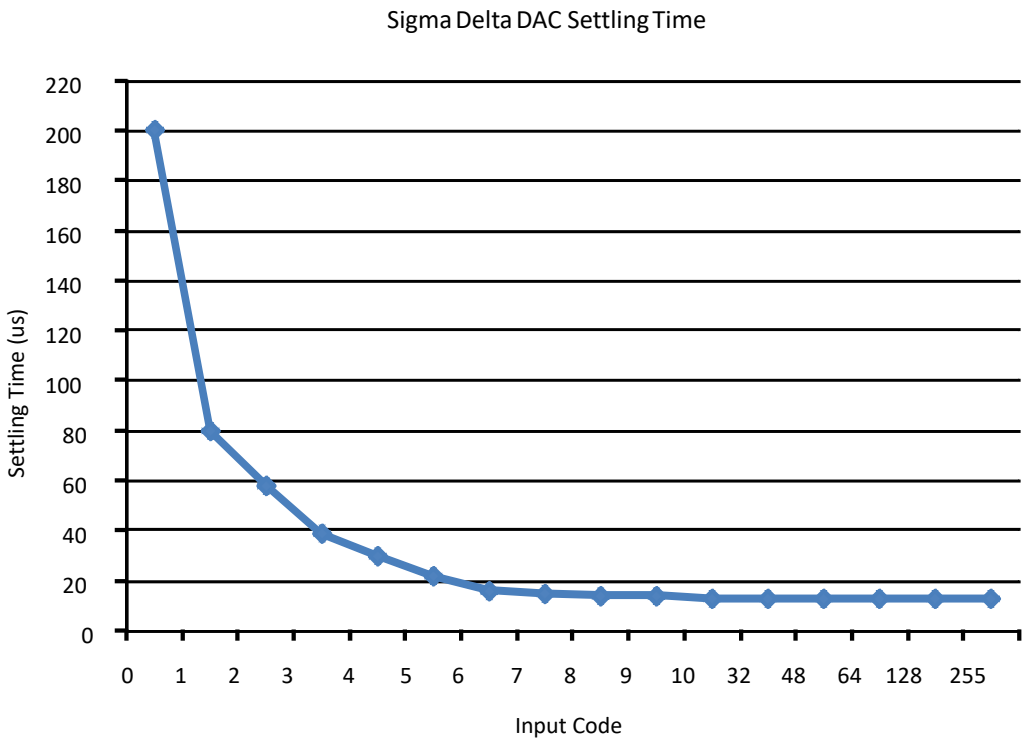
| Specification | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Resolution | — | 8 | — | 24 | Bits |
| Output range | — | — | 0 to 2.56 | — | V |
| | Current output mode | — | 0 to 256 | — | µA |

| .....continued | | | | | |
|---|---|---|---|---|---|
| **Specification** | **Test Conditions** | **Min.** | **Typ.** | **Max.** | **Units** |
| Output Impedance | — | 6 | 10 | 12 | KΩ |
| | Current output mode | 10 | — | — | MΩ |
| Output voltage compliance | Current output mode | — | 0–3.0 | — | V |
| | –40 °C to +100 °C | 0–2.7 | — | 0–3.4 | V |
| Gain error | Voltage output mode | — | 0.3 | ±2 | % |
| | A2F060: –40 °C to +100 °C | — | 0.3 | ±2 | % |
| | A2F200: –40 °C to +100 °C | — | 1.2 | ±5.3 | % |
| | A2F500: –40 °C to +100 °C | — | 0.3 | ±2 | % |
| | Current output mode | — | 0.3 | ±2 | % |
| | A2F060: –40 °C to +100 °C | — | 0.3 | ±2 | % |
| | A2F200: –40 °C to +100 °C | — | 1.2 | ±5.3 | % |
| | A2F500: –40 °C to +100 °C | — | 0.3 | ±2 | % |
| Output referred offset | DACBYTE0 = h'00 (8-bit) | — | 0.25 | ±1 | mV |
| | –40 °C to +100 °C | — | 1 | ±2.5 | mV |
| | Current output mode | — | 0.3 | ±1 | µA |
| | –40 °C to +100 °C | — | 1 | ±2.5 | µA |
| Integral non-linearity | RMS deviation from BFSL | — | 0.1 | 0.3 | % FS[1] |
| Differential non-linearity | — | — | 0.05 | 0.4 | % FS[1] |
| Analog settling time | — | — | Refer to Figure 15-2 | — | µs |
| Power supply rejection ratio | DC, full scale output | 33 | 34 | — | dB |
| Sigma-delta DAC power supply current requirements (not including VAREFx) | Input = 0, EN = 1 (operational mode) | — | — | — | — |
| | VCC33SDDx | | 30 | 35 | µA |
| | VCC15A | | 3 | 5 | µA |
| | Input = Half scale, EN = 1 (operational mode) | — | — | — | — |
| | VCC33SDDx | — | 160 | 165 | µA |
| | VCC15A | — | 33 | 35 | µA |
| | Input = Full scale, EN = 1 (operational mode) | — | — | — | — |
| | VCC33SDDx | — | 280 | 285 | µA |
| | VCC15A | — | 70 | 75 | µA |

**Note:**

1. FS is full-scale error, defined as the difference between the actual value that triggers the transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error. Refer to the Analog-to-Digital Converter chapter of the SmartFusion Programmable Analog User's Guide for more information.

**Figure 15-2.** Sigma-Delta DAC Setting Time




## 15.7 Voltage Regulator (Ask a Question)

**Table 15-7.** Voltage Regulator

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{OUT}$ | Output voltage | $T_J$ = 25 °C | — | 1.425 | 1.5 | 1.575 | V |
| $V_{OS}$ | Output offset voltage | $T_J$ = 25 °C | — | — | 11 | — | mV |
| ICC33A | Operation current | $T_J$ = 25 °C | $I_{LOAD}$ = 1 mA | — | 3.4 | — | mA |
| | | | $I_{LOAD}$ = 100 mA | — | 11 | — | mA |
| | | | $I_{LOAD}$ = 0.5A | — | 21 | — | mA |
| $\Delta V_{OUT}$ | Load regulation | $T_J$ = 25 °C | $I_{LOAD}$ = 1 mA to 0.5 A | — | 5.8 | — | mV |
| $\Delta V_{OUT}$ | Line regulation | $T_J$ = 25 °C | VCC33A = 2.97V to 3.63V<br>$I_{LOAD}$ = 1 mA | — | 5.3 | — | mV/V |
| | | | VCC33A = 2.97V to 3.63V<br>$I_{LOAD}$ = 100 mA | — | 5.3 | — | mV/V |
| | | | VCC33A = 2.97V to 3.63V<br>$I_{LOAD}$ = 500mA | — | 5.3 | — | mV/V |
| | Dropout voltage [1] | $T_J$ = 25 °C | $I_{LOAD}$ = 1 mA | — | 0.63 | — | V |
| | | | $I_{LOAD}$ = 100 mA | — | 0.84 | — | V |
| | | | $I_{LOAD}$ = 0.5A | — | 1.35 | — | V |
| $I_{PTBASE}$ | PTBase current | $T_J$ = 25 °C | $I_{LOAD}$ = 1 mA | — | 48 | — | µA |
| | | | $I_{LOAD}$ = 100 mA | — | 736 | — | µA |
| | | | $I_{LOAD}$ = 0.5A | — | 12 | — | mA |
| — | Startup time[2] | $T_J$ = 25 °C | — | — | 200 | — | µs |

**Notes:**

1. Dropout voltage is defined as the minimum VCC33A voltage. The parameter is specified with respect to the output voltage. The specification represents the minimum input-to-output differential voltage required to maintain regulation.
2. Assumes 10 µF.

**Figure 15-3.** Typical Output Voltage

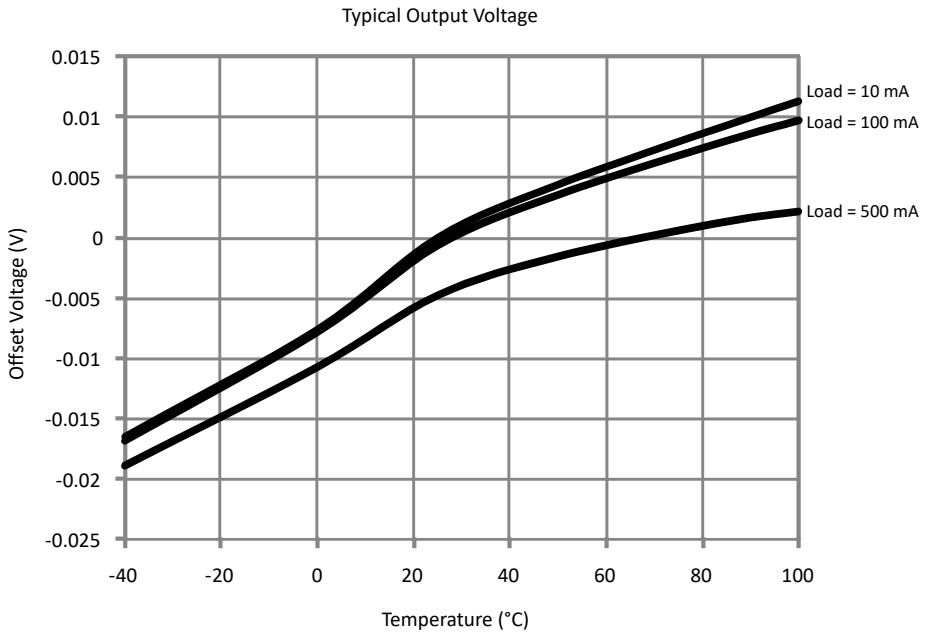
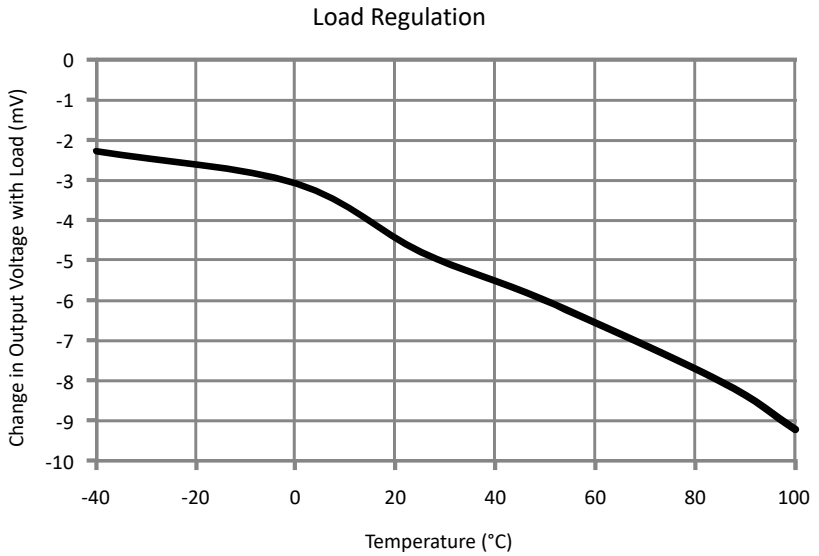



**Figure 15-4.** Load Regulation



# 16. Serial Peripheral Interface (SPI) Characteristics (Ask a Question)

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_x_CLK. For timing parameter definitions, refer to Figure 16-1.

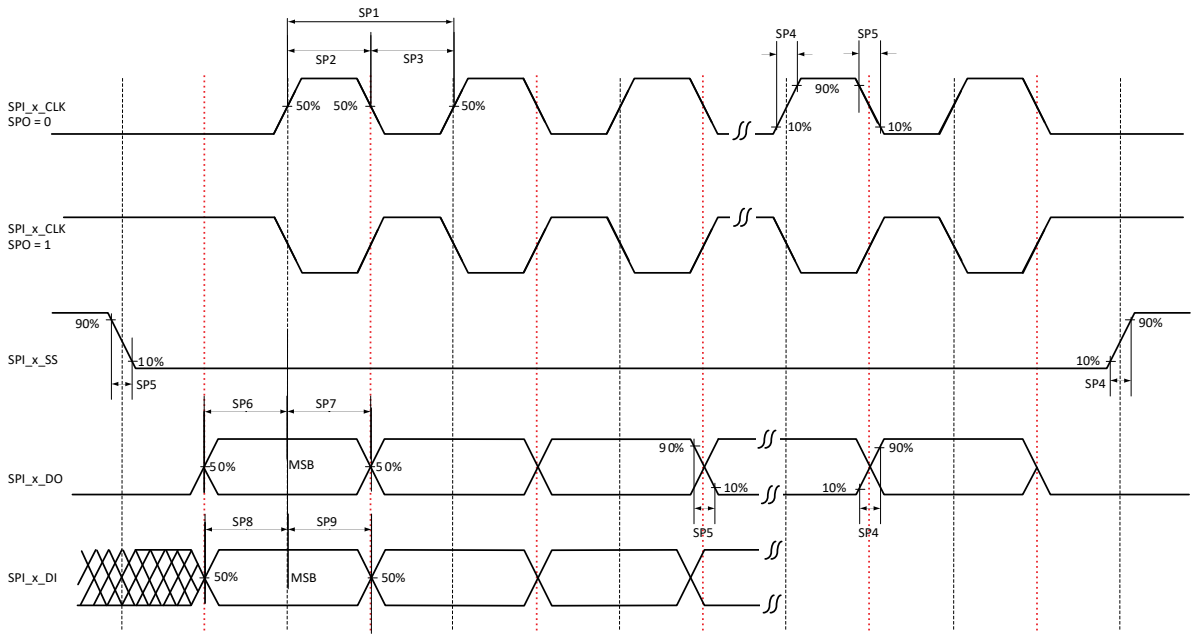
**Table 16-1.** SPI Characteristics —Commercial Case Conditions: $T_J$ = 85 °C, VDD = 1.425V, –1 Speed Grade

| Symbol | Description and Condition | A2F060[1] | A2F200 | A2F500 | Unit |
|---|---|---|---|---|---|
| sp1 | SPI_x_CLK minimum period | | | | |
| | SPI_x_CLK = PCLK/2 | 20 | NA | 20 | ns |
| | SPI_x_CLK = PCLK/4 | 40 | 40 | 40 | ns |
| | SPI_x_CLK = PCLK/8 | 80 | 80 | 80 | ns |
| | SPI_x_CLK = PCLK/16 | 0.16 | 0.16 | 0.16 | µs |
| | SPI_x_CLK = PCLK/32 | 0.32 | 0.32 | 0.32 | µs |
| | SPI_x_CLK = PCLK/64 | 0.64 | 0.64 | 0.64 | µs |
| | SPI_x_CLK = PCLK/128 | 1.28 | 1.28 | 1.28 | µs |
| | SPI_x_CLK = PCLK/256 | 2.56 | 2.56 | 2.56 | µs |
| sp2 | SPI_x_CLK minimum pulse width high | | | | |
| | SPI_x_CLK = PCLK/2 | 10 | NA | 10 | ns |
| | SPI_x_CLK = PCLK/4 | 20 | 20 | 20 | ns |
| | SPI_x_CLK = PCLK/8 | 40 | 40 | 40 | ns |
| | SPI_x_CLK = PCLK/16 | 0.08 | 0.08 | 0.08 | µs |
| | SPI_x_CLK = PCLK/32 | 0.16 | 0.16 | 0.16 | µs |
| | SPI_x_CLK = PCLK/64 | 0.32 | 0.32 | 0.32 | µs |
| | SPI_x_CLK = PCLK/128 | 0.64 | 0.64 | 0.64 | µs |
| | SPI_x_CLK = PCLK/256 | 1.28 | 1.28 | 1.28 | us |
| sp3 | SPI_x_CLK minimum pulse width low | | | | |
| | SPI_x_CLK = PCLK/2 | 10 | NA | 10 | ns |
| | SPI_x_CLK = PCLK/4 | 20 | 20 | 20 | ns |
| | SPI_x_CLK = PCLK/8 | 40 | 40 | 40 | ns |
| | SPI_x_CLK = PCLK/16 | 0.08 | 0.08 | 0.08 | µs |
| | SPI_x_CLK = PCLK/32 | 0.16 | 0.16 | 0.16 | µs |
| | SPI_x_CLK = PCLK/64 | 0.32 | 0.32 | 0.32 | µs |
| | SPI_x_CLK = PCLK/128 | 0.64 | 0.64 | 0.64 | µs |
| | SPI_x_CLK = PCLK/256 | 1.28 | 1.28 | 1.28 | µs |
| sp4 | SPI_x_CLK, SPI_x_DO, SPI_x_SS rise time (10%-90%) [2] | 4.7 | 4.7 | 4.7 | ns |
| sp5 | SPI_x_CLK, SPI_x_DO, SPI_x_SS fall time (10%-90%) [2] | 3.4 | 3.4 | 3.4 | ns |
| sp6 | Data from master (SPI_x_DO) setup time [3] | (SPI_x_CLK_period/2) – 4.0 | | | ns |
| sp7 | Data from master (SPI_x_DO) hold time [3] | (SPI_x_CLK_period/2) – 4.0 | | | ns |
| sp8 | SPI_x_DI setup time [3] | 10.4 (load of 20 pF)<br>11.2 (load of 35 pF) | | | ns |
| sp9 | SPI_x_DI hold time [3] | 2.5 | | | ns |

**Notes:**

1. Part No A2F060 is discontinued
2. These values are provided for a load of 35 pF. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microchip website: www.microchip.com/en-us/products/fpgas-and-plds/system-on-chip-fpgas/smartfusion-fpgas#ibis.
3. For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the SmartFusion Microcontroller Subsystem User's Guide.

**Figure 16-1.** SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)



# 17. Inter-Integrated Circuit ($I^2C$) Characteristics (Ask a Question)

This section describes the DC and switching of the $I^2C$ interface. Unless otherwise noted, all output characteristics given are for a 100 pF load on the pins. For timing parameter definitions, refer to Figure 17-1.

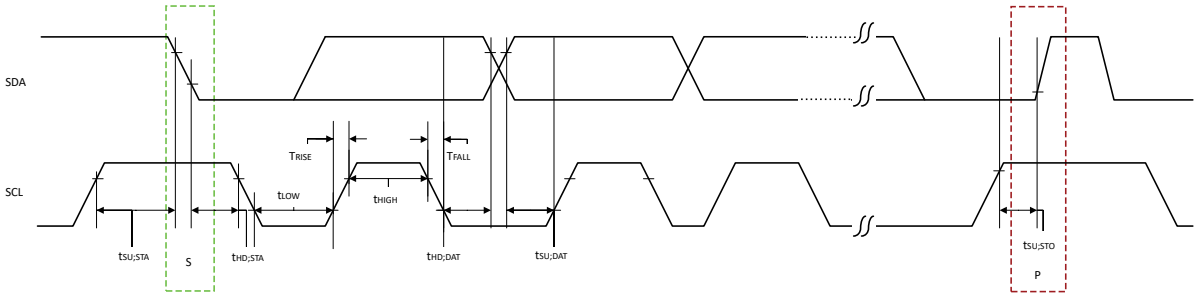
**Table 17-1.** $I^2C$ Characteristics Commercial Case Conditions: $T_J$ = 85 °C, VDD = 1.425V, –1 Speed Grade

| Parameter | Definition | Condition | Value | Unit |
|---|---|---|---|---|
| $V_{IL}$ | Minimum input low voltage | — | See Table 5-18 | — |
| | Maximum input low voltage | — | See Table 5-18 | — |
| $V_{IH}$ | Minimum input high voltage | — | See Table 5-18 | — |
| | Maximum input high voltage | — | See Table 5-18 | — |
| $V_{OL}$ | Maximum output voltage low | $I_{OL}$ = 8 mA | See Table 5-18 | — |
| $I_{IL}$ | Input current high | — | See Table 5-18 | — |
| $I_{IH}$ | Input current low | — | See Table 5-18 | — |
| $V_{hyst}$ | Hysteresis of Schmitt trigger inputs | — | See Table 5-15 | V |
| $T_{FALL}$ | Fall time[2] | VIHmin to VILMax, $C_{load}$ = 400 pF | 15.0 | ns |
| | | VIHmin to VILMax, $C_{load}$ = 100 pF | 4.0 | ns |
| $T_{RISE}$ | Rise time [2] | VILMax to VIHmin, $C_{load}$ = 400 pF | 19.5 | ns |
| | | VILMax to VIHmin, $C_{load}$ = 100 pF | 5.2 | ns |
| $C_{in}$ | Pin capacitance | VIN = 0, f = 1.0 MHz | 8.0 | pF |
| $R_{pull-up}$ | Output buffer maximum pull-down Resistance [1] | — | 50 | Ω |
| $R_{pull-down}$ | Output buffer maximum pull-up Resistance [1] | — | 150 | Ω |
| $D_{max}$ | Maximum data rate | Fast mode | 400 | Kbps |
| $t_{LOW}$ | Low period of I2C_x_SCL [3] | — | 1 | pclk cycles |
| $t_{HIGH}$ | High period of I2C_x_SCL [3] | — | 1 | pclk cycles |
| $t_{HD;STA}$ | START hold time [3] | — | 1 | pclk cycles |
| $t_{SU;STA}$ | START setup time [3] | — | 1 | pclk cycles |
| $t_{HD;DAT}$ | DATA hold time [3] | — | 1 | pclk cycles |
| $t_{SU;DAT}$ | DATA setup time [3] | — | 1 | pclk cycles |
| $t_{SU;STO}$ | STOP setup time [3] | — | 1 | pclk cycles |
| $t_{FILT}$ | Maximum spike width filtered | — | 50 | ns |

**Notes:**

1. These maximum values are provided for information only. Minimum output buffer resistance values depend on VCCxxxxIOBx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microchip website at www.microchip.com/en-us/products/fpgas-and-plds/system-on-chip-fpgas/smartfusion-fpgas#ibis.
2. These values are provided for a load of 100 pF and 400 pF. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microchip website at www.microchip.com/en-us/products/fpgas-and-plds/system-on-chip-fpgas/smartfusion-fpgas#ibis.
3. For allowable Pclk configurations, refer to the Inter-Integrated Circuit ($I^2C$) Peripherals section in the SmartFusion Microcontroller Subsystem User's Guide .

**Figure 17-1.** I²C Timing Parameter Definition



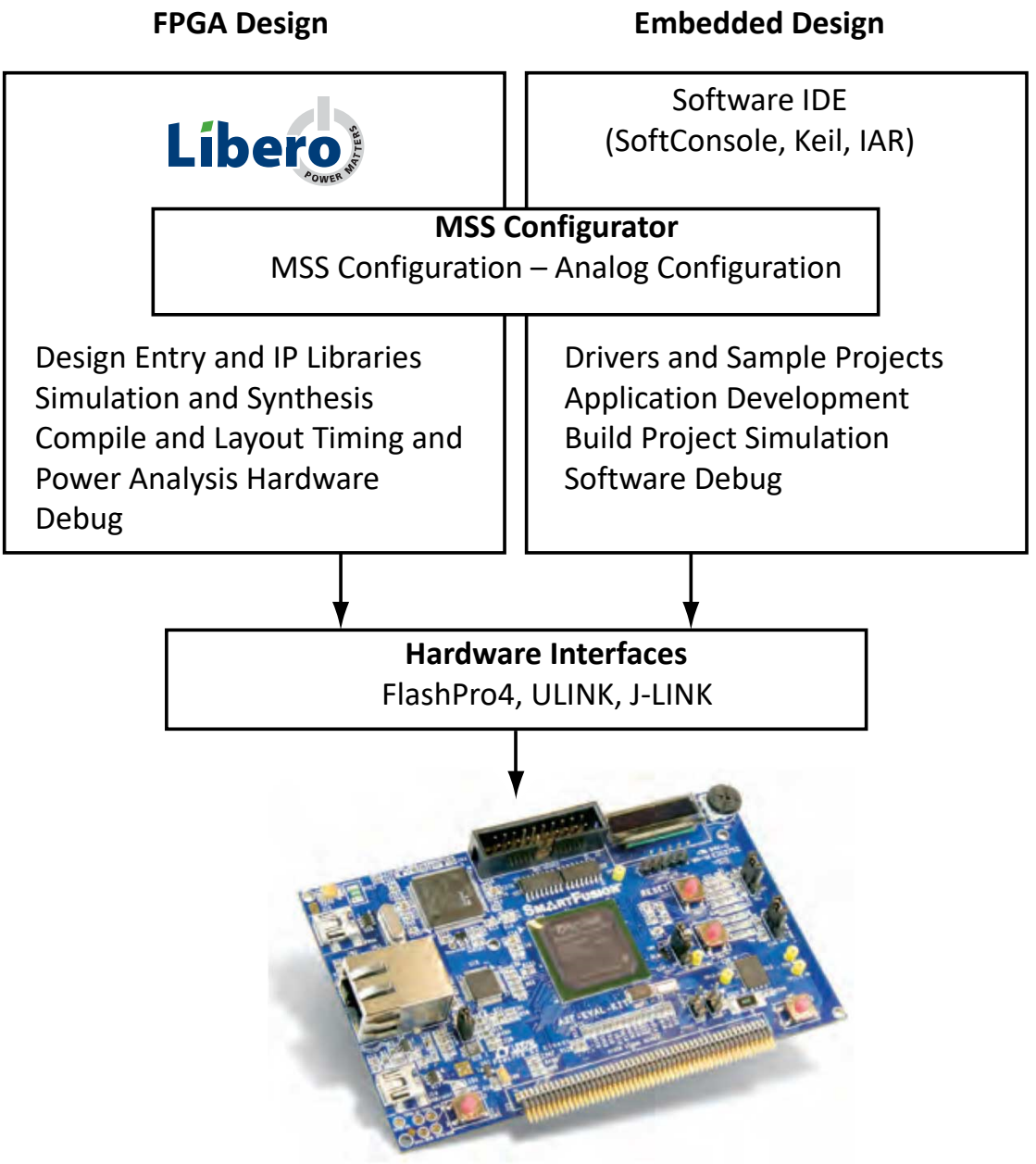
# 18. SmartFusion Development Tools (Ask a Question)

Designing with SmartFusion cSoCs involves three different types of design: FPGA design, embedded design and analog design. These roles can be filled by three different designers, two designers or even a single designer, depending on company structure and project complexity.

## 18.1 Types of Design Tools (Ask a Question)

Microchip has developed design tools and flows to meet the needs of these three types of designers so they can work together smoothly on a single project, as shown in the following figure.

**Figure 18-1.** Three Design Roles



### 18.1.1 FPGA Design (Ask a Question)

Libero System-on-Chip (SoC) software is Microchip's comprehensive software toolset for designing with all Microchip FPGAs and cSoCs. Libero® SoC includes industry-leading synthesis, simulation and debug tools from Synopsys® and Mentor Graphics®, as well as innovative timing and power optimization and analysis.

### 18.1.2 Embedded Design (Ask a Question)

Microchip offers free SoftConsole Eclipse based IDE, which includes the GNU C/C++ compiler and GDB debugger. Microchip also offers evaluation versions of software from Keil and IAR, with full versions available from respective suppliers.

### 18.1.3 Analog Design (Ask a Question)

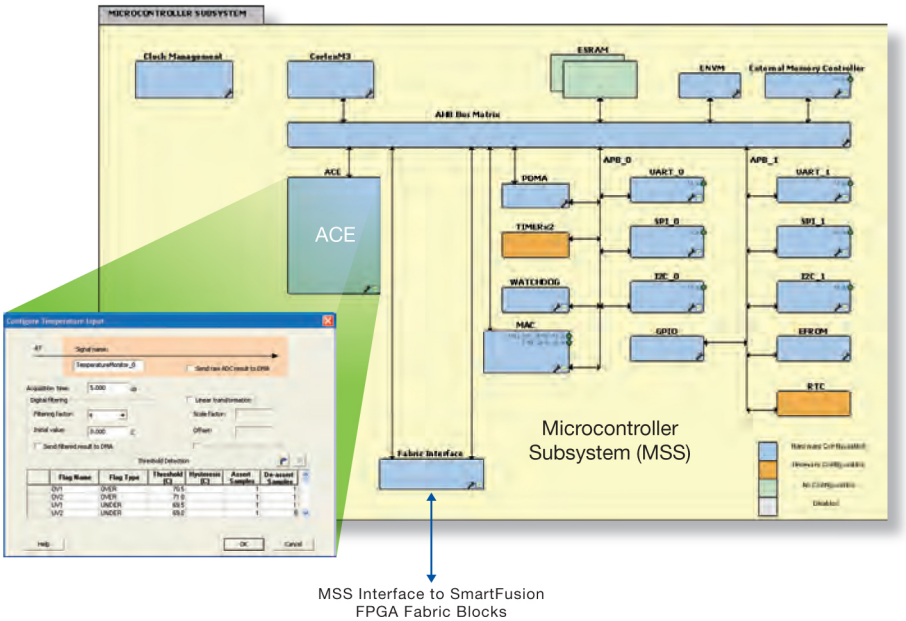
The MSS configurator provides graphical configuration for current, voltage and temperature monitors, sample sequencing setup and post-processing configuration, and DAC output.

The MSS configurator creates a bridge between the FPGA fabric and embedded designers so device configuration can be easily shared between multiple developers.

The MSS configurator includes the following:

- A simple configurator for the embedded designer to control the MSS peripherals and I/Os
- A method to import and view a hardware configuration from the FPGA flow into the embedded flow containing the memory map
- Automatic generation of drivers for any peripherals or soft IP used in the system configuration
- Comprehensive analog configuration for the programmable analog components
- Creation of a standard MSS block to be used in SmartDesign for connection of FPGA fabric designs and IP

**Figure 18-2.** MSS Configurator




## 18.2 SmartFusion Ecosystem (Ask a Question)

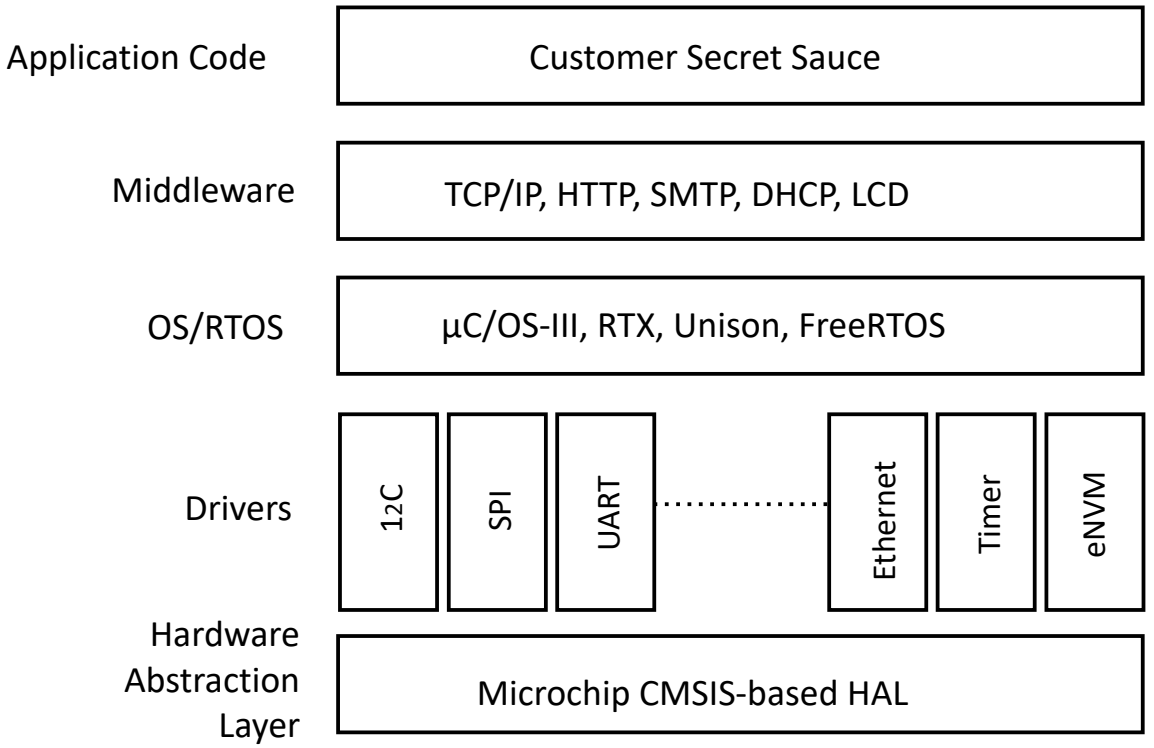
The Microchip SoC Products Group has a long history of supplying comprehensive FPGA development tools and recognizes the benefit of partnering with industry leaders to deliver the optimum usability and productivity to customers. Taking the same approach with processor

development, Microchip has partnered with key industry leaders in the microcontroller space to provide the robust SmartFusion ecosystem.

Microchip is partnering with Keil and IAR to provide Software IDE support to SmartFusion system designers. The result is a robust solution that can be easily adopted by developers who are already doing embedded design. The learning path is straightforward for FPGA designers.

Support for the SoC Products Group device and ecosystem resources is represented in the following figure.

**Figure 18-3.** SmartFusion Ecosystem




The preceding figure shows the SmartFusion stack with examples of drivers, RTOS, and middleware from Microchip and partners. By leveraging the SmartFusion stack, designers can decide at which level to add their own customization to their design, thus speeding time to market and reducing overhead in the design.

### 18.2.1 ARM (Ask a Question)

Because an ARM processor was chosen for SmartFusion cSoCs, Microchip's customers can benefit from the extensive ARM ecosystem. By building on Microchip supplied hardware abstraction layer (HAL) and drivers, third party vendors can easily port RTOS and middleware for the SmartFusion cSoC.

- ARM Cortex-M Series Processors
- ARM Cortex-M3 Processor Resource
- ARM Cortex-M3 Technical Reference Manual
- ARM Cortex-M3 Processor Software Development for ARM7TDMI Processor Programmers White Paper

### Compile and Debug

Microchip's SoftConsole is a free Eclipse-based IDE that enables the rapid production of C and C++ executables for Microchip FPGA and cSoCs using Cortex-M3, Cortex-M1 and Core8051s. For SmartFusion support, SoftConsole includes the GNU C/C++ compiler and GDB debugger. Additional examples can be found on the SoftConsole page:

- Using UART with SmartFusion: SoftConsole Standalone Flow Tutorial
  - Design Files
- Displaying POT Level with LEDs: Libero SoC and SoftConsole Flow Tutorial for SmartFusion
  - Design Files

IAR Embedded Workbench® for ARM/Cortex is an integrated development environment for building and debugging embedded ARM applications using assembler, C and C++. It includes a project manager, editor, build and debugger tools with support for RTOS-aware debugging on hardware or in a simulator.

- Designing SmartFusion cSoC with IAR Systems
- IAR Embedded Workbench IDE User Guide for ARM
- Download Evaluation or Kickstart version of IAR Embedded Workbench for ARM

Keil's Microcontroller Development Kit comes in two editions: MDK-ARM and MDK Basic. Both editions feature µVision®, the ARM Compiler, MicroLib, and RTX, but the MDK Basic edition is limited to 256K so that small applications are more affordable.

- Designing SmartFusion cSoC with Keil
- Using Keil µVision and Microchip SmartFusion cSoC
  - Programming file for use with this tutorial
- Keil Microcontroller Development Kit for ARM Product Manuals
- Download Evaluation version of Keil MDK-ARM

| CMSIS COMPLIANT ARM® Cortex™ Microcontroller Software Interface Standard | MICROCHIP | KEIL™ An ARM® Company | IAR SYSTEMS |
|---|---|---|---|
| Software IDE | SoftConsole® | Vision IDE | Embedded Workbench |
| Website | www.microchip.com/en-us/products/fpgas-and-plds/fpga-and-soc-design-tools/soc-fpga/softconsole | www.keil.com | www.iar.com |
| Free versions from SoC Products Group | Free with Libero® SoC | 32K code limited | 32K code limited |
| Available from Vendor | N/A | Full version | Full version |
| Compiler | GNU GCC | RealView C/C++ | IAR ARM Compiler |
| Debugger | GDB debug | Vision Debugger | C-SPY Debugger |
| Instruction Set Simulator | No | Vision Simulator | Yes |
| Debug Hardware | FlashPro4 | ULINK2 or ULINK-ME | J-LINK or J-LINK Lite |

## 18.2.2 Operating Systems (Ask a Question)

FreeRTOS™ is a portable, open source, royalty free, mini real-time kernel (a free-to-download and free-to-deploy RTOS that can be used in commercial applications without any requirement to expose your proprietary source code). FreeRTOS is scalable and designed specifically for small embedded systems. This FreeRTOS version ported by Microchip is 6.0.1. For more information, visit the FreeRTOS website: www.freertos.org

- SmartFusion Webserver Demo Using uIP and FreeRTOS
- SmartFusion cSoC: Running Webserver, TFTP on lwIP TCP/IP Stack Application Note

Emcraft Systems provides porting of the open-source U-boot firmware and uClinux™ kernel to the SmartFusion cSoC, a Linux® -based cross-development framework, and other complementary components. Combined with the release of its A2F-Linux Evaluation Kit, this provides a low-cost platform for evaluation and development of Linux (uClinux) on the Cortex-M3 CPU core of the Microchip SmartFusion cSoC.

- Emcraft Linux on Microchip's SmartFusion cSoC

Keil offers the RTX Real-Time Kernel as a royalty-free, deterministic RTOS designed for ARM and Cortex-M devices. It allows you to create programs that simultaneously perform multiple functions and helps to create applications which are better structured and more easily maintained.

- The RTX Real-Time Kernel is included with MDK-ARM. Download the Evaluation version of Keil MDK-ARM.
- RTX source code is available as part of Keil/ARM Real-Time Library (RL-ARM), a group of tightly-coupled libraries designed to solve the real-time and communication challenges of embedded systems based on ARM-powered microcontroller devices. The RL-ARM library now supports SmartFusion cSoCs and designers with additional key features listed in the 18.3. Middleware.

Micrium supports SmartFusion cSoCs with the company's flagship µC/OS family, recognized for a variety of features and benefits, including unparalleled reliability, performance, dependability, impeccable source code and vast documentation. Micrium supports the following products for SmartFusion cSoCs and continues to work with Microchip on additional projects.

- SmartFusion Quickstart Guide for Micrium µC/OS-III Examples
  - Design Files

µC/OS-III™, Micrium's newest RTOS, is designed to save time on your next embedded project and puts greater control of the software in your hands.

RoweBots provides an ultra tiny Linux-compatible RTOS called Unison for SmartFusion. Unison consists of a set of modular software components, which, like Linux, are either free or commercially licensed. Unison offers POSIX® and Linux compatibility with hard real-time performance, complete I/O modules and an easily understood environment for device driver programming. Seamless integration with FPGA and analog features are fast and easy.

- Unison V4-based products include a free Unison V4 Linux and POSIX-compatible kernel with serial I/O, file system, six demonstration programs, upgraded documentation and source code for Unison V4, and free (for non-commercial use) Unison V4 TCP/IP server. Commercial license upgrade is available for Unison V4 TCP/IP server with three demonstration programs, DHCP client and source code.
- Unison V5-based products include commercial Unison V5 Linux- and POSIX-compatible kernel with serial I/O, file system, extensive feature set, full documentation, source code and more than 20 demonstration programs, Unison V5 TCP/IPv4 with extended feature set, sockets interface, multiple network interfaces, PPP support, DHCP client, documentation, source code and six demonstration programs, and multiple other features.

## 18.3 Middleware (Ask a Question)

Microchip has ported both uIP and lwIP for Ethernet support as well as including TFTP file service.

- SmartFusion Webserver Demo Using uIP and FreeRTOS
- SmartFusion: Running Webserver, TFTP on lwIP TCP/IP Stack Application Note

The Keil/ARM Real-Time Library (RL-ARM)[1], in addition to RTX source, includes the following:

- RL-TCPnet (TCP/IP) – The Keil RL-TCPnet library, supporting full TCP/IP and UDP protocols, is a full networking suite specifically written for small ARM and Cortex-M processor-based microcontrollers. TCPnet is now ported to and supports SmartFusion Cortex-M3. It is highly optimized, has a small code footprint, and gives excellent performance, providing a wide range of application level protocols and examples such as FTP, SNMP, SOAP and AJAX. An HTTP server example of TCPnet working in a SmartFusion design is available.
- Flash File System (RL-Flash) allows your embedded applications to create, save, read, and modify files in standard storage devices such as ROM, RAM, or FlashROM, using a standard serial peripheral interface (SPI). Many ARM-based microcontrollers have a practical requirement for a standard file system. With RL-FlashFS you can implement new features in embedded applications such as data logging, storing program state during standby modes, or storing firmware upgrades.

Micrium, in addition to µC/OS-III®, offers the following support for SmartFusion cSoC:

- µC/TCP-IP™ is a compact, reliable, and high-performance stack built from the ground up by Micrium and has the quality, scalability, and reliability that translates into a rapid configuration of network options, remarkable ease-of-use, and rapid time-to-market.
- µC/Probe™ is one of the most useful tools in embedded systems design and puts you in the driver's seat, allowing you to take charge of virtually any variable, memory location, and I/O port in your embedded product, while your system is running.

**Note:**

1. The CAN and USB functions within RL-ARM are not supported for SmartFusion cSoC.

## 18.4 References (Ask a Question)

### 18.4.1 PCB Files (Ask a Question)

- A2F500 SmartFusion Development Kit PCB Files

### 18.4.2 Application Notes (Ask a Question)

- SmartFusion cSoC Board Design Guidelines

# 19. SmartFusion Programming (Ask a Question)

SmartFusion cSoCs have three separate Flash areas that can be programmed:

1. The FPGA fabric
2. The embedded nonvolatile memories (eNVMs)
3. The embedded Flash ROM (eFROM)

There are essentially three methodologies for programming these areas:

1. In-system programming (ISP)
2. In-application programming (IAP)
   a. A2F060 and A2F500: The FPGA fabric, eNVM, and eFROM
   b. A2F200: Only the FPGA fabric and the eNVM
3. Pre-programming (non-ISP)

Programming, whether ISP or IAP methodologies are employed, can be done in two ways:

1. Securely using the on-chip AES decryption logic
2. In plain text

## 19.1 In-System Programming (Ask a Question)

In-System Programming is performed with the aid of external JTAG programming hardware. Table "Supported JTAG Programming Hardware" describes the JTAG programming hardware that will program a SmartFusion cSoC and table "JTAG Pin Descriptions" defines the JTAG pins that provide the interface for the programming hardware.

**Table 19-1.** Supported JTAG Programming Hardware

| Dongle | Source | JTAG | SWD[1] | SWV[2] | Program FPGA | Program eFROM | Program eNVM |
|---|---|---|---|---|---|---|---|
| FlashPro3/4 | SoC Products Group | Yes | No | No | Yes | Yes | Yes |
| ULINK Pro | Keil | Yes | Yes | Yes | Yes[3] | Yes[3] | Yes |
| ULINK2 | Keil | Yes | Yes | Yes | Yes[3] | Yes[3] | Yes |
| IAR J-Link | IAR | Yes | Yes | Yes | Yes[3] | Yes[3] | Yes |

**Notes:**

1. SWD = ARM Serial Wire Debug
2. SWV = ARM Serial Wire Viewer
3. Planned support

**Table 19-2.** JTAG Pin Descriptions

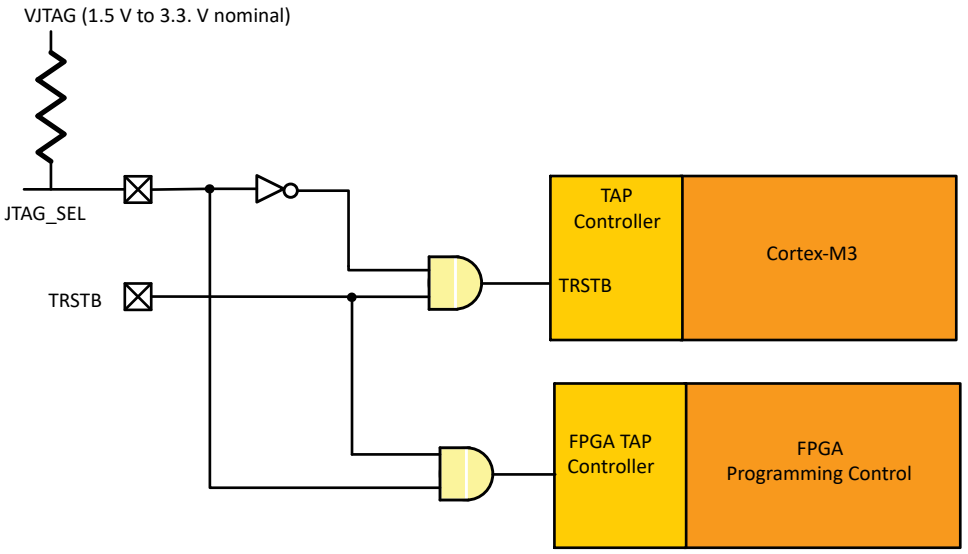
| Pin Name | Description |
|---|---|
| JTAGSEL | ARM Cortex-M3 or FPGA test access port (TAP) controller selection |
| TRSTB | Test reset bar |
| TCK | Test clock |
| TMS | Test mode select |
| TDI | Test data input |
| TDO | Test data output |

The JTAGSEL pin selects the FPGA TAP controller or the Cortex-M3 debug logic. When JTAGSEL is asserted, the FPGA TAP controller is selected and the TRSTB input into the Cortex-M3 is held in a reset state (logic 0), as depicted in the following figure. Users should tie the JTAGSEL pin high externally.

Microchip's free Eclipse-based IDE, SoftConsole, has the ability to control the JTAGSEL pin directly with the FlashPro4 programmer. Manual jumpers are provided on the evaluation and development kits to allow manual selection of this function for the J-Link and ULINK debuggers.

**Note:** Standard ARM JTAG connectors do not have access to the JTAGSEL pin. SoftConsole automatically selects the appropriate TAP controller using the CTXSELECT JTAG command. When using SoftConsole, the state of JTAGSEL is a "don't care."

**Figure 19-1.** TRSTB Logic




## 19.2 In-Application Programming (Ask a Question)

In-application programming refers to the ability to reprogram the various flash areas under direct supervision of the Cortex-M3.

### 19.2.1 Reprogramming the FPGA Fabric Using the Cortex-M3 (Ask a Question)

In this mode, the Cortex-M3 is executing the programming algorithm on-chip. The IAP driver can be incorporated into the design project and executed from eNVM or eSRAM. The SoC Products Group provides working example projects for SoftConsole, IAR, and Keil development environments. These can be downloaded via the SoC Products Group Firmware Catalog. The new bitstream to be programmed into the FPGA can reside on the user's printed circuit board (PCB) in a separate SPI flash memory. Alternately, the user can modify the existing projects supplied by the SoC Products Group and, via custom handshaking software, throttle the download of the new image and program the FPGA a piece at a time in real time. A cost-effective and reliable approach would be to store the bitstream in an external SPI flash. Another option is storing a redundant bitstream image in an external SPI flash and loading the newest version into the FPGA only when receiving an IAP command. Since the FPGA I/Os are tristated or held at predefined or last known state during FPGA programming, the user must use MSS I/Os to interface to external memories. Since there are two SPI controllers in the MSS, the user can dedicate one to an SPI flash and the other to the particulars of an application. The amount of flash memory required to program the FPGA always exceeds the size of the eNVM block that is on-chip. The external memory controller (EMC) cannot be used as an

interface to a memory device for storage of a bitstream because its I/O pads are FPGA I/Os; hence they are tristated when the FPGA is in a programming state.

The MSS resets itself after IAP of the FPGA fabric. This reset is internally asserted on MSS_RESETN by the power supply monitor (PSM) and reset controller of the MSS.

### 19.2.2 Re-Programming the eNVM Blocks Using the Cortex-M3 (Ask a Question)

In this mode the Cortex-M3 is executing the eNVM programming algorithm from eSRAM. Since individual pages (132 bytes) of the eNVM can be write-protected, the programming algorithm software can be protected from inadvertent erasure. When reprogramming the eNVM, both MSS I/Os and FPGA I/Os are available as interfaces for sourcing the new eNVM image. The SoC Products Group provides working example projects for SoftConsole, IAR, and Keil development environments. These can be downloaded via the SoC Products Group Firmware Catalog.

Alternately, the eNVM can be reprogrammed by the Cortex-M3 via the IAP driver. This is necessary when using an encrypted image.

### 19.2.3 Secure Programming (Ask a Question)

For background, refer to the "Security in Low Power Flash Devices" chapter of the Fusion FPGA Fabric User's Guide on the SoC Products Group website. SmartFusion ISP behaves identically to Fusion ISP. IAP of SmartFusion cSoCs is accomplished by using the IAP driver. Only the FPGA fabric and the eNVM can be reprogrammed with the protection of security measures by using the IAP driver.

## 19.3 Typical Programming and Erase Times (Ask a Question)

The following table documents the typical programming and erase times for two components of SmartFusion cSoCs, FPGA fabric and eNVM, using the SoC Products Group's FlashPro hardware and software. These times will be different for other ISP and IAP methods. The Program action in FlashPro software includes erase, program, and verify to complete.

The typical programming (including erase) time per page of the eNVM is 8 ms.

**Table 19-3.** Typical Programming and Erase Times

| | FPGA Fabric (seconds) | | | eNVM (seconds) | | | FlashROM (seconds) | | |
|---|---|---|---|---|---|---|---|---|---|
| | A2F060 [1] | A2F200 | A2F500 | A2F060 | A2F200 | A2F500 | A2F060 | A2F200 | A2F500 |
| Erase | 21 | 21 | 21 | N/A | N/A | N/A | 21 | 21 | 21 |
| Program | 28 | 35 | 48 | 18 | 39 | 71 | 22 | 22 | 22 |
| Verify | 2 | 6 | 12 | 9 | 18 | 37 | 1 | 1 | 1 |

**Note:**

1. Part No A2F060 is discontinued.

## 19.4 References (Ask a Question)

### 19.4.1 User's Guides (Ask a Question)

- DirectC User's Guide
- SmartFusion Microcontroller Subsystem User Guide
- In-System Programming (ISP) of Microsemi's Low-Power Flash Devices Using FlashPro4/3/3X
- Flash Program User Guide
- Programming Flash Devices HandBook

### 19.4.2 Application Notes on IAP Programming Technique (Ask a Question)

- SmartFusion cSoC: Programming FPGA Fabric and eNVM Using In-Application Programming Interface App Note

- SmartFusion cSoC: Basic Bootloader and Field Upgrade eNVM Through IAP Interface App Note

# 20. Supply Pins (Ask a Question)

**Table 20-1.** Supply Pins

| Name | Type | Description |
|---|---|---|
| GND | Ground | Digital ground to the FPGA fabric, microcontroller subsystem and GPIOs |
| GND15ADC0 | Ground | Quiet analog ground to the 1.5V circuitry of the first analog-to-digital converter (ADC) |
| GND15ADC1 | Ground | Quiet analog ground to the 1.5V circuitry of the second ADC |
| GND15ADC2 | Ground | Quite analog ground to the 1.5V circuitry of the third ADC |
| GND33ADC0 | Ground | Quiet analog ground to the 3.3V circuitry of the first ADC |
| GND33ADC1 | Ground | Quiet analog ground to the 3.3V circuitry of the second ADC |
| GND33ADC2 | Ground | Quiet analog ground to the 3.3V circuitry of the third ADC |
| GNDA | Ground | Quiet analog ground to the analog front-end |
| GNDAQ | Ground | Quiet analog ground to the analog I/O of SmartFusion® cSoCs |
| GNDENVM | Ground | Digital ground to the embedded nonvolatile memory (eNVM) |
| GNDLPXTAL | Ground | Analog ground to the low power 32 KHz crystal oscillator circuitry |
| GNDMAINXTAL | Ground | Analog ground to the main crystal oscillator circuitry |
| GNDQ | Ground | Quiet digital ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ needs to always be connected on the board to GND. |
| GNDRCOSC | Ground | Analog ground to the integrated RC oscillator circuit |
| GNDSDD0 | Ground | Analog ground to the first sigma-delta DAC |
| GNDSDD1 | Ground | Common analog ground to the second and third sigma-delta DACs |
| GNDTM0 | Ground | Analog temperature monitor common ground for signal conditioning blocks SCB 0 and SCB 1 (see information for pins TM0 and TM1 in the Analog Front-End (AFE)) section. |
| GNDTM1 | Ground | Analog temperature monitor common ground for signal conditioning block SCB 2 and SBCB 3 (see information for pins TM2 and TM3 in the Analog Front-End (AFE) section). |
| GNDTM2 | Ground | Analog temperature monitor common ground for signal conditioning block SCB4 |
| GNDVAREF | Ground | Analog ground reference used by the ADC. This pad should be connected to a quiet analog ground. |
| VCC | Supply | Digital supply to the FPGA fabric and MSS, nominally 1.5V. VCC is also required for powering the JTAG state machine, in addition to VJTAG. Even when a SmartFusion cSoC is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the SmartFusion cSoC. |
| VCC15A | Supply | Clean analog 1.5V supply to the analog circuitry. Always power this pin. |
| VCC15ADC0 | Supply | Analog 1.5V supply to the first ADC. Always power this pin. |
| VCC15ADC1 | Supply | Analog 1.5V supply to the second ADC. Always power this pin. |
| VCC15ADC2 | Supply | Analog 1.5V supply to the third ADC. Always power this pin. |
| VCC33A | Supply | Clean 3.3V analog supply to the analog circuitry. VCC33A is also used to feed the 1.5V voltage regulator for designs that do not provide an external supply to VCC. Refer to the Voltage Regulator (VR), Power Supply Monitor (PSM), and Power Modes section in the SmartFusion Microcontroller Subsystem User's Guide for more information. |
| VCC33ADC0 | Supply | Analog 3.3V supply to the first ADC. If unused, Microchip recommends connecting this pin to a 3.3V supply.[1] |
| VCC33ADC1 | Supply | Analog 3.3V supply to the second ADC. If unused, Microchip recommends connecting this pin to a 3.3V supply.[1] |
| VCC33ADC2 | Supply | Analog 3.3V supply to the third ADC. If unused, Microchip recommends connecting this pin to a 3.3V supply.[1] |
| VCC33AP | Supply | Analog clean 3.3V supply to the charge pump. To avoid high current draw, VCC33AP should be powered up simultaneously with or after VCC33A. Can be pulled down if unused.[1] |

| .....continued | | |
|---|---|---|
| **Name** | **Type** | **Description** |
| VCC33N | Supply | –3.3V output from the voltage converter. A 2.2 µF capacitor must be connected from this pin to GND. Analog charge pump capacitors are not needed if none of the analog SCB features are used and none of the SDDs are used. In that case it should be left unconnected. |
| VCC33SDD0 | Supply | Analog 3.3V supply to the first sigma-delta DAC |
| VCC33SDD1 | Supply | Common analog 3.3V supply to the second and third sigma-delta DACs |
| VCCENVM | Supply | Digital 1.5V power supply to the embedded nonvolatile memory blocks. To avoid high current draw, VCC should be powered up before or simultaneously with VCCENVM. |
| VCCESRAM | Supply | Digital 1.5V power supply to the embedded SRAM blocks. Available only on the 208PQFP package. It should be connected to VCC (in other packages, it is internally connected to VCC). |
| VCCFPGAIOB0 | Supply | Digital supply to the FPGA fabric I/O bank 0 (north FPGA I/O bank) for the output buffers and I/O logic.<br>Each bank can have a separate VCCFPGAIO connection. All I/Os in a bank will run off the same VCCFPGAIO supply. VCCFPGAIO can be 1.5V, 1.8V, 2.5V, or 3.3V, nominal voltage. Unused I/O banks should have their corresponding VCCFPGAIO pins tied to GND. |
| VCCFPGAIOB1 | Supply | Digital supply to the FPGA fabric I/O bank 1 (east FPGA I/O bank) for the output buffers and I/O logic.<br>Each bank can have a separate VCCFPGAIO connection. All I/Os in a bank will run off the same VCCFPGAIO supply. VCCFPGAIO can be 1.5V, 1.8V, 2.5V, or 3.3V, nominal voltage. Unused I/O banks should have their corresponding VCCFPGAIO pins tied to GND. |
| VCCFPGAIOB5 | Supply | Digital supply to the FPGA fabric I/O bank 5 (west FPGA I/O bank) for the output buffers and I/O logic.<br>Each bank can have a separate VCCFPGAIO connection. All I/Os in a bank will run off the same VCCFPGAIO supply. VCCFPGAIO can be 1.5V, 1.8V, 2.5V, or 3.3V, nominal voltage. Unused I/O banks should have their corresponding VCCFPGAIO pins tied to GND. |
| VCCLPXTAL | Supply | Analog supply to the low power 32 KHz crystal oscillator. Always power this pin.[1] |
| VCCMAINXTAL | Supply | Analog supply to the main crystal oscillator circuit. Always power this pin.[1] |
| VCCMSSIOB2 | Supply | Supply voltage to the microcontroller subsystem I/O bank 2 (east MSS I/O bank) for the output buffers and I/O logic.<br>Each bank can have a separate VCCMSSIO connection. All I/Os in a bank will run off the same VCCMSSIO supply. VCCMSSIO can be 1.5V, 1.8V, 2.5V, or 3.3V, nominal voltage. Unused I/O banks should have their corresponding VCCMSSIO pins tied to GND. |
| VCCMSSIOB4 | Supply | Supply voltage to the microcontroller subsystem I/O bank 4 (west MSS I/O bank) for the output buffers and I/O logic.<br>Each bank can have a separate VCCMSSIO connection. All I/Os in a bank will run off the same VCCMSSIO supply. VCCMSSIO can be 1.5V, 1.8V, 2.5V, or 3.3V, nominal voltage. Unused I/O banks should have their corresponding VCCMSSIO pins tied to GND. |
| VCCPLLx | Supply | Analog 1.5V supply to the PLL. Always power this pin. |
| VCCRCOSC | Supply | Analog supply to the integrated RC oscillator circuit. Always power this pin.[1] |
| VCOMPLAx | Supply | Analog ground for the PLL |
| VDDBAT | Supply | External battery connection to the low power 32 KHz crystal oscillator (along with VCCLPXTAL), RTC, and battery switchover circuit. Can be pulled down if unused. |
| VJTAG | Supply | Digital supply to the JTAG controller<br>SmartFusion cSoCs have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5V to 3.3V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned to be used, the VJTAG pin together with the TRSTB pin could be tied to GND. Note that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a SmartFusion cSoC is in a JTAG chain of interconnected boards and it is desired to power down the board containing the device, this can be done provided both VJTAG and VCC to the device remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode. See JTAG Pins. |

| .....continued | | |
|---|---|---|
| **Name** | **Type** | **Description** |
| VPP | Supply | Digital programming circuitry supply<br>SmartFusion cSoCs support single-voltage in-system programming (ISP) of the configuration flash, embedded FlashROM (eFROM), and embedded nonvolatile memory (eNVM).<br>For programming, VPP should be in the 3.3V ± 5% range. During normal device operation, VPP can be left floating or can be tied to any voltage between 0V and 3.6V. When the VPP pin is tied to ground, it shuts off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry. For proper programming, 0.01 µF, and 0.1 µF to 1 µF capacitors, (both rated at 16V) are to be connected in parallel across VPP and GND, and positioned as close to the FPGA pins as possible. |

**Notes:**

1. The following 3.3V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.
2. The following 1.5V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.
3. For more details on VCCPLLx capacitor recommendations, refer to the application note AC359, SmartFusion cSoC Board Design Guidelines, the “PLL Power Supply Decoupling Scheme” section.

## User-Defined Supply Pins

**Table 20-2.** User-Defined Supply Pins

| Name | Type | Polarity/Bus Size | Description |
|---|---|---|---|
| VAREF0 | Input | 1 | Analog reference voltage for first ADC.<br>The SmartFusion® cSoC can be configured to generate a 2.56V internal reference that can be used by the ADC. While using the internal reference, the reference voltage is output on the VAREFOUT pin for use as a system reference. If a different reference voltage is required, it can be supplied by an external source and applied to this pin. The valid range of values that can be supplied to the ADC is 1.0V to 3.3V. When VAREF0 is internally generated, a bypass capacitor must be connected from this pin to ground. The value of the bypass capacitor should be between 3.3 µF and 22 µF, which is based on the needs of the individual designs. The choice of the capacitor value has an impact on the settling time it takes the VAREF0 signal to reach the required specification of 2.56V to initiate valid conversions by the ADC. If the lower capacitor value is chosen, the settling time required for VAREF0 to achieve 2.56V will be shorter than when selecting the larger capacitor value. The above range of capacitor values supports the accuracy specification of the ADC, which is detailed in the datasheet. Designers choosing the smaller capacitor value will not obtain as much margin in the accuracy as that achieved with a larger capacitor value. See the Analog-to-Digital Converter (ADC) section in the SmartFusion Programmable Analog User’s Guide for more information. The SoC Products Group recommends customers use 10 µF as the value of the bypass capacitor. Designers choosing to use an external VAREF0 need to ensure that a stable and clean VAREF0 source is supplied to the VAREF0 pin before initiating conversions by the ADC. To use the internal voltage reference, the VAREFOUT pin must be connected to the appropriate ADC VAREFx input on the PCB. For example, VAREFOUT can be connected to VAREF0 only, if ADC0 alone is used. VAREFOUT can be connected to VAREF1 only, if ADC1 alone is used. VAREFOUT can be connected to VAREF2 only, if ADC2 alone is used. VAREFOUT can be connected to VAREF0, VAREF1 and VAREF2 together, if ADC0, ADC1, and ADC2 all are used. |
| VAREF1 | Input | 1 | Analog reference voltage for second ADC<br>See VAREF0 above for more information. |
| VAREF2 | Input | 1 | Analog reference voltage for third ADC<br>See VAREF0 above for more. |
| VAREFOUT | Out | 1 | Internal 2.56V voltage reference output. Can be used to provide the two ADCs with a unique voltage reference externally by connecting VAREFOUT to both VAREF0 and VAREF1. To use the internal voltage reference, you must connect the VAREFOUT pin to the appropriate ADC VAREFx input—either the VAREF0 or VAREF1 pin—on the PCB. |

### Global I/O Naming Conventions

Gmn (Gxxx) refers to Global I/Os. These Global I/Os are used to connect the input to global networks. Global networks have high fanout and low skew. The naming convention for Global I/Os is as follows:

- G = Global
- m = Global pin location associated with each CCC on the device:
  - A (northwest corner)
  - B (northeast corner)
  - C (east middle)
  - D (southeast corner)
  - E (southwest corner)
  - F (west middle)

n = Global input MUX and pin number of the associated Global location m—A0, A1, A2, B0, B1, B2, C0, C1, or C2.

Global (GL) I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities.

Unused GL pins are configured as inputs with pull-up resistors. See more detailed descriptions of global I/O connectivity in the clocking resources chapter of the SmartFusion FPGA Fabric User's Guide and the clock conditioning circuitry chapter of the SmartFusion Microcontroller Subsystem User's Guide.

All inputs other than GC/GF are direct inputs into the quadrant clocks. The inputs to the global network are multiplexed, and only one input can be used as a global input. For example, if GAA0 is used as a quadrant global input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs other than GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. For more details, refer to the Global Input Selections section of the SmartFusion Fabric User Guide.

# 21. User Pins (Ask a Question)

**Table 21-1.** User Pins

| Name | Type | Polarity/Bus Size | Description |
|---|---|---|---|
| GPIO_x | In/out | 32 | Microcontroller Subsystem (MSS) General Purpose I/O (GPIO). The MSS GPIO pin functions as an input, output, tristate, or bidirectional buffer with configurable interrupt generation and Schmitt trigger support. Input and output signal levels are compatible with the I/O standard selected.<br>Unused GPIO pins are tristated and do not include pull-up or pull-down resistors.<br>During power-up, the used GPIO pins are tristated with no pull-up or pull-down resistors until Sys boot configures them.<br>Some of these pins are also multiplexed with integrated peripherals in the MSS (SPI, $I^2C$, and UART). These pins are located in Bank-2 (GPIO_16 to GPIO_31) for A2F060, A2F200, and A2F500 devices.<br>GPIOs can be routed to dedicated I/O buffers (MSSIOBUF) or in some cases to the FPGA fabric interface through an IOMUX. This allows GPIO pins to be multiplexed as either I/Os for the FPGA fabric, the ARM® Cortex-M3 or for given integrated MSS peripherals. The MSS peripherals are not multiplexed with each other; they are multiplexed only with the GPIO block. For more information, see the General Purpose I/O Block (GPIO) section in the SmartFusion Microcontroller Subsystem User's Guide. |
| IO | In/out | — | FPGA user I/O |

### User I/O Naming Conventions

The naming convention used for each FPGA user I/O is Gmn/IOuxwByVz, where:

Gmn is only used for I/Os that also have CCC access—i.e., global pins. Refer to the Global I/O Naming Conventions.

- u = I/O pair number in bank, starting at 00 from the northwest I/O bank and proceeding in a clockwise direction.
- x = P (positive) or N (negative) or S (single-ended) or R (regular, single-ended).
- w = D (Differential Pair), P (Pair), or S (Single-Ended). D (Differential Pair) if both members of the pair are bonded out to adjacent pins or are separated only by one GND or NC pin; P (Pair) if both members of the pair are bonded out but do not meet the adjacency requirement; or S (Single-Ended) if the I/O pair is not bonded out. For Differential Pairs (D), adjacency for ball grid packages means only vertical or horizontal. Diagonal adjacency does not meet the requirements for a true differential pair.
- B = Bank
- y = Bank number starting at 0 from northwest I/O bank and incrementing clockwise.
- V = Reference voltage
- z = VREF mini bank number.

The FPGA user I/O pin functions as an input, output, tristate or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected. Unused I/O pins are disabled by Libero SoC software and include a weak pull-up resistor. During power-up, the used I/O pins are tristated with no pull-up or pull-down resistors until I/O enable (there is a delay after voltage stabilizes, and different I/O banks power up sequentially to avoid a surge of ICCI).

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

Some of these pins are also multiplexed with integrated peripherals in the MSS (Ethernet MAC and external memory controller).

All unused MSS I/Os are tristated by default (with output buffer disabled). However, you can configure it as weak pull-up or pull-down by using Libero SoC I/O attributor window. The Schmitt trigger is disabled. Essentially, I/Os have the reset values as defined in Table 19-25 IOMUX_n_CR, in the SmartFusion Microcontroller Subsystem User's Guide.

By default, during programming I/Os become tristated and weakly pulled up to VCCxxxxIOBx. You can modify the I/O states during programming in FlashPro. For more details, refer to 2.4. Specifying I/O States During Programming . With the VCCI and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration. For more information, see the SmartFusion FPGA User I/Os section in the SmartFusion FPGA Fabric User's Guide.

### Special Function Pins

The following table lists the special function pins.

**Table 21-2.** Special Function Pins

| Name | Type | Polarity/Bus Size | Description |
|---|---|---|---|
| NC | — | — | No connect<br>This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device. |
| DC | — | — | Do not connect.<br>This pin should not be connected to any signals on the PCB. These pins should be left unconnected. |
| LPXIN | In | 1 | Low power 32 KHz crystal oscillator.<br>Input from the 32 KHz oscillator. Pin for connecting a low power 32 KHz watch crystal. If not used, the LPXIN pin can be left floating. For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the SmartFusion Microcontroller Subsystem User's Guide. |
| LPXOUT | In | 1 | Low power 32 KHz crystal oscillator.<br>Output to the 32 KHz oscillator. Pin for connecting a low power 32 KHz watch crystal. If not used, the LPXOUT pin can be left floating. For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the SmartFusion Microcontroller Subsystem User's Guide. |
| MAINXIN | In | 1 | Main crystal oscillator circuit.<br>Input to the crystal oscillator circuit. Pin for connecting an external crystal, ceramic resonator, or RC network. When using an external crystal or ceramic oscillator, external capacitors are also recommended. Refer to documentation from the crystal oscillator manufacturer for proper capacitor value.<br>If an external RC network or clock input is used, the RC components are connected to the MAINXIN pin, with MAINXOUT left floating. When the main crystal oscillator is not being used, MAINXIN and MAINXOUT pins can be left floating.<br>For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the SmartFusion Microcontroller Subsystem User's Guide. |

| .....continued | | | |
|---|---|---|---|
| **Name** | **Type** | **Polarity/Bus Size** | **Description** |
| MAINXOUT | Out | 1 | Main crystal oscillator circuit.<br>Output from the crystal oscillator circuit. Pin for connecting external crystal or ceramic resonator. When using an external crystal or ceramic oscillator, external capacitors are also recommended. Refer to documentation from the crystal oscillator manufacturer for proper capacitor value.<br>If an external RC network or clock input is used, the RC components are connected to the MAINXIN pin, with MAINXOUT left floating. When the main crystal oscillator is not being used, MAINXIN and MAINXOUT pins can be left floating.<br>For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the SmartFusion Microcontroller Subsystem User's Guide. |
| NCAP | — | 1 | Negative capacitor connection.<br>This is the negative terminal of the charge pump. A capacitor, with a 2.2 µF recommended value, is required to connect between PCAP and NCAP. Analog charge pump capacitors are not needed if none of the analog SCB features are used and none of the SDDs are used. In that case it should be left unconnected. |
| PCAP | — | 1 | Positive Capacitor connection.<br>This is the positive terminal of the charge pump. A capacitor, with a 2.2 µF recommended value, is required to connect between PCAP and NCAP. If this pin is not used, it must be left unconnected/floating. In this case, no capacitor is needed. Analog charge pump capacitors are not needed if none of the analog SCB features are used, and none of the SDDs are used. |
| PTBASE | — | 1 | Pass transistor base connection<br>This is the control signal of the voltage regulator. This pin should be connected to the base of an external pass transistor used with the 1.5V internal voltage regulator and can be floating if not used. |
| PTEM | — | 1 | Pass transistor emitter connection.<br>This is the feedback input of the voltage regulator.<br>This pin should be connected to the emitter of an external pass transistor used with the 1.5V internal voltage regulator and can be floating if not used. |
| MSS_RESET_N | — | Low | Low Reset signal which can be used as an external reset and can also be used as a system level reset under control of the Cortex-M3 processor. MSS_RESET_N is an output asserted low after power-on reset. The direction of MSS_RESET_N changes during the execution of the Microchip System Boot when chip-level reset is enabled. The Microchip System Boot reconfigures MSS_RESET_N to become a reset input signal when chip-level reset is enabled. It has an internal pull-up so it can be left floating. In the current software, the MSS_RESET_N is modeled as an external input signal only. |
| PU_N | In | Low | Push-button is the connection for the external momentary switch used to turn on the 1.5V voltage regulator and can be floating if not used. |

### JTAG Pins

SmartFusion cSoCs have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5V to 3.3V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the SmartFusion cSoC part must be supplied to allow JTAG signals to transition the SmartFusion cSoC. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility with supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned to be used, the VJTAG pin together with the TRSTB pin could be tied to GND.

**Table 21-3.** JTAG Pins

| Name | Type | Polarity/Bus Size | Description |
|---|---|---|---|
| JTAGSEL | In | 1 | JTAG controller selection<br>Depending on the state of the JTAGSEL pin, an external JTAG controller will either see the FPGA fabric TAP/auxiliary TAP (High) or the Cortex-M3 JTAG debug interface (Low).<br>The JTAGSEL pin should be connected to an external pull-up resistor such that the default configuration selects the FPGA fabric TAP. |
| TCK | In | 1 | Test clock<br>Serial input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, it is recommended to tie off TCK to GND or VJTAG through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.<br>Note that to operate at all VJTAG voltages, 500 Ω to 1kΩ will satisfy the requirements. Refer to Table 21-4 for more information.<br>Can be left floating when unused. |
| TDI | In | 1 | Test data<br>Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin. |
| TDO | Out | 1 | Test data<br>Serial output for JTAG boundary scan, ISP, and UJTAG usage. |
| TMS | In | HIGH | Test mode select<br>The TMS pin controls the use of the IEEE1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.<br>Can be left floating when unused. |
| TRSTB | In | HIGH | Boundary scan reset pin<br>The TRST pin functions as an active low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the TAP is held in reset mode. The resistor values must be chosen from Table 21-4 and must satisfy the parallel resistance value requirement. The values in Table 21-4 correspond to the resistor recommended when a single device is used. The values correspond to the equivalent parallel resistor when multiple devices are connected via a JTAG chain.<br>In critical applications, an upset in the JTAG circuit could allow entering an undesired JTAG state. In such cases, it is recommended that you tie off TRST to GND through a resistor placed close to the FPGA pin.<br>The TRSTB pin also resets the serial wire JTAG – debug port (SWJ-DP) circuitry within the Cortex-M3.<br>Can be left floating when unused. |

**Table 21-4.** Recommended Tie-Off Values for the TCK and TRST Pins

| VJTAG | Tie-Off Resistance[1, 2] |
|---|---|
| VJTAG at 3.3V | 200Ω to 1 kΩ |
| VJTAG at 2.5V | 200Ω to 1 kΩ |
| VJTAG at 1.8V | 500Ω to 1 kΩ |
| VJTAG at 1.5V | 500Ω to 1 kΩ |

**Notes:**

1. The TCK pin can be pulled up/down.
2. The TRST pin can only be pulled down.

Equivalent parallel resistance if more than one device is on JTAG chain.

## Microcontroller Subsystem (MSS)

**Table 21-5.** Microcontroller Subsystem (MSS)

| Name | Type | Polarity/ Bus Size | Description |
|---|---|---|---|
| **External Memory Controller** | | | |
| EMC_ABx | Out | 26 | External memory controller address bus<br>Can also be used as an FPGA user I/O (see Table 21-1). |
| EMC_BYTENx | Out | LOW/2 | External memory controller byte enable<br>Can also be used as an FPGA user I/O (see Table 21-1). |
| EMC_CLK | Out | Rise | External memory controller clock<br>Can also be used as an FPGA user I/O (see Table 21-1). |
| EMC_CSx_N | Out | LOW/2 | External memory controller chip selects<br>Can also be used as an FPGA User IO (see Table 21-1). |
| EMC_DBx | In/out | 16 | External memory controller data bus<br>Can also be used as an FPGA user I/O (see Table 21-1). |
| EMC_OENx_N | Out | LOW/2 | External memory controller output enables<br>Can also be used as an FPGA User IO (see Table 21-1). |
| EMC_RW_N | Out | Level | External memory controller read/write. Read = High, write = Low.<br>Can also be used as an FPGA user I/O (see Table 21-1). |
| **Inter-Integrated Circuit ($I^2C$) Peripherals** | | | |
| I2C_0_SCL | In/out | 1 | $I^2C$ bus serial clock output. First $I^2C$.<br>Can also be used as an MSS GPIO (see Table 21-1). |
| I2C_0_SDA | In/out | 1 | $I^2C$ bus serial data input/output. First $I^2C$.<br>Can also be used as an MSS GPIO (see Table 21-1). |
| I2C_1_SCL | In/out | 1 | $I^2C$ bus serial clock output. Second $I^2C$.<br>Can also be used as an MSS GPIO (see Table 21-1). |
| I2C_1_SDA | In/out | 1 | $I^2C$ bus serial data input/output. Second $I^2C$.<br>Can also be used as an MSS GPIO (see Table 21-1). |
| **Serial Peripheral Interface (SPI) Controllers** | | | |
| SPI_0_CLK | Out | 1 | Clock. First SPI.<br>Can also be used as an MSS GPIO (see Table 21-1). |
| SPI_0_DI | In | 1 | Data input. First SPI.<br>Can also be used as an MSS GPIO (see Table 21-1). |
| SPI_0_DO | Out | 1 | Data output. First SPI.<br>Can also be used as an MSS GPIO (see Table 21-1). |
| SPI_0_SS | Out | 1 | Slave select (chip select). First SPI.<br>Can also be used as an MSS GPIO (see Table 21-1). |
| SPI_1_CLK | Out | 1 | Clock. Second SPI.<br>Can also be used as an MSS GPIO (see Table 21-1). |
| SPI_1_DI | In | 1 | Data input. Second SPI.<br>Can also be used as an MSS GPIO (see Table 21-1). |
| SPI_1_DO | Out | 1 | Data output. Second SPI.<br>Can also be used as an MSS GPIO (see Table 21-1). |
| SPI_1_SS | Out | 1 | Slave select (chip select). Second SPI.<br>Can also be used as an MSS GPIO (see Table 21-1). |
| **Universal Asynchronous Receiver/Transmitter (UART) Peripherals** | | | |
| UART_0_RXD | In | 1 | Receive data. First UART.<br>Can also be used as an MSS GPIO (see Table 21-1). |
| UART_0_TXD | Out | 1 | Transmit data. First UART.<br>Can also be used as an MSS GPIO (see Table 21-1). |

| .....continued | | | |
|---|---|---|---|
| **Name** | **Type** | **Polarity/ Bus Size** | **Description** |
| UART_1_RXD | In | 1 | Receive data. Second UART.<br>Can also be used as an MSS GPIO (see Table 21-1). |
| UART_1_TXD | Out | 1 | Transmit data. Second UART.<br>Can also be used as an MSS GPIO (see Table 21-1). |
| **Ethernet MAC** | | | |
| MAC_CLK | In | Rise | Receive clock. 50 MHz ±50 ppm clock source received from RMII PHY.<br>Can be left floating when unused. |
| MAC_CRSDV | In | High | Carrier sense/receive data valid for RMII PHY<br>Can also be used as an FPGA User IO (see Table 21-1). |
| MAC_MDC | Out | Rise | RMII management clock<br>Can also be used as an FPGA User IO (see Table 21-1). |
| MAC_MDIO | In/Out | 1 | RMII management data input/output<br>Can also be used as an FPGA User IO (see Table 21-1). |
| MAC_RXDx | In | 2 | Ethernet MAC receive data. Data recovered and decoded by PHY. The RXD[0] signal is the least significant bit.<br>Can also be used as an FPGA User I/O (see Table 21-1). |
| MAC_RXER | In | HIGH | Ethernet MAC receive error. If MACRX_ER is asserted during reception, the frame is received and status of the frame is updated with MACRX_ER.<br>Can also be used as an FPGA user I/O (see Table 21-1). |
| MAC_TXDx | Out | 2 | Ethernet MAC transmit data. The TXD[0] signal is the least significant bit.<br>Can also be used as an FPGA user I/O (see Table 21-1). |
| MAC_TXEN | Out | HIGH | Ethernet MAC transmit enable. When asserted, indicates valid data for the PHY on the TXD port.<br>Can also be used as an FPGA User I/O (see Table 21-1). |

## Analog Front-End (AFE)

**Table 21-6.** Analog Front-End (AFE)

| Name | Type | Description | Associated With | |
|---|---|---|---|---|
| | | | ADC/SDD | SCB |
| ABPS0 | In | SCB 0 / active bipolar prescaler input 1.<br>See the Active Bipolar Prescaler (ABPS) section in the SmartFusion Programmable Analog User's Guide. | ADC0 | SCB0 |
| ABPS1 | In | SCB 0 / active bipolar prescaler Input 2 | ADC0 | SCB0 |
| ABPS2 | In | SCB 1 / active bipolar prescaler Input 1 | ADC0 | SCB1 |
| ABPS3 | In | SCB 1 / active bipolar prescaler Input 2 | ADC0 | SCB1 |
| ABPS4 | In | SCB 2 / active bipolar prescaler Input 1 | ADC1 | SCB2 |
| ABPS5 | In | SCB 2 / active bipolar prescaler Input 2 | ADC1 | SCB2 |
| ABPS6 | In | SCB 3 / active bipolar prescaler Input 1 | ADC1 | SCB3 |
| ABPS7 | In | SCB 3 / active bipolar prescaler input 2 | ADC1 | SCB3 |
| ABPS8 | In | SCB 4 / active bipolar prescaler input 1 | ADC2 | SCB4 |
| ABPS9 | In | SCB 4 / active bipolar prescaler input 2 | ADC2 | SCB4 |
| ADC0 | In | ADC 0 direct input 0 / FPGA Input.<br>See the "Sigma-Delta Digital-to-Analog Converter (DAC)" section in the SmartFusion Programmable Analog User's Guide. | ADC0 | SCB0 |
| ADC1 | In | ADC 0 direct input 1 / FPGA input | ADC0 | SCB0 |
| ADC2 | In | ADC 0 direct input 2 / FPGA input | ADC0 | SCB1 |
| ADC3 | In | ADC 0 direct input 3 / FPGA input | ADC0 | SCB1 |

| .....continued | | | | |
|---|---|---|---|---|
| Name | Type | Description | Associated With | |
| | | | ADC/SDD | SCB |
| ADC4 | In | ADC 1 direct input 0 / FPGA input | ADC1 | SCB2 |
| ADC5 | In | ADC 1 direct input 1 / FPGA input | ADC1 | SCB2 |
| ADC6 | In | ADC 1 direct input 2 / FPGA input | ADC1 | SCB3 |
| ADC7 | In | ADC 1 direct input 3 / FPGA input | ADC1 | SCB3 |
| ADC8 | In | ADC 2 direct input 0 / FPGA input | ADC2 | SCB4 |
| ADC9 | In | ADC 2 direct input 1 / FPGA input | ADC2 | SCB4 |
| ADC10 | In | ADC 2 direct input 2 / FPGA input | ADC2 | N/A |
| ADC11 | In | ADC 2 direct input 3 / FPGA input | ADC2 | N/A |
| CM0 | In | SCB 0 / high side of current monitor / comparator<br>Positive input. See the Current Monitor section in the SmartFusion Programmable Analog User's Guide. | ADC0 | SCB0 |
| CM1 | In | SCB 1 / high side of current monitor / comparator. Positive input. | ADC0 | SCB1 |
| CM2 | In | SCB 2 / high side of current monitor / comparator. Positive input. | ADC1 | SCB2 |
| CM3 | In | SCB 3 / high side of current monitor / comparator. Positive input. | ADC1 | SCB3 |
| CM4 | In | SCB 4 / high side of current monitor / comparator. Positive input. | ADC2 | SCB4 |
| TM0 | In | SCB 0 / low side of current monitor / comparator<br>Negative input / high side of temperature monitor. See the Temperature Monitor section. | ADC0 | SCB0 |
| TM1 | In | SCB 1 / low side of current monitor / comparator. Negative input / high side of temperature monitor. | ADC0 | SCB1 |
| TM2 | In | SCB 2 / low side of current monitor / comparator. Negative input / high side of temperature monitor. | ADC1 | SCB2 |
| TM3 | In | SCB 3 low side of current monitor / comparator. Negative input / high side of temperature monitor. | ADC1 | SCB3 |
| TM4 | In | SCB 4 low side of current monitor / comparator. Negative input / high side of temperature monitor. | ADC2 | SCB4 |
| SDD0 | Out | Output of SDD0<br>See the Sigma-Delta Digital-to-Analog Converter (DAC) section in the SmartFusion Programmable Analog User's Guide. | SDD0 | N/A |
| SDD1 | Out | Output of SDD1 | SDD1 | N/A |
| SDD2 | Out | Output of SDD2 | SDD2 | N/A |

**Note:** Unused analog inputs should be grounded. This aids in shielding and prevents an undesired coupling path.

### Analog Front-End Pin-Level Function Multiplexing

The following table lists the relationships between the various internal signals found in the analog front-end (AFE) and how they are multiplexed onto the external package pins. Note that, in general, only one function is available for those pads that have numerous functions listed. The exclusion to this rule is when a comparator is used; the ADC can still convert either input side of the comparator.

**Table 21-7.** Relationships Between Signals in the Analog Front-End

| Pin | ADC Channel | Dir.-In Option | Prescaler | Current Mon. | Temp. Mon. | Compar. | LVTTL | SDD MUX | SDD |
|---|---|---|---|---|---|---|---|---|---|
| ABPS0 | ADC0_CH1 | — | ABPS0_IN | — | — | — | — | — | — |
| ABPS1 | ADC0_CH2 | — | ABPS1_IN | — | — | — | — | — | — |
| ABPS2 | ADC0_CH5 | — | ABPS2_IN | — | — | — | — | — | — |
| ABPS3 | ADC0_CH6 | — | ABPS3_IN | — | — | — | — | — | — |
| ABPS4 | ADC1_CH1 | — | ABPS4_IN | — | — | — | — | — | — |

**.....continued**

| Pin | ADC Channel | Dir.-In Option | Prescaler | Current Mon. | Temp. Mon. | Compar. | LVTTL | SDD MUX | SDD |
|---|---|---|---|---|---|---|---|---|---|
| ABPS5 | ADC1_CH2 | — | ABPS5_IN | — | — | — | — | — | — |
| ABPS6 | ADC1_CH5 | — | ABPS6_IN | — | — | — | — | — | — |
| ABPS7 | ADC1_CH6 | — | ABPS7_IN | — | — | — | — | — | — |
| ABPS8 | ADC2_CH1 | — | ABPS8_IN | — | — | — | — | — | — |
| ABPS9 | ADC2_CH2 | — | ABPS9_IN | — | — | — | — | — | — |
| ADC0 | ADC0_CH9 | Yes | — | — | — | CMP1_P | LVTTL0_IN | — | — |
| ADC1 | ADC0_CH10 | Yes | — | — | — | CMP1_N | LVTTL1_IN | SDDM0_OUT | — |
| ADC2 | ADC0_CH11 | Yes | — | — | — | CMP3_P | LVTTL2_IN | — | — |
| ADC3 | ADC0_CH12 | Yes | — | — | — | CMP3_N | LVTTL3_IN | SDDM1_OUT | — |
| ADC4 | ADC1_CH9 | Yes | — | — | — | CMP5_P | LVTTL4_IN | — | — |
| ADC5 | ADC1_CH10 | Yes | — | — | — | CMP5_N | LVTTL5_IN | SDDM2_OUT | — |
| ADC6 | ADC1_CH11 | Yes | — | — | — | CMP7_P | LVTTL6_IN | — | — |
| ADC7 | ADC1_CH12 | Yes | — | — | — | CMP7_N | LVTTL7_IN | SDDM3_OUT | — |
| ADC8 | ADC2_CH9 | Yes | — | — | — | CMP9_P | LVTTL8_IN | — | — |
| ADC9 | ADC2_CH10 | Yes | — | — | — | CMP9_N | LVTTL9_IN | SDDM4_OUT | — |
| ADC10 | ADC2_CH11 | Yes | — | — | — | — | LVTTL10_IN | — | — |
| ADC11 | ADC2_CH12 | Yes | — | — | — | — | LVTTL11_IN | — | — |
| CM0 | ADC0_CH3 | Yes | — | CM0_H | — | CMP0_P | — | — | — |
| CM1 | ADC0_CH7 | Yes | — | CM1_H | — | CMP2_P | — | — | — |
| CM2 | ADC1_CH3 | Yes | — | CM2_H | — | CMP4_P | — | — | — |
| CM3 | ADC1_CH7 | Yes | — | CM3_H | — | CMP6_P | — | — | — |
| CM4 | ADC2_CH3 | Yes | — | CM4_H | — | CMP8_P | — | — | — |
| SDD0 | ADC0_CH15 | — | — | — | — | — | — | — | SDD0_OUT |
| SDD1 | ADC1_CH15 | — | — | — | — | — | — | — | SDD1_OUT |
| SDD2 | ADC2_CH15 | — | — | — | — | — | — | — | SDD2_OUT |
| TM0 | ADC0_CH4 | Yes | — | CM0_L | TM0_IO | CMP0_N | — | — | — |
| TM1 | ADC0_CH8 | Yes | — | CM1_L | TM1_IO | CMP2_N | — | — | — |
| TM2 | ADC1_CH4 | Yes | — | CM2_L | TM2_IO | CMP4_N | — | — | — |
| TM3 | ADC1_CH8 | Yes | — | CM3_L | TM3_IO | CMP6_N | — | — | — |
| TM4 | ADC2_CH4 | Yes | — | CM4_L | TM4_IO | CMP8_N | — | — | — |

**Notes:**

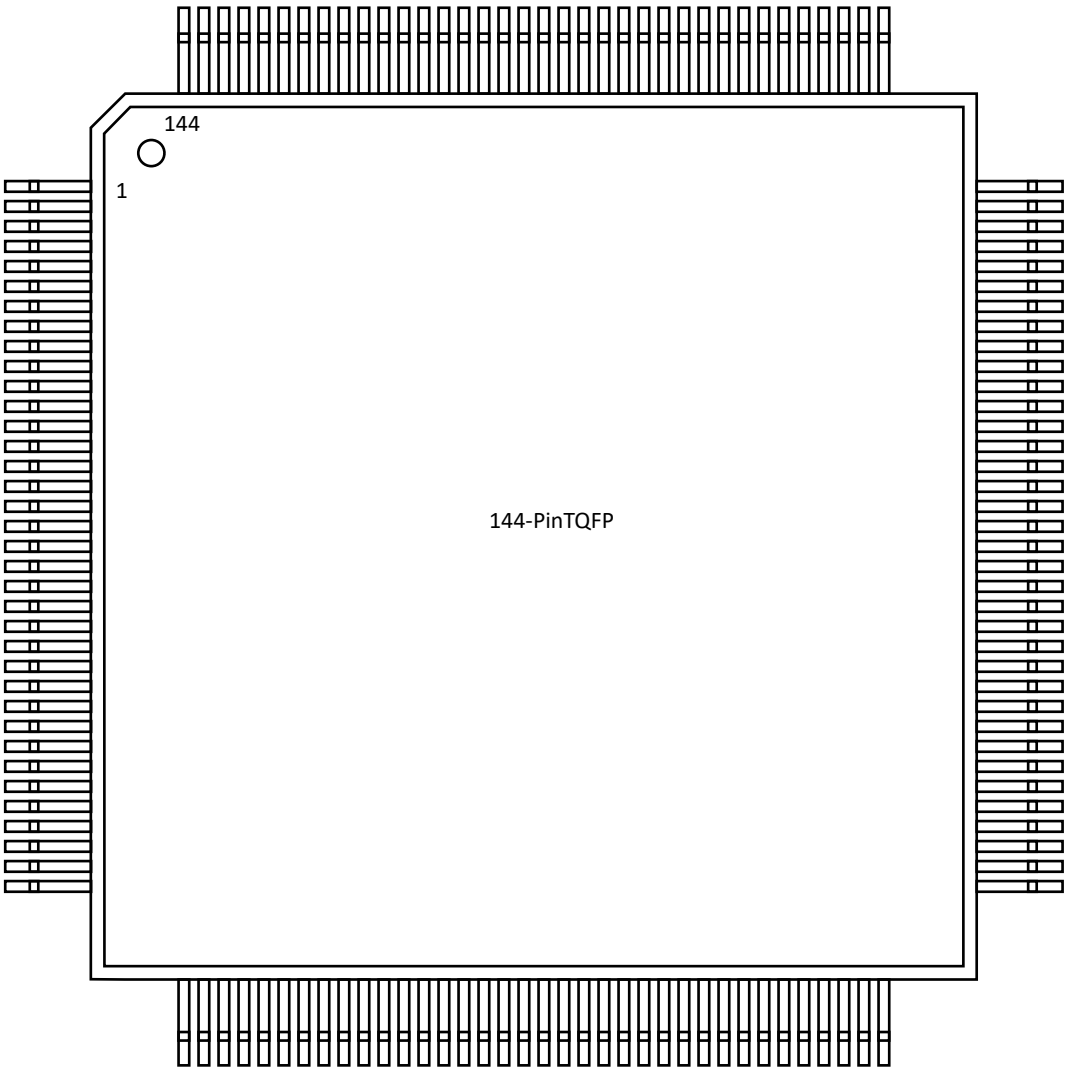
1. ABPSx_IN: Input to active bipolar prescaler channel x.
2. CMx_H/L: Current monitor channel x, high/low side.
3. TMx_IO: Temperature monitor channel x.
4. CMPx_P/N: Comparator channel x, positive/negative input.
5. LVTTLx_IN: LVTTL I/O channel x.
6. SDDMx_OUT: Output from sigma-delta DAC MUX channel x.
7. SDDx_OUT: Direct output from sigma-delta DAC channel x.

# 22. Pin Assignment Tables (Ask a Question)

## 22.1 Pin Assignment Tables (Ask a Question)

### TQ144

**Figure 22-1.** TQ144




**Note:** For Package Manufacturing and Environmental information, visit the Resource Center at www.microchip.com/en-us/support/package-drawings/fpga-packaging.

**Table 22-1.** TQ144

| TQ144 | |
|---|---|
| Pin Number | A2F060[1] Function |
| 1 | VCCPLL0 |
| 2 | VCOMPLA0 |

| .....continued | |
|---|---|
| TQ144 | |
| Pin Number | A2F060[1] Function |
| 3 | GNDQ |
| 4 | GFA2/IO42PDB5V0 |
| 5 | GFB2/IO42NDB5V0 |
| 6 | GFC2/IO41PDB5V0 |
| 7 | IO41NDB5V0 |
| 8 | VCC |
| 9 | GND |
| 10 | VCCFPGAIOB5 |
| 11 | IO38PDB5V0 |
| 12 | IO38NDB5V0 |
| 13 | IO36PDB5V0 |
| 14 | IO36NDB5V0 |
| 15 | GND |
| 16 | GNDRCOSC |
| 17 | VCCRCOSC |
| 18 | MSS_RESET_N |
| 19 | GPIO_0/IO33RSB4V0 |
| 20 | GPIO_1/IO32RSB4V0 |
| 21 | GPIO_2/IO31RSB4V0 |
| 22 | GPIO_3/IO30RSB4V0 |
| 23 | GPIO_4/IO29RSB4V0 |
| 24 | GND |
| 25 | VCCMSSIOB4 |
| 26 | VCC |
| 27 | GPIO_5/IO28RSB4V0 |
| 28 | GPIO_6/IO27RSB4V0 |
| 29 | GPIO_7/IO26RSB4V0 |
| 30 | GPIO_8/IO25RSB4V0 |
| 31 | VCCESRAM |
| 32 | GNDSDD0 |
| 33 | VCC33SDD0 |
| 34 | VCC15A |
| 35 | PCAP |
| 36 | NCAP |
| 37 | VCC33AP |
| 38 | VCC33N |
| 39 | SDD0 |
| 40 | GNDA |
| 41 | GNDAQ |
| 42 | GNDAQ |
| 43 | ADC0 |
| 44 | ADC1 |
| 45 | ADC2 |
| 46 | ADC3 |

| .....continued | |
|---|---|
| TQ144 | |
| Pin Number | A2F060[1] Function |
| 47 | ADC4 |
| 48 | ADC5 |
| 49 | ADC6 |
| 50 | ADC7 |
| 51 | ADC8 |
| 52 | ADC9 |
| 53 | ADC10 |
| 54 | NC |
| 55 | NC |
| 56 | NC |
| 57 | GND15ADC0 |
| 58 | VCC15ADC0 |
| 59 | GND33ADC0 |
| 60 | VCC33ADC0 |
| 61 | GND33ADC0 |
| 62 | VAREF0 |
| 63 | ABPS0 |
| 64 | ABPS1 |
| 65 | CM0 |
| 66 | TM0 |
| 67 | GNDTM0 |
| 68 | GNDAQ |
| 69 | GNDA |
| 70 | GNDVAREF |
| 71 | VAREFOUT |
| 72 | PU_N |
| 73 | VCC33A |
| 74 | PTEM |
| 75 | PTBASE |
| 76 | SPI_0_DO/GPIO_16 |
| 77 | SPI_0_DI/GPIO_17 |
| 78 | SPI_0_CLK/GPIO_18 |
| 79 | SPI_0_SS/GPIO_19 |
| 80 | UART_0_RXD/GPIO_21 |
| 81 | UART_0_TXD/GPIO_20 |
| 82 | UART_1_RXD/GPIO_29 |
| 83 | UART_1_TXD/GPIO_28 |
| 84 | VCC |
| 85 | VCCMSSIOB2 |
| 86 | GND |
| 87 | I2C_1_SDA/GPIO_30 |
| 88 | I2C_1_SCL/GPIO_31 |
| 89 | I2C_0_SDA/GPIO_22 |
| 90 | I2C_0_SCL/GPIO_23 |

| .....continued | |
|---|---|
| **TQ144** | |
| **Pin Number** | **A2F060[1] Function** |
| 91 | GNDENVM |
| 92 | VCCENVM |
| 93 | JTAGSEL |
| 94 | TCK |
| 95 | TDI |
| 96 | TMS |
| 97 | TDO |
| 98 | TRSTB |
| 99 | VJTAG |
| 100 | VDDBAT |
| 101 | VCCLPXTAL |
| 102 | LPXOUT |
| 103 | LPXIN |
| 104 | GNDLPXTAL |
| 105 | GNDMAINXTAL |
| 106 | MAINXOUT |
| 107 | MAINXIN |
| 108 | VCCMAINXTAL |
| 109 | VPP |
| 110 | GNDQ |
| 111 | GCA1/IO20PDB0V0 |
| 112 | GCA0/IO20NDB0V0 |
| 113 | GCB1/IO19PDB0V0 |
| 114 | GCB0/IO19NDB0V0 |
| 115 | GCC1/IO18PDB0V0 |
| 116 | GCC0/IO18NDB0V0 |
| 117 | VCCFPGAIOB0 |
| 118 | GND |
| 119 | VCC |
| 120 | IO14PDB0V0 |
| 121 | IO14NDB0V0 |
| 122 | IO13NSB0V0 |
| 123 | IO11PDB0V0 |
| 124 | IO11NDB0V0 |
| 125 | IO09PDB0V0 |
| 126 | IO09NDB0V0 |
| 127 | VCCFPGAIOB0 |
| 128 | GND |
| 129 | IO07PDB0V0 |
| 130 | IO07NDB0V0 |
| 131 | IO06PDB0V0 |
| 132 | IO06NDB0V0 |
| 133 | IO05PDB0V0 |
| 134 | IO05NDB0V0 |

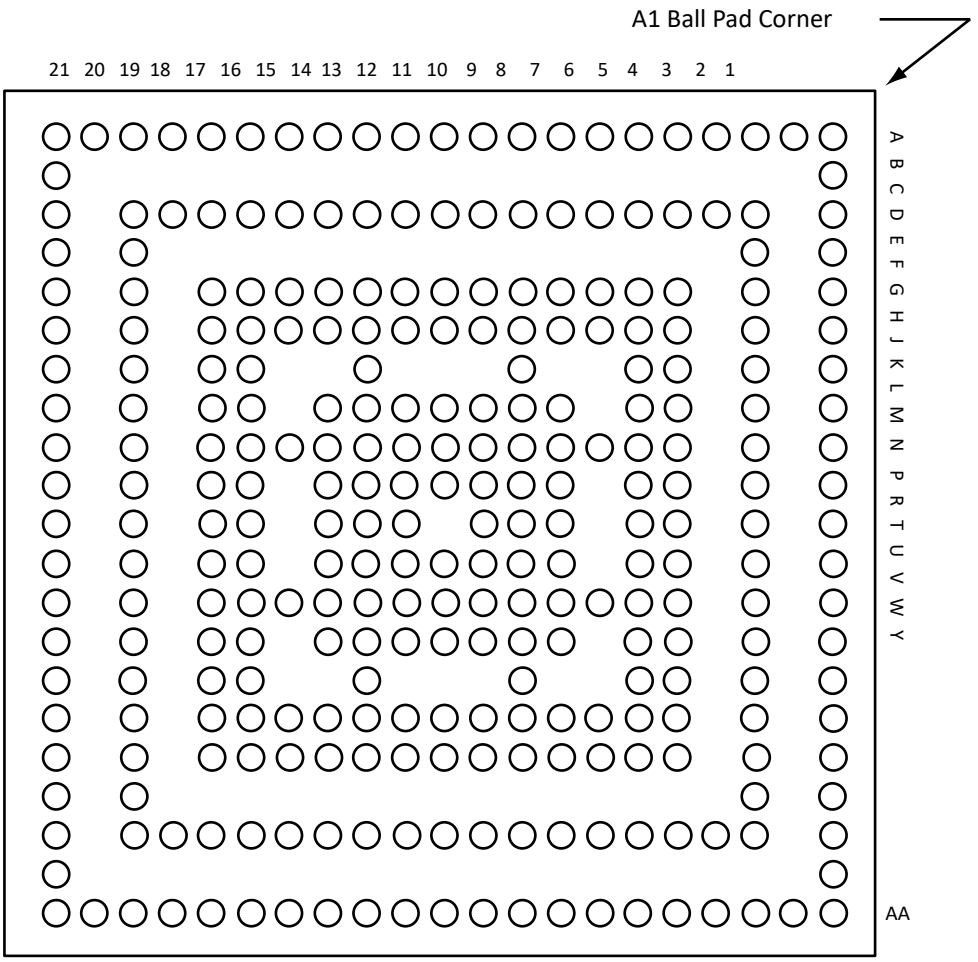
| .....continued | |
|---|---|
| TQ144 | |
| Pin Number | A2F060[1] Function |
| 135 | IO03PDB0V0 |
| 136 | IO03NDB0V0 |
| 137 | VCCFPGAIOB0 |
| 138 | GND |
| 139 | VCC |
| 140 | IO01PDB0V0 |
| 141 | IO01NDB0V0 |
| 142 | IO00PDB0V0 |
| 143 | IO00NDB0V0 |
| 144 | GNDQ |

**Note:**

1. Part No A2F060 is discontinued.

## CS288

**Figure 22-2.** CS288 (Bottom View)



**Note:** For Package Manufacturing and Environmental information, visit the Resource Center at www.microchip.com/en-us/support/package-drawings/fpga-packaging.

**Table 22-2.** CS288

| Pin No. | CS288 | | |
|---|---|---|---|
| | A2F060 [1] Function | A2F200 Function | A2F500 Function |
| A1[2] | VCCFPGAIOB0 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| A2 | GNDQ | GNDQ | GNDQ |
| A3[2] | EMC_CLK/IO00NDB0V0 | EMC_CLK/GAA0/IO00NDB0V0 | EMC_CLK/GAA0/IO02NDB0V0 |
| A4[2] | EMC_RW_N/IO00PDB0V0 | EMC_RW_N/GAA1/IO00PDB0V0 | EMC_RW_N/GAA1/IO02PDB0V0 |
| A5 | GND | GND | GND |
| A6[2] | EMC_CS1_N/IO01PDB0V0 | EMC_CS1_N/GAB1/IO01PDB0V0 | EMC_CS1_N/GAB1/IO05PDB0V0 |
| A7[2] | EMC_CS0_N/IO01NDB0V0 | EMC_CS0_N/GAB0/IO01NDB0V0 | EMC_CS0_N/GAB0/IO05NDB0V0 |
| A8[2] | EMC_AB[0]/IO04NPB0V0 | EMC_AB[0]/IO04NPB0V0 | EMC_AB[0]/IO06NPB0V0 |
| A9 | VCCFPGAIOB0 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| A10[2] | EMC_AB[4]/IO06NDB0V0 | EMC_AB[4]/IO06NDB0V0 | EMC_AB[4]/IO10NDB0V0 |
| A11[2] | EMC_AB[8]/IO08NPB0V0 | EMC_AB[8]/IO08NPB0V0 | EMC_AB[8]/IO13NPB0V0 |
| A12[2] | EMC_AB[14]/IO11NPB0V0 | EMC_AB[14]/IO11NPB0V0 | EMC_AB[14]/IO15NPB0V0 |
| A13 | GND | GND | GND |
| A14[2] | EMC_AB[18]/IO13NDB0V0 | EMC_AB[18]/IO13NDB0V0 | EMC_AB[18]/IO18NDB0V0 |
| A15[2] | EMC_AB[24]/IO16NDB0V0 | EMC_AB[24]/IO16NDB0V0 | EMC_AB[24]/IO20NDB0V0 |
| A16[2] | EMC_AB[25]/IO16PDB0V0 | EMC_AB[25]/IO16PDB0V0 | EMC_AB[25]/IO20PDB0V0 |
| A17 | VCCFPGAIOB0 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| A18[2] | EMC_AB[20]/IO14NDB0V0 | EMC_AB[20]/IO14NDB0V0 | EMC_AB[20]/IO21NDB0V0 |
| A19[2] | EMC_AB[21]/IO14PDB0V0 | EMC_AB[21]/IO14PDB0V0 | EMC_AB[21]/IO21PDB0V0 |
| A20 | GNDQ | GNDQ | GNDQ |
| A21 | GND | GND | GND |
| AA1[2] | ADC1 | ABPS1 | ABPS1 |
| AA2 | GNDAQ | GNDAQ | GNDAQ |
| AA3 | GNDA | GNDA | GNDA |
| AA4 | VCC33N | VCC33N | VCC33N |
| AA5 | SDD0 | SDD0 | SDD0 |
| AA6[2] | ADC0 | ABPS0 | ABPS0 |
| AA7[2] | NC | GNDTM0 | GNDTM0 |
| AA8[2] | NC | ABPS2 | ABPS2 |
| AA9[2] | NC | VAREF0 | VAREF0 |
| AA10[2] | NC | GND15ADC0 | GND15ADC0 |
| AA11[2] | ADC9 | ADC6 | ADC6 |
| AA12[2] | ABPS1 | ABPS7 | ABPS7 |
| AA13[2] | ADC6 | TM2 | TM2 |
| AA14[2] | NC | ABPS4 | ABPS4 |
| AA15[2] | NC | SDD1 | SDD1 |
| AA16 | GNDVAREF | GNDVAREF | GNDVAREF |
| AA17 | VAREFOUT | VAREFOUT | VAREFOUT |
| AA18 | PU_N | PU_N | PU_N |
| AA19 | VCC33A | VCC33A | VCC33A |
| AA20 | PTEM | PTEM | PTEM |
| AA21 | GND | GND | GND |

**.....continued**

| Pin No. | CS288 | | |
|---|---|---|---|
| | A2F060 [1] Function | A2F200 Function | A2F500 Function |
| B1 | GND | GND | GND |
| B21[2] | IO17PDB0V0 | GBB2/IO20NDB1V0 | GBB2/IO27NDB1V0 |
| C1[2] | EMC_DB[15]/IO45PDB5V0 | EMC_DB[15]/GAA2/IO71PDB5V0 | EMC_DB[15]/GAA2/IO88PDB5V0 |
| C3[2] | VCOMPLA0 | VCOMPLA | VCOMPLA0 |
| C4[2] | VCCPLL0 | VCCPLL | VCCPLL0 |
| C5 | VCCFPGAIOB0 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| C6[2] | EMC_AB[1]/IO04PPB0V0 | EMC_AB[1]/IO04PPB0V0 | EMC_AB[1]/IO06PPB0V0 |
| C7 | GND | GND | GND |
| C8[2] | EMC_OEN0_N/IO03NDB0V0 | EMC_OEN0_N/IO03NDB0V0 | EMC_OEN0_N/IO08NDB0V0 |
| C9[2] | EMC_AB[2]/IO05NDB0V0 | EMC_AB[2]/IO05NDB0V0 | EMC_AB[2]/IO09NDB0V0 |
| C10[2] | EMC_AB[5]/IO06PDB0V0 | EMC_AB[5]/IO06PDB0V0 | EMC_AB[5]/IO10PDB0V0 |
| C11 | VCCFPGAIOB0 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| C12[2] | EMC_AB[9]/IO08PPB0V0 | EMC_AB[9]/IO08PPB0V0 | EMC_AB[9]/IO13PPB0V0 |
| C13[2] | EMC_AB[15]/IO11PPB0V0 | EMC_AB[15]/IO11PPB0V0 | EMC_AB[15]/IO15PPB0V0 |
| C14[2] | EMC_AB[19]/IO13PDB0V0 | EMC_AB[19]/IO13PDB0V0 | EMC_AB[19]/IO18PDB0V0 |
| C15 | GND | GND | GND |
| C16[2] | EMC_AB[22]/IO15NDB0V0 | EMC_AB[22]/IO15NDB0V0 | EMC_AB[22]/IO19NDB0V0 |
| C17[2] | EMC_AB[23]/IO15PDB0V0 | EMC_AB[23]/IO15PDB0V0 | EMC_AB[23]/IO19PDB0V0 |
| C18[2] | NC | NC | VCCPLL1 |
| C19[2] | NC | NC | VCOMPLA1 |
| C21[2] | IO17NDB0V0 | GBA2/IO20PDB1V0 | GBA2/IO27PDB1V0 |
| D1[2] | EMC_DB[14]/IO45NDB5V0 | EMC_DB[14]/GAB2/IO71NDB5V0 | EMC_DB[14]/GAB2/IO88NDB5V0 |
| D3 | VCCFPGAIOB5 | VCCFPGAIOB5 | VCCFPGAIOB5 |
| D19 | GND | GND | GND |
| D21 | VCCFPGAIOB1 | VCCFPGAIOB1 | VCCFPGAIOB1 |
| E1[2] | EMC_DB[13]/IO44PDB5V0 | EMC_DB[13]/GAC2/IO70PDB5V0 | EMC_DB[13]/GAC2/IO87PDB5V0 |
| E3[2] | EMC_DB[12]/IO44NDB5V0 | EMC_DB[12]/IO70NDB5V0 | EMC_DB[12]/IO87NDB5V0 |
| E5 | GNDQ | GNDQ | GNDQ |
| E6[2] | EMC_BYTEN[0]/IO02NDB0V0 | EMC_BYTEN[0]/GAC0/IO02NDB0V0 | EMC_BYTEN[0]/GAC0/IO07NDB0V0 |
| E7[2] | EMC_BYTEN[1]/IO02PDB0V0 | EMC_BYTEN[1]/GAC1/IO02PDB0V0 | EMC_BYTEN[1]/GAC1/IO07PDB0V0 |
| E8[2] | EMC_OEN1_N/IO03PDB0V0 | EMC_OEN1_N/IO03PDB0V0 | EMC_OEN1_N/IO08PDB0V0 |
| E9[2] | EMC_AB[3]/IO05PDB0V0 | EMC_AB[3]/IO05PDB0V0 | EMC_AB[3]/IO09PDB0V0 |
| E10[2] | EMC_AB[10]/IO09NDB0V0 | EMC_AB[10]/IO09NDB0V0 | EMC_AB[10]/IO11NDB0V0 |
| E11[2] | EMC_AB[7]/IO07PDB0V0 | EMC_AB[7]/IO07PDB0V0 | EMC_AB[7]/IO12PDB0V0 |
| E12[2] | EMC_AB[13]/IO10PDB0V0 | EMC_AB[13]/IO10PDB0V0 | EMC_AB[13]/IO14PDB0V0 |
| E13[2] | EMC_AB[16]/IO12NDB0V0 | EMC_AB[16]/IO12NDB0V0 | EMC_AB[16]/IO17NDB0V0 |
| E14[2] | EMC_AB[17]/IO12PDB0V0 | EMC_AB[17]/IO12PDB0V0 | EMC_AB[17]/IO17PDB0V0 |
| E15[2] | GCC0/IO18NPB0V0 | GCB0/IO27NDB1V0 | GCB0/IO34NDB1V0 |
| E16[2] | GCA1/IO20PPB0V0 | GCB1/IO27PDB1V0 | GCB1/IO34PDB1V0 |
| E17[2] | GCC1/IO18PPB0V0 | GCB2/IO24PDB1V0 | GCB2/IO33PDB1V0 |
| E19[2] | GCB2/IO22PPB1V0 | GCA0/IO28NDB1V0 | GCA0/IO36NDB1V0[2] |
| E21[2] | IO21NDB1V0 | GCA1/IO28PDB1V0 | GCA1/IO36PDB1V0[2] |
| F1 | VCCFPGAIOB5 | VCCFPGAIOB5 | VCCFPGAIOB5 |
| F3[2] | GFB2/IO42NDB5V0 | GFB2/IO68NDB5V0 | GFB2/IO85NDB5V0 |

**.....continued**

| Pin No. | CS288 | | |
|---|---|---|---|
| | A2F060 [1] Function | A2F200 Function | A2F500 Function |
| F5[2] | GFA2/IO42PDB5V0 | GFA2/IO68PDB5V0 | GFA2/IO85PDB5V0 |
| F6[2] | EMC_DB[11]/IO43PDB5V0 | EMC_DB[11]/IO69PDB5V0 | EMC_DB[11]/IO86PDB5V0 |
| F7 | GND | GND | GND |
| F8[2] | NC | GFC1/IO66PPB5V0 | GFC1/IO83PPB5V0 |
| F9 | VCCFPGAIOB0 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| F10[2] | EMC_AB[11]/IO09PDB0V0 | EMC_AB[11]/IO09PDB0V0 | EMC_AB[11]/IO11PDB0V0 |
| F11[2] | EMC_AB[6]/IO07NDB0V0 | EMC_AB[6]/IO07NDB0V0 | EMC_AB[6]/IO12NDB0V0 |
| F12[2] | EMC_AB[12]/IO10NDB0V0 | EMC_AB[12]/IO10NDB0V0 | EMC_AB[12]/IO14NDB0V0 |
| F13 | GND | GND | GND |
| F14[2] | GCB1/IO19PPB0V0 | GCC1/IO26PPB1V0 | GCC1/IO35PPB1V0 |
| F15 | GNDQ | GNDQ | GNDQ |
| F16 | VCCFPGAIOB1 | VCCFPGAIOB1 | VCCFPGAIOB1 |
| F17[2] | GCB0/IO19NPB0V0 | IO24NDB1V0 | IO33NDB1V0 |
| F19[2] | IO23NDB1V0 | GDB1/IO30PDB1V0 | GDB1/IO39PDB1V0 |
| F21[2] | GCA2/IO21PDB1V0 | GDB0/IO30NDB1V0 | GDB0/IO39NDB1V0 |
| G1[2] | IO41NDB5V0 | IO67NDB5V0 | IO84NDB5V0 |
| G3[2] | GFC2/IO41PDB5V0 | GFC2/IO67PDB5V0 | GFC2/IO84PDB5V0 |
| G5[2] | NC | GFB1/IO65PDB5V0 | GFB1/IO82PDB5V0 |
| G6[2] | EMC_DB[10]/IO43NDB5V0 | EMC_DB[10]/IO69NDB5V0 | EMC_DB[10]/IO86NDB5V0 |
| G9[2] | NC | GFC0/IO66NPB5V0 | GFC0/IO83NPB5V0 |
| G13[2] | GCA0/IO20NPB0V0 | GCC0/IO26NPB1V0 | GCC0/IO35NPB1V0 |
| G16[2] | NC | GDA0/IO31NDB1V0 | GDA0/IO40NDB1V0 |
| G17[2] | IO22NPB1V0 | GDC1/IO29PDB1V0 | GDC1/IO38PDB1V0 |
| G19[2] | GCC2/IO23PDB1V0 | GDC0/IO29NDB1V0 | GDC0/IO38NDB1V0 |
| G21 | GND | GND | GND |
| H1[2] | EMC_DB[9]/IO40PPB5V0 | EMC_DB[9]/GEC1/IO63PPB5V0 | EMC_DB[9]/GEC1/IO80PPB5V0 |
| H3 | GND | GND | GND |
| H5[2] | NC | GFB0/IO65NDB5V0 | GFB0/IO82NDB5V0 |
| H6[2] | EMC_DB[7]/IO39PDB5V0 | EMC_DB[7]/GEB1/IO62PDB5V0 | EMC_DB[7]/GEB1/IO79PDB5V0 |
| H8 | GND | GND | GND |
| H9 | VCC | VCC | VCC |
| H10 | GND | GND | GND |
| H11 | VCC | VCC | VCC |
| H12 | GND | GND | GND |
| H13 | VCC | VCC | VCC |
| H14 | GND | GND | GND |
| H16[2] | NC | GDA1/IO31PDB1V0 | GDA1/IO40PDB1V0 |
| H17[2] | NC | GDC2/IO32PPB1V0 | GDC2/IO41PPB1V0 |
| H19 | VCCFPGAIOB1 | VCCFPGAIOB1 | VCCFPGAIOB1 |
| H21[2] | NC | GDB2/IO33PDB1V0 | GDB2/IO42PDB1V0 |
| J1[2] | EMC_DB[4]/IO38NPB5V0 | EMC_DB[4]/GEA0/IO61NPB5V0 | EMC_DB[4]/GEA0/IO78NPB5V0 |
| J3[2] | EMC_DB[8]/IO40NPB5V0 | EMC_DB[8]/GEC0/IO63NPB5V0 | EMC_DB[8]/GEC0/IO80NPB5V0 |
| J5[2] | EMC_DB[1]/IO36PDB5V0 | EMC_DB[1]/GEB2/IO59PDB5V0 | EMC_DB[1]/GEB2/IO76PDB5V0 |
| J6[2] | EMC_DB[6]/IO39NDB5V0 | EMC_DB[6]/GEB0/IO62NDB5V0 | EMC_DB[6]/GEB0/IO79NDB5V0 |

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| Pin No. | CS288 | | |
|---|---|---|---|
| | A2F060 [1] Function | A2F200 Function | A2F500 Function |
| J7 | VCCFPGAIOB5 | VCCFPGAIOB5 | VCCFPGAIOB5 |
| J8 | VCC | VCC | VCC |
| J9 | GND | GND | GND |
| J10 | VCC | VCC | VCC |
| J11 | GND | GND | GND |
| J12 | VCC | VCC | VCC |
| J13 | GND | GND | GND |
| J14 | VCC | VCC | VCC |
| J15 | VPP | VPP | VPP |
| J16[2] | NC | IO32NPB1V0 | IO41NPB1V0 |
| J17 | NC | GNDQ | GNDQ |
| J19 | VCCMAINXTAL | VCCMAINXTAL | VCCMAINXTAL |
| J21[2] | NC | GDA2/IO33NDB1V0 | GDA2/IO42NDB1V0 |
| K1 | GND | GND | GND |
| K3[2] | EMC_DB[5]/IO38PPB5V0 | EMC_DB[5]/GEA1/IO61PPB5V0 | EMC_DB[5]/GEA1/IO78PPB5V0 |
| K5[2] | EMC_DB[0]/IO36NDB5V0 | EMC_DB[0]/GEA2/IO59NDB5V0 | EMC_DB[0]/GEA2/IO76NDB5V0 |
| K6[2] | EMC_DB[3]/IO37PPB5V0 | EMC_DB[3]/GEC2/IO60PPB5V0 | EMC_DB[3]/GEC2/IO77PPB5V0 |
| K8 | GND | GND | GND |
| K9 | VCC | VCC | VCC |
| K10 | GND | GND | GND |
| K11 | VCC | VCC | VCC |
| K12 | GND | GND | GND |
| K13 | VCC | VCC | VCC |
| K14 | GND | GND | GND |
| K16 | LPXOUT | LPXOUT | LPXOUT |
| K17 | GNDLPXTAL | GNDLPXTAL | GNDLPXTAL |
| K19 | GNDMAINXTAL | GNDMAINXTAL | GNDMAINXTAL |
| K21 | MAINXIN | MAINXIN | MAINXIN |
| L1 | GNDRCOSC | GNDRCOSC | GNDRCOSC |
| L3 | VCCFPGAIOB5 | VCCFPGAIOB5 | VCCFPGAIOB5 |
| L5[2] | EMC_DB[2]/IO37NPB5V0 | EMC_DB[2]/IO60NPB5V0 | EMC_DB[2]/IO77NPB5V0 |
| L6[2] | NC | GNDQ | GNDQ |
| L8 | VCC | VCC | VCC |
| L9 | GND | GND | GND |
| L10 | VCC | VCC | VCC |
| L12 | VCC | VCC | VCC |
| L13 | GND | GND | GND |
| L14 | VCC | VCC | VCC |
| L16 | VCCLPXTAL | VCCLPXTAL | VCCLPXTAL |
| L17 | VDDBAT | VDDBAT | VDDBAT |
| L19 | LPXIN | LPXIN | LPXIN |
| L21 | MAINXOUT | MAINXOUT | MAINXOUT |
| M1 | VCCRCOSC | VCCRCOSC | VCCRCOSC |
| M3 | MSS_RESET_N | MSS_RESET_N | MSS_RESET_N |

**.....continued**

| Pin No. | CS288 | | |
|---|---|---|---|
| | A2F060 [1] Function | A2F200 Function | A2F500 Function |
| M5[2] | GPIO_5/IO28RSB4V0 | GPIO_5/IO42RSB4V0 | GPIO_5/IO51RSB4V0 |
| M6 | GND | GND | GND |
| M8 | GND | GND | GND |
| M9 | VCC | VCC | VCC |
| M10 | GND | GND | GND |
| M11 | VCC | VCC | VCC |
| M12 | GND | GND | GND |
| M13 | VCC | VCC | VCC |
| M14 | GND | GND | GND |
| M16 | TMS | TMS | TMS |
| M17 | VJTAG | VJTAG | VJTAG |
| M19 | TDO | TDO | TDO |
| M21 | TRSTB | TRSTB | TRSTB |
| N1 | VCCMSSIOB4 | VCCMSSIOB4 | VCCMSSIOB4 |
| N3 | GND | GND | GND |
| N5[2] | GPIO_4/IO29RSB4V0 | GPIO_4/IO43RSB4V0 | GPIO_4/IO52RSB4V0 |
| N6[2] | GPIO_8/IO25RSB4V0 | GPIO_8/IO39RSB4V0 | GPIO_8/IO48RSB4V0 |
| N7[2] | GPIO_9/IO24RSB4V0 | GPIO_9/IO38RSB4V0 | GPIO_9/IO47RSB4V0 |
| N8 | VCC | VCC | VCC |
| N9 | GND | GND | GND |
| N10 | VCC | VCC | VCC |
| N11 | GND | GND | GND |
| N12 | VCC | VCC | VCC |
| N13 | GND | GND | GND |
| N14 | VCC | VCC | VCC |
| N15 | GND | GND | GND |
| N16 | TCK | TCK | TCK |
| N17 | TDI | TDI | TDI |
| N19 | GNDENVM | GNDENVM | GNDENVM |
| N21 | VCCENVM | VCCENVM | VCCENVM |
| P1[2] | GPIO_0/IO33RSB4V0 | MAC_MDC/IO48RSB4V0 | MAC_MDC/IO57RSB4V0 |
| P3[2] | GPIO_7/IO26RSB4V0 | GPIO_7/IO40RSB4V0 | GPIO_7/IO49RSB4V0 |
| P5[2] | GPIO_6/IO27RSB4V0 | GPIO_6/IO41RSB4V0 | GPIO_6/IO50RSB4V0 |
| P6 | VCCMSSIOB4 | VCCMSSIOB4 | VCCMSSIOB4 |
| P8 | GND | GND | GND |
| P9 | VCC | VCC | VCC |
| P10 | GND | GND | GND |
| P11 | VCC | VCC | VCC |
| P12 | GND | GND | GND |
| P13 | VCC | VCC | VCC |
| P14 | GND | GND | GND |
| P16 | JTAGSEL | JTAGSEL | JTAGSEL |
| P17 | I2C_0_SCL/GPIO_23 | I2C_0_SCL/GPIO_23 | I2C_0_SCL/GPIO_23 |
| P19 | VCCMSSIOB2 | VCCMSSIOB2 | VCCMSSIOB2 |

**.....continued**

| Pin No. | CS288 | | |
|---|---|---|---|
| | A2F060 [1] Function | A2F200 Function | A2F500 Function |
| P21 | GND | GND | GND |
| R1[2] | GPIO_2/IO31RSB4V0 | MAC_MDIO/IO49RSB4V0 | MAC_MDIO/IO58RSB4V0 |
| R3[2] | GPIO_1/IO32RSB4V0 | MAC_TXEN/IO52RSB4V0 | MAC_TXEN/IO61RSB4V0 |
| R5[2] | GPIO_3/IO30RSB4V0 | MAC_TXD[0]/IO56RSB4V0 | MAC_TXD[0]/IO65RSB4V0 |
| R6[2] | GPIO_10/IO35RSB4V0 | MAC_CRSDV/IO51RSB4V0 | MAC_CRSDV/IO60RSB4V0 |
| R9 | GNDA | GNDA | GNDA |
| R13 | GNDA | GNDA | GNDA |
| R16 | UART_1_RXD/GPIO_29 | UART_1_RXD/GPIO_29 | UART_1_RXD/GPIO_29 |
| R17 | UART_1_TXD/GPIO_28 | UART_1_TXD/GPIO_28 | UART_1_TXD/GPIO_28 |
| R19 | I2C_0_SDA/GPIO_22 | I2C_0_SDA/GPIO_22 | I2C_0_SDA/GPIO_22 |
| R21 | I2C_1_SDA/GPIO_30 | I2C_1_SDA/GPIO_30 | I2C_1_SDA/GPIO_30 |
| T1 | GND | GND | GND |
| T3[2] | NC | MAC_TXD[1]/IO55RSB4V0 | MAC_TXD[1]/IO64RSB4V0 |
| T5[2] | NC | MAC_RXD[1]/IO53RSB4V0 | MAC_RXD[1]/IO62RSB4V0 |
| T6[2] | GPIO_11/IO34RSB4V0 | MAC_RXER/IO50RSB4V0 | MAC_RXER/IO59RSB4V0 |
| T7[2] | NC | CM1 | CM1 |
| T8[2] | NC | ADC1 | ADC1 |
| T9[2] | NC | GND33ADC0 | GND33ADC0 |
| T10[2] | NC | VCC15ADC0 | VCC15ADC0 |
| T11[2] | GND33ADC0 | GND33ADC1 | GND33ADC1 |
| T12[2] | VAREF0 | VAREF1 | VAREF1 |
| T13[2] | ADC7 | ADC4 | ADC4 |
| T14[2] | TM0 | TM3 | TM3 |
| T15 | SPI_1_SS/GPIO_27 | SPI_1_SS/GPIO_27 | SPI_1_SS/GPIO_27 |
| T16 | VCCMSSIOB2 | VCCMSSIOB2 | VCCMSSIOB2 |
| T17 | UART_0_RXD/GPIO_21 | UART_0_RXD/GPIO_21 | UART_0_RXD/GPIO_21 |
| T19 | UART_0_TXD/GPIO_20 | UART_0_TXD/GPIO_20 | UART_0_TXD/GPIO_20 |
| T21 | I2C_1_SCL/GPIO_31 | I2C_1_SCL/GPIO_31 | I2C_1_SCL/GPIO_31 |
| U1[2] | NC | MAC_RXD[0]/IO54RSB4V0 | MAC_RXD[0]/IO63RSB4V0 |
| U3 | VCCMSSIOB4 | VCCMSSIOB4 | VCCMSSIOB4 |
| U5 | VCC33SDD0 | VCC33SDD0 | VCC33SDD0 |
| U6 | VCC15A | VCC15A | VCC15A |
| U7[2] | NC | ABPS3 | ABPS3 |
| U8[2] | NC | ADC2 | ADC2 |
| U9[2] | NC | VCC33ADC0 | VCC33ADC0 |
| U10[2] | GND15ADC0 | GND15ADC1 | GND15ADC1 |
| U11[2] | VCC33ADC0 | VCC33ADC1 | VCC33ADC1 |
| U12[2] | ADC10 | ADC7 | ADC7 |
| U13[2] | ABPS0 | ABPS6 | ABPS6 |
| U14[2] | GNDTM0 | GNDTM1 | GNDTM1 |
| U15 | SPI_1_CLK/GPIO_26 | SPI_1_CLK/GPIO_26 | SPI_1_CLK/GPIO_26 |
| U16 | SPI_0_CLK/GPIO_18 | SPI_0_CLK/GPIO_18 | SPI_0_CLK/GPIO_18 |
| U17 | SPI_0_SS/GPIO_19 | SPI_0_SS/GPIO_19 | SPI_0_SS/GPIO_19 |
| U19 | GND | GND | GND |

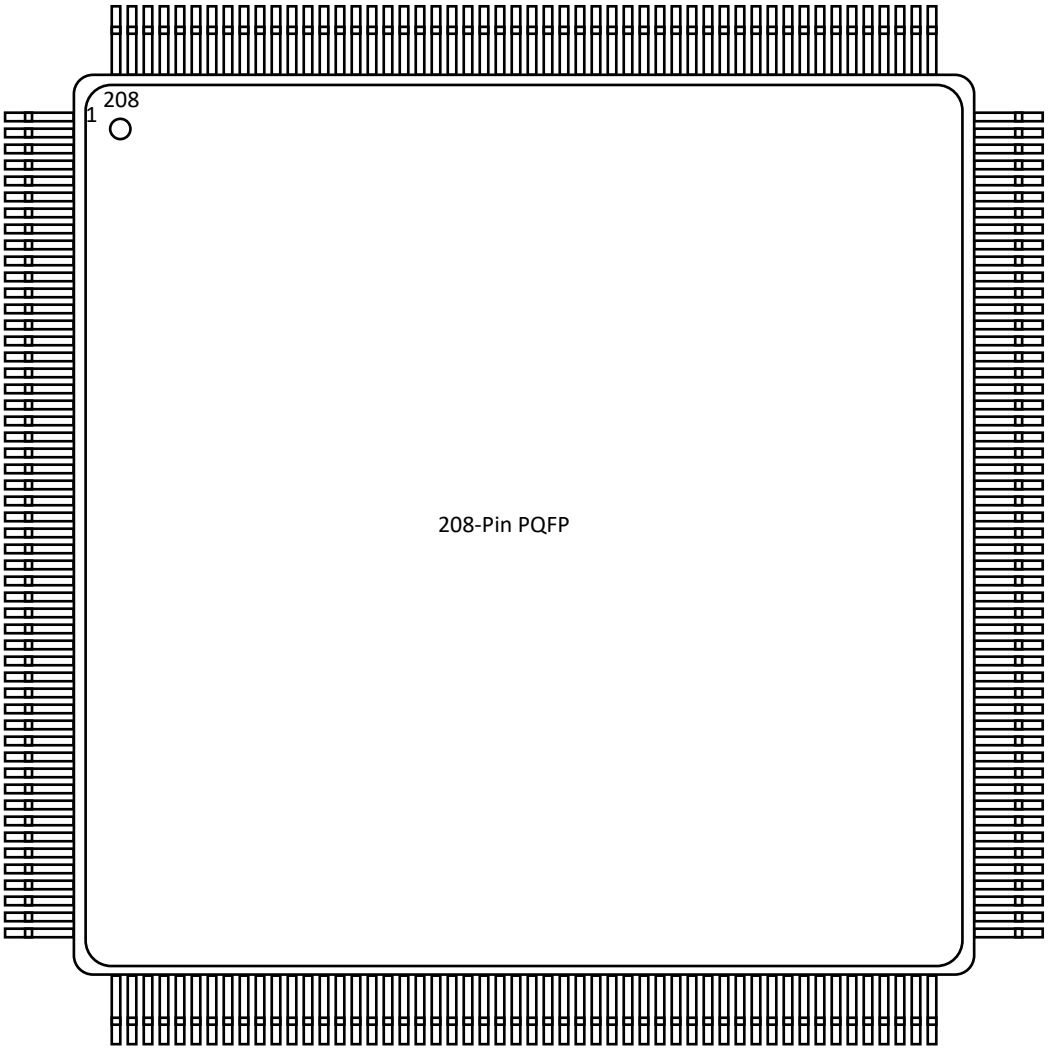
| .....continued | | | |
|---|---|---|---|
| Pin No. | CS288 | | |
| | A2F060 [1] Function | A2F200 Function | A2F500 Function |
| U21 | SPI_1_DO/GPIO_24 | SPI_1_DO/GPIO_24 | SPI_1_DO/GPIO_24 |
| V1[2] | NC | MAC_CLK | MAC_CLK |
| V3 | GNDSDD0 | GNDSDD0 | GNDSDD0 |
| V19 | SPI_1_DI/GPIO_25 | SPI_1_DI/GPIO_25 | SPI_1_DI/GPIO_25 |
| V21 | VCCMSSIOB2 | VCCMSSIOB2 | VCCMSSIOB2 |
| W1 | PCAP | PCAP | PCAP |
| W3 | NCAP | NCAP | NCAP |
| W4[2] | ADC2 | CM0 | CM0 |
| W5[2] | ADC3 | TM0 | TM0 |
| W6[2] | ADC4 | TM1 | TM1 |
| W7[2] | NC | ADC0 | ADC0 |
| W8[2] | NC | ADC3 | ADC3 |
| W9[2] | NC | GND33ADC0 | GND33ADC0 |
| W10[2] | VCC15ADC0 | VCC15ADC1 | VCC15ADC1 |
| W11[2] | GND33ADC0 | GND33ADC1 | GND33ADC1 |
| W12[2] | ADC8 | ADC5 | ADC5 |
| W13[2] | CM0 | CM3 | CM3 |
| W14[2] | ADC5 | CM2 | CM2 |
| W15[2] | NC | ABPS5 | ABPS5 |
| W16 | GNDAQ | GNDAQ | GNDAQ |
| W17[2] | NC | VCC33SDD1 | VCC33SDD1 |
| W18[2] | NC | GNDSDD1 | GNDSDD1 |
| W19 | PTBASE | PTBASE | PTBASE |
| W21 | SPI_0_DI/GPIO_17 | SPI_0_DI/GPIO_17 | SPI_0_DI/GPIO_17 |
| Y1 | VCC33AP | VCC33AP | VCC33AP |
| Y21 | SPI_0_DO/GPIO_16 | SPI_0_DO/GPIO_16 | SPI_0_DO/GPIO_16 |

**Notes:**

1. Part No A2F060 is discontinued.
2. Denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device. This note is applicable to entire row.
3. The signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the “Glitchless MUX” section in the SmartFusion Microcontroller Subsystem User’s Guide for more details.

## PQ208

**Figure 22-3.** PQ208




**Note:** For Package Manufacturing and Environmental information, visit the Resource Center at www.microchip.com/en-us/support/package-drawings/fpga-packaging.

**Table 22-3.** PQ208

| Pin Number | PQ208 | |
|---|---|---|
| | A2F200 | A2F500 |
| 1[1] | VCCPLL | VCCPLL0 |
| 2[1] | VCOMPLA | VCOMPLA0 |
| 3 | GNDQ | GNDQ |
| 4[1] | EMC_DB[15]/GAA2/IO71PDB5V0 | GAA2/IO88PDB5V0 |
| 5[1] | EMC_DB[14]/GAB2/IO71NDB5V0 | GAB2/IO88NDB5V0 |
| 6[1] | EMC_DB[13]/GAC2/IO70PDB5V0 | GAC2/IO87PDB5V0 |
| 7[1] | EMC_DB[12]/IO70NDB5V0 | IO87NDB5V0 |

| .....continued | | |
|---|---|---|
| Pin Number | PQ208 | |
| | A2F200 | A2F500 |
| 8 | VCC | VCC |
| 9 | GND | GND |
| 10 | VCCFPGAIOB5 | VCCFPGAIOB5 |
| 11[1] | EMC_DB[11]/IO69PDB5V0 | IO86PDB5V0 |
| 12[1] | EMC_DB[10]/IO69NDB5V0 | IO86NDB5V0 |
| 13[1] | GFA2/IO68PSB5V0 | GFA2/IO85PSB5V0 |
| 14[1] | GFA1/IO64PDB5V0 | GFA1/IO81PDB5V0 |
| 15[1] | GFA0/IO64NDB5V0 | GFA0/IO81NDB5V0 |
| 16[1] | EMC_DB[9]/GEC1/IO63PDB5V0 | GEC1/IO80PDB5V0 |
| 17[1] | EMC_DB[8]/GEC0/IO63NDB5V0 | GEC0/IO80NDB5V0 |
| 18[1] | EMC_DB[7]/GEB1/IO62PDB5V0 | GEB1/IO79PDB5V0 |
| 19[1] | EMC_DB[6]/GEB0/IO62NDB5V0 | GEB0/IO79NDB5V0 |
| 20[1] | EMC_DB[5]/GEA1/IO61PDB5V0 | GEA1/IO78PDB5V0 |
| 21[1] | EMC_DB[4]/GEA0/IO61NDB5V0 | GEA0/IO78NDB5V0 |
| 22 | VCC | VCC |
| 23 | GND | GND |
| 24 | VCCFPGAIOB5 | VCCFPGAIOB5 |
| 25[1] | EMC_DB[3]/GEC2/IO60PDB5V0 | GEC2/IO77PDB5V0 |
| 26[1] | EMC_DB[2]/IO60NDB5V0 | IO77NDB5V0 |
| 27[1] | EMC_DB[1]/GEB2/IO59PDB5V0 | GEB2/IO76PDB5V0 |
| 28[1] | EMC_DB[0]/GEA2/IO59NDB5V0 | GEA2/IO76NDB5V0 |
| 29 | VCC | VCC |
| 30 | GND | GND |
| 31 | GNDRCOSC | GNDRCOSC |
| 32 | VCCRCOSC | VCCRCOSC |
| 33 | MSS_RESET_N | MSS_RESET_N |
| 34 | VCCESRAM | VCCESRAM |
| 35[1] | MAC_MDC/IO48RSB4V0 | MAC_MDC/IO57RSB4V0 |
| 36[1] | MAC_MDIO/IO49RSB4V0 | MAC_MDIO/IO58RSB4V0 |
| 37[1] | MAC_TXEN/IO52RSB4V0 | MAC_TXEN/IO61RSB4V0 |
| 38[1] | MAC_CRSDV/IO51RSB4V0 | MAC_CRSDV/IO60RSB4V0 |
| 39[1] | MAC_RXER/IO50RSB4V0 | MAC_RXER/IO59RSB4V0 |
| 40 | GND | GND |
| 41 | VCCMSSIOB4 | VCCMSSIOB4 |
| 42 | VCC | VCC |
| 43[1] | MAC_TXD[0]/IO56RSB4V0 | MAC_TXD[0]/IO65RSB4V0 |
| 44[1] | MAC_TXD[1]/IO55RSB4V0 | MAC_TXD[1]/IO64RSB4V0 |
| 45[1] | MAC_RXD[0]/IO54RSB4V0 | MAC_RXD[0]/IO63RSB4V0 |
| 46[1] | MAC_RXD[1]/IO53RSB4V0 | MAC_RXD[1]/IO62RSB4V0 |
| 47 | MAC_CLK | MAC_CLK |
| 48 | GNDSDD0 | GNDSDD0 |
| 49 | VCC33SDD0 | VCC33SDD0 |
| 50 | VCC15A | VCC15A |
| 51 | PCAP | PCAP |

| .....continued | | |
|---|---|---|
| Pin Number | PQ208 | |
| | A2F200 | A2F500 |
| 52 | NCAP | NCAP |
| 53 | VCC33AP | VCC33AP |
| 54 | VCC33N | VCC33N |
| 55 | SDD0 | SDD0 |
| 56 | GNDA | GNDA |
| 57 | GNDAQ | GNDAQ |
| 58 | ABPS0 | ABPS0 |
| 59 | ABPS1 | ABPS1 |
| 60 | CM0 | CM0 |
| 61 | TM0 | TM0 |
| 62 | GNDTM0 | GNDTM0 |
| 63 | TM1 | TM1 |
| 64 | CM1 | CM1 |
| 65 | ABPS3 | ABPS3 |
| 66 | ABPS2 | ABPS2 |
| 67 | ADC0 | ADC0 |
| 68 | ADC1 | ADC1 |
| 69 | ADC2 | ADC2 |
| 70 | ADC3 | ADC3 |
| 71 | VAREF0 | VAREF0 |
| 72 | GND33ADC0 | GND33ADC0 |
| 73 | VCC33ADC0 | VCC33ADC0 |
| 74 | GND33ADC0 | GND33ADC0 |
| 75 | VCC15ADC0 | VCC15ADC0 |
| 76 | GND15ADC0 | GND15ADC0 |
| 77 | GND15ADC1 | GND15ADC1 |
| 78 | VCC15ADC1 | VCC15ADC1 |
| 79 | GND33ADC1 | GND33ADC1 |
| 80 | VCC33ADC1 | VCC33ADC1 |
| 81 | GND33ADC1 | GND33ADC1 |
| 82 | VAREF1 | VAREF1 |
| 83 | ADC7 | ADC7 |
| 84 | ADC6 | ADC6 |
| 85 | ADC5 | ADC5 |
| 86 | ADC4 | ADC4 |
| 87 | ABPS6 | ABPS6 |
| 88 | ABPS7 | ABPS7 |
| 89 | CM3 | CM3 |
| 90 | TM3 | TM3 |
| 91 | GNDTM1 | GNDTM1 |
| 92 | TM2 | TM2 |
| 93 | CM2 | CM2 |
| 94 | ABPS5 | ABPS5 |
| 95 | ABPS4 | ABPS4 |

**.....continued**

| Pin Number | PQ208 | |
|---|---|---|
| | A2F200 | A2F500 |
| 96 | GNDAQ | GNDAQ |
| 97 | GNDA | GNDA |
| 98 | NC | NC |
| 99 | GNDVAREF | GNDVAREF |
| 100 | VAREFOUT | VAREFOUT |
| 101 | PU_N | PU_N |
| 102 | VCC33A | VCC33A |
| 103 | PTEM | PTEM |
| 104 | PTBASE | PTBASE |
| 105 | SPI_0_DO/GPIO_16 | SPI_0_DO/GPIO_16 |
| 106 | SPI_0_DI/GPIO_17 | SPI_0_DI/GPIO_17 |
| 107 | SPI_0_CLK/GPIO_18 | SPI_0_CLK/GPIO_18 |
| 108 | SPI_0_SS/GPIO_19 | SPI_0_SS/GPIO_19 |
| 109 | UART_0_RXD/GPIO_21 | UART_0_RXD/GPIO_21 |
| 110 | UART_0_TXD/GPIO_20 | UART_0_TXD/GPIO_20 |
| 111 | UART_1_RXD/GPIO_29 | UART_1_RXD/GPIO_29 |
| 112 | UART_1_TXD/GPIO_28 | UART_1_TXD/GPIO_28 |
| 113 | VCC | VCC |
| 114 | VCCMSSIOB2 | VCCMSSIOB2 |
| 115 | GND | GND |
| 116 | I2C_1_SDA/GPIO_30 | I2C_1_SDA/GPIO_30 |
| 117 | I2C_1_SCL/GPIO_31 | I2C_1_SCL/GPIO_31 |
| 118 | I2C_0_SDA/GPIO_22 | I2C_0_SDA/GPIO_22 |
| 119 | I2C_0_SCL/GPIO_23 | I2C_0_SCL/GPIO_23 |
| 120 | GNDENVM | GNDENVM |
| 121 | VCCENVM | VCCENVM |
| 122 | JTAGSEL | JTAGSEL |
| 123 | TCK | TCK |
| 124 | TDI | TDI |
| 125 | TMS | TMS |
| 126 | TDO | TDO |
| 127 | TRSTB | TRSTB |
| 128 | VJTAG | VJTAG |
| 129 | VDDBAT | VDDBAT |
| 130 | VCCLPXTAL | VCCLPXTAL |
| 131 | LPXOUT | LPXOUT |
| 132 | LPXIN | LPXIN |
| 133 | GNDLPXTAL | GNDLPXTAL |
| 134 | GNDMAINXTAL | GNDMAINXTAL |
| 135 | MAINXOUT | MAINXOUT |
| 136 | MAINXIN | MAINXIN |
| 137 | VCCMAINXTAL | VCCMAINXTAL |
| 138 | GND | GND |
| 139 | VCC | VCC |

**.....continued**

| Pin Number | PQ208 | |
|---|---|---|
| | A2F200 | A2F500 |
| 140 | VPP | VPP |
| 141 | VCCFPGAIOB1 | VCCFPGAIOB1 |
| 142[1] | GDA0/IO31NDB1V0 | GDA0/IO40NDB1V0 |
| 143[1] | GDA1/IO31PDB1V0 | GDA1/IO40PDB1V0 |
| 144[1] | GDC0/IO29NSB1V0 | GDC0/IO38NSB1V0 |
| 145[1] | GCA0/IO28NDB1V0 | GCA0/IO36NDB1V0 [2] |
| 146[1] | GCA1/IO28PDB1V0 | GCA1/IO36PDB1V0[2] |
| 147 | VCCFPGAIOB1 | VCCFPGAIOB1 |
| 148 | GND | GND |
| 149 | VCC | VCC |
| 150[1] | IO25NDB1V0 | IO30NDB1V0 |
| 151[1] | GCC2/IO25PDB1V0 | GBC2/IO30PDB1V0 |
| 152[1] | IO23NDB1V0 | IO28NDB1V0 |
| 153[1] | GCA2/IO23PDB1V0 | GCA2/IO28PDB1V0[2] |
| 154[1] | GBC2/IO21PSB1V0 | GBB2/IO27NDB1V0 |
| 155[1] | GBA2/IO20PSB1V0 | GBA2/IO27PDB1V0 |
| 156 | GNDQ | GNDQ |
| 157 | GNDQ | GNDQ |
| 158 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| 159[1] | GBA1/IO19PDB0V0 | GBA1/IO23PDB0V0 |
| 160[1] | GBA0/IO19NDB0V0 | GBA0/IO23NDB0V0 |
| 161 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| 162 | GND | GND |
| 163 | VCC | VCC |
| 164[1] | EMC_AB[25]/IO16PDB0V0 | IO21PDB0V0 |
| 165[1] | EMC_AB[24]/IO16NDB0V0 | IO21NDB0V0 |
| 166[1] | EMC_AB[23]/IO15PDB0V0 | IO20PDB0V0 |
| 167[1] | EMC_AB[22]/IO15NDB0V0 | IO20NDB0V0 |
| 168[1] | EMC_AB[21]/IO14PDB0V0 | IO19PDB0V0 |
| 169[1] | EMC_AB[20]/IO14NDB0V0 | IO19NDB0V0 |
| 170[1] | EMC_AB[19]/IO13PDB0V0 | IO18PDB0V0 |
| 171[1] | EMC_AB[18]/IO13NDB0V0 | IO18NDB0V0 |
| 172[1] | EMC_AB[17]/IO12PDB0V0 | IO17PDB0V0 |
| 173[1] | EMC_AB[16]/IO12NDB0V0 | IO17NDB0V0 |
| 174 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| 175 | GND | GND |
| 176 | VCC | VCC |
| 177[1] | EMC_AB[15]/IO11PDB0V0 | IO14PDB0V0 |
| 178[1] | EMC_AB[14]/IO11NDB0V0 | IO14NDB0V0 |
| 179[1] | EMC_AB[13]/IO10PDB0V0 | IO13PDB0V0 |
| 180[1] | EMC_AB[12]/IO10NDB0V0 | IO13NDB0V0 |
| 181[1] | EMC_AB[11]/IO09PDB0V0 | IO12PDB0V0 |
| 182[1] | EMC_AB[10]/IO09NDB0V0 | IO12NDB0V0 |
| 183[1] | EMC_AB[9]/IO08PDB0V0 | IO11PDB0V0 |

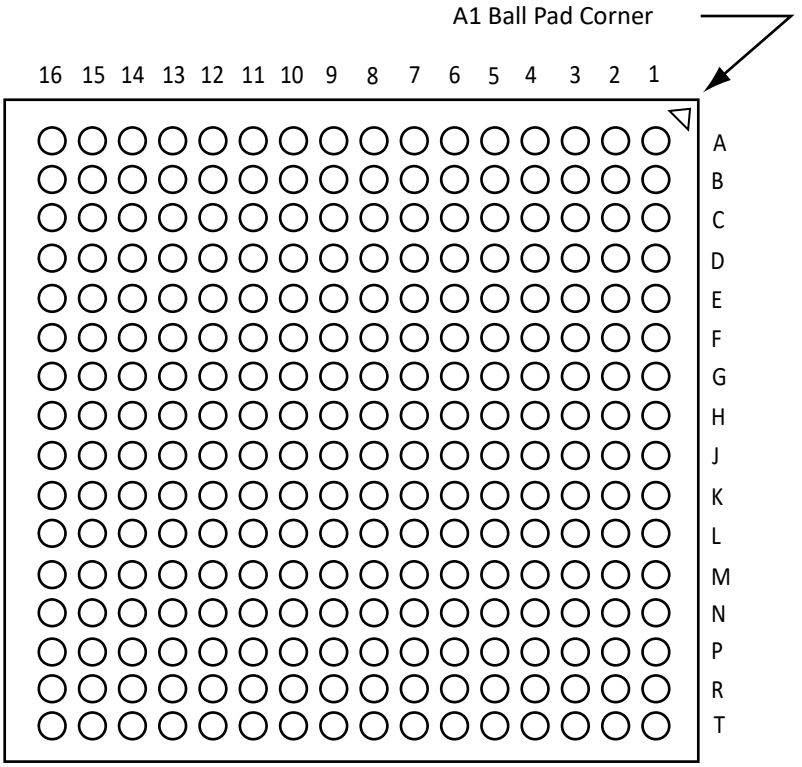
| .....continued | | |
|---|---|---|
| Pin Number | PQ208 | |
| | A2F200 | A2F500 |
| 184[1] | EMC_AB[8]/IO08NDB0V0 | IO11NDB0V0 |
| 185[1] | EMC_AB[7]/IO07PDB0V0 | IO10PDB0V0 |
| 186[1] | EMC_AB[6]/IO07NDB0V0 | IO10NDB0V0 |
| 187 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| 188 | GND | GND |
| 189 | VCC | VCC |
| 190[1] | EMC_AB[5]/IO06PDB0V0 | IO08PDB0V0 |
| 191[1] | EMC_AB[4]/IO06NDB0V0 | IO08NDB0V0 |
| 192[1] | EMC_AB[3]/IO05PDB0V0 | GAC1/IO07PDB0V0 |
| 193[1] | EMC_AB[2]/IO05NDB0V0 | GAC0/IO07NDB0V0 |
| 194[1] | EMC_AB[1]/IO04PDB0V0 | IO04PDB0V0 |
| 195[1] | EMC_AB[0]/IO04NDB0V0 | IO04NDB0V0 |
| 196[1] | EMC_OEN1_N/IO03PDB0V0 | IO03PDB0V0 |
| 197[1] | EMC_OEN0_N/IO03NDB0V0 | IO03NDB0V0 |
| 198[1] | EMC_BYTEN[1]/GAC1/IO02PDB0V0 | GAA1/IO02PDB0V0 |
| 199[1] | EMC_BYTEN[0]/GAC0/IO02NDB0V0 | GAA0/IO02NDB0V0 |
| 200 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| 201 | GND | GND |
| 202 | VCC | VCC |
| 203[1] | EMC_CS1_N/GAB1/IO01PDB0V0 | IO01PDB0V0 |
| 204[1] | EMC_CS0_N/GAB0/IO01NDB0V0 | IO01NDB0V0 |
| 205[1] | EMC_RW_N/GAA1/IO00PDB0V0 | IO00PDB0V0 |
| 206[1] | EMC_CLK/GAA0/IO00NDB0V0 | IO00NDB0V0 |
| 207 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| 208 | GNDQ | GNDQ |

**Notes:**

1. Denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device. This note is applicable to entire row.
2. Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.

## FG256

**Figure 22-4.** FG256




**Note:** For Package Manufacturing and Environmental information, visit the Resource Center at www.microchip.com/en-us/support/package-drawings/fpga-packaging.

**Table 22-4.** FG256

| Pin No. | FG256 | | |
|---|---|---|---|
| | A2F060[1] Function | A2F200 Function | A2F500 Function |
| A1 | GND | GND | GND |
| A2 | VCCFPGAIOB0 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| A3[2] | EMC_AB[0]/IO04NDB0V0 | EMC_AB[0]/IO04NDB0V0 | EMC_AB[0]/IO06NDB0V0 |
| A4[2] | EMC_AB[1]/IO04PDB0V0 | EMC_AB[1]/IO04PDB0V0 | EMC_AB[1]/IO06PDB0V0 |
| A5 | GND | GND | GND |
| A6[2] | EMC_AB[3]/IO05PDB0V0 | EMC_AB[3]/IO05PDB0V0 | EMC_AB[3]/IO09PDB0V0 |
| A7[2] | EMC_AB[5]/IO06PDB0V0 | EMC_AB[5]/IO06PDB0V0 | EMC_AB[5]/IO10PDB0V0 |
| A8 | VCCFPGAIOB0 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| A9 | GND | GND | GND |
| A10[2] | EMC_AB[14]/IO11NDB0V0 | EMC_AB[14]/IO11NDB0V0 | EMC_AB[14]/IO15NDB0V0 |
| A11[2] | EMC_AB[15]/IO11PDB0V0 | EMC_AB[15]/IO11PDB0V0 | EMC_AB[15]/IO15PDB0V0 |
| A12 | GND | GND | GND |
| A13[2] | EMC_AB[20]/IO14NDB0V0 | EMC_AB[20]/IO14NDB0V0 | EMC_AB[20]/IO21NDB0V0 |
| A14[2] | EMC_AB[24]/IO16NDB0V0 | EMC_AB[24]/IO16NDB0V0 | EMC_AB[24]/IO20NDB0V0 |
| A15 | VCCFPGAIOB0 | VCCFPGAIOB0 | VCCFPGAIOB0 |

**.....continued**

| Pin No. | FG256 | | |
|---|---|---|---|
| | A2F060[1] Function | A2F200 Function | A2F500 Function |
| A16 | GND | GND | GND |
| B1[2] | EMC_DB[15]/IO45PDB5V0 | EMC_DB[15]/GAA2/IO71PDB5V0 | EMC_DB[15]/GAA2/IO88PDB5V0 |
| B2 | GND | GND | GND |
| B3[2] | EMC_BYTEN[1]/IO02PDB0V0 | EMC_BYTEN[1]/GAC1/IO02PDB0V0 | EMC_BYTEN[1]/GAC1/IO07PDB0V0 |
| B4[2] | EMC_OEN0_N/IO03NDB0V0 | EMC_OEN0_N/IO03NDB0V0 | EMC_OEN0_N/IO08NDB0V0 |
| B5[2] | EMC_OEN1_N/IO03PDB0V0 | EMC_OEN1_N/IO03PDB0V0 | EMC_OEN1_N/IO08PDB0V0 |
| B6[2] | EMC_AB[2]/IO05NDB0V0 | EMC_AB[2]/IO05NDB0V0 | EMC_AB[2]/IO09NDB0V0 |
| B7[2] | EMC_AB[4]/IO06NDB0V0 | EMC_AB[4]/IO06NDB0V0 | EMC_AB[4]/IO10NDB0V0 |
| B8[2] | EMC_AB[9]/IO08PDB0V0 | EMC_AB[9]/IO08PDB0V0 | EMC_AB[9]/IO13PDB0V0 |
| B9[2] | EMC_AB[12]/IO10NDB0V0 | EMC_AB[12]/IO10NDB0V0 | EMC_AB[12]/IO14NDB0V0 |
| B10[2] | EMC_AB[13]/IO10PDB0V0 | EMC_AB[13]/IO10PDB0V0 | EMC_AB[13]/IO14PDB0V0 |
| B11[2] | EMC_AB[16]/IO12NDB0V0 | EMC_AB[16]/IO12NDB0V0 | EMC_AB[16]/IO17NDB0V0 |
| B12[2] | EMC_AB[18]/IO13NDB0V0 | EMC_AB[18]/IO13NDB0V0 | EMC_AB[18]/IO18NDB0V0 |
| B13[2] | EMC_AB[21]/IO14PDB0V0 | EMC_AB[21]/IO14PDB0V0 | EMC_AB[21]/IO21PDB0V0 |
| B14[2] | EMC_AB[25]/IO16PDB0V0 | EMC_AB[25]/IO16PDB0V0 | EMC_AB[25]/IO20PDB0V0 |
| B15 | GND | GND | GND |
| B16 | GNDQ | GNDQ | GNDQ |
| C1[2] | EMC_DB[14]/IO45NDB5V0 | EMC_DB[14]/GAB2/IO71NDB5V0 | EMC_DB[14]/GAB2/IO88NDB5V0 |
| C2[2] | VCCPLL0 | VCCPLL | VCCPLL0 |
| C3[2] | EMC_BYTEN[0]/IO02NDB0V0 | EMC_BYTEN[0]/GAC0/IO02NDB0V0 | EMC_BYTEN[0]/GAC0/IO07NDB0V0 |
| C4 | VCCFPGAIOB0 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| C5[2] | EMC_CS0_N/IO01NDB0V0 | EMC_CS0_N/GAB0/IO01NDB0V0 | EMC_CS0_N/GAB0/IO05NDB0V0 |
| C6[2] | EMC_CS1_N/IO01PDB0V0 | EMC_CS1_N/GAB1/IO01PDB0V0 | EMC_CS1_N/GAB1/IO05PDB0V0 |
| C7 | GND | GND | GND |
| C8[2] | EMC_AB[8]/IO08NDB0V0 | EMC_AB[8]/IO08NDB0V0 | EMC_AB[8]/IO13NDB0V0 |
| C9[2] | EMC_AB[11]/IO09PDB0V0 | EMC_AB[11]/IO09PDB0V0 | EMC_AB[11]/IO11PDB0V0 |
| C10 | VCCFPGAIOB0 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| C11[2] | EMC_AB[17]/IO12PDB0V0 | EMC_AB[17]/IO12PDB0V0 | EMC_AB[17]/IO17PDB0V0 |
| C12[2] | EMC_AB[19]/IO13PDB0V0 | EMC_AB[19]/IO13PDB0V0 | EMC_AB[19]/IO18PDB0V0 |
| C13 | GND | GND | GND |
| C14[2] | GCC0/IO18NPB0V0 | GBA2/IO20PPB1V0 | GBA2/IO27PPB1V0 |
| C15[2] | GCB0/IO19NDB0V0 | GCA2/IO23PDB1V0 | GCA2/IO28PDB1V0[2] |
| C16[2] | GCB1/IO19PDB0V0 | IO23NDB1V0 | IO28NDB1V0 |
| D1 | VCCFPGAIOB5 | VCCFPGAIOB5 | VCCFPGAIOB5 |
| D2[2] | VCOMPLA0 | VCOMPLA | VCOMPLA0 |
| D3 | GND | GND | GND |
| D4 | GNDQ | GNDQ | GNDQ |
| D5[2] | EMC_CLK/IO00NDB0V0 | EMC_CLK/GAA0/IO00NDB0V0 | EMC_CLK/GAA0/IO02NDB0V0 |
| D6[2] | EMC_RW_N/IO00PDB0V0 | EMC_RW_N/GAA1/IO00PDB0V0 | EMC_RW_N/GAA1/IO02PDB0V0 |
| D7[2] | EMC_AB[6]/IO07NDB0V0 | EMC_AB[6]/IO07NDB0V0 | EMC_AB[6]/IO12NDB0V0 |
| D8[2] | EMC_AB[7]/IO07PDB0V0 | EMC_AB[7]/IO07PDB0V0 | EMC_AB[7]/IO12PDB0V0 |
| D9[2] | EMC_AB[10]/IO09NDB0V0 | EMC_AB[10]/IO09NDB0V0 | EMC_AB[10]/IO11NDB0V0 |
| D10[2] | EMC_AB[22]/IO15NDB0V0 | EMC_AB[22]/IO15NDB0V0 | EMC_AB[22]/IO19NDB0V0 |
| D11[2] | EMC_AB[23]/IO15PDB0V0 | EMC_AB[23]/IO15PDB0V0 | EMC_AB[23]/IO19PDB0V0 |

**.....continued**

| Pin No. | FG256 | | |
|---|---|---|---|
| | A2F060[1] Function | A2F200 Function | A2F500 Function |
| D12 | GNDQ | GNDQ | GNDQ |
| D13[2] | GCC1/IO18PPB0V0 | GBB2/IO20NPB1V0 | GBB2/IO27NPB1V0 |
| D14[2] | GCA0/IO20NDB0V0 | GCB2/IO24PDB1V0 | GCB2/IO33PDB1V0 |
| D15[2] | GCA1/IO20PDB0V0 | IO24NDB1V0 | IO33NDB1V0 |
| D16 | VCCFPGAIOB1 | VCCFPGAIOB1 | VCCFPGAIOB1 |
| E1[2] | EMC_DB[13]/IO44PDB5V0 | EMC_DB[13]/GAC2/IO70PDB5V0 | EMC_DB[13]/GAC2/IO87PDB5V0 |
| E2[2] | EMC_DB[12]/IO44NDB5V0 | EMC_DB[12]/IO70NDB5V0 | EMC_DB[12]/IO87NDB5V0 |
| E3[2] | GFA2/IO42PDB5V0 | GFA2/IO68PDB5V0 | GFA2/IO85PDB5V0 |
| E4[2] | EMC_DB[10]/IO43NPB5V0 | EMC_DB[10]/IO69NPB5V0 | EMC_DB[10]/IO86NPB5V0 |
| E5 | GNDQ | GNDQ | GNDQ |
| E6 | GND | GND | GND |
| E7 | VCCFPGAIOB0 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| E8 | GND | GND | GND |
| E9 | VCCFPGAIOB0 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| E10 | GND | GND | GND |
| E11 | VCCFPGAIOB0 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| E12[2] | GCB2/IO22PDB1V0 | GCA1/IO28PDB1V0 | GCA1/IO36PDB1V0[2] |
| E13 | VCCFPGAIOB1 | VCCFPGAIOB1 | VCCFPGAIOB1 |
| E14[2] | GCA2/IO21PDB1V0 | GCB1/IO27PDB1V0 | GCB1/IO34PDB1V0 |
| E15[2] | GCC2/IO23PDB1V0 | GDC1/IO29PDB1V0 | GDC1/IO38PDB1V0 |
| E16[2] | IO23NDB1V0 | GDC0/IO29NDB1V0 | GDC0/IO38NDB1V0 |
| F1[2] | EMC_DB[9]/IO40PDB5V0 | EMC_DB[9]/GEC1/IO63PDB5V0 | EMC_DB[9]/GEC1/IO80PDB5V0 |
| F2 | GND | GND | GND |
| F3[2] | GFB2/IO42NDB5V0 | GFB2/IO68NDB5V0 | GFB2/IO85NDB5V0 |
| F4 | VCCFPGAIOB5 | VCCFPGAIOB5 | VCCFPGAIOB5 |
| F5[2] | EMC_DB[11]/IO43PPB5V0 | EMC_DB[11]/IO69PPB5V0 | EMC_DB[11]/IO86PPB5V0 |
| F6 | VCCFPGAIOB5 | VCCFPGAIOB5 | VCCFPGAIOB5 |
| F7 | GND | GND | GND |
| F8 | VCC | VCC | VCC |
| F9 | GND | GND | GND |
| F10 | VCC | VCC | VCC |
| F11 | GND | GND | GND |
| F12[2] | IO22NDB1V0 | GCA0/IO28NDB1V0 | GCA0/IO36NDB1V0[2] |
| F13 | NC | GNDQ | GNDQ |
| F14[2] | IO21NDB1V0 | GCB0/IO27NDB1V0 | GCB0/IO34NDB1V0 |
| F15 | GND | GND | GND |
| F16 | VCCENVM | VCCENVM | VCCENVM |
| G1[2] | EMC_DB[8]/IO40NDB5V0 | EMC_DB[8]/GEC0/IO63NDB5V0 | EMC_DB[8]/GEC0/IO80NDB5V0 |
| G2[2] | EMC_DB[7]/IO39PDB5V0 | EMC_DB[7]/GEB1/IO62PDB5V0 | EMC_DB[7]/GEB1/IO79PDB5V0 |
| G3[2] | EMC_DB[6]/IO39NDB5V0 | EMC_DB[6]/GEB0/IO62NDB5V0 | EMC_DB[6]/GEB0/IO79NDB5V0 |
| G4[2] | GFC2/IO41PDB5V0 | GFC2/IO67PDB5V0 | GFC2/IO84PDB5V0 |
| G5[2] | IO41NDB5V0 | IO67NDB5V0 | IO84NDB5V0 |
| G6 | GND | GND | GND |
| G7 | VCC | VCC | VCC |

**.....continued**

| Pin No. | FG256 | | |
|---|---|---|---|
| | A2F060[1] Function | A2F200 Function | A2F500 Function |
| G8 | GND | GND | GND |
| G9 | VCC | VCC | VCC |
| G10 | GND | GND | GND |
| G11 | VCCFPGAIOB1 | VCCFPGAIOB1 | VCCFPGAIOB1 |
| G12 | VPP | VPP | VPP |
| G13 | TRSTB | TRSTB | TRSTB |
| G14 | TMS | TMS | TMS |
| G15 | TCK | TCK | TCK |
| G16 | GNDENVM | GNDENVM | GNDENVM |
| H1 | GND | GND | GND |
| H2[2] | EMC_DB[5]/IO38PPB5V0 | EMC_DB[5]/GEA1/IO61PPB5V0 | EMC_DB[5]/GEA1/IO78PPB5V0 |
| H3 | VCCFPGAIOB5 | VCCFPGAIOB5 | VCCFPGAIOB5 |
| H4[2] | EMC_DB[1]/IO36PDB5V0 | EMC_DB[1]/GEB2/IO59PDB5V0 | EMC_DB[1]/GEB2/IO76PDB5V0 |
| H5[2] | EMC_DB[0]/IO36NDB5V0 | EMC_DB[0]/GEA2/IO59NDB5V0 | EMC_DB[0]/GEA2/IO76NDB5V0 |
| H6 | VCCFPGAIOB5 | VCCFPGAIOB5 | VCCFPGAIOB5 |
| H7 | GND | GND | GND |
| H8 | VCC | VCC | VCC |
| H9 | GND | GND | GND |
| H10 | VCC | VCC | VCC |
| H11 | GND | GND | GND |
| H12 | VJTAG | VJTAG | VJTAG |
| H13 | TDO | TDO | TDO |
| H14 | TDI | TDI | TDI |
| H15 | JTAGSEL | JTAGSEL | JTAGSEL |
| H16 | GND | GND | GND |
| J1[2] | EMC_DB[4]/IO38NPB5V0 | EMC_DB[4]/GEA0/IO61NPB5V0 | EMC_DB[4]/GEA0/IO78NPB5V0 |
| J2[2] | EMC_DB[3]/IO37PDB5V0 | EMC_DB[3]/GEC2/IO60PDB5V0 | EMC_DB[3]/GEC2/IO77PDB5V0 |
| J3[2] | EMC_DB[2]/IO37NDB5V0 | EMC_DB[2]/IO60NDB5V0 | EMC_DB[2]/IO77NDB5V0 |
| J4 | GNDRCOSC | GNDRCOSC | GNDRCOSC |
| J5 | NC | GNDQ | GNDQ |
| J6 | GND | GND | GND |
| J7 | VCC | VCC | VCC |
| J8 | GND | GND | GND |
| J9 | VCC | VCC | VCC |
| J10 | GND | GND | GND |
| J11 | VCCMSSIOB2 | VCCMSSIOB2 | VCCMSSIOB2 |
| J12 | I2C_0_SCL/GPIO_23 | I2C_0_SCL/GPIO_23 | I2C_0_SCL/GPIO_23 |
| J13 | I2C_0_SDA/GPIO_22 | I2C_0_SDA/GPIO_22 | I2C_0_SDA/GPIO_22 |
| J14 | I2C_1_SCL/GPIO_31 | I2C_1_SCL/GPIO_31 | I2C_1_SCL/GPIO_31 |
| J15 | VCCMSSIOB2 | VCCMSSIOB2 | VCCMSSIOB2 |
| J16 | I2C_1_SDA/GPIO_30 | I2C_1_SDA/GPIO_30 | I2C_1_SDA/GPIO_30 |
| K1[2] | GPIO_1/IO32RSB4V0 | MAC_MDIO/IO49RSB4V0 | MAC_MDIO/IO58RSB4V0 |
| K2[2] | GPIO_0/IO33RSB4V0 | MAC_MDC/IO48RSB4V0 | MAC_MDC/IO57RSB4V0 |
| K3 | VCCMSSIOB4 | VCCMSSIOB4 | VCCMSSIOB4 |

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| Pin No. | FG256 | | |
|---|---|---|---|
| | A2F060[1] Function | A2F200 Function | A2F500 Function |
| K4 | MSS_RESET_N | MSS_RESET_N | MSS_RESET_N |
| K5 | VCCRCOSC | VCCRCOSC | VCCRCOSC |
| K6 | VCCMSSIOB4 | VCCMSSIOB4 | VCCMSSIOB4 |
| K7 | GND | GND | GND |
| K8 | VCC | VCC | VCC |
| K9 | GND | GND | GND |
| K10 | VCC | VCC | VCC |
| K11 | GND | GND | GND |
| K12 | UART_0_RXD/GPIO_21 | UART_0_RXD/GPIO_21 | UART_0_RXD/GPIO_21 |
| K13 | GND | GND | GND |
| K14 | UART_1_TXD/GPIO_28 | UART_1_TXD/GPIO_28 | UART_1_TXD/GPIO_28 |
| K15 | UART_1_RXD/GPIO_29 | UART_1_RXD/GPIO_29 | UART_1_RXD/GPIO_29 |
| K16 | UART_0_TXD/GPIO_20 | UART_0_TXD/GPIO_20 | UART_0_TXD/GPIO_20 |
| L1 | GND | GND | GND |
| L2[2] | GPIO_2/IO31RSB4V0 | MAC_TXEN/IO52RSB4V0 | MAC_TXEN/IO61RSB4V0 |
| L3[2] | GPIO_3/IO30RSB4V0 | MAC_CRSDV/IO51RSB4V0 | MAC_CRSDV/IO60RSB4V0 |
| L4[2] | GPIO_4/IO29RSB4V0 | MAC_RXER/IO50RSB4V0 | MAC_RXER/IO59RSB4V0 |
| L5[2] | GPIO_9/IO24RSB4V0 | MAC_CLK | MAC_CLK |
| L6 | GND | GND | GND |
| L7 | VCC | VCC | VCC |
| L8 | GND | GND | GND |
| L9 | VCC | VCC | VCC |
| L10 | GND | GND | GND |
| L11 | VCCMSSIOB2 | VCCMSSIOB2 | VCCMSSIOB2 |
| L12 | SPI_1_DO/GPIO_24 | SPI_1_DO/GPIO_24 | SPI_1_DO/GPIO_24 |
| L13 | SPI_1_SS/GPIO_27 | SPI_1_SS/GPIO_27 | SPI_1_SS/GPIO_27 |
| L14 | SPI_1_CLK/GPIO_26 | SPI_1_CLK/GPIO_26 | SPI_1_CLK/GPIO_26 |
| L15 | SPI_1_DI/GPIO_25 | SPI_1_DI/GPIO_25 | SPI_1_DI/GPIO_25 |
| L16 | GND | GND | GND |
| M1[2] | GPIO_5/IO28RSB4V0 | MAC_TXD[0]/IO56RSB4V0 | MAC_TXD[0]/IO65RSB4V0 |
| M2[2] | GPIO_6/IO27RSB4V0 | MAC_TXD[1]/IO55RSB4V0 | MAC_TXD[1]/IO64RSB4V0 |
| M3[2] | GPIO_7/IO26RSB4V0 | MAC_RXD[0]/IO54RSB4V0 | MAC_RXD[0]/IO63RSB4V0 |
| M4 | GND | GND | GND |
| M5[2] | NC | ADC3 | ADC3 |
| M6[2] | NC | GND15ADC0 | GND15ADC0 |
| M7[2] | GND33ADC0 | GND33ADC1 | GND33ADC1 |
| M8[2] | GND33ADC0 | GND33ADC1 | GND33ADC1 |
| M9[2] | ADC7 | ADC4 | ADC4 |
| M10[2] | GNDTM0 | GNDTM1 | GNDTM1 |
| M11[2] | ADC6 | TM2 | TM2 |
| M12[2] | ADC5 | CM2 | CM2 |
| M13 | SPI_0_SS/GPIO_19 | SPI_0_SS/GPIO_19 | SPI_0_SS/GPIO_19 |
| M14 | VCCMSSIOB2 | VCCMSSIOB2 | VCCMSSIOB2 |
| M15 | SPI_0_CLK/GPIO_18 | SPI_0_CLK/GPIO_18 | SPI_0_CLK/GPIO_18 |

**.....continued**

| Pin No. | FG256 | | |
|---|---|---|---|
| | A2F060[1] Function | A2F200 Function | A2F500 Function |
| M16 | SPI_0_DI/GPIO_17 | SPI_0_DI/GPIO_17 | SPI_0_DI/GPIO_17 |
| N1[2] | GPIO_8/IO25RSB4V0 | MAC_RXD[1]/IO53RSB4V0 | MAC_RXD[1]/IO62RSB4V0 |
| N2 | VCCMSSIOB4 | VCCMSSIOB4 | VCCMSSIOB4 |
| N3 | VCC15A | VCC15A | VCC15A |
| N4 | VCC33AP | VCC33AP | VCC33AP |
| N5[2] | NC | ABPS3 | ABPS3 |
| N6[2] | ADC4 | TM1 | TM1 |
| N7[2] | NC | GND33ADC0 | GND33ADC0 |
| N8[2] | VCC33ADC0 | VCC33ADC1 | VCC33ADC1 |
| N9[2] | ADC8 | ADC5 | ADC5 |
| N10[2] | CM0 | CM3 | CM3 |
| N11 | GNDAQ | GNDAQ | GNDAQ |
| N12 | VAREFOUT | VAREFOUT | VAREFOUT |
| N13[2] | NC | GNDSDD1 | GNDSDD1 |
| N14[2] | NC | VCC33SDD1 | VCC33SDD1 |
| N15 | GND | GND | GND |
| N16 | SPI_0_DO/GPIO_16 | SPI_0_DO/GPIO_16 | SPI_0_DO/GPIO_16 |
| P1 | GNDSDD0 | GNDSDD0 | GNDSDD0 |
| P2 | VCC33SDD0 | VCC33SDD0 | VCC33SDD0 |
| P3 | VCC33N | VCC33N | VCC33N |
| P4 | GNDA | GNDA | GNDA |
| P5 | GNDAQ | GNDAQ | GNDAQ |
| P6[2] | NC | CM1 | CM1 |
| P7[2] | NC | ADC2 | ADC2 |
| P8[2] | NC | VCC15ADC0 | VCC15ADC0 |
| P9[2] | ADC9 | ADC6 | ADC6 |
| P10[2] | TM0 | TM3 | TM3 |
| P11 | GNDA | GNDA | GNDA |
| P12 | VCCMAINXTAL | VCCMAINXTAL | VCCMAINXTAL |
| P13 | GNDLPXTAL | GNDLPXTAL | GNDLPXTAL |
| P14 | VDDBAT | VDDBAT | VDDBAT |
| P15 | PTEM | PTEM | PTEM |
| P16 | PTBASE | PTBASE | PTBASE |
| R1 | PCAP | PCAP | PCAP |
| R2 | SDD0 | SDD0 | SDD0 |
| R3[2] | ADC0 | ABPS0 | ABPS0 |
| R4[2] | ADC3 | TM0 | TM0 |
| R5[2] | NC | ABPS2 | ABPS2 |
| R6[2] | NC | ADC1 | ADC1 |
| R7[2] | NC | VCC33ADC0 | VCC33ADC0 |
| R8[2] | VCC15ADC0 | VCC15ADC1 | VCC15ADC1 |
| R9[2] | ADC10 | ADC7 | ADC7 |
| R10[2] | ABPS1 | ABPS7 | ABPS7 |
| R11[2] | NC | ABPS4 | ABPS4 |

**.....continued**

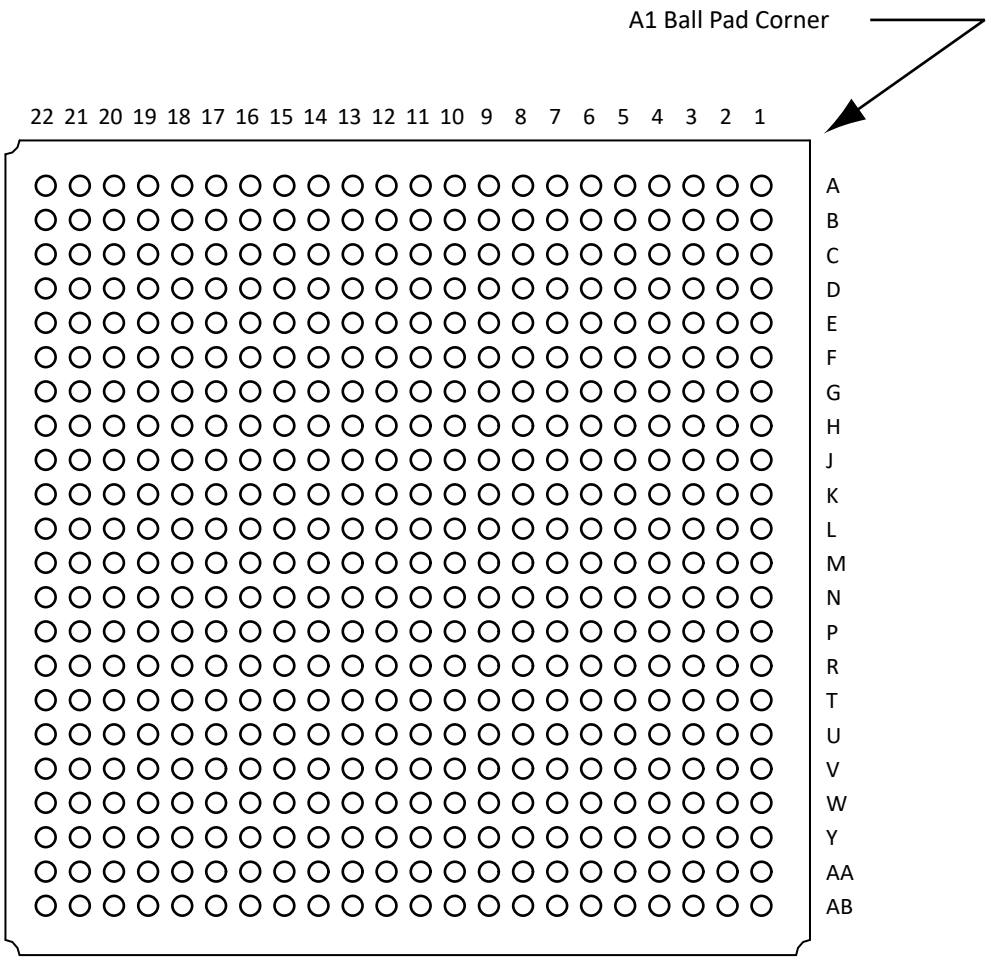
| Pin No. | FG256 | | |
|---|---|---|---|
| | A2F060[1] Function | A2F200 Function | A2F500 Function |
| R12 | MAINXIN | MAINXIN | MAINXIN |
| R13 | MAINXOUT | MAINXOUT | MAINXOUT |
| R14 | LPXIN | LPXIN | LPXIN |
| R15 | LPXOUT | LPXOUT | LPXOUT |
| R16 | VCC33A | VCC33A | VCC33A |
| T1 | NCAP | NCAP | NCAP |
| T2[2] | ADC1 | ABPS1 | ABPS1 |
| T3[2] | ADC2 | CM0 | CM0 |
| T4[2] | NC | GNDTM0 | GNDTM0 |
| T5[2] | NC | ADC0 | ADC0 |
| T6[2] | NC | VAREF0 | VAREF0 |
| T7[2] | NC | GND33ADC0 | GND33ADC0 |
| T8[2] | GND15ADC0 | GND15ADC1 | GND15ADC1 |
| T9[2] | VAREF0 | VAREF1 | VAREF1 |
| T10[2] | ABPS0 | ABPS6 | ABPS6 |
| T11[2] | NC | ABPS5 | ABPS5 |
| T12[2] | NC | SDD1 | SDD1 |
| T13 | GNDVAREF | GNDVAREF | GNDVAREF |
| T14 | GNDMAINXTAL | GNDMAINXTAL | GNDMAINXTAL |
| T15 | VCCLPXTAL | VCCLPXTAL | VCCLPXTAL |
| T16 | PU_N | PU_N | PU_N |

**Notes:**

1. Part No A2F060 is discontinued.
2. Denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device. This note is applicable to entire row.
3. Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the “Glitchless MUX” section in the SmartFusion Microcontroller Subsystem User’s Guide for more details.

## FG484

**Figure 22-5.** FG484




**Note:** For Package Manufacturing and Environmental information, visit the Resource Center at www.microchip.com/en-us/support/package-drawings/fpga-packaging.

**Table 22-5.** FG484

| Pin Number | FG484 | |
|---|---|---|
| | A2F200 Function | A2F500 Function |
| A1 | GND | GND |
| A2 | NC | NC |
| A3 | NC | NC |
| A4 | GND | GND |
| A5[1] | EMC_CS0_N/GAB0/IO01NDB0V0 | EMC_CS0_N/GAB0/IO05NDB0V0 |
| A6[1] | EMC_CS1_N/GAB1/IO01PDB0V0 | EMC_CS1_N/GAB1/IO05PDB0V0 |
| A7 | GND | GND |
| A8[1] | EMC_AB[0]/IO04NDB0V0 | EMC_AB[0]/IO06NDB0V0 |
| A9[1] | EMC_AB[1]/IO04PDB0V0 | EMC_AB[1]/IO06PDB0V0 |
| A10 | GND | GND |

| .....continued | | |
|---|---|---|
| Pin Number | FG484 | |
| | A2F200 Function | A2F500 Function |
| A11 | NC | NC |
| A12[1] | EMC_AB[7]/IO07PDB0V0 | EMC_AB[7]/IO12PDB0V0 |
| A13 | GND | GND |
| A14[1] | EMC_AB[12]/IO10NDB0V0 | EMC_AB[12]/IO14NDB0V0 |
| A15[1] | EMC_AB[13]/IO10PDB0V0 | EMC_AB[13]/IO14PDB0V0 |
| A16 | GND | GND |
| A17[1] | NC | IO16NDB0V0 |
| A18[1] | NC | IO16PDB0V0 |
| A19 | GND | GND |
| A20 | NC | NC |
| A21 | NC | NC |
| A22 | GND | GND |
| AA1[1] | GPIO_4/IO43RSB4V0 | GPIO_4/IO52RSB4V0 |
| AA2[1] | GPIO_12/IO37RSB4V0 | GPIO_12/IO46RSB4V0 |
| AA3[1] | MAC_MDC/IO48RSB4V0 | MAC_MDC/IO57RSB4V0 |
| AA4[1] | MAC_RXER/IO50RSB4V0 | MAC_RXER/IO59RSB4V0 |
| AA5[1] | MAC_TXD[0]/IO56RSB4V0 | MAC_TXD[0]/IO65RSB4V0 |
| AA6 | ABPS0 | ABPS0 |
| AA7 | TM1 | TM1 |
| AA8 | ADC1 | ADC1 |
| AA9 | GND15ADC1 | GND15ADC1 |
| AA10 | GND33ADC1 | GND33ADC1 |
| AA11 | CM3 | CM3 |
| AA12 | GNDTM1 | GNDTM1 |
| AA13[1] | NC | ADC10 |
| AA14[1] | NC | ADC9 |
| AA15[1] | NC | GND15ADC2 |
| AA16 | MAINXIN | MAINXIN |
| AA17 | MAINXOUT | MAINXOUT |
| AA18 | LPXIN | LPXIN |
| AA19 | LPXOUT | LPXOUT |
| AA20 | NC | NC |
| AA21 | NC | NC |
| AA22 | SPI_1_CLK/GPIO_26 | SPI_1_CLK/GPIO_26 |
| AB1 | GND | GND |
| AB2[1] | GPIO_13/IO36RSB4V0 | GPIO_13/IO45RSB4V0 |
| AB3[1] | GPIO_14/IO35RSB4V0 | GPIO_14/IO44RSB4V0 |
| AB4 | GND | GND |
| AB5 | PCAP | PCAP |
| AB6 | NCAP | NCAP |
| AB7 | ABPS3 | ABPS3 |
| AB8 | ADC3 | ADC3 |
| AB9 | GND15ADC0 | GND15ADC0 |
| AB10 | VCC33ADC1 | VCC33ADC1 |

| .....continued | | |
|---|---|---|
| Pin Number | FG484 | |
| | A2F200 Function | A2F500 Function |
| AB11 | VAREF1 | VAREF1 |
| AB12 | TM2 | TM2 |
| AB13 | CM2 | CM2 |
| AB14 | ABPS4 | ABPS4 |
| AB15 | GNDAQ | GNDAQ |
| AB16 | GNDMAINXTAL | GNDMAINXTAL |
| AB17 | GNDLPXTAL | GNDLPXTAL |
| AB18 | VCCLPXTAL | VCCLPXTAL |
| AB19 | VDDBAT | VDDBAT |
| AB20 | PTBASE | PTBASE |
| AB21 | NC | NC |
| AB22 | GND | GND |
| B1[1] | EMC_DB[15]/GAA2/IO71PDB5V0 | EMC_DB[15]/GAA2/IO88PDB5V0 |
| B2 | GND | GND |
| B3 | NC | NC |
| B4 | NC | NC |
| B5 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| B6[1] | EMC_RW_N/GAA1/IO00PDB0V0 | EMC_RW_N/GAA1/IO02PDB0V0 |
| B7[1] | NC | IO04PPB0V0 |
| B8 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| B9[1] | EMC_BYTEN[0]/GAC0/IO02NDB0V0 | EMC_BYTEN[0]/GAC0/IO07NDB0V0 |
| B10[1] | EMC_AB[2]/IO05NDB0V0 | EMC_AB[2]/IO09NDB0V0 |
| B11[1] | EMC_AB[3]/IO05PDB0V0 | EMC_AB[3]/IO09PDB0V0 |
| B12[1] | EMC_AB[6]/IO07NDB0V0 | EMC_AB[6]/IO12NDB0V0 |
| B13[1] | EMC_AB[14]/IO11NDB0V0 | EMC_AB[14]/IO15NDB0V0 |
| B14[1] | EMC_AB[15]/IO11PDB0V0 | EMC_AB[15]/IO15PDB0V0 |
| B15 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| B16[1] | EMC_AB[18]/IO13NDB0V0 | EMC_AB[18]/IO18NDB0V0 |
| B17[1] | EMC_AB[19]/IO13PDB0V0 | EMC_AB[19]/IO18PDB0V0 |
| B18 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| B19[1] | GBB0/IO18NDB0V0 | GBB0/IO24NDB0V0 |
| B20[1] | GBB1/IO18PDB0V0 | GBB1/IO24PDB0V0 |
| B21 | GND | GND |
| B22[1] | GBA2/IO20PDB1V0 | GBA2/IO27PDB1V0 |
| C1[1] | EMC_DB[14]/GAB2/IO71NDB5V0 | EMC_DB[14]/GAB2/IO88NDB5V0 |
| C2 | NC | NC |
| C3 | NC | NC |
| C4[1] | NC | IO01NDB0V0 |
| C5[1] | NC | IO01PDB0V0 |
| C6[1] | EMC_CLK/GAA0/IO00NDB0V0 | EMC_CLK/GAA0/IO02NDB0V0 |
| C7[1] | NC | IO03PPB0V0 |
| C8[1] | NC | IO04NPB0V0 |
| C9[1] | EMC_BYTEN[1]/GAC1/IO02PDB0V0 | EMC_BYTEN[1]/GAC1/IO07PDB0V0 |
| C10[1] | EMC_OEN1_N/IO03PDB0V0 | EMC_OEN1_N/IO08PDB0V0 |

**.....continued**

| Pin Number | FG484 | |
|---|---|---|
| | A2F200 Function | A2F500 Function |
| C11 | GND | GND |
| C12 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| C13[1] | EMC_AB[8]/IO08NDB0V0 | EMC_AB[8]/IO13NDB0V0 |
| C14[1] | EMC_AB[16]/IO12NDB0V0 | EMC_AB[16]/IO17NDB0V0 |
| C15[1] | EMC_AB[17]/IO12PDB0V0 | EMC_AB[17]/IO17PDB0V0 |
| C16[1] | EMC_AB[24]/IO16NDB0V0 | EMC_AB[24]/IO20NDB0V0 |
| C17[1] | EMC_AB[22]/IO15NDB0V0 | EMC_AB[22]/IO19NDB0V0 |
| C18[1] | EMC_AB[23]/IO15PDB0V0 | EMC_AB[23]/IO19PDB0V0 |
| C19[1] | GBA0/IO19NPB0V0 | GBA0/IO23NPB0V0 |
| C20 | NC | NC |
| C21[1] | GBC2/IO21PDB1V0 | GBC2/IO30PDB1V0 |
| C22[1] | GBB2/IO20NDB1V0 | GBB2/IO27NDB1V0 |
| D1 | GND | GND |
| D2[1] | EMC_DB[12]/IO70NDB5V0 | EMC_DB[12]/IO87NDB5V0 |
| D3[1] | EMC_DB[13]/GAC2/IO70PDB5V0 | EMC_DB[13]/GAC2/IO87PDB5V0 |
| D4 | NC | NC |
| D5 | NC | NC |
| D6 | GND | GND |
| D7[1] | NC | IO00NPB0V0 |
| D8[1] | NC | IO03NPB0V0 |
| D9 | GND | GND |
| D10[1] | EMC_OEN0_N/IO03NDB0V0 | EMC_OEN0_N/IO08NDB0V0 |
| D11[1] | EMC_AB[10]/IO09NDB0V0 | EMC_AB[10]/IO11NDB0V0 |
| D12[1] | EMC_AB[11]/IO09PDB0V0 | EMC_AB[11]/IO11PDB0V0 |
| D13[1] | EMC_AB[9]/IO08PDB0V0 | EMC_AB[9]/IO13PDB0V0 |
| D14 | GND | GND |
| D15[1] | GBC1/IO17PPB0V0 | GBC1/IO22PPB0V0 |
| D16[1] | EMC_AB[25]/IO16PDB0V0 | EMC_AB[25]/IO20PDB0V0 |
| D17 | GND | GND |
| D18[1] | GBA1/IO19PPB0V0 | GBA1/IO23PPB0V0 |
| D19 | NC | NC |
| D20 | NC | NC |
| D21[1] | IO21NDB1V0 | IO30NDB1V0 |
| D22 | GND | GND |
| E1[1] | GFC2/IO67PPB5V0 | GFC2/IO84PPB5V0 |
| E2 | VCCFPGAIOB5 | VCCFPGAIOB5 |
| E3[1] | GFA2/IO68PDB5V0 | GFA2/IO85PDB5V0 |
| E4 | GND | GND |
| E5 | NC | NC |
| E6 | GNDQ | GNDQ |
| E7 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| E8[1] | NC | IO00PPB0V0 |
| E9 | NC | NC |
| E10 | VCCFPGAIOB0 | VCCFPGAIOB0 |

| .....continued | | |
|---|---|---|
| Pin Number | FG484 | |
| | A2F200 Function | A2F500 Function |
| E11[1] | EMC_AB[4]/IO06NDB0V0 | EMC_AB[4]/IO10NDB0V0 |
| E12[1] | EMC_AB[5]/IO06PDB0V0 | EMC_AB[5]/IO10PDB0V0 |
| E13 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| E14[1] | GBC0/IO17NPB0V0 | GBC0/IO22NPB0V0 |
| E15 | NC | NC |
| E16 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| E17[1] | NC | VCOMPLA1 |
| E18[1] | NC | IO25NPB1V0 |
| E19 | GND | GND |
| E20 | NC | NC |
| E21 | VCCFPGAIOB1 | VCCFPGAIOB1 |
| E22[1] | IO22NDB1V0 | IO32NDB1V0 |
| F1[1] | GFB1/IO65PPB5V0 | GFB1/IO82PPB5V0 |
| F2[1] | IO67NPB5V0 | IO84NPB5V0 |
| F3[1] | GFB2/IO68NDB5V0 | GFB2/IO85NDB5V0 |
| F4[1] | EMC_DB[10]/IO69NPB5V0 | EMC_DB[10]/IO86NPB5V0 |
| F5 | VCCFPGAIOB5 | VCCFPGAIOB5 |
| F6[1] | VCCPLL | VCCPLL0 |
| F7[1] | VCOMPLA | VCOMPLA0 |
| F8 | NC | NC |
| F9 | NC | NC |
| F10 | NC | NC |
| F11 | NC | NC |
| F12 | NC | NC |
| F13[1] | EMC_AB[20]/IO14NDB0V0 | EMC_AB[20]/IO21NDB0V0 |
| F14[1] | EMC_AB[21]/IO14PDB0V0 | EMC_AB[21]/IO21PDB0V0 |
| F15 | GNDQ | GNDQ |
| F16[1] | NC | VCCPLL1 |
| F17[1] | NC | IO25PPB1V0 |
| F18 | VCCFPGAIOB1 | VCCFPGAIOB1 |
| F19[1] | IO23NDB1V0 | IO28NDB1V0 |
| F20[1] | NC | IO31PDB1V0 |
| F21[1] | NC | IO31NDB1V0 |
| F22[1] | IO22PDB1V0 | IO32PDB1V0 |
| G1 | GND | GND |
| G2[1] | GFB0/IO65NPB5V0 | GFB0/IO82NPB5V0 |
| G3[1] | EMC_DB[9]/GEC1/IO63PDB5V0 | EMC_DB[9]/GEC1/IO80PDB5V0 |
| G4[1] | GFC1/IO66PPB5V0 | GFC1/IO83PPB5V0 |
| G5[1] | EMC_DB[11]/IO69PPB5V0 | EMC_DB[11]/IO86PPB5V0 |
| G6 | GNDQ | GNDQ |
| G7 | NC | NC |
| G8 | GND | GND |
| G9 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| G10 | GND | GND |

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| Pin Number | FG484 | |
|---|---|---|
| | A2F200 Function | A2F500 Function |
| G11 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| G12 | GND | GND |
| G13 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| G14 | GND | GND |
| G15 | VCCFPGAIOB0 | VCCFPGAIOB0 |
| G16 | GNDQ | GNDQ |
| G17[1] | NC | IO26PDB1V0 |
| G18[1] | NC | IO26NDB1V0 |
| G19[1] | GCA2/IO23PDB1V0 | GCA2/IO28PDB1V0[2] |
| G20[1] | IO24NDB1V0 | IO33NDB1V0 |
| G21[1] | GCB2/IO24PDB1V0 | GCB2/IO33PDB1V0 |
| G22 | GND | GND |
| H1[1] | EMC_DB[7]/GEB1/IO62PDB5V0 | EMC_DB[7]/GEB1/IO79PDB5V0 |
| H2 | VCCFPGAIOB5 | VCCFPGAIOB5 |
| H3[1] | EMC_DB[8]/GEC0/IO63NDB5V0 | EMC_DB[8]/GEC0/IO80NDB5V0 |
| H4 | GND | GND |
| H5[1] | GFC0/IO66NPB5V0 | GFC0/IO83NPB5V0 |
| H6[1] | GFA1/IO64PDB5V0 | GFA1/IO81PDB5V0 |
| H7 | GND | GND |
| H8 | VCC | VCC |
| H9 | GND | GND |
| H10 | VCC | VCC |
| H11 | GND | GND |
| H12 | VCC | VCC |
| H13 | GND | GND |
| H14 | VCC | VCC |
| H15 | GND | GND |
| H16 | VCCFPGAIOB1 | VCCFPGAIOB1 |
| H17[1] | IO25NDB1V0 | IO29NDB1V0 |
| H18[1] | GCC2/IO25PDB1V0 | GCC2/IO29PDB1V0 |
| H19 | GND | GND |
| H20[1] | GCC0/IO26NPB1V0 | GCC0/IO35NPB1V0 |
| H21 | VCCFPGAIOB1 | VCCFPGAIOB1 |
| H22[1] | GCB0/IO27NDB1V0 | GCB0/IO34NDB1V0 |
| J1[1] | EMC_DB[6]/GEB0/IO62NDB5V0 | EMC_DB[6]/GEB0/IO79NDB5V0 |
| J2[1] | EMC_DB[5]/GEA1/IO61PDB5V0 | EMC_DB[5]/GEA1/IO78PDB5V0 |
| J3[1] | EMC_DB[4]/GEA0/IO61NDB5V0 | EMC_DB[4]/GEA0/IO78NDB5V0 |
| J4[1] | EMC_DB[3]/GEC2/IO60PPB5V0 | EMC_DB[3]/GEC2/IO77PPB5V0 |
| J5 | VCCFPGAIOB5 | VCCFPGAIOB5 |
| J6[1] | GFA0/IO64NDB5V0 | GFA0/IO81NDB5V0 |
| J7 | VCCFPGAIOB5 | VCCFPGAIOB5 |
| J8 | GND | GND |
| J9 | VCC | VCC |
| J10 | GND | GND |

| .....continued | | |
|---|---|---|
| Pin Number | FG484 | |
| | A2F200 Function | A2F500 Function |
| J11 | VCC | VCC |
| J12 | GND | GND |
| J13 | VCC | VCC |
| J14 | GND | GND |
| J15 | VCC | VCC |
| J16 | GND | GND |
| J17[1] | NC | IO37PDB1V0 |
| J18 | VCCFPGAIOB1 | VCCFPGAIOB1 |
| J19[1] | GCA0/IO28NDB1V0 | GCA0/IO36NDB1V0[2] |
| J20[1] | GCA1/IO28PDB1V0 | GCA1/IO36PDB1V0[2] |
| J21[1] | GCC1/IO26PPB1V0 | GCC1/IO35PPB1V0 |
| J22[1] | GCB1/IO27PDB1V0 | GCB1/IO34PDB1V0 |
| K1 | GND | GND |
| K2[1] | EMC_DB[0]/GEA2/IO59NDB5V0 | EMC_DB[0]/GEA2/IO76NDB5V0 |
| K3[1] | EMC_DB[1]/GEB2/IO59PDB5V0 | EMC_DB[1]/GEB2/IO76PDB5V0 |
| K4[1] | NC | IO74PPB5V0 |
| K5[1] | EMC_DB[2]/IO60NPB5V0 | EMC_DB[2]/IO77NPB5V0 |
| K6[1] | NC | IO75PDB5V0 |
| K7 | GND | GND |
| K8 | VCC | VCC |
| K9 | GND | GND |
| K10 | VCC | VCC |
| K11 | GND | GND |
| K12 | VCC | VCC |
| K13 | GND | GND |
| K14 | VCC | VCC |
| K15 | GND | GND |
| K16 | VCCFPGAIOB1 | VCCFPGAIOB1 |
| K17[1] | NC | IO37NDB1V0 |
| K18[1] | GDA1/IO31PDB1V0 | GDA1/IO40PDB1V0 |
| K19[1] | GDA0/IO31NDB1V0 | GDA0/IO40NDB1V0 |
| K20[1] | GDC1/IO29PDB1V0 | GDC1/IO38PDB1V0 |
| K21[1] | GDC0/IO29NDB1V0 | GDC0/IO38NDB1V0 |
| K22 | GND | GND |
| L1[1] | NC | IO73PDB5V0 |
| L2[1] | NC | IO73NDB5V0 |
| L3[1] | NC | IO72PPB5V0 |
| L4 | GND | GND |
| L5[1] | NC | IO74NPB5V0 |
| L6[1] | NC | IO75NDB5V0 |
| L7 | VCCFPGAIOB5 | VCCFPGAIOB5 |
| L8 | GND | GND |
| L9 | VCC | VCC |
| L10 | GND | GND |

| .....continued | | |
|---|---|---|
| Pin Number | FG484 | |
| | A2F200 Function | A2F500 Function |
| L11 | VCC | VCC |
| L12 | GND | GND |
| L13 | VCC | VCC |
| L14 | GND | GND |
| L15 | VCC | VCC |
| L16 | GND | GND |
| L17 | GNDQ | GNDQ |
| L18[1] | GDA2/IO33NDB1V0 | GDA2/IO42NDB1V0 |
| L19 | VCCFPGAIOB1 | VCCFPGAIOB1 |
| L20[1] | GDB1/IO30PDB1V0 | GDB1/IO39PDB1V0 |
| L21[1] | GDB0/IO30NDB1V0 | GDB0/IO39NDB1V0 |
| L22[1] | GDC2/IO32PDB1V0 | GDC2/IO41PDB1V0 |
| M1[1] | NC | IO71PDB5V0 |
| M2[1] | NC | IO71NDB5V0 |
| M3 | VCCFPGAIOB5 | VCCFPGAIOB5 |
| M4[1] | NC | IO72NPB5V0 |
| M5 | GNDQ | GNDQ |
| M6[1] | NC | IO68PDB5V0 |
| M7 | GND | GND |
| M8 | VCC | VCC |
| M9 | GND | GND |
| M10 | VCC | VCC |
| M11 | GND | GND |
| M12 | VCC | VCC |
| M13 | GND | GND |
| M14 | VCC | VCC |
| M15 | GND | GND |
| M16 | VCCFPGAIOB1 | VCCFPGAIOB1 |
| M17 | NC | NC |
| M18[1] | GDB2/IO33PDB1V0 | GDB2/IO42PDB1V0 |
| M19 | VJTAG | VJTAG |
| M20 | GND | GND |
| M21 | VPP | VPP |
| M22[1] | IO32NDB1V0 | IO41NDB1V0 |
| N1 | GND | GND |
| N2[1] | NC | IO70PDB5V0 |
| N3[1] | NC | IO70NDB5V0 |
| N4 | VCCRCOSC | VCCRCOSC |
| N5 | VCCFPGAIOB5 | VCCFPGAIOB5 |
| N6[1] | NC | IO68NDB5V0 |
| N7 | VCCFPGAIOB5 | VCCFPGAIOB5 |
| N8 | GND | GND |
| N9 | VCC | VCC |
| N10 | GND | GND |

| .....continued | | |
|---|---|---|
| Pin Number | FG484 | |
| | A2F200 Function | A2F500 Function |
| N11 | VCC | VCC |
| N12 | GND | GND |
| N13 | VCC | VCC |
| N14 | GND | GND |
| N15 | VCC | VCC |
| N16[1] | NC | GND |
| N17 | NC | NC |
| N18 | VCCFPGAIOB1 | VCCFPGAIOB1 |
| N19 | VCCENVM | VCCENVM |
| N20 | GNDENVM | GNDENVM |
| N21 | NC | NC |
| N22 | GND | GND |
| P1[1] | NC | IO69NDB5V0 |
| P2[1] | NC | IO69PDB5V0 |
| P3 | GNDRCOSC | GNDRCOSC |
| P4 | GND | GND |
| P5 | NC | NC |
| P6 | NC | NC |
| P7 | GND | GND |
| P8 | VCC | VCC |
| P9 | GND | GND |
| P10 | VCC | VCC |
| P11 | GND | GND |
| P12 | VCC | VCC |
| P13 | GND | GND |
| P14 | VCC | VCC |
| P15 | GND | GND |
| P16 | VCCFPGAIOB1 | VCCFPGAIOB1 |
| P17 | TDI | TDI |
| P18 | TCK | TCK |
| P19 | GND | GND |
| P20 | TMS | TMS |
| P21 | TDO | TDO |
| P22 | TRSTB | TRSTB |
| R1 | MSS_RESET_N | MSS_RESET_N |
| R2 | VCCFPGAIOB5 | VCCFPGAIOB5 |
| R3[1] | GPIO_1/IO46RSB4V0 | GPIO_1/IO55RSB4V0 |
| R4 | NC | NC |
| R5 | NC | NC |
| R6 | NC | NC |
| R7 | NC | NC |
| R8 | GND | GND |
| R9 | VCC | VCC |
| R10 | GND | GND |

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| Pin Number | FG484 | |
|---|---|---|
| | A2F200 Function | A2F500 Function |
| R11 | VCC | VCC |
| R12 | GND | GND |
| R13 | VCC | VCC |
| R14 | GND | GND |
| R15 | VCC | VCC |
| R16 | JTAGSEL | JTAGSEL |
| R17 | NC | NC |
| R18 | NC | NC |
| R19 | NC | NC |
| R20 | NC | NC |
| R21 | VCCFPGAIOB1 | VCCFPGAIOB1 |
| R22 | NC | NC |
| T1 | GND | GND |
| T2 | VCCMSSIOB4 | VCCMSSIOB4 |
| T3[1] | GPIO_8/IO39RSB4V0 | GPIO_8/IO48RSB4V0 |
| T4[1] | GPIO_11/IO57RSB4V0 | GPIO_11/IO66RSB4V0 |
| T5 | GND | GND |
| T6 | MAC_CLK | MAC_CLK |
| T7 | VCCMSSIOB4 | VCCMSSIOB4 |
| T8 | VCC33SDD0 | VCC33SDD0 |
| T9 | VCC15A | VCC15A |
| T10 | GNDAQ | GNDAQ |
| T11 | GND33ADC0 | GND33ADC0 |
| T12 | ADC7 | ADC7 |
| T13[1] | NC | TM4 |
| T14[1] | NC | VAREF2 |
| T15 | VAREFOUT | VAREFOUT |
| T16 | VCCMSSIOB2 | VCCMSSIOB2 |
| T17 | SPI_1_DO/GPIO_24 | SPI_1_DO/GPIO_24 |
| T18 | GND | GND |
| T19 | NC | NC |
| T20 | NC | NC |
| T21 | VCCMSSIOB2 | VCCMSSIOB2 |
| T22 | GND | GND |
| U1 | GND | GND |
| U2[1] | GPIO_5/IO42RSB4V0 | GPIO_5/IO51RSB4V0 |
| U3[1] | GPIO_10/IO58RSB4V0 | GPIO_10/IO67RSB4V0 |
| U4 | VCCMSSIOB4 | VCCMSSIOB4 |
| U5[1] | MAC_RXD[1]/IO53RSB4V0 | MAC_RXD[1]/IO62RSB4V0 |
| U6 | NC | NC |
| U7 | VCC33AP | VCC33AP |
| U8 | VCC33N | VCC33N |
| U9 | CM1 | CM1 |
| U10 | VAREF0 | VAREF0 |

| .....continued | | |
|---|---|---|
| Pin Number | FG484 | |
| | A2F200 Function | A2F500 Function |
| U11 | GND33ADC1 | GND33ADC1 |
| U12 | ADC4 | ADC4 |
| U13[1] | NC | GNDTM2 |
| U14[1] | NC | ADC11 |
| U15 | GNDVAREF | GNDVAREF |
| U16 | VCC33SDD1 | VCC33SDD1 |
| U17 | SPI_0_DO/GPIO_16 | SPI_0_DO/GPIO_16 |
| U18 | UART_0_RXD/GPIO_21 | UART_0_RXD/GPIO_21 |
| U19 | VCCMSSIOB2 | VCCMSSIOB2 |
| U20 | I2C_1_SCL/GPIO_31 | I2C_1_SCL/GPIO_31 |
| U21 | I2C_0_SCL/GPIO_23 | I2C_0_SCL/GPIO_23 |
| U22 | GND | GND |
| V1[1] | GPIO_0/IO47RSB4V0 | GPIO_0/IO56RSB4V0 |
| V2[1] | GPIO_6/IO41RSB4V0 | GPIO_6/IO50RSB4V0 |
| V3[1] | GPIO_9/IO38RSB4V0 | GPIO_9/IO47RSB4V0 |
| V4[1] | MAC_MDIO/IO49RSB4V0 | MAC_MDIO/IO58RSB4V0 |
| V5[1] | MAC_RXD[0]/IO54RSB4V0 | MAC_RXD[0]/IO63RSB4V0 |
| V6 | GND | GND |
| V7 | SDD0 | SDD0 |
| V8 | ABPS1 | ABPS1 |
| V9 | ADC2 | ADC2 |
| V10 | VCC33ADC0 | VCC33ADC0 |
| V11 | ADC6 | ADC6 |
| V12 | ADC5 | ADC5 |
| V13 | ABPS5 | ABPS5 |
| V14[1] | NC | ADC8 |
| V15[1] | NC | GND33ADC2 |
| V16 | NC | NC |
| V17 | GND | GND |
| V18 | SPI_0_DI/GPIO_17 | SPI_0_DI/GPIO_17 |
| V19 | SPI_1_DI/GPIO_25 | SPI_1_DI/GPIO_25 |
| V20 | UART_1_TXD/GPIO_28 | UART_1_TXD/GPIO_28 |
| V21 | I2C_0_SDA/GPIO_22 | I2C_0_SDA/GPIO_22 |
| V22 | I2C_1_SDA/GPIO_30 | I2C_1_SDA/GPIO_30 |
| W1[1] | GPIO_2/IO45RSB4V0 | GPIO_2/IO54RSB4V0 |
| W2[1] | GPIO_7/IO40RSB4V0 | GPIO_7/IO49RSB4V0 |
| W3 | GND | GND |
| W4[1] | MAC_CRSDV/IO51RSB4V0 | MAC_CRSDV/IO60RSB4V0 |
| W5[1] | MAC_TXD[1]/IO55RSB4V0 | MAC_TXD[1]/IO64RSB4V0 |
| W6[1] | NC | SDD2 |
| W7 | GNDA | GNDA |
| W8 | TM0 | TM0 |
| W9 | ABPS2 | ABPS2 |
| W10 | GND33ADC0 | GND33ADC0 |

| .....continued | | |
|---|---|---|
| Pin Number | FG484 | |
| | A2F200 Function | A2F500 Function |
| W11 | VCC15ADC1 | VCC15ADC1 |
| W12 | ABPS6 | ABPS6 |
| W13[1] | NC | CM4 |
| W14[1] | NC | ABPS9 |
| W15[1] | NC | VCC33ADC2 |
| W16 | GNDA | GNDA |
| W17 | PU_N | PU_N |
| W18 | GNDSDD1 | GNDSDD1 |
| W19 | SPI_0_CLK/GPIO_18 | SPI_0_CLK/GPIO_18 |
| W20 | GND | GND |
| W21 | SPI_1_SS/GPIO_27 | SPI_1_SS/GPIO_27 |
| W22 | UART_1_RXD/GPIO_29 | UART_1_RXD/GPIO_29 |
| Y1[1] | GPIO_3/IO44RSB4V0 | GPIO_3/IO53RSB4V0 |
| Y2 | VCCMSSIOB4 | VCCMSSIOB4 |
| Y3[1] | GPIO_15/IO34RSB4V0 | GPIO_15/IO43RSB4V0 |
| Y4[1] | MAC_TXEN/IO52RSB4V0 | MAC_TXEN/IO61RSB4V0 |
| Y5 | VCCMSSIOB4 | VCCMSSIOB4 |
| Y6 | GNDSDD0 | GNDSDD0 |
| Y7 | CM0 | CM0 |
| Y8 | GNDTM0 | GNDTM0 |
| Y9 | ADC0 | ADC0 |
| Y10 | VCC15ADC0 | VCC15ADC0 |
| Y11 | ABPS7 | ABPS7 |
| Y12 | TM3 | TM3 |
| Y13[1] | NC | ABPS8 |
| Y14[1] | NC | GND33ADC2 |
| Y15[1] | NC | VCC15ADC2 |
| Y16 | VCCMAINXTAL | VCCMAINXTAL |
| Y17 | SDD1 | SDD1 |
| Y18 | PTEM | PTEM |
| Y19 | VCC33A | VCC33A |
| Y20 | SPI_0_SS/GPIO_19 | SPI_0_SS/GPIO_19 |
| Y21 | VCCMSSIOB2 | VCCMSSIOB2 |
| Y22 | UART_0_TXD/GPIO_20 | UART_0_TXD/GPIO_20 |

**Notes:**

1. Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device. This note is applicable for entire row.
2. Indicates that the signal assigned to the pins as a CLKBUF/CLKBUF_LVPECL/CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. Refer to the 'Glitchless MUX' section in the SmartFusion Microcontroller Subsystem User's Guide for more details.

# 23. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

| Revision | Date | Description |
|---|---|---|
| A | 08/2023 | The following is a summary of changes made in this revision.<br>• The document was migrated to the Microchip template.<br>• The document number was updated to DS60001821A from 51700112.<br>• Added a Note for A2F060 regarding the discontinuation of the device. See Table 1, Table 2, Table 4, Table 5, Table 4-2, Figure 3, Table 4-7, Table 4-8, Table 7-3, Table 12-1, Table 16-1, Table 19-3, Table 22-1, Table 22-2, and Table 22-4.<br>• Updated all the Microsemi references with Microchip references. |
| 14.0 | 11/2018 | Information about SPI timing was updated. See Table 16-1 . |
| 13.0 | 03/2015 | Updated Unused MSS I/O Configuration information in 21. User I/O Naming Conventions . |
| | | • Updated Table 12-1.<br>• Changed the maximum clock frequency for the control logic – 5 cycles to 50 MHz for A2F060 and A2F200 devices .<br>• Added the following Note: “Moving from 5:1:1:1 mode to 6:1:1:1 mode results in throughput change that is dependent on the system functionality. When the Cortex-M3 code is executed from eNVM - with sequential firmware (sequential address reads), the throughput reduction can be around 10%” |
| 12.0 | 11/2013 | CS288 package dimensions added to Table 3. |
| | | Added Table 19-3. |
| | | Definition of Ethernet MAC clarified in the 2. General Description |
| | | Clarified GC and GF global inputs in 20. Global I/O Naming Conventions and link to SF Fabric UG added. |
| 11.0 | 09/2013 | Modified the description for VAREF0 in the 20. User-Defined Supply Pins. |
| | | Updated the 22. Pin Assignment Tables with a note for A2F500, all packages with GCAx saying: “Signal assigned to those pins as a CLKBUF or CLKBUF_LVPECL or CLKBUF_LVDS goes through a glitchless mux. In order for the glitchless mux to operate correctly, the signal must be a free-running clock signal. |

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|---|---|---|
| **Revision** | **Date** | **Description** |
| 10.0 | 01/2013 | The SmartFusion cSoC Family Product Table has been updated to specify that External Memory Controller support for A2F060-TQ144 is not available. |
| | | The following Note was added to the Table 2 table: "There are no LVTTL capable direct inputs available on A2F060 devices." |
| | | The Product Ordering Codes has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio". |
| | | Added a note to Table 3-3:The programming temperature range supported is Tambient = 0°C to 85°C. |
| | | Statements about the state of the I/Os during programming were updated in the following sections: 3.3. I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial) and 21. User I/O Naming Conventions. |
| | | In Table 3-4, the upper value of temperature ranges was corrected from "Min." to "Max." |
| | | Information for A2F200M3F-CS288 was added to Table 3-6. The die size column was removed.<br>Also added details for A2F200M3F-PQG208I |
| | | Added the following note to Table 5-47 and Table 5-50: "The above mentioned timing parameters correspond to 24 mA drive strength." |
| | | The note in Table 10-1 referring the reader to SmartGen was revised to refer instead to the online help associated with the core. |
| | | The SRAM collision data in Table 11-1 and Table 11-2 was updated. |
| | | The maximum input bias current for comparators 1, 3, 5, 7, and 9, in Table 15-5, was revised from 60 to 100 nA. |
| | | Corrected the Start-up time unit from "ms" to "µs" in Table 15-7 |
| | | Added the 18.4. References for 18. SmartFusion Development Tools. |
| | | Updated the 18.4. References for Programming.Added the 19.4.2. Application Notes on IAP Programming Technique |
| | | A note was added to the Table 20-1 table, referring to the SmartFusion cSoC Board Design Guidelines application note for details on VCCPLLx capacitor recommendations. |
| | | In the 20. Supply Pins, the VPP capacitor value section has been modified to: "For proper programming, 0.01µF, and 0.1µF to 1µF capacitors, (both rated at 16V) are to be connected in parallel across VPP and GND, and positioned as close to the FPGA pins as possible." |
| | | In the 20. User-Defined Supply Pins, added description 'These pins are located in Bank-2 (GPIO_16 to GPIO_31) for A2F060, A2F200, and A2F500 devices.' for GPIO_x. |
| | | Updated the MAINXIN and MAINXOUT pin descriptions in the 21. Special Function Pins to read "If an external RC network or clock input is used, the RC components are connected to the MAINXIN pin, with MAINXOUT left floating. When the main crystal oscillator is not being used, MAINXIN and MAINXOUT pins can be left floating." |
| | | Live at Power-Up (LAPU) has been replaced with 'Instant On'. |

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|---|---|---|
| **Revision** | **Date** | **Description** |
| 9.0 | 09/2012 | The number of signal conditioning blocks (SCBs) for A2F500 in the Table 1 was corrected to 4. Previously it had incorrectly been listed as 2. |
| | | The Product Ordering Codes was revised to clarify that only one eNVM size for each device is currently available.. |
| | | Information pertaining to analog I/Os was added to the 2.4. Specifying I/O States During Programming |
| | | The formulas in the table notes for Table 5-11were corrected. |
| | | Maximum values for VIL and VIH were corrected in LVPECL Table 5-48. |
| | | Minimum pulse width High and Low values were added to the tables in the 7.2. Global Tree Timing Characteristics. The maximum frequency for global clock parameter was removed from these tables because a frequency on the global is only an indication of what the global network can do. There are other limiters such as the SRAM, I/Os, and PLL. SmartTime software should be used to determine the design frequency.. |
| | | The temperature range for accuracy in Table 8-1 was changed from "0°C to 85°C" to "–40°C to 100°C" .The units for jitter were changed from ps to ps RMS. |
| | | In Table 9-1, the output jitter for the 10 MHz crystal was corrected from 50 ps RMS to 1 ns RS . Values for the startup time of VILXTAL were added. |
| | | In Table 9-2, output jitter was changed from 50 ps RMS to 30 ps RMS . A value for ISTBXTAL standby current was added. Startup time for a test load of 30 pF was added. . |
| | | The following note was added to Table 10-1 in regard to delay increments in programmable delay blocks:<br>"When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to SmartGen online help for more information." |
| | | Figure 11-8 and Figure 11-9 have been added. |
| | | Information regarding the MSS resetting itself after IAP of the FPGA fabric was added to the 19.2.1. Reprogramming the FPGA Fabric Using the Cortex-M3 . |
| | | Instructions for unused VCC33ADCx pins were revised in 20. Supply Pins . |
| | | Libero IDE was changed to Libero SoC throughout the document . |

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| Revision | Date | Description |
|---|---|---|
| 8.0 | 03/2012 | In the . Analog Front-End (AFE) section, the resolution for the first-order sigma delta DAC was corrected from 12-bit to "8-bit, 16-bit, or 24-bit." The same correction was made in the SmartFusion cSoC Family Product Table. |
| | | The SmartFusion cSoC Family Product Table was revised to break out the features by package as well as device.<br>The table now indicates that only one SPI is available for the PQ208 package in A2F200 and A2F500, and in the TQ144 package for A2F060.<br>The EMC address bus size has been corrected to 26 bits. |
| | | Table 4 was revised to change the CS288 package for A2F200 and A2F500 from preliminary to production status. |
| | | TQ144 package information for A2F060 was added to Table 2, Table 4, Product Ordering Codes, and Table 5. |
| | | Table 3 is new . |
| | | The Halogen-Free Packaging code (H) was removed from the Product Ordering Codes . |
| | | The 2.4. Specifying I/O States During Programming is new . |
| | | The reference to guidelines for global spines and VersaTile rows, given in the Global Clock Dynamic Contribution—$P_{CLOCK}$ section, was corrected to the "Device Architecture" chapter in the SmartFusion FPGA Fabric User's Guide . |
| | | The AC Loading figures in the 5.4. Single-Ended I/O Characteristics were updated to match tables in the 5.2. Summary of I/O Timing Characteristics – Default I/O Software Settings section. . |
| | | The following sentence was deleted from the 5.4. 2.5V LVCMOS section: "It uses a 5V–tolerant input buffer and push-pull output buffer." |
| | | In the 11. FPGA Fabric SRAM Timing Characteristics tables, reference was made to a new application note, Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs, which covers these cases in detail . |
| | | The note for Table 15-1 was modified to include the statement that the restriction on the TM pad being no greater than 10 mV above the CM pad is applicable only if current monitor is used . |
| | | The unit "FR" in Table 15-4 and Table 15-6, used to designate full-scale error, was changed to "FS" and clarified with a table note . |
| | | The description of 19.2. In-Application Programming methodology was changed to state the difference for A2F060 and A2F500 compared to A2F200 . |
| | | The 20. Global I/O Naming Conventions section is new . The description for IO 21. User Pins was revised accordingly and moved out of the table and into a new section: 21. User I/O Naming Conventions . |
| | | The descriptions for MAINXIN and MAINXOUT were revised to state how they should be handled if using an external RC network or clock input . |
| | | The description and type was revised for the MSS_RESET_N pin . |
| | | The 22.1. TQ144 section and pin table for A2F060 are new. |

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| Revision | Date | Description |
|---|---|---|
| 7.0 | 08/2011 | The title of the datasheet was changed from SmartFusion Intelligent Mixed Signal FPGAs to SmartFusion Customizable System-on-Chip (cSoC). Terminology throughout was changed accordingly. The term cSoC defines a category of devices that include at least FPGA fabric and a processor subsystem of some sort. It can also include any of the following: analog, SerDes, ASIC blocks, customer specific IP, or application-specific IP. SmartFusion is Microsemi's first cSoC . |
| | | The SmartFusion cSoC Family Product Table was revised to remove the note stating that the A2F060 device is under definition and subject to change . A note was added for EMC, stating that it is not available on A2F500 for the PQ208 package . |
| | | Table 4 table was revised. The status for A2F060 CS288 and FG256 moved from Advance to Preliminary. A2F200 PQ208 and A2F500 PQ208 moved from Advance to Production . |
| | | Table 2 was revised. The number of direct analog inputs for A2F060 packages increased from 6 to 11. The number of MSS I/Os for the A2F060 FG256 package increased from 25 to 26 . A note was added stating that EMC is not available for the A2F500 PQ208 package . |
| | | The note associated with the Figure 2 diagram was corrected from "Architecture for A2F500" to "Architecture for A2F200" . |
| | | The Licensed DPA Logo was added to the Product Ordering Codes. The trademarked Licensed DPA Logo identifies that a product is covered by a DPA counter-measures license from Cryptography Research . |
| | | The 2.3. Security section and 19.2.3. Secure Programming section were updated to clarify that although no existing security measures can give an absolute guarantee, SmartFusion cSoCs implement the best security available in the industry . |
| | | Storage temperature, TSTG, and junction temperature, TJ, were added to Table 3-1 . |
| | | AC/DC characteristics for A2F060 were added to the "SmartFusion DC and Switching Characteristics" chapter . The following tables were updated:<br>Table 4-7<br>Table 4-8<br>Table 12-1<br>Table 15-6<br>Table 16-1 |

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| Revision | Date | Description |
|---|---|---|
| | | The following sentence was removed from the 3.3. I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial) section because it is incorrect : “The many different supplies can power up in any sequence with minimized current spikes or surges.” |
| | | Table 2-8 • Quiescent Supply Current Characteristics was divided into two tables: one for power supplies configurations and one for quiescent supply current. SoC mode was added to both tables and VCOMPLAx was removed from Table 4-1. Quiescent supply current values were updated in Table 4-2 . |
| | | The Total Static Power Consumption—PSTAT section was revised: ”NeNVM-BLOCKS * PDC4“ was removed from the equation for PSTAT . |
| | | Table 4-7 and Table 4-8 were revised to reflect updates in the SmartFusion power calculator . |
| | | Table 7-3 is new . |
| | | Output duty cycle was corrected to 50% in Table 8-1. It was incorrectly noted as 1% previously. Operating current for 3.3 domain was added . |
| | | Table 10-1 was revised to add information and measurements regarding CCC output peak-to-peak period jitter . |
| | | The port names in the SRAM Timing Waveforms, SRAM Timing Characteristics tables, Figure 11-10, and the FIFO Timing Waveforms tables were revised to ensure consistency with the software names . |
| | | Table 12-1 was revised to correct the maximum frequencies . |
| | | Table 15-5 was moved to the SmartFusion DC and Switching Characteristics section from the SmartFusion Programmable Analog User’s Guide because the information is extracted from characterization . |
| | | The hysteresis section in Table 15-5 was revised . |
| | | The 18. SmartFusion Development Tools was extensively updated . |
| | | The text following Table 19-2 was updated to add information on control of the JTAGSEL pin. Manual jumpers on the evaluation and development kits allow manual selection of this function for J-Link and ULINK debuggers . |

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| Revision | Date | Description |
|---|---|---|
| | | Usage instructions, such as how to handle the pin when unused, were added for the following supply pins, in Table 20-1:<br>VCC15A<br>VCC15ADC0 through VCC15ADC2<br>VCC33ADC0 through VCC33ADC2<br>VCC33AP<br>VCC33ADC2“<br>VCCLPXTAL“<br>VCCMAINXTAL<br>VCCMSSIOB2<br>VCCPLLx<br>VCCRCOSC<br>VDDBAT |
| | | The “IO” description in 21. User I/O Naming Conventionssection was revised to clarify the definitions of u, I/O pair, and w, differential pair . Information on configuration of unused I/Os (including unused MSS I/Os, was added . |
| | | Usage instructions were added for the following pins :<br>MSS_RESET_N<br>TCK<br>TMS<br>TRSTB<br>MAC_CLK |
| | | Package names used in the 22. Pin Assignment Tables section were revised to match standards given in Package Mechanical Drawings . |
| | | The pin assignments for A2F060 for 22.1. TQ144 and 22.1. FG256 have been revised due to the device status change from advance to preliminary.<br>The 22.1. TQ144 and 22.1. FG256 pin assignment sections previously compared functions between A2F060/A2F200 devices in one table and A2F200/A2F500 in a separate table. Functions for all three devices have now been combined into one table for each package . |
| | | The 22.1. PQ208 pin table was revised for A2F500 to remove EMC functions, which are not available for this device/package combination. |
| 6.0 | 03/2011 | The 22.1. PQ208 package was added to product tables and Product Ordering Codes for A2F200 and A2F500. |
| | | Table 2 was revised to add the CS288 package for A2F060 and the PQ208 package for A2F200 and A2F500. A row was added for shared analog inputs . |
| | | Table 4 was updated . |
| | | VCCESRAM was added to Table 3-1, Table 3-3, Table 4-1, and the Table 20-1 . |
| | | The following note was removed from Table 4-1:<br>“Current monitors and temperature monitors should not be used when Power-Down and/or Sleep mode are required by the application.“ |

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|---|---|---|
| **Revision** | **Date** | **Description** |
| | | Dynamic power values were updated in the following tables. The table subtitles changed where FPGA I/O banks were involved to note "I/O assigned to EMC I/O pins" .<br>Table 4-4<br>Table 4-6. |
| | | The 5.1. Timing Model section was updated . |
| | | Values in the timing tables for the following sections were updated. Table subtitles were updated for FPGA I/O banks to note "I/O assigned to EMC I/O pins" .<br>5.2. Overview of I/O Performancesection: Table 5-6, Table 5-7,<br>5.3. Detailed I/O DC Characteristicssection: Table 5-20, Table 5-21, Table 5-22, Table 5-26, Table 5-27, Table 5-28, Table 5-32, Table 5-33, Table 5-32, Table 5-38, Table 5-39, Table 5-40, Table 5-43, Table 5-44<br>LVDS section: Table 5-47<br>LVPECL section: Table 5-50<br>7.2. Global Tree Timing Characteristicssection: Table 7-1, Table 7-2 |
| | | The 22.1. PQ208 section and pin tables are new . |
| | | Global clocks were removed from the A2F060 pin table for the 22.1. CS288 and 22.1. FG256 packages, resulting in changed function names for affected pins . |
| 5.0 | 12/2010 | Table 3-2 was revised. The recommended CM[n] pad voltage (relative to ground) was changed from –11 to –0.3 . |
| | | Table 3-7 was revised to change the values for 100 °C. |
| | | Power-down and Sleep modes, and all associated notes, were removed from Table 4-1 . IDC3 and IDC4 were renamed to IDC1 and IDC2 . These modes are no longer supported. A note was added to the table stating that current monitors and temperature monitors should not be used when Power-down and/or Sleep mode are required by the application. |
| | | The "Power-Down and Sleep Mode Implementation" section was deleted . |
| | | Values for PAC9 and PAC10 for LVDS and LVPECL were revised in Table 4-3 and Table 4-5. |
| | | Values for PAC1 through PAC4, PDC1, and PDC2 were added for A2F500 in Table 4-7 and Table 4-8 |
| | | The equation for Total Dynamic Power Consumption in SoC Mode was revised to add $P_{MSS}$. The Microcontroller Subsystem Dynamic Contribution—PMSS section is new . |
| | | Information in Table 5-6 (applicable to FPGA I/O banks) and Table 5-7 (applicable to MSS I/O banks) was updated. |
| | | Available values for the Std. speed were added to the timing tables from Table 5-20 to Table 14-1 .<br>One or more values changed for the –1 speed in tables covering 3.3 V LVCMOS, 2.5 V LVCMOS, 1.8 V LVCMOS, 1.5 V LVCMOS, Combinatorial Cell Propagation Delays, and A2F200 Global Resources. |
| | | Table 7-1 is new. |
| | | Table 12-1 was revised . |
| | | The programmable analog specifications tables were revised with updated information. |
| | | Table 19-1 was revised by adding a note to indicate "planned support" for several of the items in the table. |
| | | The note on JTAGSEL in the 19.1. In-System Programming section was revised to state that SoftConsole selects the appropriate TAP controller using the CTXSELECT JTAG command. When using SoftConsole, the state of JTAGSEL is a "don't care" . |
| | | Table 22-2 and Table 22-4 pin tables for A2F060 are new, comparing the A2F060 function with the A2F200 function . |
| | | The "Handling When Unused" column was removed from Table 22-4 pin table for A2F200 and A2F500 . |

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| **Revision** | **Date** | **Description** |
| 4.0 | 09/2010 | Table 4-1 was revised. VCCRCOSC was moved to a column of its own with new values. VCCENVM was added to the table. Standby mode for VJTAG and VPP was changed from 0 V to N/A. ”Disable“ was changed to ”Off“ in the eNVM column. The column for RCOSC was deleted. |
| | | The ”Power-Down and Sleep Mode Implementation“ section was revised to include VCCROSC. |

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| Revision | Date | Description |
|---|---|---|
| 3.0 | 09/2010 | The I/Os and Operating Voltage section was revised to list "single 3.3 V power supply with on-chip 1.5 V regulator" and "external 1.5 V is allowed" . |
| | | The CS288 package was added to Table 2 , Product Ordering Codes, and Table 5 table. The number of direct analog inputs for the FG256 package in A2F060 was changed from 8 to 6. |
| | | Two notes were added to the SmartFusion cSoC Family Product Table indicating limitations for features of the A2F500 device:<br>Two PLLs are available in CS288 and FG484 (one PLL in FG256).<br>[ADCs, DACs, SCBs, comparators, current monitors, and bipolar high voltage monitors are] Available on FG484 only. FG256 and CS288 packages offer the same programmable analog capabilities as A2F200.<br>Table cells were merged in rows containing the same values for easier reading. |
| | | The security feature option was added to the Product Ordering Codes table. |
| | | In Table 3-3, the VDDBAT recommended operating range was changed from "2.97 to 3.63" to "2.7 to 3.63".Recommended operating range was changed to "3.15 to 3.45" for the following voltages:<br>VCC33A<br>VCC33ADCx<br>VCC33AP<br>VCC33SDDx<br>VCCMAINXTAL<br>VCCLPXTAL<br>Two notes were added to the table :<br>1. The following 3.3V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.<br>2. The following 1.5V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx. |
| | | In Table 3-3, the description for VCCLPXTAL was corrected to change "32 Hz" to "32 KHz" . |
| | | The 3.2. Power Supply Sequencing Requirementsection is new. |
| | | Table 4-1 was revised to change most on/off entries to voltages. Note 5 was added, stating that "on" means proper voltage is applied. The values of 6 µA and 16 µA were removed for IDC1 and IDC2 for 3.3 V. A note was added for IDC1 and IDC2: "Power mode and Sleep mode are consuming higher current than expected in the current version of silicon. These specifications will be updated when new version of the silicon is available" . |
| | | The "Power-Down and Sleep Mode Implementation" section is new . |
| | | A note was added to Table 10-1, pertaining to fout_CCC, stating that "one of the CCC outputs (GLA0) is used as an MSS clock and is limited to 100 MHz (maximum) by software" . |
| | | Table 12-1 was revised. Values were included for A2F200 and A2F500, for –1 and Std. speed grades. A note was added to define 6:1:1:1 and 5:1:1:1 . |
| | | The units were corrected (mV instead of V) for input referred offset voltage, GDEC[1:0] = 00 in Table 15-4. |
| | | The test condition values for operating current (ICC33A, typical) were changed in Table 15-7 . |
| | | Figure 15-3 was revised to add legends for the three curves, stating the load represented by each . |
| | | The "SmartFusion Programming" chapter was moved to this document from the SmartFusion Subsystem Microcontroller User's Guide. The 19.3. Typical Programming and Erase Times section was added to this chapter. |
| | | Figure 19-1 was revised to change 1.5 V to "VJTAG (1.5 V to 3.3 V nominal)" . |
| | | Two notes were added to the Table 20-1:<br>1. The following supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.<br>2. The following 1.5V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx. |
| | | The descriptions for the VCC33N, NCAP, and PCAP pins were revised to include information on what to do if analog SCB features and SDDs are not used. |
| | | Information was added to the 21. User Pins table regarding tristating of used and unused |

| .....continued | | |
|---|---|---|
| **Revision** | **Date** | **Description** |
| 2.0 | 05/2010 | Embedded nonvolatile flash memory (eNVM) was changed from ”64 to 512 Kbytes“ to ”128 to 512 Kbytes“ in the Microcontroller Subsystem (MSS) and Table 1. |
| | | The main oscillator range of values was changed to ”32 KHz to 20 MHz“ in the Microcontroller Subsystem (MSS) and Table 1. |
| | | The value for tPD was changed from 50 ns to 15 ns for the high-speed voltage comparators listed in the . Analog Front-End (AFE) section. |
| | | The number of PLLs for A2F200 was changed from 2 to 1 in the SmartFusion cSoC Family Product Table. |
| | | Values for direct analog input, total analog input, and total I/Os were updated for the FG256 package, A2F060, in the Table 2. The Max. column was removed from the table. |
| | | The Speed Grade section of the Product Ordering Codes table was revised. |
| 1.0 | 03/2010 | The Product Ordering Codes table was revised to add ”blank“ as an option for lead-free packaging and application (junction temperature range). |
| | | Table 3-3 was revised. Ta (ambient temperature) was replaced with TJ (junction temperature). |
| | | PDC5 was deleted from Table 4-8. |
| | | The formulas in the footnotes for Table 5-11 were revised. |
| | | The values for input biased current were revised in Table 15-1. |

.....continued

| Revision | Date | Description |
|---|---|---|
| 0 | 03/2010 | The #unique_88 was updated to change the throughput for 10-bit mode from 600 Ksps to 550 Ksps. |
| | | The A2F060 device was added to product information tables. |
| | | The Product Ordering Codes table was updated to removed Std. speed and add speed grade 1. Pre-production was removed from the application ordering code category. |
| | | Figure 1 was revised. |
| | | The "Datasheet Categories" section was updated, referencing the Figure 1, which is new. |
| | | The "VCCI" parameter was renamed to "VCCxxxxIOBx."<br>"Advanced I/Os" were renamed to "FPGA I/Os."<br>Generic pin names that represent multiple pins were standardized with a lower case x as a placeholder. For example, VAREFx designates VAREF0, VAREF1, and VAREF2.<br>Modes were renamed as follows:<br>Operating mode was renamed to SoC mode.<br>32KHz Active mode was renamed to Standby mode.<br>Battery mode was renamed to Time Keeping mode.<br>Table entries have been filled with values as data has become available. |
| | | Table 3-1, Table 3-2, and Table 3-3 were revised extensively. |
| | | Device names were updated in Table 3-6. |
| | | Table 4-1 was revised extensively. |
| | | Table 4-4 was revised extensively. |
| | | Removed "Example of Power Calculation." |
| | | Table 4-7 was revised extensively. |
| | | Table 4-8 was revised extensively. |
| | | The 4.4. Power Calculation Methodology section was revised. |
| | | Table 8-1 was revised extensively. |
| | | Table 9-2 was revised extensively. |
| | | The parameter tRSTBQ was changed to TC2CWRH in Table 11-1. |
| | | The 12-bit mode row for integral non-linearity was removed from Table 15-3. The typical value for 10-bit mode was revised. The table note was punctuated correctly to make it clear. |
| | | Figure 37-34 • Write Access after Write onto Same Address, Figure 37-34 • Read Access after Write onto Same Address, and Figure 37-34 • Write Access after Read onto Same Address were deleted. |
| | | Table 15-7 was revised extensively. |
| | | The 16. Serial Peripheral Interface (SPI) Characteristics section and 17. Inter-Integrated Circuit (I2C) Characteristics section are new. |
| | | 18. SmartFusion Development Tools was replaced with new content. |
| | | The pin description tables were revised by adding additional pins to reflect the pinout for A2F500. |
| | | The descriptions for GNDSDD1 and VCC33SDD1 were revised. |
| | | The description for VCC33A" was revised. |
| | | The pin tables for the Table 22-4 and Table 22-5 were replaced with tables that compare pin functions across densities for each package. |

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| Revision | Date | Description |
|---|---|---|
| Draft B | 12/2009 | The "Digital I/Os" section was renamed to the I/Os and Operating Voltage section and information was added regarding digital and analog VCC. |
| | | The SmartFusion cSoC Family Product Table and Table 2 were revised. |
| | | The terminology for the analog blocks was changed to "programmable analog," consisting of two blocks: the analog front-end and analog compute engine. This is reflected throughout the text and in the Figure 1. |
| | | The Product Ordering Codes was revised to add G as an ordering code for eNVM size. |
| | | Timing tables were populated with information that has become available for speed grade –1. |
| | | All occurrences of the VMV parameter were removed. |
| | | The SDD[n] voltage parameter was removed from Table 3-2. |
| | | Table 36-4 • Flash Programming Limits – Retention, Storage and Operating Temperature was replaced with Table 3-4. |
| | | The 3.4. Thermal Characteristics section was revised extensively. |
| | | Table 4-1 was revised significantly. |
| | | Table 4-7 and Table 4-8 were updated. |
| | | Figure 5-1 was updated. |
| | | The temperature associated with the reliability for LVTTL/LVCMOS in Table 5-16 was changed from 110º to 100º. |
| | | The values in Table 6-1 were updated. |
| | | Table 9-2 is new. Table 9-1 was revised. |
| | | Table 12-1 and Table 13-1 are new. |
| | | The performance tables in the 15. Programmable Analog Specifications section were revised, including new data available. Table 15-6 is new. |
| | | The "256-Pin FBGA" table for A2F200 is new. |

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