

3.3 V 200 MHz 1:2 LVCMOS/LVTTL Low Skew Fanout Buffer

NB3M8302C



Description

The NB3M8302C is 1:2 fanout buffer with LVCMOS/LVTTL input and output. The device supports the core supply voltage of 3.3 V (V_{DD} pin) and output supply voltage of 2.5 V or 3.3 V (V_{DDO} pin). The V_{DDO} pin powers the two single ended LVCMOS/LVTTL outputs.

The NB3M8302C is Form, Fit and Function (pin to pin) compatible to ICS8302 and ICS8302I. The NB3M8302C is qualified for industrial operating temperature range.

Features

- Input Clock Frequency up to 200 MHz
- Low Output to Output Skew: 25 ps typical
- Low Part to Part Skew: 250 ps typical
- Low Additive RMS Phase Jitter
- Input Clock Accepts LVCMOS/ LVTTL Levels
- Operating Voltage:
 - ♦ Core Supply: $V_{DD} = 3.3 \text{ V} \pm 5\%$
 - ♦ Output Supply: $V_{DDO} = 3.3 \text{ V} \pm 5\%$ or $2.5 \text{ V} \pm 5\%$
- Operating Temperature Range:
 - ♦ Industrial: -40°C to $+85^{\circ}\text{C}$
- These Devices are Pb-Free and are RoHS Compliant

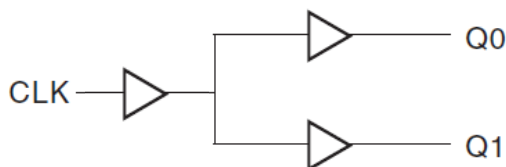
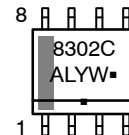


Figure 1. Block Diagram

MARKING DIAGRAM



| | |
|---|---------------------|
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| W | = Work Week |
| ▪ | = Pb-Free Package |

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NB3M8302C

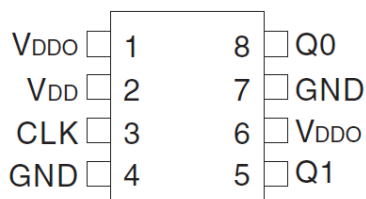


Figure 2. Pin Configuration (Top View)

Table 1. PIN DESCRIPTION

| Pin Number | Name | Type | Description |
|------------|------|----------------------|------------------------------------|
| 1, 6 | VDDO | Output Power | Clock output Supply pin. |
| 2 | VDD | Input and Core Power | Input and Core Supply pin. |
| 3 | CLK | LVC MOS/LVTTL Input | Clock Input. Internally pull-down. |
| 4, 7 | GND | Ground | Supply Ground. |
| 5 | Q1 | LVC MOS/LVTTL Output | LVC MOS/LVTTL Clock output. |
| 8 | Q0 | LVC MOS/LVTTL Output | LVC MOS/LVTTL Clock output. |

Table 2. MAXIMUM RATINGS

| Symbol | Parameter | Condition | Min | Max | Unit |
|------------------------------------|--|--|---------|-------------------------|------|
| V _{DD} , V _{DDO} | Power Supply | | – | 4.6 | V |
| V _I | Input Voltage | | –0.5 | V _{DD} + 0.5 V | V |
| T _{stg} | Storage Temperature | | –65 | +150 | °C |
| θ _{JA} | Thermal Resistance (Junction to Ambient) SOIC–8 | 0 lfpm 500 lfpm | | 80 55 | °C/W |
| θ _{JC} | Thermal Resistance (Junction to Case) (Note 1) | | | 12–17 | °C/W |
| T _{sol} | Wave Solder | 3 sec | | 265 | °C |
| MSL | Moisture Sensitivity SOIC–8 | Indefinite Time Out of Drypack (Note 2) | Level 1 | | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)
2. For additional information, see Application Note [AND8003/D](#).

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Table 3. DC OPERATING CHARACTERISTICS

($V_{DD} = V_{DDO} = 3.3 \text{ V} \pm 5\%$, $V_{DD} = 3.3 \text{ V} \pm 5\%$, $V_{DDO} = 2.5 \text{ V} \pm 5\%$; $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|-----------|--|--|-------|-----|-------|---------------|
| R_{IN} | Input Pull-down Resistor (CLK Pin) | | | 51 | | $k\Omega$ |
| C_{IN} | Input Capacitance | | | 4 | | pF |
| R_{OUT} | Output Impedance (Note 3) | | 5 | 7 | 12 | Ω |
| C_{PD} | Power Dissipation Capacitance (per output) | $V_{DD} = V_{DDO} = 3.465 \text{ V}$ | | 22 | | pF |
| | | $V_{DD} = 3.465 \text{ V}$, $V_{DDO} = 2.625 \text{ V}$ | | 16 | | |
| V_{DD} | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| I_{IH} | Input High Current | $V_{IN} = V_{DD} = 3.465 \text{ V}$ | | | 150 | μA |
| I_{IL} | Input Low Current | $V_{DD} = 3.465 \text{ V}$, $V_{IN} = 0.0 \text{ V}$ | -0.5 | | | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Outputs terminated with 50Ω to $V_{DDO}/2$. See Figure 4 for supply considerations.

Table 4. DC OPERATING CHARACTERISTICS ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Symbol | Parameter | Condition | Min | Max | Unit |
|--------|-----------|-----------|-----|-----|------|
|--------|-----------|-----------|-----|-----|------|

$V_{DD} = 3.3 \text{ V} \pm 5\%$, $V_{DDO} = 2.5 \text{ V} \pm 5\%$

| | | | | | |
|-----------|-----------------------|-----------------------------|-------|-------|---|
| V_{DDO} | Output Supply Voltage | | 2.375 | 2.625 | V |
| V_{OH} | Output HIGH Voltage | $I_{OH} = -16 \text{ mA}$ | 2.1 | | V |
| | | $I_{OH} = -100 \mu\text{A}$ | 2.2 | | |
| | | 50Ω to $V_{DDO}/2$ | 1.8 | | |
| V_{OL} | Output LOW Voltage | $I_{OL} = 16 \text{ mA}$ | | 0.15 | V |
| | | $I_{OL} = 100 \mu\text{A}$ | | 0.2 | |
| | | 50Ω to $V_{DDO}/2$ | | 0.5 | |

$V_{DD} = V_{DDO} = 3.3 \text{ V} \pm 5\%$

| | | | | | |
|-----------|-----------------------|-----------------------------|-------|-------|---|
| V_{DDO} | Output Supply Voltage | | 3.135 | 3.465 | V |
| V_{OH} | Output HIGH Voltage | $I_{OH} = -16 \text{ mA}$ | 2.9 | | V |
| | | $I_{OH} = -100 \mu\text{A}$ | 2.9 | | |
| | | 50Ω to $V_{DDO}/2$ | 2.6 | | |
| V_{OL} | Output LOW Voltage | $I_{OL} = 16 \text{ mA}$ | | 0.15 | V |
| | | $I_{OL} = 100 \mu\text{A}$ | | 0.2 | |
| | | 50Ω to $V_{DDO}/2$ | | 0.5 | |

Table 5. DC OPERATING CHARACTERISTICS ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$; $V_{DD} = V_{DDO} = 3.3 \text{ V} \pm 5\%$, $V_{DD} = 3.3 \text{ V} \pm 5\%$, $V_{DDO} = 2.5 \text{ V} \pm 5\%$)

| Symbol | Parameter | Condition | Min | Max | Unit |
|-----------|--------------------------------|-----------|------|----------------|------|
| I_{DD} | Quiescent Power Supply Current | No Load | | 13 | mA |
| I_{DDO} | Quiescent Power Supply Current | No Load | | 4 | mA |
| V_{IH} | Input HIGH Voltage | | 2 | $V_{DD} + 0.3$ | V |
| V_{IL} | Input LOW Voltage | | -0.3 | 1.3 | V |

Table 6. AC CHARACTERISTICS (Note 4)

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|-------------------------------------|--|-----|-----|-----|------|
| $T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}; V_{DD} = V_{DDO} = 3.3 \text{ V} \pm 5\%$ | | | | | | |
| F_{IN} | Input Frequency | | | | 200 | MHz |
| t_{PLH} | Propagation Delay (Note 5) | $F_{in} = 200 \text{ MHz}$ | 1.9 | | 3.1 | ns |
| t_{SKEW} | Output to Output Skew (Note 6) | | | 25 | 85 | ps |
| | Part to Part Skew (Note 6) | | | 250 | 800 | |
| t_{SKEWDC} | Output Duty Cycle (see Figure 3) | $F_{in} \leq 133 \text{ MHz}$ | 45 | | 55 | % |
| | | $133 \text{ MHz} < F_{in} < 200 \text{ MHz}$ | 40 | | 60 | |
| t_r/t_f | Output rise and fall times (Note 7) | 20% to 80%, $R_S = 33 \Omega$ | 250 | | 800 | ps |

$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}; V_{DD} = 3.3 \text{ V} \pm 5\%, V_{DDO} = 2.5 \text{ V} \pm 5\%$

| | | | | | | |
|--------------|-------------------------------------|--|-----|-----|-----|-----|
| F_{IN} | Input Frequency | | | | 200 | MHz |
| t_{PLH} | Propagation Delay (Note 5) | $F_{in} = 200 \text{ MHz}$ | 2.0 | | 3.3 | ns |
| t_{SKEW} | Output to Output Skew (Note 6) | | | 25 | 85 | ps |
| | Part to Part Skew (Note 6) | | | 250 | 800 | |
| t_{SKEWDC} | Output Duty Cycle (see Figure 3) | $F_{in} \leq 133 \text{ MHz}$ | 45 | | 55 | % |
| | | $133 \text{ MHz} < F_{in} < 200 \text{ MHz}$ | 40 | | 60 | |
| t_r/t_f | Output rise and fall times (Note 7) | 20% to 80%, $R_S = 33 \Omega$ | 200 | | 650 | ps |

4. Clock input with 50% duty cycle. Outputs terminated with 50Ω to $V_{DDO}/2$. See Figures 3 and 4.

5. Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.

6. Similar input conditions and the same supply voltages. Measured at $V_{DDO}/2$. See Figures 3 and 4.

7. R_S is Series Resistance at the clock outputs.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

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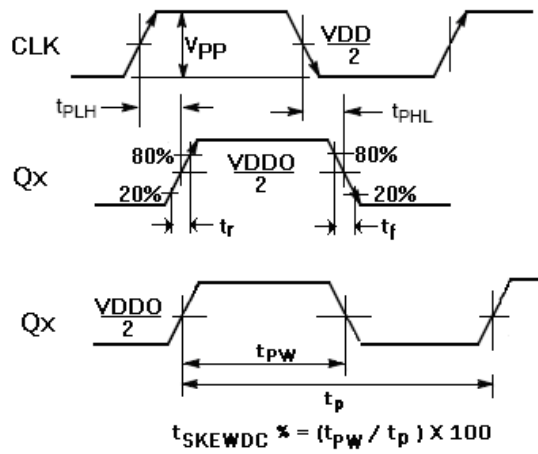
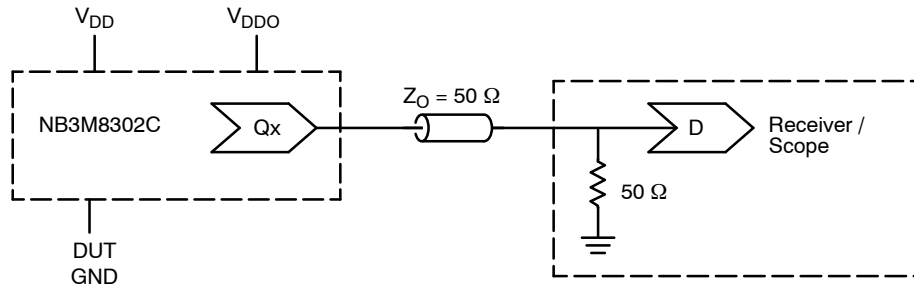


Figure 3. AC Reference Measurement



| Spec Condition: | TEST SETUP V _{DD} : | TEST SETUP V _{DDO} : | TEST SETUP DUT GND: |
|--|------------------------------|-------------------------------|---------------------|
| V _{DD} = V _{DDO} = 3.3 V ±5% | 1.65 V ±5% | 1.65 V ±5% | -1.65 V ±5% |
| V _{DD} = 3.3 V ±5%; V _{DDO} = 2.5 V ±5% | 2.05 V ±5% | 1.25 V ±5% | -1.25 V ±5% |

Figure 4. Output Driver Typical Device Evaluation and Termination Setup

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|---------------|---------------------|-----------------------|
| NB3M8302CDG | SOIC-8 (Pb-Free) | 98 Units / Rail |
| NB3M8302CDR2G | SOIC-8 (Pb-Free) | 2500 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

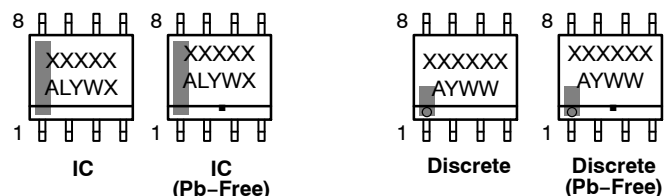


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

GENERIC
MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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ISSUE AK

DATE 16 FEB 2011

| | | | |
|---|--|--|--|
| STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER | STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1 | STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1 | STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE |
| STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE | STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE | STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd | STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2 4. COLLECTOR, #2 5. COLLECTOR, #2 6. EMITTER, #2 7. EMITTER, #1 8. COLLECTOR, #1 |
| STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON | STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND | STYLE 11: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1 | STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN |
| STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN | STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN | STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON | STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1 |
| STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC | STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE | STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1 | STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN |
| STYLE 21: PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6 | STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND | STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT | STYLE 24: PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE |
| STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT | STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC | STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN | STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN |
| STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1 | STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1 | | |

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