

TinyLogic UHS Dual Inverting Buffer with 3-STATE Outputs

NC7WZ240

Description

The NC7WZ240 is a Dual Inverting Buffer with independent active LOW enables for the 3-STATE outputs. The Ultra High Speed device is fabricated with advanced CMOS technology to achieve superior switching performance with high output drive while maintaining low static power dissipation over a broad V_{CC} operating range. The device is specified to operate over the 1.65 V to 5.5 V V_{CC} operating range. The inputs and outputs are high impedance when V_{CC} is 0 V. Inputs tolerate voltages up to 5.5 V independent of V_{CC} operating range. Outputs tolerate voltages above V_{CC} when in the 3-STATE condition.

Features

- Space Saving US8 Surface Mount Package
- MicroPak™ Pb-Free Leadless Package
- Ultra High Speed: $t_{PD} = 2.3$ ns Typ. into 50 pF at 5 V V_{CC}
- High Output Drive: ± 24 mA at 3 V V_{CC}
- Broad V_{CC} Operating Range: 1.65 V to 5.5 V
- Matches the Performance of LCX when Operated at 3.3 V V_{CC}
- Power Down High Impedance Inputs / Outputs
- Overvoltage Tolerant Inputs Facilitate 5 V to 3 V Translation
- Outputs are Overvoltage Tolerant in 3-STATE Mode
- Proprietary Noise / EMI Reduction Circuitry Implemented
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

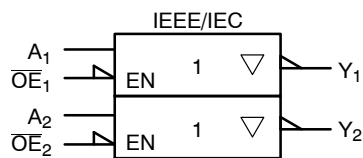
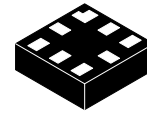
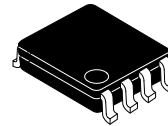


Figure 1. Logic Symbol

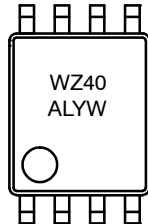
MARKING DIAGRAMS



UQFN8
1.6X1.6, 0.5P
CASE 523AY



US8
CASE 846AN



U7, WZ40 = Specific Device Code
 KK = 2-Digit Lot Run Traceability Code
 XY = 2-Digit Date Code Format
 Z = Assembly Plant Code
 A = Assembly Location
 L = Wafer Lot Number
 YW = Assembly Start Week

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 6.

Connection Diagrams

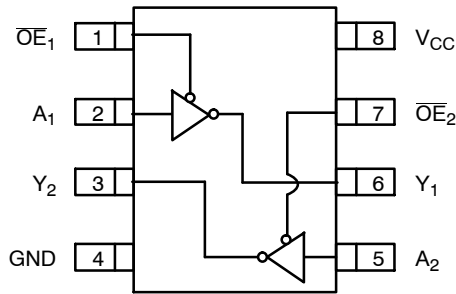


Figure 2. Pin Assignments for US8 (Top View)

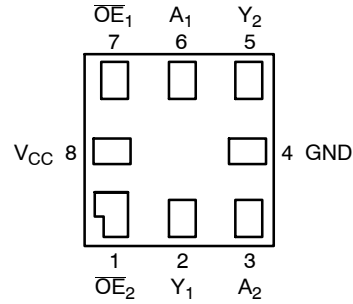
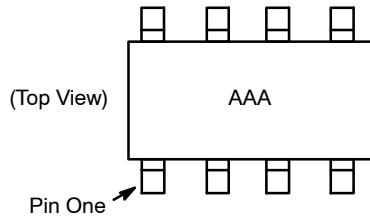


Figure 4. Pad Assignments for MicroPak (Top Thru View)



AAA represents Product Code Top Mark – see ordering code

NOTE: Orientation of Top Mark determines Pin One location. Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

Figure 3. Pin One Orientation Diagram

PIN DESCRIPTIONS

Pin Names	Description
$\overline{OE}_n$	Enable Inputs for 3-STATE Outputs
A_n	Inputs
Y_n	3-STATE Outputs

FUNCTION TABLE

Inputs		Output
$\overline{OE}$	A_n	Y_n
L	L	H
L	H	L
H	L	Z
H	H	Z

H = HIGH Logic Level

L = LOW Logic Level

Z = 3-STATE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V _{CC}	Supply Voltage		-0.5	6.5	V
V _{IN}	DC Input Voltage (Note 1)		-0.5	6.5	V
V _{OUT}	DC Output Voltage		-0.5	6.5	V
I _{IK}	DC Input Diode Current	V _{IN} < 0 V	-	-50	mA
I _{OK}	DC Output Diode Current	V _{OUT} < 0 V	-	-50	mA
I _{OUT}	DC Output Source / Sink Current		-	±50	mA
I _{CC} / I _{GND}	DC V _{CC} / Ground Current		-	±50	mA
T _{STG}	Storage Temperature Range		-65	+150	°C
T _J	Junction Lead Temperature under Bias		-	+150	°C
T _L	Junction Lead Temperature (Soldering, 10 Seconds)		-	+260	°C
P _D	Power Dissipation in Still Air	US8	-	500	mW
		MicroPak-8	-	539	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V _{CC}	Supply Voltage Operating		1.65	5.5	V
	Supply Voltage Data Retention		1.5	5.5	
V _{IN}	Input Voltage		0	5.5	V
V _{OUT}	Output Voltage	Active State	0	V _{CC}	V
		3-STATE	0	5.5	V
T _A	Operating Temperature		-40	+85	°C
t _r , t _f	Input Rise and Fall Time	V _{CC} @ 1.8 V ±0.15 V, 2.5 V ±0.2 V	0	20	ns/V
		V _{CC} @ 3.3 V ±0.3 V	0	10	
		V _{CC} @ 5.0 V ±0.5 V	0	5	
θ _{JA}	Thermal Resistance	US8	-	250	°C/W
		MicroPak-8	-	232	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. Unused inputs must be held HIGH or LOW. They may not float.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = +25°C			T _A = -40 to +85°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	HIGH Level Input Voltage		1.65 to 1.95	0.65 V _{CC}	–	–	0.65 V _{CC}	–	V
			2.3 to 5.5	0.7 V _{CC}	–	–	0.7 V _{CC}	–	
V _{IL}	LOW Level Input Voltage		1.65 to 1.95	–	–	0.35 V _{CC}	–	0.35 V _{CC}	V
			2.3 to 5.5	–	–	0.3 V _{CC}	–	0.3 V _{CC}	
V _{OH}	HIGH Level Output Voltage	V _{IN} = V _{IH} or V _{IL}	I _{OH} = –100 μA	1.65	1.55	1.65	–	1.55	V
				2.3	2.2	2.3	–	2.2	
				3.0	2.9	3.0	–	2.9	
				4.5	4.4	4.5	–	4.4	
			I _{OH} = –4 mA	1.65	1.29	1.52	–	1.29	
			I _{OH} = –8 mA	2.3	1.9	2.15	–	1.9	
			I _{OH} = –16 mA	3.0	2.4	2.80	–	2.4	
			I _{OH} = –24 mA	3.0	2.3	2.68	–	2.3	
			I _{OH} = –32 mA	4.5	3.8	4.20	–	3.8	
V _{OL}	LOW Level Output Voltage	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100 μA	1.65	–	0.0	0.10	–	V
				2.3	–	0.0	0.10	–	
				3.0	–	0.0	0.10	–	
				4.5	–	0.0	0.10	–	
			I _{OL} = 4 mA	1.65	–	0.08	0.24	–	
			I _{OL} = 8 mA	2.3	–	0.10	0.3	–	
			I _{OL} = 16 mA	3.0	–	0.15	0.4	–	
			I _{OL} = 24 mA	3.0	–	0.22	0.55	–	
			I _{OL} = 32 mA	4.5	–	0.22	0.55	–	
I _{IN}	Input Leakage Current	V _{IN} = 5.5 V, GND	1.65 to 5.5	–	–	±0.1	–	±1	μA
I _{OZ}	3-STATE Output Leakage	V _{IN} = V _{IH} or V _{IL} 0 ≤ V _{OUT} ≤ 5.5 V	1.65 to 5.5	–	–	±0.5	–	±5	μA
I _{OFF}	Power Off Leakage Current	V _{IN} or V _{OUT} = 5.5 V	0.0	–	–	1	–	10	μA
I _{CC}	Quiescent Supply Current	V _{IN} = 5.5 V, GND	1.65 to 5.5	–	–	1	–	10	μA

NOISE CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = +25°C		Unit
				Typ	Max	
V _{OLP} (Note 3)	Quiet Output Maximum Dynamic V _{OL}	C _L = 50 pF	5.0	–	1.0	V
V _{OLV} (Note 3)	Quiet Output Minimum Dynamic V _{OL}	C _L = 50 pF	5.0	–	1.0	V
V _{OHV} (Note 3)	Quiet Output Minimum Dynamic V _{OH}	C _L = 50 pF	5.0	–	4.0	V
V _{IHD} (Note 3)	Minimum HIGH Level Dynamic Input Voltage	C _L = 50 pF	5.0	–	3.5	V
V _{ILD} (Note 3)	Maximum LOW Level Dynamic Input Voltage	C _L = 50 pF	5.0	–	1.5	V

3. Parameter guaranteed by design.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = +25°C			T _A = -40 to +85°C		Unit
				Min	Typ	Max	Min	Max	
t _{PLH} , t _{PHL}	Propagation Delay A _n to Y _n (Figure 5, 7)	C _L = 15 pF R _D = 1 MΩ S1 = Open	1.8 ±0.15	–	–	12.0	–	13.0	ns
			2.5 ±0.2	–	–	7.5	–	8.0	
			3.3 ±0.3	–	–	5.2	–	5.5	
			5.0 ±0.5	–	–	4.5	–	4.8	
		C _L = 50 pF, R _D = 500 Ω S1 = Open	3.3 ±0.3	–	–	5.7	–	6.0	
			5.0 ±0.5	–	–	5.0	–	5.3	
t _{OSLH} , t _{OSHL}	Output to Output Skew (Note 4) (Figure 5, 7)	C _L = 50 pF, R _D = 500 Ω S1 = Open	3.3 ±0.3	–	–	1.0	–	1.0	ns
			5.0 ±0.5	–	–	0.8	–	0.8	
t _{PZL} , t _{PZH}	Output Enable Time (Figure 5, 7)	C _L = 50 pF R _D , R _U = 500 Ω S1 = GND for t _{PZH} S1 = V _I for t _{PZL} V _I = 2 x V _{CC}	1.8 ±0.15	–	–	14.0	–	15.0	ns
			2.5 ±0.2	–	–	8.5	–	9.0	
			3.3 ±0.3	–	–	6.2	–	6.5	
			5.5 ±0.5	–	–	5.5	–	5.8	
t _{PLZ} , t _{PHZ}	Output Disable Time (Figure 5, 7)	C _L = 50 pF R _D , R _U = 500 Ω S1 = GND for t _{PZH} S1 = V _I for t _{PZL} V _I = 2 x V _{CC}	1.8 ±0.15	–	–	12.0	–	13.0	ns
			2.5 ±0.2	–	–	8.0	–	8.5	
			3.3 ±0.3	–	–	5.7	–	6.0	
			5.0 ±0.5	–	–	4.7	–	5.0	
C _{IN}	Input Capacitance		0	–	2.5	–	–	–	pF
C _{OUT}	Output Capacitance		5.0	–	4	–	–	–	pF
C _{PD}	Power Dissipation Capacitance (Figure 6)	(Note 5)	3.3	–	10	–	–	–	pF
			5.0	–	12	–	–	–	

4. Parameter guaranteed by design. t_{OSLH} = |t_{PLHmax} – t_{PLHmin}|; t_{OSHL} = |t_{PHLmax} – t_{PHLmin}|.

5. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (see Figure 6) C_{PD} is related to I_{CCD} dynamic operating current by the expression:
I_{CCD} = (C_{PD}) (V_{CC}) (f_{IN}) + (I_{CCstatic}).

AC Loading and Waveforms

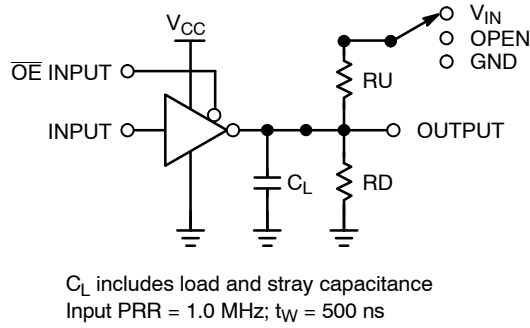


Figure 5. AC Test Circuit

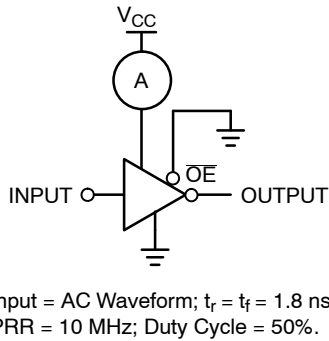


Figure 6. I_{CCD} Test Circuit

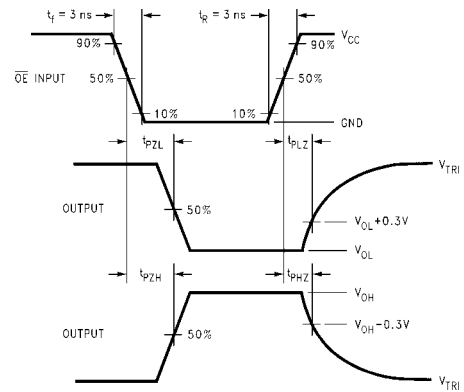
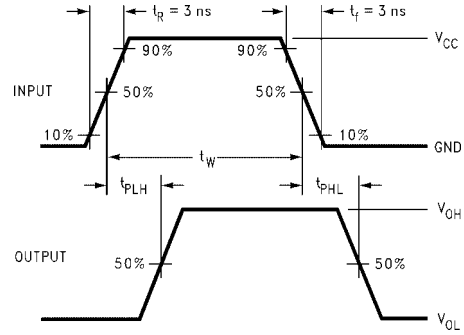


Figure 7. AC Waveforms

ORDERING INFORMATION

Order Number	Top Mark	Package	Shipping [†]
NC7WZ240K8X	WZ40	8-Lead US8, JEDEC MO-187, Variation CA 3.1 mm Wide	3000 / Tape & Reel
NC7WZ240L8X	U7	8-Lead MicroPak, 1.6 mm Wide (Pb-Free)	5000 / Tape & Reel

DISCONTINUED (Note 7)

NC7WZ240K8X-L22236	WZ40	8-Lead US8, JEDEC MO-187, Variation CA 3.1 mm Wide	3000 / Tape & Reel
NC7WZ240L8X-L22185	U7	8-Lead MicroPak, 1.6 mm Wide (Pb-Free)	5000 / Tape & Reel

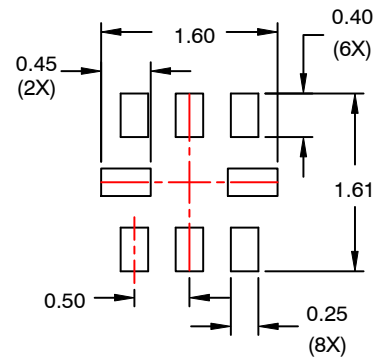
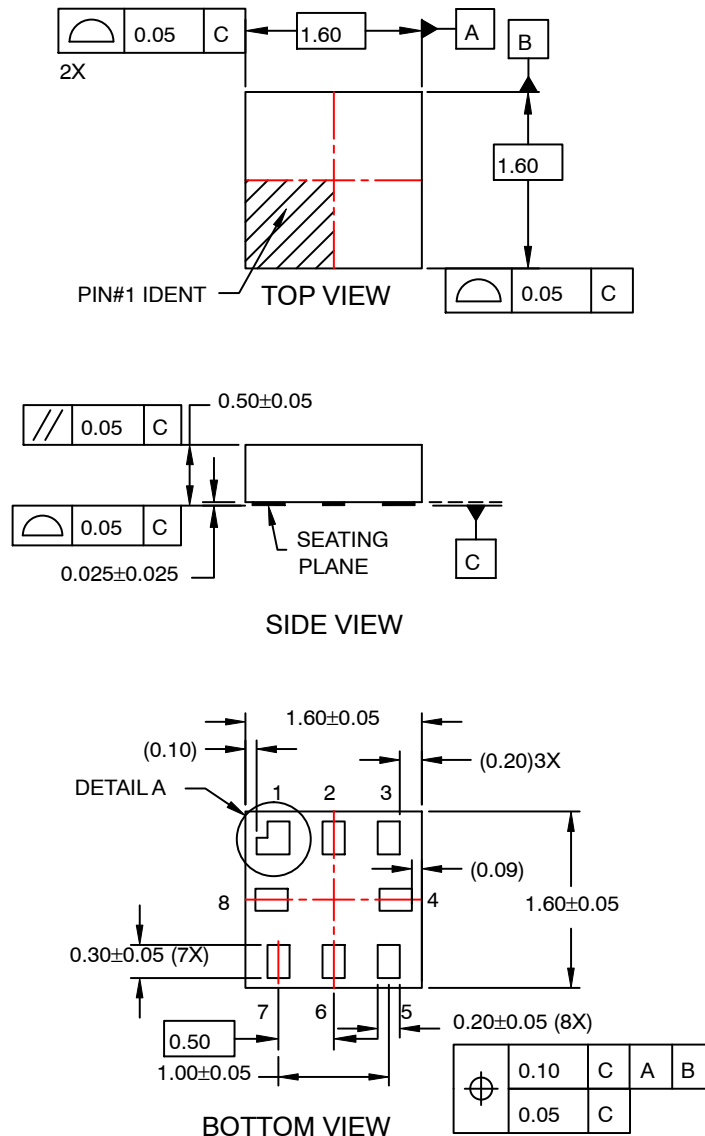
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

6. Pb-Free package per JEDEC J-STD-020B.

7. **DISCONTINUED:** These devices are not recommended for new design. Please contact your onsemi representative for information. The most current information on these devices may be available on www.onsemi.com.

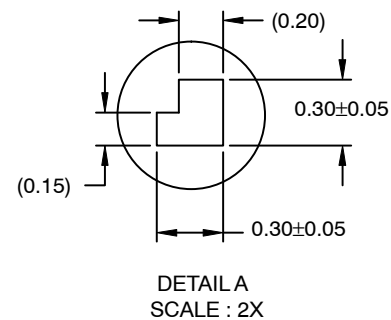
UQFN8 1.6X1.6, 0.5P
CASE 523AY
ISSUE O

DATE 31 AUG 2016



NOTES:

- A. PACKAGE CONFORMS TO JEDEC MO-255 VARIATION UAAD.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

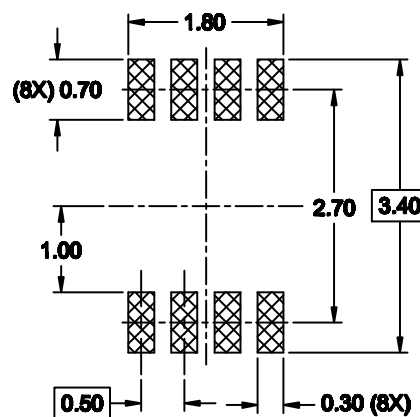
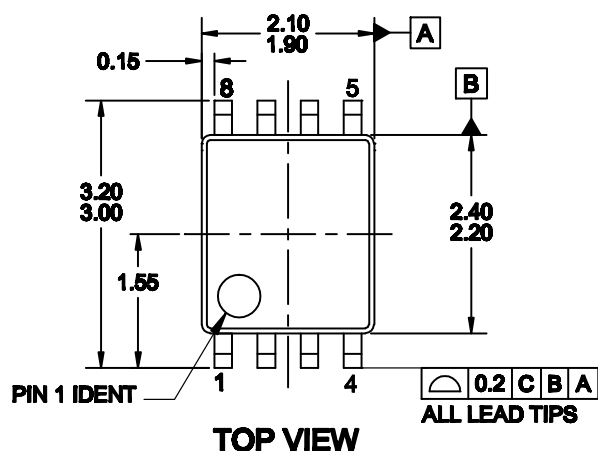


DOCUMENT NUMBER:	98AON13591G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	UQFN8 1.6X1.6, 0.5P	PAGE 1 OF 1

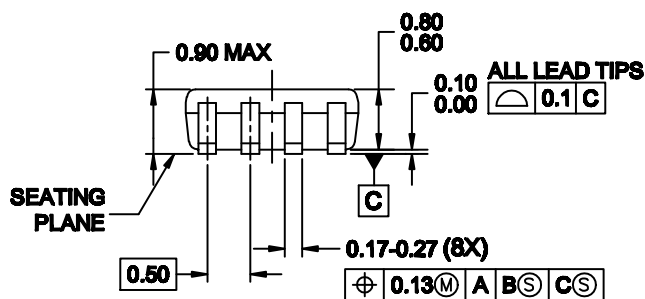
onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

US8
CASE 846AN
ISSUE O

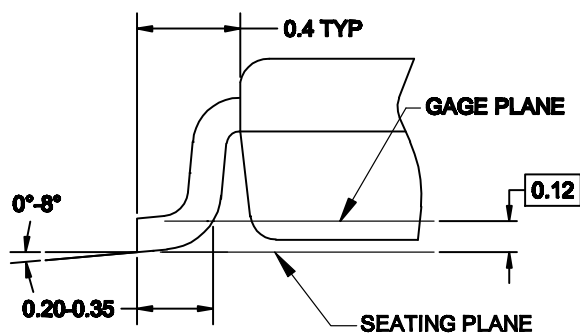
DATE 31 DEC 2016



RECOMMENDED LAND PATTERN



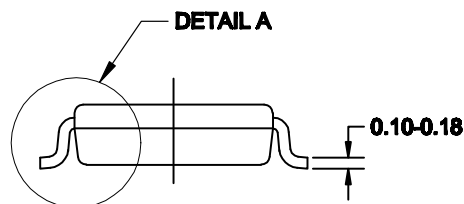
SIDE VIEW



DETAIL A

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-187**
- B. DIMENSIONS ARE IN MILLIMETERS.**
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS,
MOLD FLASH, AND TIE BAR EXTRUSIONS.**
- D. DIMENSIONS AND TOLERANCES PER
ANSI Y14.5M, 1994.**



DOCUMENT NUMBER:	98AON13778G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	US8	PAGE 1 OF 1

onsemi and **onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales