

TinyLogic UHS Dual 2-Input NAND Gate (Open Drain Output)

NC7WZ38

Description

The NC7WZ38 is a dual 2-Input NAND Gate with open drain output stage from ON Semiconductor's Ultra High Speed Series of TinyLogic. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad V_{CC} operating range. The device is specified to operate over the 1.65 V to 5.5 V V_{CC} range. The inputs and output are high impedance when V_{CC} is 0 V. Inputs tolerate voltages up to 5.5 V independent of V_{CC} operating voltage. The open drain output stage will tolerate voltages up to 5.5 V independent of V_{CC} when in the high impedance state.

Features

- Space Saving US8 Surface Mount Package
- MicroPakTM Pb-Free Leadless Package
- Open Drain Output Stage for OR Tied Applications
- Ultra High Speed: t_{PD} 2.2 ns Typ. into 50 pF at 5 V V_{CC}
- High Output Sink Drive: ±24 mA at 3 V V_{CC}
- Broad V_{CC} Operating Range: 1.65 V to 5.5 V
- Matches the Performance of LCX when Operated at 3.3 V V_{CC}
- Power Down High Impedance Inputs / Output
- Overvoltage Tolerant Inputs Facilitate 5 V to 3 V Translation
- Patented Noise / EMI Reduction Circuitry Implemented
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

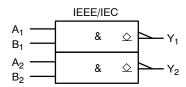


Figure 1. Logic Symbol

MARKING DIAGRAMS



UQFN8 1.6X1.6, 0.5P CASE 523AY





HSS CASE 846AN



U5, WZ38 = Specific Device Code

ΚK = 2-Digit Lot Run Traceability Code XY = 2-Digit Date Code Format Ζ = Assembly Plant Code Α = Assembly Site L = Wafer Lot Number YW = Assembly Start Week

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet. NOTE: Some of the devices on this data sheet have been DISCONTINUED. Please refer to the table on page 5.

1

Connection Diagram

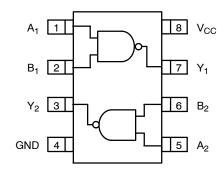
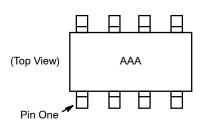


Figure 2. Connection Diagram (Top View)



AAA represents Product Code Top Mark - see ordering code

NOTE: Orientation of Top Mark determines Pin One location. Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

Figure 3. Pin One Orientation Diagram

PIN DESCRIPTIONS

Pin Names	Description
A _n , B _n	Inputs
Y _n	Output

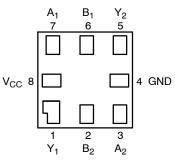


Figure 4. Pad Assignments for MicroPak (Top Thru View)

FUNCTION TABLE $(Y = \overline{AB})$

Inp	Output	
Α	Y	
L	L	*H
L	Н	*H
Н	L	*H
Н	Н	L

H = HIGH Logic Level

L = LOW Logic Level

*H = HIGH Impedance Output State (Open Drain)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parame	Min	Max	Unit	
V _{CC}	Supply Voltage		-0.5	6.5	V
V _{IN}	DC Input Voltage		-0.5	6.5	V
V _{OUT}	DC Output Voltage		-0.5	6.5	V
I _{IK}	DC Input Diode Current	OC Input Diode Current V _{IN} < 0 V		-50	mA
I _{OK}	DC Output Diode Current	V _{OUT} < 0 V	-	-50	mA
I _{OUT}	DC Output Current	-	±50	mA	
I _{CC} / I _{GND}	DC V _{CC} / GND Current	-	±100	mA	
T _{STG}	Storage Temperature	-65	+150	°C	
TJ	Junction Temperature under Bias	-	150	°C	
TL	Junction Lead Temperature (Solde	-	260	°C	
P _D	Power Dissipation in Still Air	US8 MicroPak-8	- -	500 539	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol		Parameter	Min	Max	Unit
V _{CC}	Supply Voltage Operating		1.65	5.5	V
	Supply Voltage Data Rete	ntion	1.5	5.5	
V _{IN}	Input Voltage		0	5.5	V
V _{OUT}	Output Voltage		0	V _{CC}	V
T _A	Operating Temperature		-40	+85	°C
t _r , t _f	Input Rise and Fall Time V _{CC} = 1.8 V ±0.15 V, 2.5 V ±0.2 V		0	20	ns/V
	V _{CC} = 3.3 V ±0.3 V		0	10	
	V _{CC} = 5.0 V ±0.5 V		0	5	
$\theta_{\sf JA}$	Thermal Resistance	US8 MicroPak-8	- -	250 232	°C/W

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. Unused inputs must be held HIGH or LOW. They may not float.

DC ELECTICAL CHARACTERISTICS

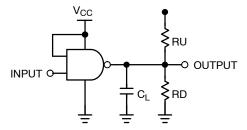
					Т,	Δ = +25°	°C	T _A = -40	to +85°C	
Symbol	Parameter	V _{CC} (V)	Co	Conditions		Тур	Max	Min	Max	Unit
V _{IH}	HIGH Level Input	1.65 to 1.95			0.65 V _{CC}	-	-	0.65 V _{CC}	_	V
	Voltage	2.3 to 5.5			0.7 V _{CC}	-	-	0.7 V _{CC}	_	
V _{IL}	LOW Level Input	1.65 to 1.95			-	-	0.35 V _{CC}	_	0.35 V _{CC}	V
	Voltage	2.3 to 5.5			-	_	0.3 V _{CC}	_	0.3 V _{CC}	
I _{LKG}	HIGH Level Output Leakage	5.5	$V_{IN} = V_{IL}$ $V_{OUT} = V_{CC}$ or GND		-	_	±5	-	±10	μΑ
V _{OL}	LOW Level Output	1.65	$V_{IN} = V_{IH}$	I _{OL} = 100 μA	=	0.0	0.1	_	0.1	V
	Voltage	2.3			-	0.0	0.1	_	0.1	
		3.0			-	0.0	0.1	_	0.1	
		4.5			-	0.0	0.1	_	0.1	
		1.65		I _{OL} = 4 mA	-	0.08	0.24	_	0.24	
		2.3		I _{OL} = 8 mA	-	0.10	0.3	_	0.3	
		3.0		I _{OL} = 16 mA	-	0.15	0.4	_	0.4	
		3.0		I _{OL} = 24 mA	-	0.22	0.55	_	0.55	
		4.5		I _{OL} = 32 mA	-	0.22	0.55	_	0.55	
I _{IN}	Input Leakage Current	5.5	V _{IN} = 5.5 V, GND		-	_	±0.1	_	±1	μΑ
l _{OFF}	Power Off Leakage Current	0.0	V _{IN} or V _{OUT} = 5.5 V		-	-	1	-	10	μΑ
Icc	Quiescent Supply Current	1.65 to 5.5	V _{IN} = 5.5 V	/, GND	-	_	1	-	10	μΑ

AC ELECTRICAL CHARACTERISTICS

				$T_A = +25^{\circ}C$			T _A = −40 to +85°C			
Symbol	Parameter	V _{CC} (V)	Conditions	Min	Тур	Max	Min	Max	Unit	
t_{PZL}	Propagation Delay	1.8 ±0.15	C _L = 50 pF,	-	5.2	9.2	-	9.6	ns	
	(Figure 5, 7)	2.5 ±0.2	RU = 500 Ω , RD = 500 Ω ,	_	3.5	5.7	-	6.1	1	
		3.3 ±0.3	$V_I = 2 \times V_{CC}$	-	2.8	4.1	-	4.5		
		5.0 ±0.5		-	2.2	3.4	-	3.6		
t_{PLZ}	Propagation Delay (Figure 5, 7)	1.8 ±0.15	$C_L = 50 \text{ pF},$ $RU = 500 \Omega,$ $RD = 500 \Omega,$ $V_I = 2 \text{ x } V_{CC}$	-	4.6	9.2	-	9.6	ns	
		2.5 ±0.2		$.5 \pm 0.2$ RD = 500 Ω,	-	3.2	5.7	-	6.1	
		3.3 ±0.3			-	2.4	4.1	-	4.5	
		5.0 ±0.5		-	1.6	3.4	-	3.6		
C _{IN}	Input Capacitance	0		-	2.5	-	-	-	pF	
C _{OUT}	Output Capacitance	0		-	4.2	-	-	-	pF	
C_{PD}	Power Dissipation Capacitance	3.3	(Note 2)	-	7	-	_	-	pF	
	(Figure 6)	5.0		-	9	_	_	_	1	

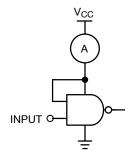
^{2.} C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (see Figure 6) C_{PD} is related to I_{CCD} dynamic operating current by the expression: I_{CCD} = (C_{PD}) (V_{CC}) (f_{IN}) + (I_{CC}static).

AC Loading and Waveforms



 C_L includes load and stray capacitance Input PRR = 1.0 MHz, t_W = 500 ns $\,$

Figure 5. AC Test Circuit



Input = AC Waveform; $t_r = t_f = 1.8$ ns; PRR = 10 MHz; Duty Cycle = 50%.

Figure 6. I_{CCD} Test Circuit

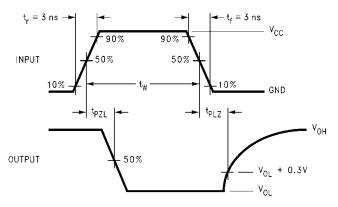


Figure 7. AC Waveforms

ORDERING INFORMATION

Order Number	Top Mark	Package	Shipping [†]
NC7WZ38K8X	WZ38	8-Lead US8, JEDEC MO-187, Variation CA 3.1 mm Wide	3000 / Tape & Reel
NC7WZ38L8X	U5	8-Lead MicroPak, 1.6 mm Wide (Pb-Free)	5000 / Tape & Reel

DISCONTINUED (Note 4)

NC7WZ38K8X-L22236	WZ38	8-Lead US8, JEDEC MO-187, Variation CA 3.1 mm Wide	3000 / Tape & Reel
NC7WZ38L8X-L22185	U5	8-Lead MicroPak, 1.6 mm Wide (Pb-Free)	5000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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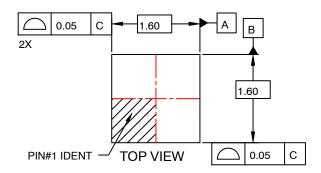
^{3.} Pb-Free package per JEDEC J-STD-020B.

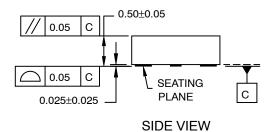
^{4.} **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

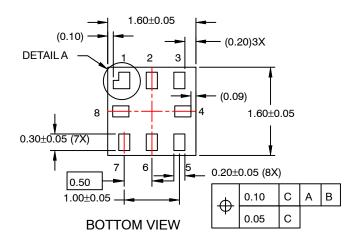


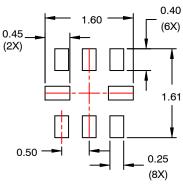
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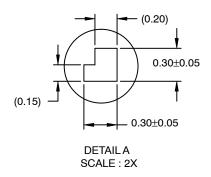




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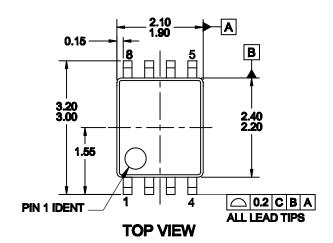
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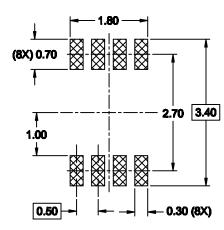
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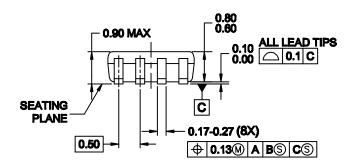
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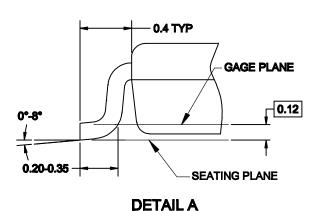
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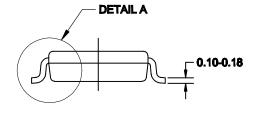


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SIDE VIEW





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