NID5004N

Self-Protected FET with Temperature and Current Limit

40 V, 6.5 A, Single N−Channel, DPAK

Self−protected FETs are a series of power MOSFETs which utilize ON Semiconductor HDPlus™ technology. The self−protected MOSFET incorporates protection features such as integrated thermal and current limits. The self−protected MOSFETs include an integrated Drain−to−Gate Clamp that provides overvoltage protection from transients and avalanche. The device is protected from Electrostatic Discharge (ESD) by utilizing an integrated Gate−to−Source Clamp.

Features

- Short Circuit Protection
- In Rush Current Limit
- Thermal Shutdown with Automatic Restart
- Avalanche Rated
- Overvoltage Protection
- ESD Protection (4 kV HBM)
- Controlled Slew Rate for Low Noise Switching
- AEC Q101 Qualified
- This is a Pb−Free Device

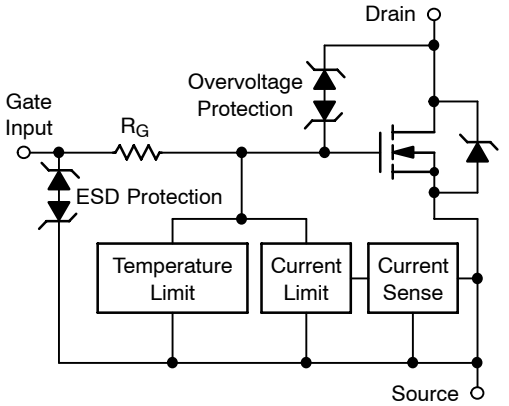
Applications

- Solenoid Driver
- Relay Driver
- Small Motors
- Lighting
- Relay Replacement
- Load Switching

ON Semiconductor®

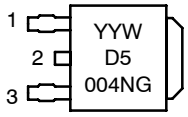
http://onsemi.com

V_{DSS} (Clamped)	$R_{DS(on)}$ Typ	I_D Typ (Limited)
40 V	110 mΩ @ 10 V	6.5 A



DPAK
CASE 369C
STYLE 2

MARKING DIAGRAM



D5004N = Device Code
Y = Year
WW = Work Week
G = Pb−Free Device

1 = Gate
2 = Drain
3 = Source

ORDERING INFORMATION

Device	Package	Shipping†
NID5004NT4G	DPAK (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MOSFET MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage Internally Clamped	V_{DSS}	44	Vdc
Gate−to−Source Voltage	V_{GS}	±14	Vdc
Drain Current Continuous	I_D	Internally Limited	
Total Power Dissipation @ T_A = 25°C (Note 1) @ T_A = 25°C (Note 2)	P_D	 1.3 2.5	W
Thermal Resistance Junction−to−Case Junction−to−Ambient (Note 1) Junction−to−Ambient (Note 2)	 $R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	 3.0 95 50	°C/W
Single Pulse Drain−to−Source Avalanche Energy (V_{DD} = 30 Vdc, V_{GS} = 5.0 Vdc, I_L = 1.8 Apk, L = 160 mH, R_G = 25 Ω) (Note 3)	E_{AS}	273	mJ
Operating and Storage Temperature Range (Note 4)	T_J, T_{stg}	−55 to 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface mounted onto minimum pad size (100 sq/mm) FR4 PCB, 1 oz cu.
2. Mounted onto 1″ square pad size (700 sq/mm) FR4 PCB, 1 oz cu.
3. Not subject to Production Test
4. Normal pre−fault operating range. See thermal limit range conditions.

MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain−to−Source Clamped Breakdown Voltage (V_{GS} = 0 V, I_D = 2 mA)	$V_{(BR)DSS}$	36	40	44	V
Zero Gate Voltage Drain Current (V_{DS} = 32 V, V_{GS} = 0 V)	I_{DSS}	–	27	100	μA
Gate Input Current (V_{GS} = 5.0 V, V_{DS} = 0 V)	I_{GSS}	–	45	200	μA
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 150 μA) Threshold Temperature Coefficient	$V_{GS(th)}$	1.0 –	1.85 5.0	2.2 –	V −mV/°C
Static Drain−to−Source On−Resistance (Note 5) (V_{GS} = 10 V, I_D = 2.0 A, T_J @ 25°C)	$R_{DS(on)}$	–	110	130	mΩ
Static Drain−to−Source On−Resistance (Note 5) (V_{GS} = 5.0 V, I_D = 2.0 A, T_J @ 25°C) (V_{GS} = 5.0 V, I_D = 2.0 A, T_J @ 150°C)	$R_{DS(on)}$	– –	130 240	150 270	mΩ
Source−Drain Forward On Voltage (I_S = 7.0 A, V_{GS} = 0 V)	V_{SD}	–	0.9	1.1	V
SWITCHING CHARACTERISTICS (Note 6)					
Turn−on Delay Time	R_L = 6.6 Ω, V_{in} = 0 to 10 V, V_{DD} = 13.8 V, I_D = 2.0 A, 10% V_{in} to 10% I_D	$td_{(on)}$	–	97	115	ns
Turn−on Rise Time	R_L = 6.6 Ω, V_{in} = 0 to 10 V, V_{DD} = 13.8 V, I_D = 2.0 A, 10% I_D to 90% I_D	t_{rise}	–	282	300	ns
Turn−off Delay Time	R_L = 6.6 Ω, V_{in} = 0 to 10 V, V_{DD} = 13.8 V, I_D = 2.0 A, 90% V_{in} to 90% I_D	$td_{(off)}$	–	930	1020	ns
Turn−off Fall Time	R_L = 6.6 Ω, V_{in} = 0 to 10 V, V_{DD} = 13.8 V, I_D = 2.0 A, 90% I_D to 10% I_D	t_{fall}	–	690	750	ns
Slew Rate ON	R_L = 6.6 Ω, V_{in} = 0 to 10 V, V_{DD} = 13.8 V, I_D = 2.0 A, 70% to 50% V_{DD}	dV_{DS}/dT_{on}	–	64	–	V/μs
Slew Rate OFF	R_L = 6.6 Ω, V_{in} = 0 to 10 V, V_{DD} = 13.8 V, I_D = 2.0 A, 50% to 70% V_{DD}	dV_{DS}/dT_{off}	–	28	–	V/μs

SELF PROTECTION CHARACTERISTICS (T_J = 25°C unless otherwise noted) (Note 7)

Current Limit	V_{DS} = 10 V, V_{GS} = 5.0 V, T_J = 25°C (Note 8) V_{DS} = 10 V, V_{GS} = 5.0 V, T_J = 100°C (Note 6, 8) V_{DS} = 10 V, V_{GS} = 10 V, T_J = 25°C (Note 6, 8)	I_{LIM}	4.0 4.0 –	6.5 5.5 7.9	11 11 –	A
Temperature Limit (Turn−off)	V_{GS} = 5.0 V (Note 6)	$T_{LIM(off)}$	150	180	200	°C
Thermal Hysteresis	V_{GS} = 5.0 V	$\Delta T_{LIM(on)}$	–	10	–	°C
Temperature Limit (Turn−off)	V_{GS} = 10 V (Note 6)	$T_{LIM(off)}$	150	180	200	°C
Thermal Hysteresis	V_{GS} = 10 V	$\Delta T_{LIM(on)}$	–	20	–	°C
Input Current during Thermal Fault	V_{DS} = 0 V, V_{GS} = 5.0 V, T_J = T_J > $T_{(fault)}$ (Note 6) V_{DS} = 0 V, V_{GS} = 10 V, T_J = T_J > $T_{(fault)}$ (Note 6)	$I_{g(fault)}$	5.5 12	5.2 11	–	mA

ESD ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Electrostatic Discharge Capability Human Body Model (HBM) Machine Model (MM) (Note 6)	ESD	 4000 400	 – –	 – –	V

5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
6. Not subject to Production Test
7. Fault conditions are viewed as beyond the normal operating range of the part.
8. Current limit measured at 380 μs after gate pulse.

TYPICAL PERFORMANCE CURVES

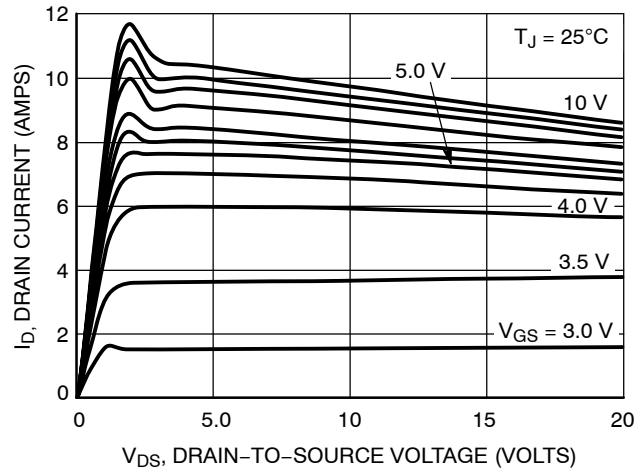


Figure 1. On−Region Characteristics

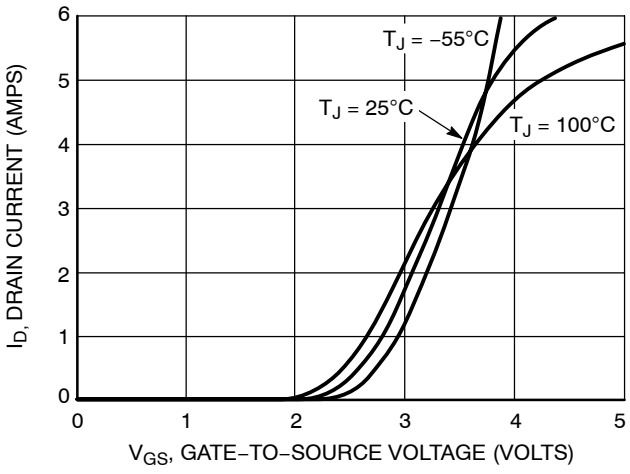


Figure 2. Transfer Characteristics

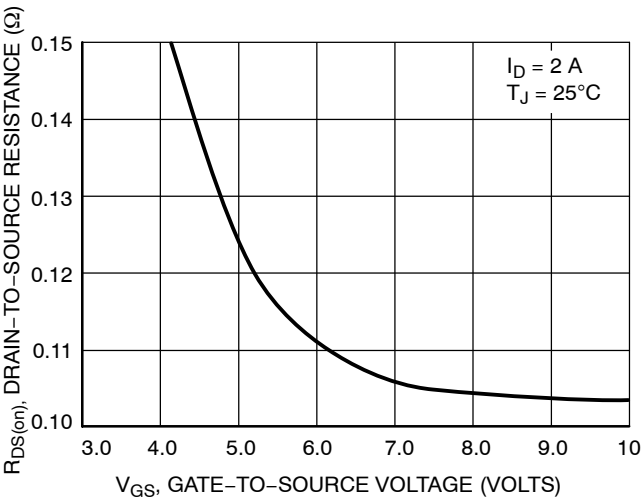


Figure 3. On−Resistance vs. Gate−to−Source Voltage

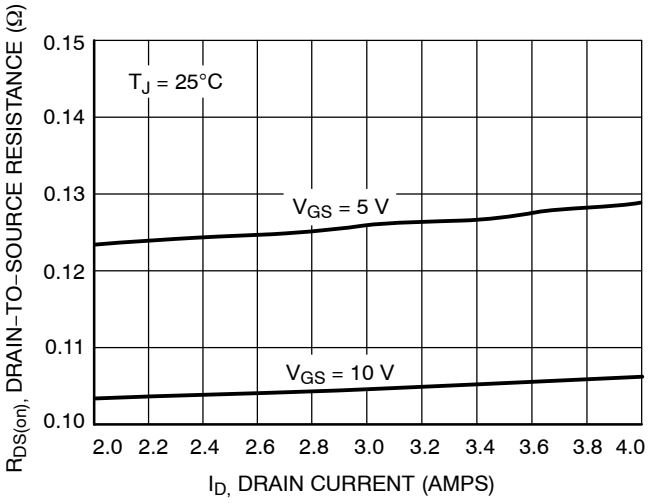


Figure 4. On−Resistance vs. Drain Current

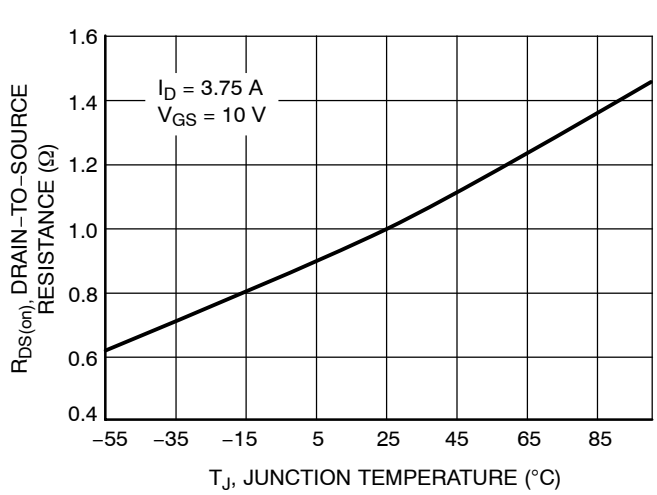


Figure 5. On−Resistance Variation with Temperature

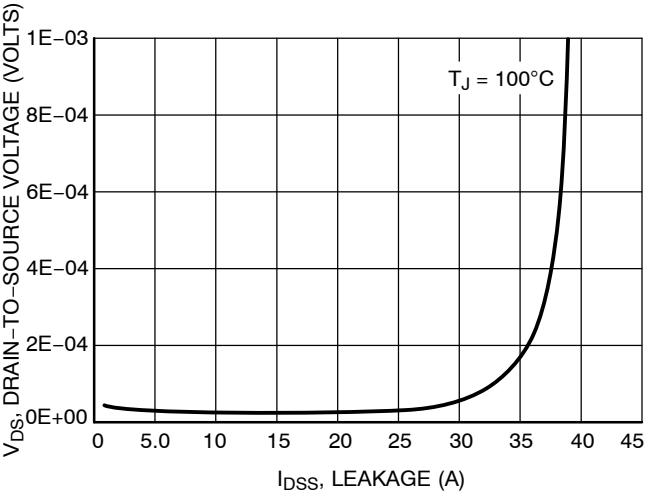


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

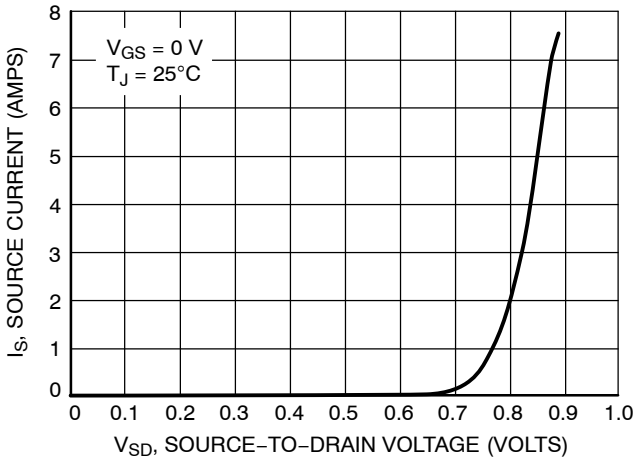


Figure 7. Diode Forward Voltage vs. Current

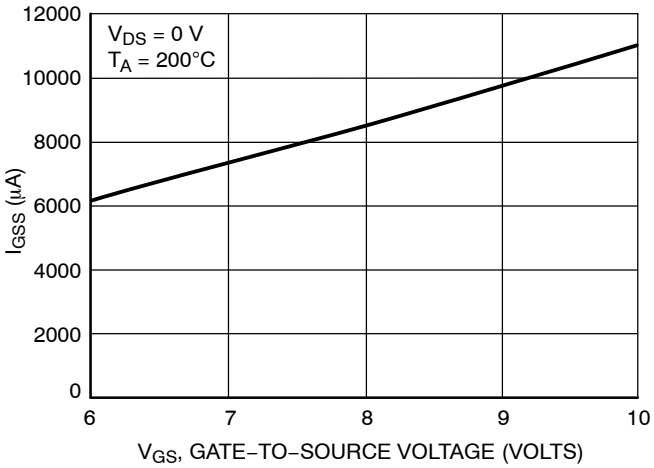


Figure 8. Input Current vs. Gate Voltage

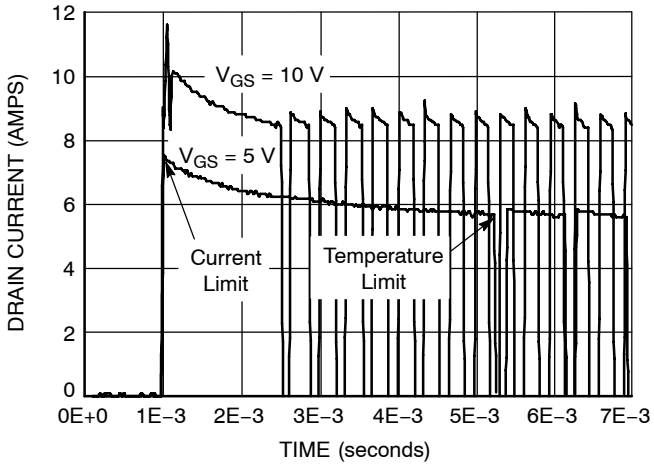


Figure 9. Short Circuit Response*

*(Actual thermal cycling response in short circuit dependent on device power level, thermal mounting, and ambient temperature conditions)

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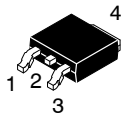
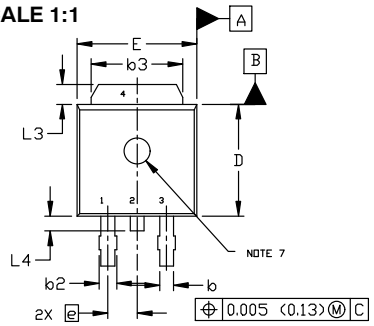


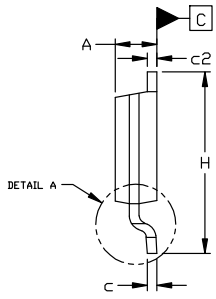
DPAK (SINGLE GAUGE)
CASE 369C
ISSUE G

DATE 31 MAY 2023

SCALE 1:1



TOP VIEW

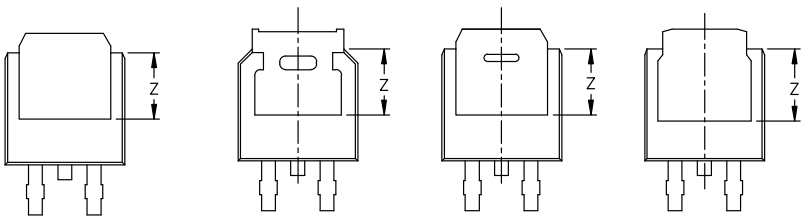


SIDE VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

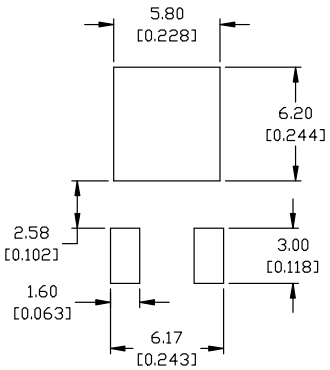
DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	----	0.040	---	1.01
Z	0.155	----	3.93	---



BOTTOM VIEW

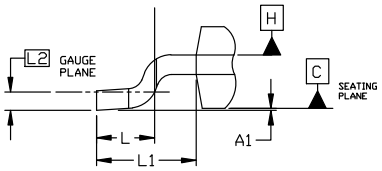
BOTTOM VIEW

ALTERNATE CONSTRUCTIONS



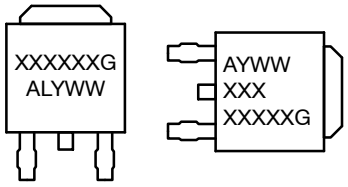
RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



DETAIL A
ROTATED 90° CW

GENERIC MARKING DIAGRAM*



IC **Discrete**

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

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DESCRIPTION:	**DPAK (SINGLE GAUGE)**	**PAGE 1 OF 1**

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