

Inverting 3-State Buffer

NL17SZ240

The NL17SZ240 is a single inverting 3-state buffer in tiny footprint packages.

Features

- Designed for 1.65 V to 5.5 V V_{CC} Operation
- 2.0 ns t_{PD} at $V_{CC} = 5$ V (typ)
- Inputs/Outputs Overvoltage Tolerant up to 5.5 V
- I_{OFF} Supports Partial Power Down Protection
- Source/Sink 24 mA at 3.0 V
- Available in SC-88A Package
- Chip Complexity < 100 FETs
- -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

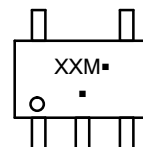


Figure 1. Logic Symbol

MARKING DIAGRAMS



SC-88A (SOT-353)
 DF SUFFIX
 CASE 419A



XX = Specific Device Code
 M = Date Code*
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

NL17SZ240

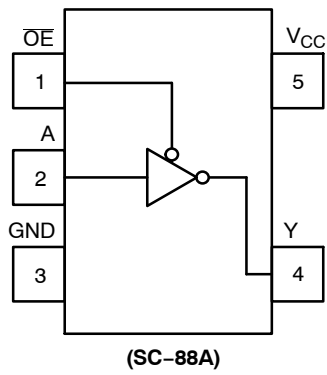


Figure 2. Pinout (Top View)

PIN ASSIGNMENT (SC-88A)

Pin	Function
1	OE
2	A
3	GND
4	Y
5	VCC

FUNCTION TABLE

Input		Output
OE	A	Y
L	L	H
L	H	L
H	X	Z

X = Don't Care

MAXIMUM RATINGS

Symbol	Characteristics	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to +6.5	V
V_{IN}	DC Input Voltage	-0.5 to +6.5	V
	DC Output Voltage Active-Mode (High or Low State) Tri-State Mode (Note 1) Power-Down Mode ($V_{CC} = 0$ V)	-0.5 to $V_{CC} + 0.5$ -0.5 to +6.5 -0.5 to +6.5	V
I_{IK}	DC Input Diode Current $V_{IN} < GND$	-50	mA
I_{OK}	DC Output Diode Current $V_{OUT} < GND$	-50	mA
I_{OUT}	DC Output Source/Sink Current	± 50	mA
I_{CC} or I_{GND}	DC Supply Current per Supply Pin or Ground Pin	± 100	mA
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs	260	°C
T_J	Junction Temperature Under Bias	+150	°C
θ_{JA}	Thermal Resistance (Note 2)	659	°C/W
P_D	Power Dissipation in Still Air	190	mW
MSL	Moisture Sensitivity	Level 1	-
F_R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	-
V_{ESD}	ESD Withstand Voltage (Note 3) Human Body Model Charged Device Model	2000 1000	V
$I_{Latchup}$	Latchup Performance (Note 4)	± 100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 10mm-by-1inch, 2 ounce copper trace no air flow per JESD51-7.
3. HBM tested to ANSI/ESDA/JEDEC JS-001-2017. CDM tested to EIA/JESD22-C101-F. JEDEC recommends that ESD qualification to EIA/JESD22-A115-A (Machine Model) be discontinued per JEDEC/JEP172A.
4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage	1.65	5.5	V
V_{IN}	DC Input Voltage	0	5.5	V
V_{OUT}	DC Output Voltage Active-Mode (High or Low State) Tri-State Mode (Note 1) Power-Down Mode ($V_{CC} = 0$ V)	0	V_{CC}	
		0	5.5	
		0	5.5	
T_A	Operating Temperature Range	-55	+125	°C
t_r, t_f	Input Rise and Fall Time $V_{CC} = 1.65$ V to 1.95 V $V_{CC} = 2.3$ V to 2.7 V $V_{CC} = 3.0$ V to 3.6 V $V_{CC} = 4.5$ V to 5.5 V	0 0 0 0	20 20 10 5	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

NL17SZ240

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-55°C ≤ T _A ≤ 125°C		Units
				Min	Typ	Max	Min	Max	
V _{IH}	High-Level Input Voltage		1.65 to 1.95	0.65 V _{CC}	–	–	0.65 V _{CC}	–	V
			2.3 to 5.5	0.70 V _{CC}	–	–	0.70 V _{CC}	–	
V _{IL}	Low-Level Input Voltage		1.65 to 1.95	–	–	0.35 V _{CC}	–	0.35 V _{CC}	V
			2.3 to 5.5	–	–	0.30 V _{CC}	–	0.30 V _{CC}	
V _{OH}	High-Level Output Voltage	V _{IN} = V _{IH} or V _{IL}	1.65 to 5.5	V _{CC} – 0.1	V _{CC}	–	V _{CC} – 0.1	–	V
		I _{OH} = –100 μA	1.65	1.29	1.4	–	1.29	–	
		I _{OH} = –4 mA	2.3	1.9	2.1	–	1.9	–	
		I _{OH} = –8 mA	2.7	2.2	2.4	–	2.2	–	
		I _{OH} = –12 mA	3.0	2.4	2.7	–	2.4	–	
		I _{OH} = –16 mA	3.0	2.3	2.5	–	2.3	–	
		I _{OH} = –24 mA	4.5	3.8	4.0	–	3.8	–	
		I _{OH} = –32 mA							
V _{OL}	Low-Level Output Voltage	V _{IN} = V _{IH} or V _{IL}	1.65 to 5.5	–		0.1	–	0.1	V
		I _{OL} = 100 μA	1.65	–	0.08	0.24	–	0.24	
		I _{OL} = 4 mA	2.3	–	0.2	0.3	–	0.3	
		I _{OL} = 8 mA	2.7	–	0.22	0.4	–	0.4	
		I _{OL} = 12 mA	3.0	–	0.28	0.4	–	0.4	
		I _{OL} = 16 mA	3.0	–	0.38	0.55	–	0.55	
		I _{OL} = 24 mA	4.5	–	0.42	0.55	–	0.55	
		I _{OL} = 32 mA							
I _{IN}	Input Leakage Current	V _{IN} = 5.5 V or GND	1.65 to 5.5	–	–	±0.1	–	±1.0	μA
I _{OZ}	3-State Output Leakage Current	V _{OUT} = 0 V to 5.5 V	1.65 to 5.5	–	–	±0.5	–	±5.0	μA
I _{OFF}	Power Off Leakage Current	V _{IN} = 5.5 V or V _{OUT} = 5.5 V	0	–	–	1.0	–	10	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5	–	–	1.0	–	10	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

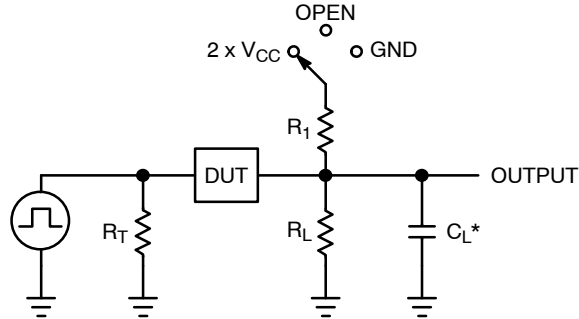
AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-55°C ≤ T _A ≤ 125°C		Units
				Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay, A to Y (Figures 3 and 4)	R _L = 1 MΩ, C _L = 15 pF	1.65 to 1.95	–	6.0	10	–	10.5	ns
		R _L = 1 MΩ, C _L = 15 pF	2.3 to 2.7	–	6.0	7.5	–	8.0	
		R _L = 1 MΩ, C _L = 15 pF	3.0 to 3.6	–	2.5	5.2	–	5.5	
		R _L = 500 Ω, C _L = 50 pF		–	2.9	5.7	–	6.0	
		R _L = 1 MΩ, C _L = 15 pF	4.5 to 5.5	–	2.0	4.5	–	4.8	
		R _L = 500 Ω, C _L = 50 pF		–	2.3	5.0	–	5.3	
t _{PZH} t _{PZL}	Output Enable Time, OE to Y (Figures 3 and 4)		1.65 to 1.95	–	7.6	9.5	–	10	ns
			2.3 to 2.7	–	3.6	8.5	–	9.0	
			3.0 to 3.6	–	2.8	6.2	–	6.5	
			4.5 to 5.5	–	2.0	5.5	–	5.8	
t _{PHZ} t _{PLZ}	Output Disable Time, OE to Y (Figures 3 and 4)		1.65 to 1.95	–	5.0	10	–	10.5	ns
			2.3 to 2.7	–	3.3	8.0	–	8.5	
			3.0 to 3.6	–	2.7	5.7	–	6.0	
			4.5 to 5.5	–	2.6	4.7	–	5.0	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Units
C_{IN}	Input Capacitance	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 0 \text{ V}$ or V_{CC}	2.5	pF
C_{OUT}	Output Capacitance	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 0 \text{ V}$ or V_{CC}	2.5	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	10 MHz, $V_{CC} = 3.3 \text{ V}$, $V_{IN} = 0 \text{ V}$ or V_{CC} 10 MHz, $V_{CC} = 5.5 \text{ V}$, $V_{IN} = 0 \text{ V}$ or V_{CC}	9 11	pF

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$. C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.



C_L includes probe and jig capacitance
 R_T is Z_{OUT} of pulse generator (typically 50 Ω)
 $f = 1 \text{ MHz}$

Figure 3. Test Circuit

Test	Switch Position	C_L , pF	R_L , Ω	R_1 , Ω
t_{PLH} / t_{PHL}	Open	See AC Characteristics Table		
t_{PLZ} / t_{PZL}	$2 \times V_{CC}$	50	500	500
t_{PHZ} / t_{PZH}	GND	50	500	500

X = Don't Care

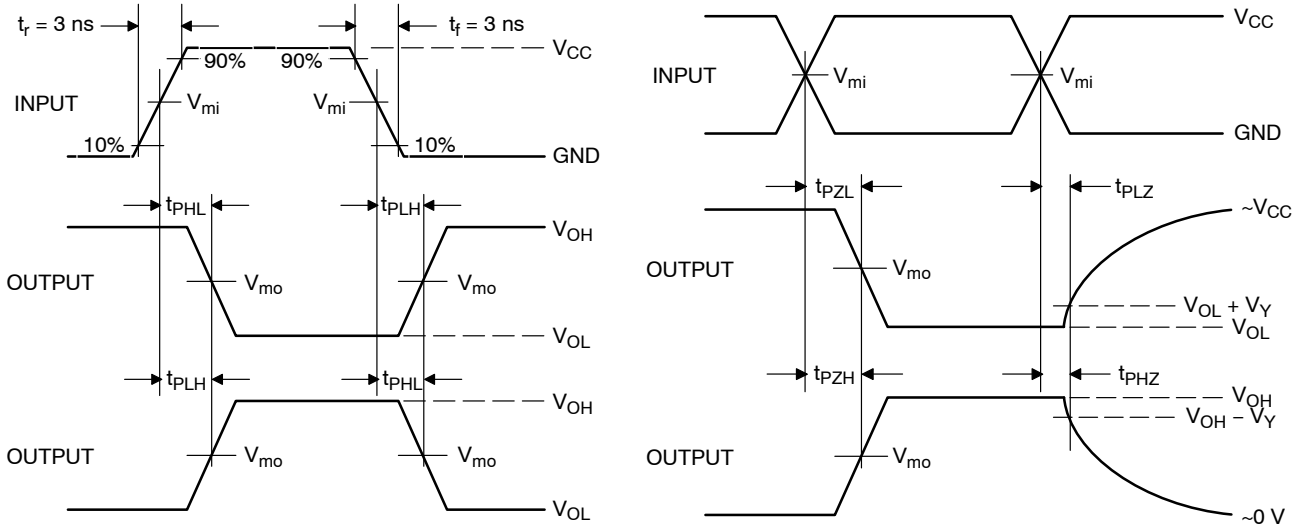


Figure 4. Switching Waveforms

V_{CC} , V	V_{mi} , V	V_{mo} , V		V_Y , V
		t_{PLH}, t_{PHL}	$t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}$	
1.65 to 1.95	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.15
2.3 to 2.7	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.15
3.0 to 3.6	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.3
4.5 to 5.5	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.3

NL17SZ240

DEVICE ORDERING INFORMATION

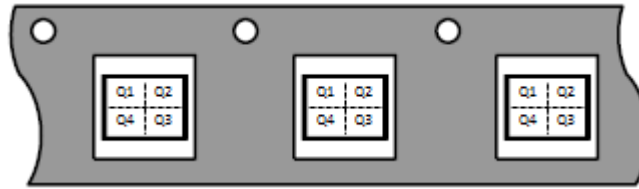
Device	Packages	Marking	Pin 1 Orientation (See below)	Shipping [†]
NL17SZ240DFT2G	SC-88A	U7	Q4	3000 / Tape & Reel
NL17SZ240DFT2G-Q*	SC-88A	U7	Q4	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

PIN 1 ORIENTATION IN TAPE AND REEL

Direction of Feed

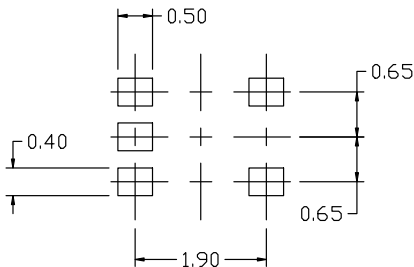
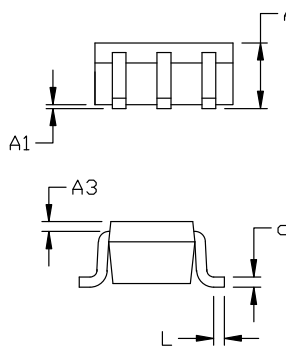
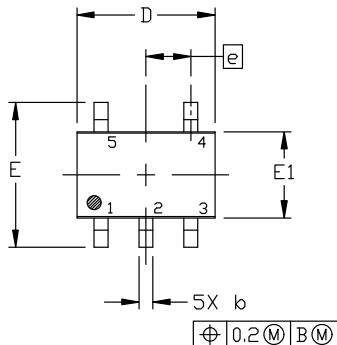




SCALE 2:1

SC-88A (SC-70-5/SOT-353)
CASE 419A-02
ISSUE M

DATE 11 APR 2023

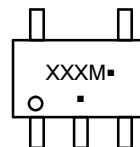

**RECOMMENDED
MOUNTING FOOTPRINT**

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.95	1.10
A1	---	---	0.10
A3	0.20 REF		
b	0.10	0.20	0.30
c	0.10	---	0.25
D	1.80	2.00	2.20
E	2.00	2.10	2.20
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.10	0.15	0.30

**GENERIC MARKING
DIAGRAM***


*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code

M = Date Code

▪ = Pb-Free Package

(Note: Microdot may be in either location)

STYLE 1:

- PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:

- PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:

- PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:

- PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:

- PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:

- PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:

- PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:

- PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:

- PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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