Serial (SPI) Tri-Color LED Driver

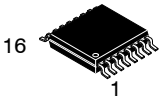
NLSF595

The NLSF595 is advanced CMOS shift register with open drain outputs fabricated with 0.6 μm silicon gate CMOS technology. This device is used in conjunction with a microcontroller, with only one dedicated line. All pins have Overvoltage Protection that allows voltages above V_{CC} up to 5.5 V to be present on the pins without damage or disruption of operation of the part, regardless of the operating voltage. This device may be used between 2.0 and 5.5 volts, the output driver level may be independent of supply voltage: 0–5.5 volts.

Features

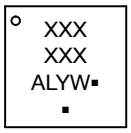
- Parallel Outputs are Open Drain Capable of Sinking > 12 mA
  - Output Withstands up to +5.5 Regardless of V_{CC}
- Standard Serial (SPI) Interface, Data, Clock, Enable (Low)
- All Inputs CMOS Level Compatible
- Frees up I/O around a Microcontroller
- Only One Pin Dedicated to this Device (Latch Enable)
- Output Enable may be Permanently Pulled Low
- High Speed Clocking, Fmax > 25 MHz (Shift Clock)
- Eight Bits Parallel Output
- Double Buffered Outputs, so Register may Fill without Affecting Output
- STD CMOS Serial Output, may be used to Cascade more than One Device
- Each Part Controls Two Tri-Color LEDs
- Two Devices can Control 5 Tri-Color LEDs
- Low Leakage: I_{CC} = 2.0 μA (Max) at T_A = 25 °C
- Latchup Performance Exceeds 100 mA
- QFN−16/TSSOP−16 Packages
- ESD Performance:
  - Human Body Model; > 2000 V
- Functionally Similar to the Popular 74VHC595
- These Devices are Pb-Free and are RoHS Compliant

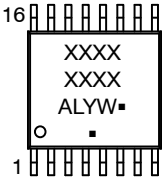
QFN−16
MN SUFFIX
CASE 485G



TSSOP−16
DT SUFFIX
CASE 948F

MARKING DIAGRAMS





A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

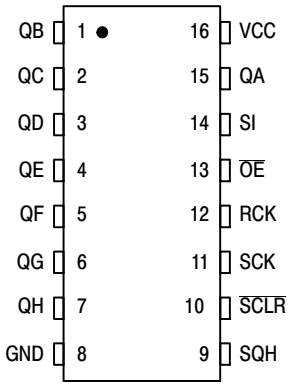


Figure 1. Pin Assignment (TSSOP−16)

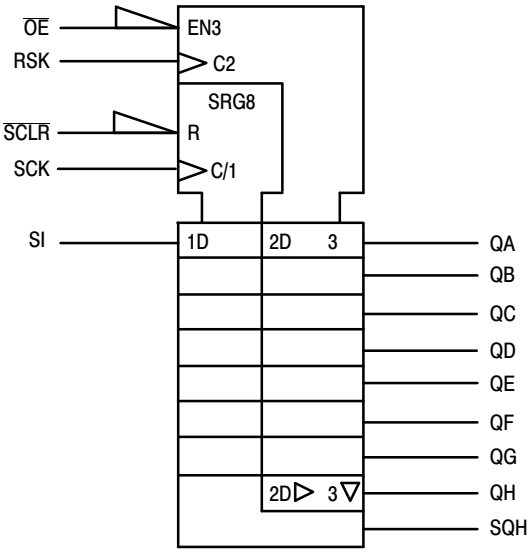


Figure 2. IEC Logic Symbol

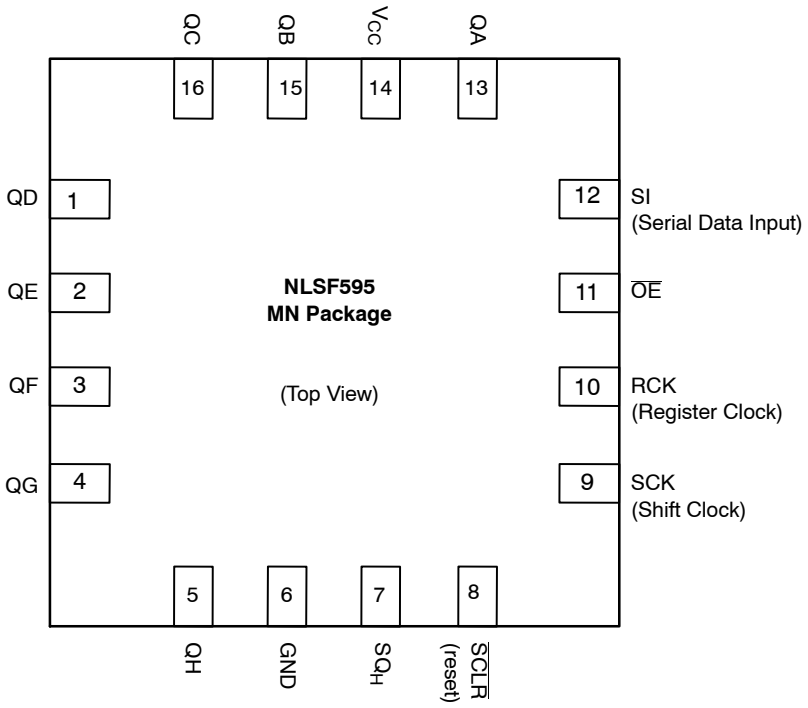


Figure 3. Pin Assignment (QFN−16)

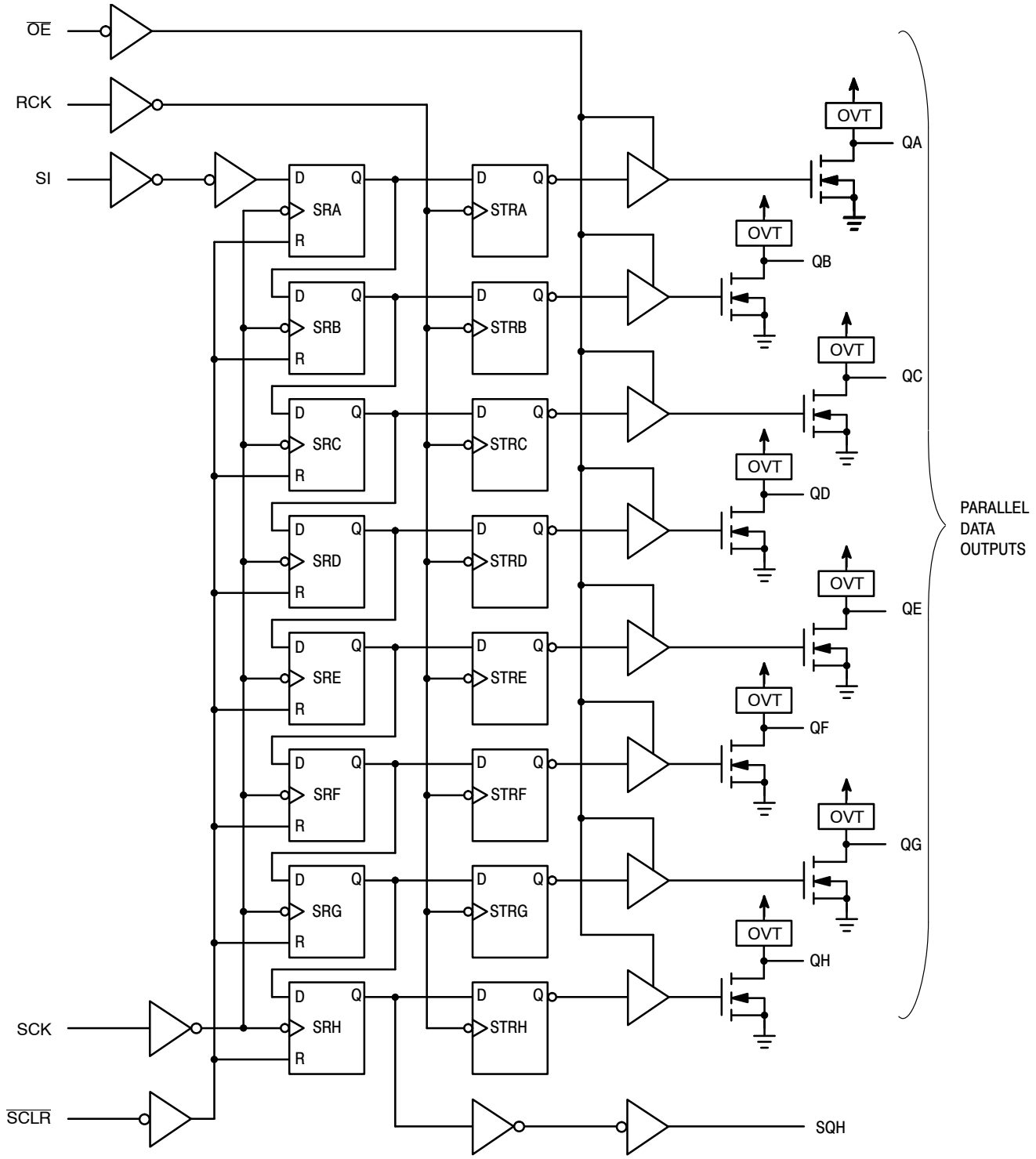


Figure 4. Expanded Logic Diagram

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_{IN}	DC Input Voltage		−0.5 to +6.5	V
V_{OUT}	DC Output Voltage		−0.5 to V_{CC}+0.5	V
I_{IN}	DC Input Current, per Pin		±20	mA
I_{OUT}	DC Output Current, per Pin		+50	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±75	mA
I_{IK}	Input Clamp Current		−20	mA
I_{OK}	Output Clamp Current		±50	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)	QFN−16 TSSOP−16	118 159	°C/W
P_D	Power Dissipation in Still Air at 25 °C	QFN−16 TSSOP−16	1062 787	mW
MSL	Moisture Sensitivity		Level 1	−
F_R	Flammability Rating Oxygen Index: 28 to 34		UL 94 V−0 @ 0.125 in.	−
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	2000 N/A	V
ILatchup	Latchup Performance (Note 4)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 76mm−by−114mm, 2−ounce copper trace no air flow per JESD51−7.
3. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.
4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Units
V_{CC}	DC Supply Voltage	2.0	5.5	V
V_{IN}	DC Input Voltage	0	5.5	V
V_{OUT}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature Range, all Package Types	−55	125	°C
t_r, t_f	Input Rise or Fall Time V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	 0 0	 50 15	ns/V

FUNCTION TABLE

Operation	Inputs					Resulting Function			
	Reset ($\overline{SCLR}$)	Serial Input (SI)	Shift Clock (SCK)	Reg Clock (RCK)	Output Enable ($\overline{OE}$)	Shift Register Contents	Storage Register Contents	Serial Output (SQH)	Parallel Outputs (QA – QH)
Clear shift register	L	X	X	L, H, ↓	L	L	U	L	U
Shift data into shift register	H	D	↑	L, H, ↓	L	$D \rightarrow SR_A$; $SR_N \rightarrow SR_{N+1}$	U	$SR_G \rightarrow SR_H$	U
Registers remains unchanged	H	X	L, H, ↓	X	L	U	**	U	**
Transfer shift register contents to storage register	H	X	L, H, ↓	↑	L	U	$SR_N \rightarrow STR_N$	*	SR_N
Storage register remains unchanged	X	X	X	L, H, ↓	L	*	U	*	U
Enable parallel outputs	X	X	X	X	L	*	**	*	Enabled
Force outputs into high impedance state	X	X	X	X	H	*	**	*	Z

SR = shift register contents
STR = storage register contents
D = data (L, H) logic level
U = remains unchanged
↓ = High-to-Low
↑ = Low-to-High
* = depends on Reset and Shift Clock inputs
** = depends on Register Clock input

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25 °C			$T_A \le 85$ °C		$T_A \le 125$ °C		Units
				Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	Minimum High-Level Input Voltage		2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85			1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		V
V_{IL}	Maximum Low-Level Input Voltage		2.0 3.0 4.5 5.5			0.59 0.9 1.35 1.65		0.59 0.9 1.35 1.65		0.59 0.9 1.35 1.65	V
V_{OH}	Minimum High-Level Serial Output Only Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50$ μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4$ mA $I_{OH} = -8$ mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		
V_{OL}	Maximum Low-Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50$ μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		$I_{OL} = 4$ mA $I_{OL} = 8$ mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	
V_{OL2}	Maximum Low-Level Output Voltage with Max. Load $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 20$ mA $I_{OL} = 25$ mA	3.0 4.5		0.8 0.5	1.0 0.6		1.1 0.7		1.25 0.8	V
I_{IN}	Maximum Input Leakage Current	$V_{IN} = 5.5$ V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			4.0		40.0		40.0	μA
I_{OZ}	Three-State Output Off-State Current QA-QH	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	5.5			±0.25		±2.5		±2.5	μA
I_{LKG}	Active (2) State Off Output Leakage Current QA-QH	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	5.5			±0.25		±2.5		±2.5	μA
I_{OFF}	Power Off Output Leakage All Outputs	$V_{IN} = 0$ or 5.5 V $V_{OUT} = 5.5$ V	0			±0.25		±2.5		±2.5	μA

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	T_A = 25 °C			$T_A \le 85$ °C		$T_A \le 125$ °C		Units
			Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency (50% Duty Cycle)	V_{CC} = 3.3 ± 0.3 V	80	150		70		70		MHz
		V_{CC} = 5.0 ± 0.5 V	135	185		115		115		
t_{PLH}, t_{PHL}	Propagation Delay, SCK to SQH	V_{CC} = 3.3 ± 0.3 V C_L = 15 pF		8.8	13.0	1.0	15.0	1.0	15.0	ns
		C_L = 50 pF		11.3	16.5	1.0	18.5	1.0	18.5	
		V_{CC} = 5.0 ± 0.5 V C_L = 15 pF		6.2	8.2	1.0	9.4	1.0	9.4	
		C_L = 50 pF		7.7	10.2	1.0	11.4	1.0	11.4	
t_{PHL}	Propagation Delay, $\overline{SCLR}$ to SQH	V_{CC} = 3.3 ± 0.3 V C_L = 15 pF		8.4	12.8	1.0	13.7	1.0	13.7	ns
		C_L = 50 pF		10.9	16.3	1.0	17.2	1.0	17.2	
		V_{CC} = 5.0 ± 0.5 V C_L = 15 pF		5.9	8.0	1.0	9.1	1.0	9.1	
		C_L = 50 pF		7.4	10.0	1.0	11.1	1.0	11.1	
t_{PLZ}	Output Disable Time RCK to QA-QH	V_{CC} = 3.3 ± 0.3 V C_L = 15 pF		7.7	11.9	1.0	13.5	1.0	13.5	ns
		C_L = 50 pF		10.2	15.4	1.0	17.0	1.0	17.0	
	Output Enable Time RCK to QA-QH	V_{CC} = 5.0 ± 0.5 V C_L = 15 pF		5.4	7.4	1.0	8.5	1.0	8.5	
		C_L = 50 pF		6.9	9.4	1.0	10.5	1.0	10.5	
t_{PZL}	Output Disable Time RCK to QA-QH	V_{CC} = 3.3 ± 0.3 V C_L = 15 pF		7.7	11.9	1.0	13.5	1.0	13.5	ns
		C_L = 50 pF		10.2	15.4	1.0	17.0	1.0	17.0	
	Output Enable Time RCK to QA-QH	V_{CC} = 5.0 ± 0.5 V C_L = 15 pF		5.4	7.4	1.0	8.5	1.0	8.5	
		C_L = 50 pF		6.9	9.4	1.0	10.5	1.0	10.5	
t_{PZL}	Output Enable Time, $\overline{OE}$ to QA-QH	V_{CC} = 3.3 ± 0.3 V C_L = 15 pF R_L = 1 kΩ		7.5	11.5	1.0	13.5	1.0	13.5	ns
		C_L = 50 pF		9.0	15.0	1.0	17.0	1.0	17.0	
		V_{CC} = 5.0 ± 0.5 V C_L = 15 pF R_L = 1 kΩ		4.8	8.6	1.0	10.0	1.0	10.0	
		C_L = 50 pF		8.3	10.6	1.0	12.0	1.0	12.0	
t_{PLZ}	Output Disable Time, $\overline{OE}$ to QA-QH	V_{CC} = 3.3 ± 0.3 V C_L = 50 pF R_L = 1 kΩ		12.1	15.7	1.0	16.2	1.0	16.2	ns
		V_{CC} = 5.0 ± 0.5 V C_L = 50 pF R_L = 1 kΩ		7.6	10.3	1.0	11.0	1.0	11.0	
C_{IN}	Input Capacitance			4	10		10		10	pF
C_{OUT}	Three-State Output Capacitance (Output in High-Impedance State), QA-QH			6			10		10	pF

		Typical @ 25 °C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 5)	87	pF

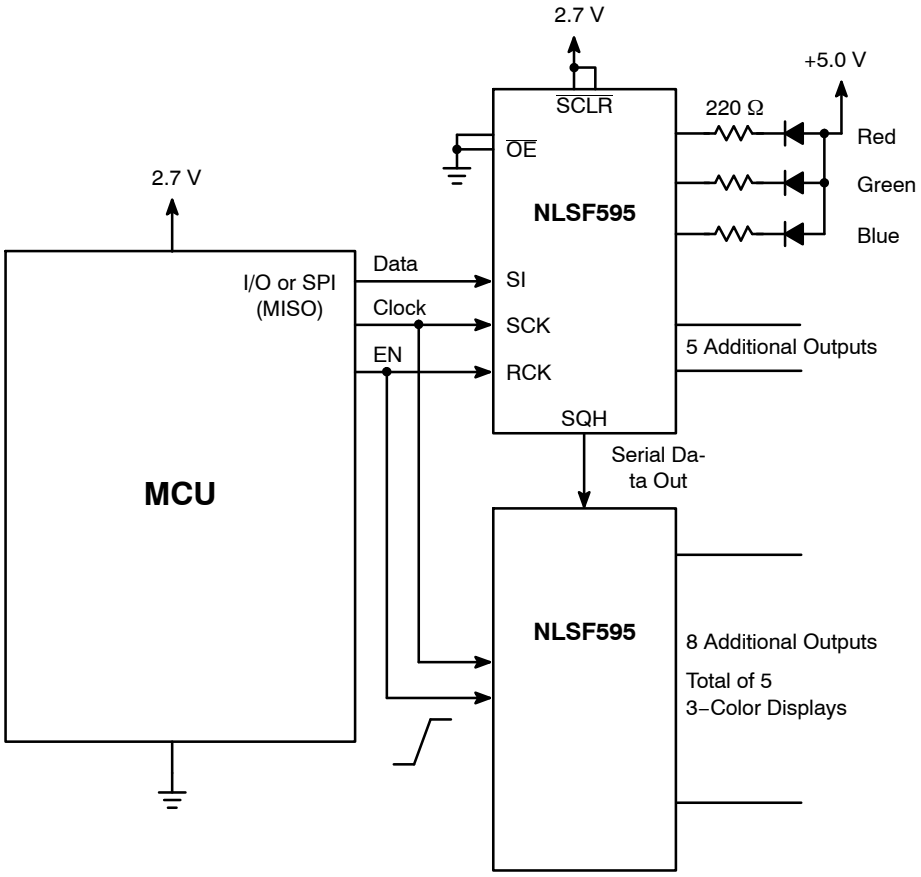
5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0 ns, C_L = 50 pF, V_{CC} = 5.0 V)

Symbol	Characteristic	T_A = 25 °C		Units
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.8	1.0	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−0.8	−1.0	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

TIMING REQUIREMENTS

Symbol	Parameter	V_{CC} V	T_A = 25 °C		T_A = − 40 to 85 °C	T_A = − 55 to 125 °C	Units
			Typ	Limit	Limit	Limit	
t_{su}	Setup Time, SI to SCK	3.3 5.0		3.5 3.0	3.5 3.0	3.5 3.0	ns
$t_{su(H)}$	Setup Time, SCK to RCK	3.3 5.0		8.0 5.0	8.5 5.0	8.5 5.0	ns
$t_{su(L)}$	Setup Time, $\overline{SCLR}$ to RCK	3.3 5.0		8.0 5.0	9.0 5.0	9.0 5.0	ns
t_h	Hold Time, SI to SCK	3.3 5.0		1.5 2.0	1.5 2.0	1.5 2.0	ns
$t_{h(L)}$	Hold Time, $\overline{SCLR}$ to RCK	3.3 5.0		0 0	0 0	1.0 1.0	ns
t_{rec}	Recovery Time, $\overline{SCLR}$ to SCK	3.3 5.0		3.0 2.5	3.0 2.5	3.0 2.5	ns
t_w	Pulse Width, SCK or RCK	3.3 5.0		5.0 5.0	5.0 5.0	5.0 5.0	ns
$t_{w(L)}$	Pulse Width, $\overline{SCLR}$	3.3 5.0		5.0 5.0	5.0 5.0	5.0 5.0	ns



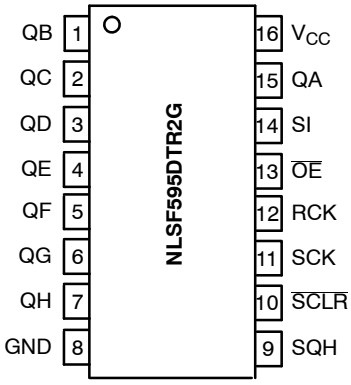
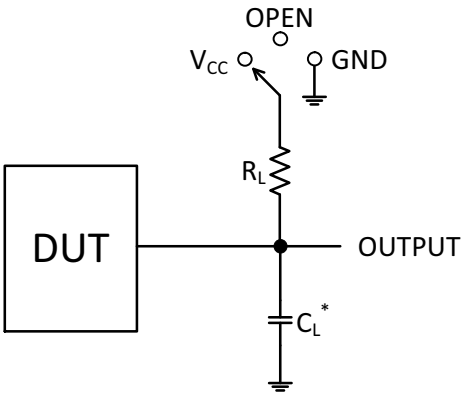


Figure 5. NLSF595 Shown Driving 5 3−Color LEDs

TEST CIRCUITS



Test	Switch Position	C_L	R_L
t_{PLH} / t_{PHL}	Open	See AC Characteristics Table	1 kΩ
t_{PLZ} / t_{PZL}	V_{CC}		
t_{PHZ} / t_{PZH}	GND		

*C_L Includes probe and jig capacitance
Input $t_R = t_F$ = 3 ns

Figure 6. Test Circuits

SWITCHING WAVEFORMS

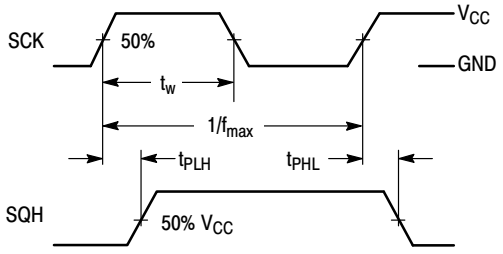


Figure 7.

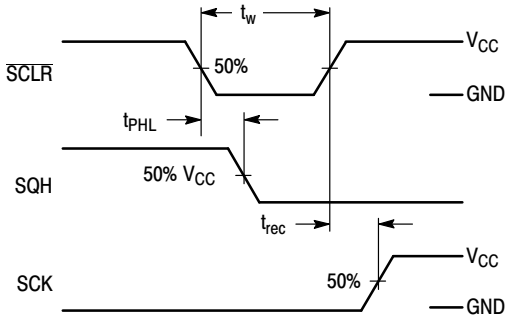


Figure 8.

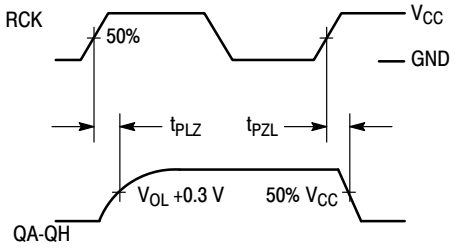


Figure 9.

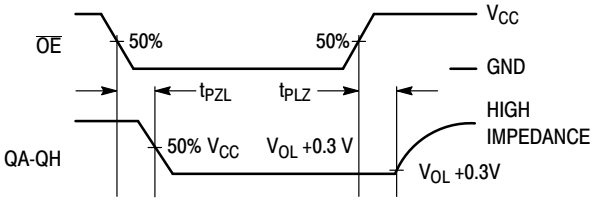


Figure 10.

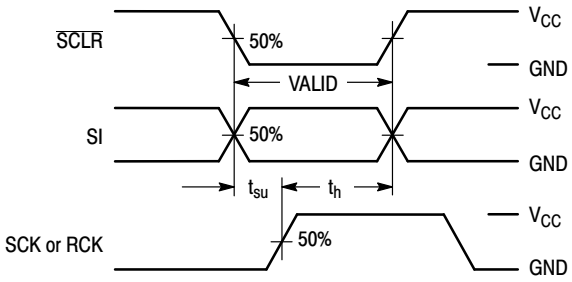


Figure 11.

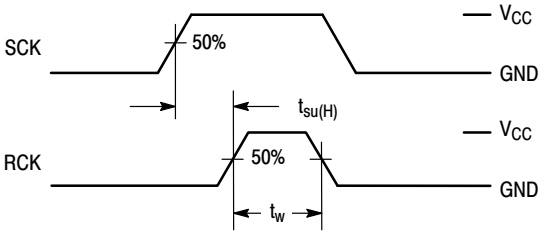


Figure 12.

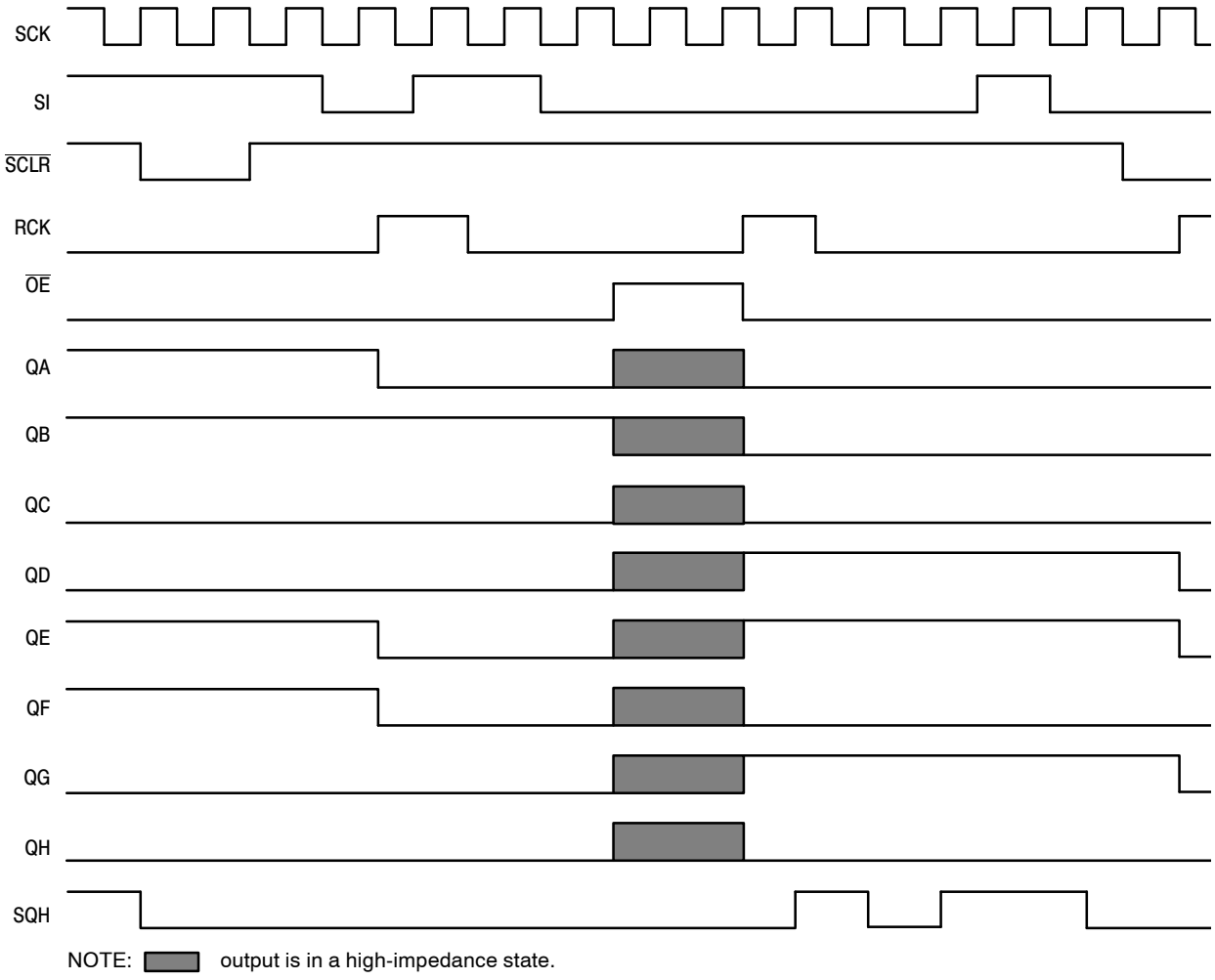


Figure 13. Timing Diagram

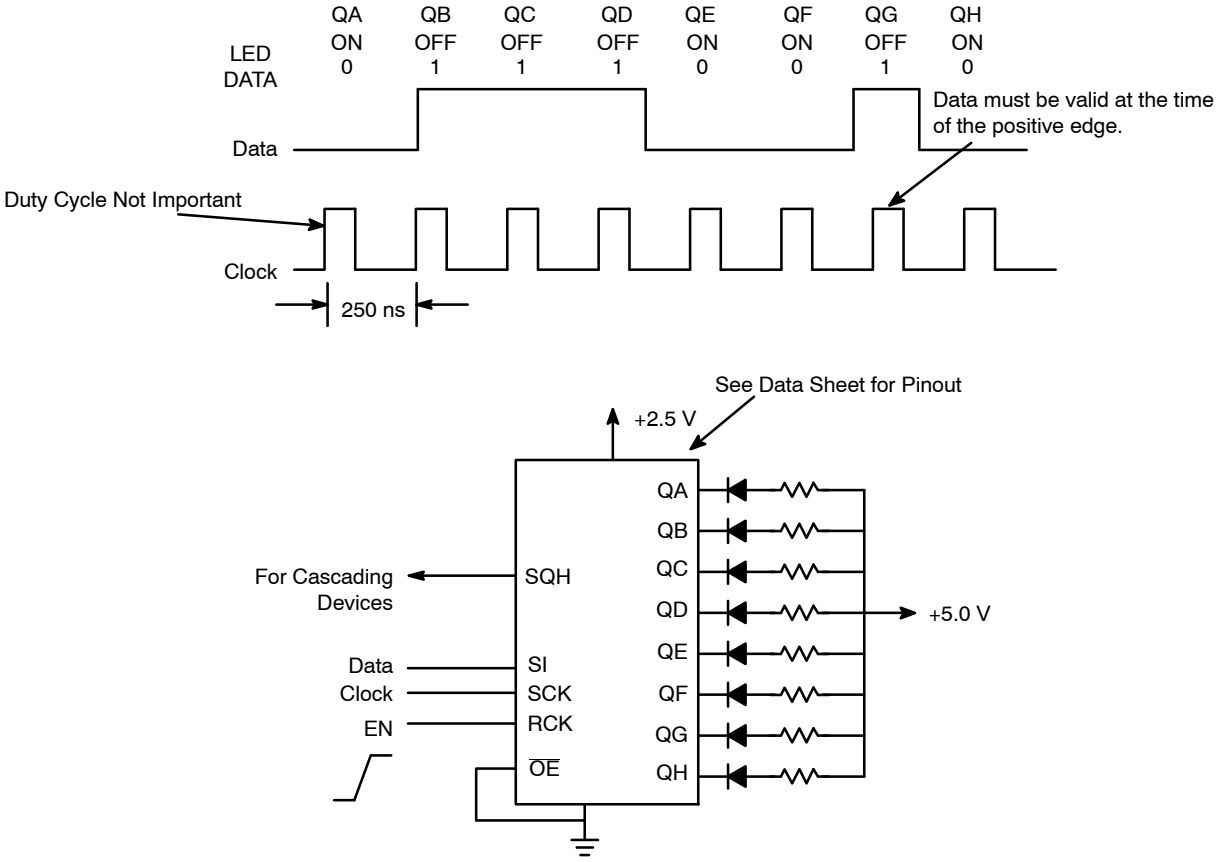


Figure 14. NLSF595 Example

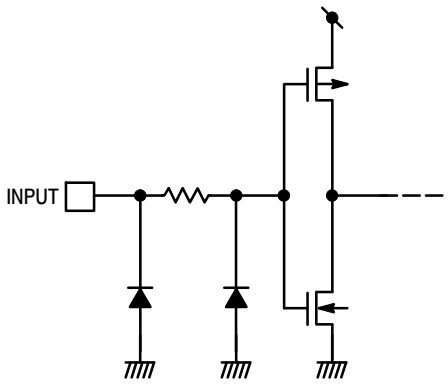


Figure 15. Input Equivalent Circuit

ORDERING INFORMATION

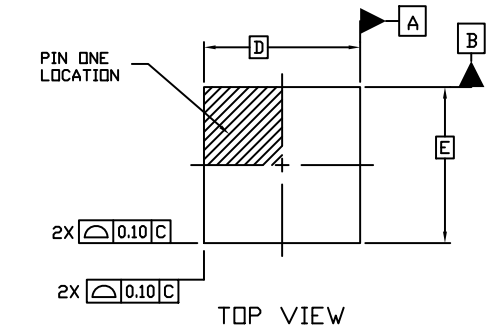
Device	Marking	Package	Shipping†
NLSF595MNR2G	SF 595	QFN−16 (Pb-Free)	3000 Units / Tape & Reel
NLSF595DTR2G	NLSF 595	TSSOP−16 (Pb-Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

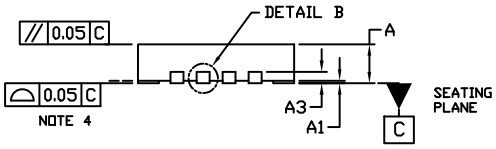
QFN16 3x3, 0.5P
CASE 485G
ISSUE G

DATE 08 OCT 2021

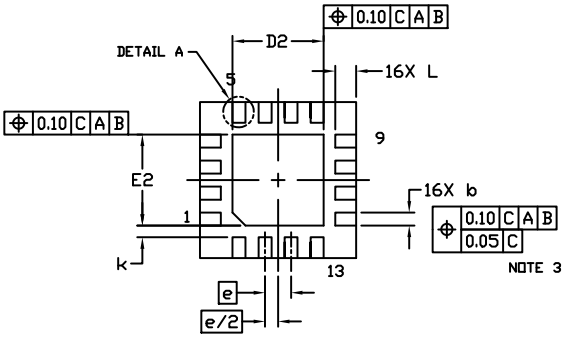
SCALE 2:1



TOP VIEW



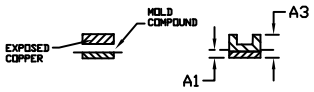
SIDE VIEW



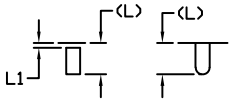
BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



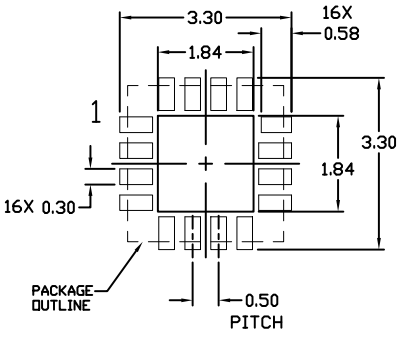
DETAIL B
ALTERNATE CONSTRUCTIONS



DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3		0.20 REF	
b	0.18	0.24	0.30
D		3.00 BSC	
D2	1.65	1.75	1.85
E		3.00 BSC	
E2	1.65	1.75	1.85
e		0.50 BSC	
k		0.18 TYP	
L	0.30	0.40	0.50
L1	0.00	0.08	0.15

MOUNTING FOOTPRINT



GENERIC MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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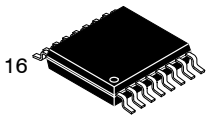
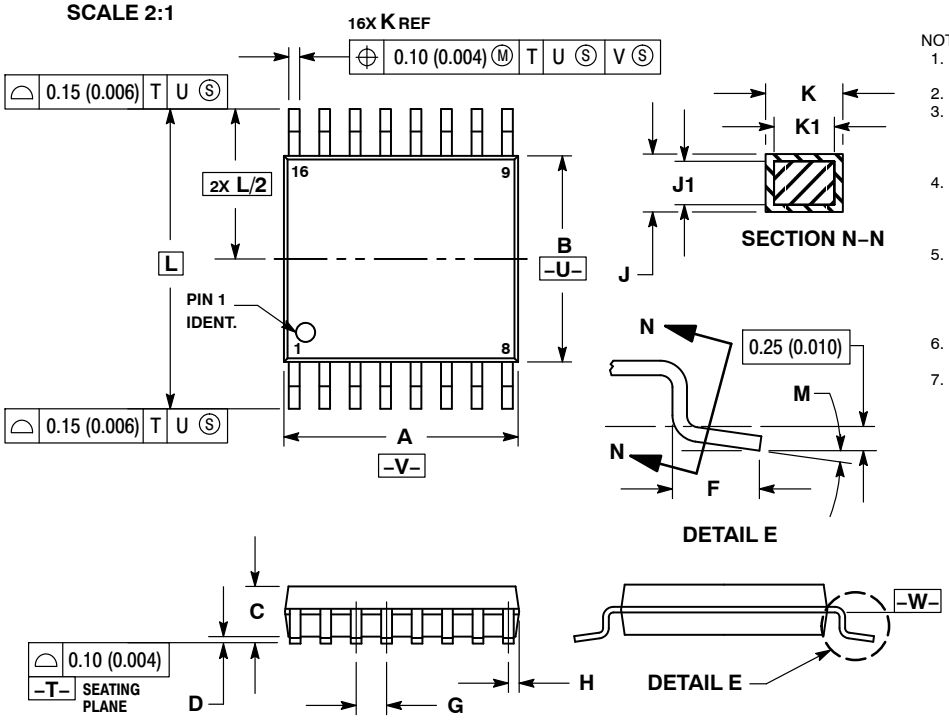
DESCRIPTION:	**QFN16 3X3, 0.5P**	**PAGE 1 OF 1**



SCALE 2:1

TSSOP−16 WB
CASE 948F
ISSUE B

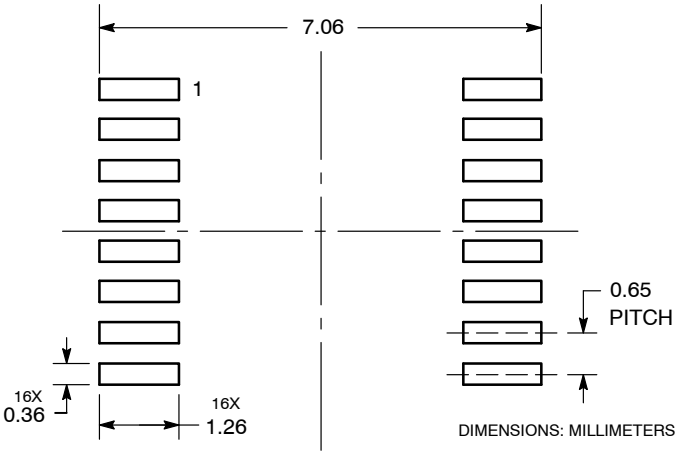
DATE 19 OCT 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

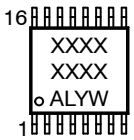
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
G or ▪	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TSSOP−16**		**PAGE 1 OF 1**

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