

Single D Flip-Flop

NLX1G74

The NLX1G74 is a high performance, full function edge-triggered D Flip-Flop in ultra-small footprint. The NLX1G74 input structures provide protection when voltages up to 7.0 V are applied, regardless of the supply voltage.

Features

- Extremely High Speed: $t_{PD} = 2.6$ ns (typical) at $V_{CC} = 5.0$ V
- Designed for 1.65 V to 5.5 V V_{CC} Operation
- Low Power Dissipation: $I_{CC} = 1$ μ A (Max) at $T_A = 25^\circ$ C
- 24 mA Balanced Output Sink and Source Capability at $V_{CC} = 3.0$ V
- Balanced Propagation Delays
- Overvoltage Tolerant (OVT) Input Pins
- Ultra Small Package
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- This is a Pb-Free Device

TRUTH TABLE

Inputs				Outputs		Operating Mode
PR	CLR	CP	D	Q	$\bar{Q}$	
L	H	X	X	H	L	Asynchronous Set Asynchronous Clear Undetermined
H	L	X	X	L	H	
L	L	X	X	H	H	
H	H	$\uparrow$	h	H	L	Load and Read Register
H	H	$\uparrow$	l	L	H	
H	H	$\uparrow$	X	NC	NC	Hold

H = High Voltage Level

h = High Voltage Level One Setup Time Prior to the Low-to-High Clock Transition

L = Low Voltage Level

l = Low Voltage Level One Setup Time Prior to the Low-to-High Clock Transition

NC = No Change

X = High or Low Voltage Level and Transitions are Acceptable

$\uparrow$ = Low-to-High Transition

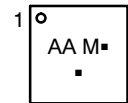
$\uparrow$ = Not a Low-to-High Transition

For I_{CC} reasons, DO NOT FLOAT Inputs



UQFN8
MU SUFFIX
CASE 523AN

MARKING DIAGRAM



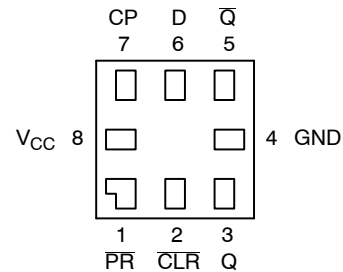
AA = Device Code

M = Date Code*

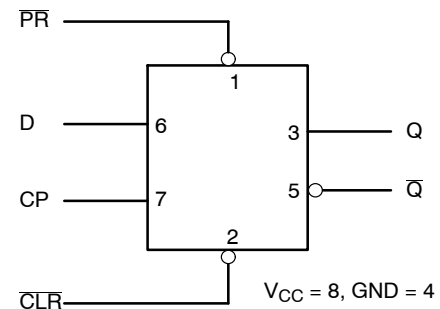
▪ = Pb-Free Package

(Note: Microdot may be in either location)

PINOUT DIAGRAM



LOGIC DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 3.

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MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage	-0.5 to +7.0	V
V_O	DC Output Voltage – Output in High or Low State (Note 1)	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current $V_I < GND$	-50	mA
I_{OK}	DC Output Diode Current $V_O < GND$	-50	mA
I_O	DC Output Sink Current	± 50	mA
I_{CC}	DC Supply Current Per Supply Pin	± 100	mA
I_{GND}	DC Ground Current Per Ground Pin	± 100	mA
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T_J	Junction Temperature Under Bias	+150	°C
θ_{JA}	Thermal Resistance (Note 2)	250	°C/W
P_D	Power Dissipation in Still Air at 85°C	250	mW
MSL	Moisture Sensitivity	Level 1	
F_R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5)	>2000 >200 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm X 1 inch, 2 ounce copper trace with no air flow.
3. Tested to EIA/JESD22-A114-A.
4. Tested to EIA/JESD22-A115-A.
5. Tested to JESD22-C101-A.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage Operating Data Retention Only	1.65 1.5	5.5 5.5	V
V_I	Input Voltage (Note 6)	0	5.5	V
V_O	Output Voltage (HIGH or LOW State)	0	V_{CC}	V
T_A	Operating Free-Air Temperature	-40	+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ $V_{CC} = 3.0\text{ V} \pm 0.3\text{ V}$ $V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$	0 0 0	20 10 5.0	ns/V

6. Unused inputs may not be left open. All inputs must be tied to a high-logic voltage level or a low-logic input voltage level.

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ORDERING INFORMATION

Device	Package	Shipping [†]
NLX1G74MUTCG	UQFN8 (Pb-Free)	3000 / Tape & Reel

DISCONTINUED (Note 7)

NLVX1G74MUTCG*	UQFN8 (Pb-Free)	3000 / Tape & Reel
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[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

7. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	High-Level Input Voltage		1.65	0.75 V _{CC}			0.75 V _{CC}		V
			2.3 to 5.5	0.7 V _{CC}			0.7 V _{CC}		
V _{IL}	Low-Level Input Voltage		1.65			0.25 V _{CC}		0.25 V _{CC}	V
			2.3 to 5.5			0.3 V _{CC}		0.3 V _{CC}	
V _{OH}	High-Level Output Voltage V _{IN} = V _{IL} or V _{IL}	I _{OH} = 100 μA	1.65 to 5.5	V _{CC} - 0.1	V _{CC}		V _{CC} - 0.1		V
		I _{OH} = -3 mA	1.65	1.29	1.52		1.29		
		I _{OH} = -8 mA	2.3	1.9	2.1		1.9		
		I _{OH} = -12 mA	2.7	2.2	2.4		2.2		
		I _{OH} = -16 mA	3.0	2.4	2.7		2.4		
		I _{OH} = -24 mA	3.0	2.3	2.5		2.3		
		I _{OH} = -32 mA	4.5	3.8	4.0		3.8		
V _{OL}	Low-Level Output Voltage V _{IN} = V _{IH}	I _{OL} = 100 μA	1.65 to 5.5		0.008	0.1		0.1	V
		I _{OL} = 3 mA	1.65		0.10	0.24		0.24	
		I _{OL} = 8 mA	2.3		0.12	0.3		0.3	
		I _{OL} = 12 mA	2.7		0.15	0.4		0.4	
		I _{OL} = 16 mA	3.0		0.19	0.4		0.4	
		I _{OL} = 24 mA	3.0		0.30	0.55		0.55	
		I _{OL} = 32 mA	4.5		0.30	0.55		0.55	
I _{IN}	Input Leakage Current	V _{IN} = V _{CC} or GND	5.5			±0.1		±1.0	μA
I _{OFF}	Power off Input Leakage Current	5.5V or V _{IN} = GND	0			1.0		10	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5			1.0		10	μA

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	V _{CC} (V)	Test Conditions	T _A = 25°C			T _A = -40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency (50% Duty Cycle) (Waveform 1)	1.8 ± 0.15	C _L = 15 pF R _D = 1 MΩ S ₁ = Open	75			75		MHz
		2.5 ± 0.2		150			150		
		3.3 ± 0.3		200			200		
		5.0 ± 0.5		250			250		
		3.3 ± 0.3	C _L = 50 pF, R _D = 500 Ω, S ₁ = Open	175			175		
		5.0 ± 0.5		200			200		
t _{PLH} , t _{PHL}	Propagation Delay, CP to Q or $\bar{Q}$ (Waveform 1)	1.8 ± 0.15	C _L = 15 pF R _D = 1 MΩ S ₁ = Open	2.5	6.5	12.5	2.5	13	ns
		2.5 ± 0.2		1.5	3.8	7.5	1.5	8.0	
		3.3 ± 0.3		1.0	2.8	6.5	1.0	7.0	
		5.0 ± 0.5		0.8	2.2	4.5	0.8	5.0	
		3.3 ± 0.3	C _L = 50 pF, R _D = 500 Ω, S ₁ = Open	1.0	3.4	7.0	1.0	7.5	
		5.0 ± 0.5		1.0	2.6	5.0	1.0	5.5	
t _{PLH} , t _{PHL}	Propagation Delay, PR or CLR to Q or $\bar{Q}$ (Waveform 2)	1.8 ± 0.15	C _L = 15 pF R _D = 1 MΩ S ₁ = Open	2.5	6.5	14	2.5	14.5	ns
		2.5 ± 0.2		1.5	3.8	9.0	1.5	9.5	
		3.3 ± 0.3		1.0	2.8	6.5	1.0	7.0	
		5.0 ± 0.5		0.8	2.2	5.0	0.8	5.5	
		3.3 ± 0.3	C _L = 50 pF, R _D = 500 Ω, S ₁ = Open	1.0	3.4	7.0	1.0	7.5	
		5.0 ± 0.5		1.0	2.6	5.0	1.0	5.5	
t _S	Setup Time, D to CP (Waveform 1)	1.8 ± 0.15	C _L = 15 pF R _D = 1 MΩ S ₁ = Open	6.5			6.5		ns
		2.5 ± 0.2		3.5			3.5		
		3.3 ± 0.3		2.0			2.0		
		5.0 ± 0.5		1.5			1.5		
		3.3 ± 0.3	C _L = 50 pF, R _D = 500 Ω, S ₁ = Open	2.0			2.0		
		5.0 ± 0.5		1.5			1.5		
t _H	Hold Time, D to CP (Waveform 1)	1.8 ± 0.15	C _L = 15 pF R _D = 1 MΩ S ₁ = Open	0.5			0.5		ns
		2.5 ± 0.2		0.5			0.5		
		3.3 ± 0.3		0.5			0.5		
		5.0 ± 0.5		0.5			0.5		
		3.3 ± 0.3	C _L = 50 pF, R _D = 500 Ω, S ₁ = Open	0.5			0.5		
		5.0 ± 0.5		0.5			0.5		
t _W	Pulse Width, CP, $\bar{CLR}$, PR (Waveform 3)	1.8 ± 0.15	C _L = 15 pF R _D = 1 MΩ S ₁ = Open	6.0			6.0		ns
		2.5 ± 0.2		4.0			4.0		
		3.3 ± 0.3		3.0			3.0		
		5.0 ± 0.5		2.0			2.0		
		3.3 ± 0.3	C _L = 50 pF, R _D = 500 Ω, S ₁ = Open	3.0			3.0		
		5.0 ± 0.5		2.0			2.0		
t _{REC}	Recover Time PR; CLR to CP (Waveform 3)	1.8 ± 0.15	C _L = 15 pF R _D = 1 MΩ S ₁ = Open	8.0			8.0		MHz
		2.5 ± 0.2		4.5			4.5		
		3.3 ± 0.3		3.0			3.0		
		5.0 ± 0.5		3.0			3.0		
		3.3 ± 0.3	C _L = 50 pF, R _D = 500 Ω, S ₁ = Open	3.0			3.0		
		5.0 ± 0.5		3.0			3.0		

8. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/2 (per flip-flop). C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

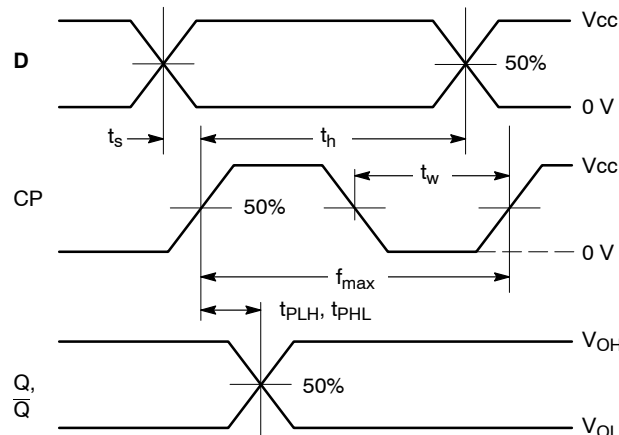
CAPACITANCE (Note 9)

Symbol	Parameter	Condition	Typical	Unit
C _{IN}	Input Capacitance	V _{CC} = 5.5 V	7.0	pF
C _{OUT}	Output Capacitance	V _{CC} = 5.5 V	7.0	pF
C _{PD}	Power Dissipation Capacitance (Note 10) Frequency = 10 MHz	V _{CC} = 3.3 V	16	pF
		V _{CC} = 5.0 V	21	

9. T_A = +25°C, f = 1 MHz

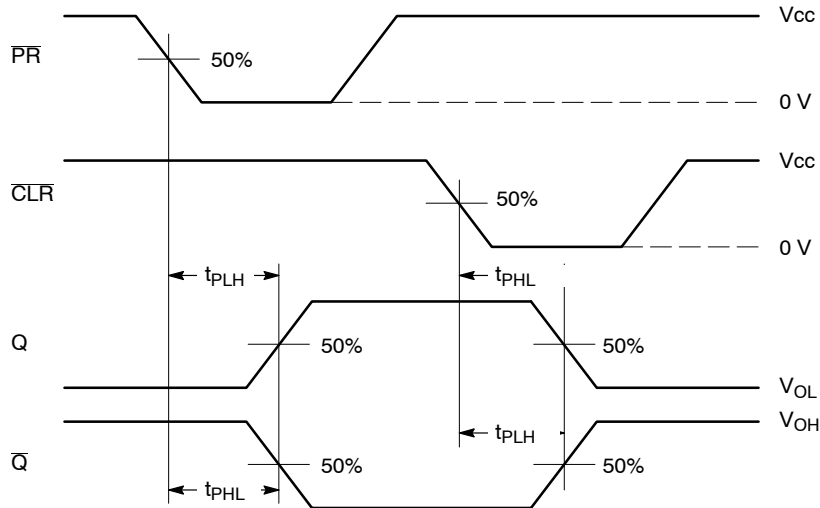
10. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 1) C_{PD} is related to I_{CCD} dynamic operating current by the expression:
I_{CCD} = C_{PD} • V_{CC} • f_{in} + I_{CC(static)}

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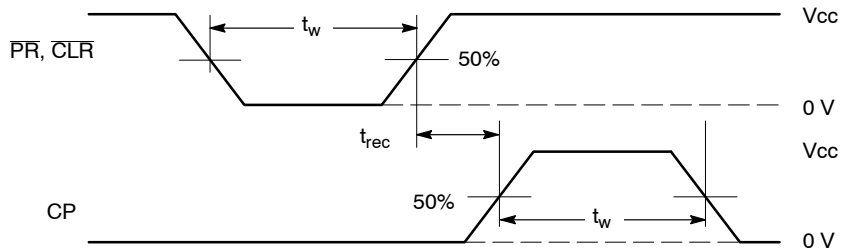
WAVEFORM 1 – PROPAGATION DELAYS, SETUP AND HOLD TIMES

$t_R = t_F = 3.0 \text{ ns}$, 10% to 90%; $f = 1 \text{ MHz}$; $t_W = 500 \text{ ns}$



WAVEFORM 2 – PROPAGATION DELAYS

$t_R = t_F = 3.0 \text{ ns}$, 10% to 90%; $f = 1 \text{ MHz}$; $t_W = 500 \text{ ns}$



WAVEFORM 3 – RECOVERY TIME

$t_R = t_F = 3.0 \text{ ns}$ from 10% to 90%; $f = 1 \text{ MHz}$; $t_W = 500 \text{ ns}$

Output Reg: $V_{OL} \leq 0.8 \text{ V}$, $V_{OH} \geq 2.0 \text{ V}$

Figure 1. AC Waveforms

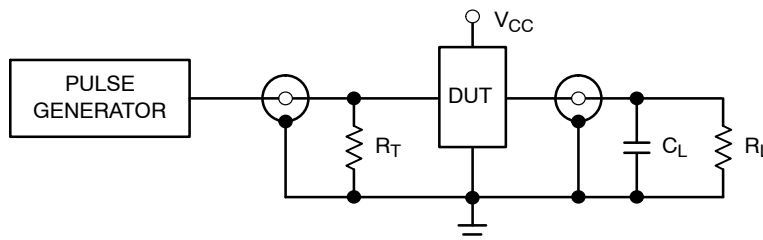


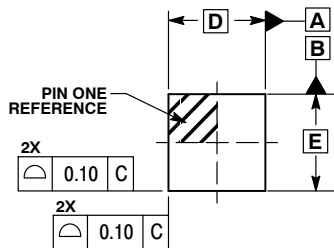
Figure 2. Test Circuit



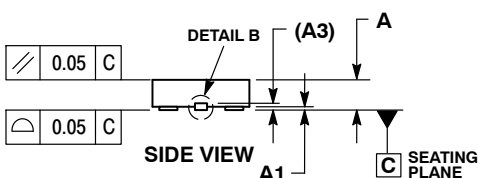
SCALE 4:1

UQFN8, 1.60x1.60, 0.50P
CASE 523AN
ISSUE O

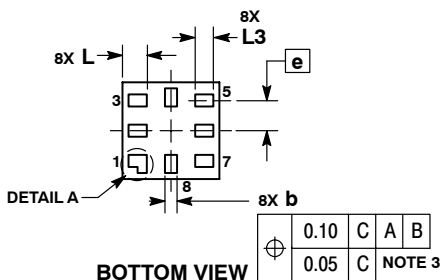
DATE 26 NOV 2008



TOP VIEW

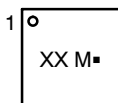


SIDE VIEW



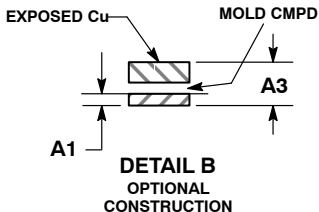
BOTTOM VIEW

GENERIC MARKING DIAGRAM*

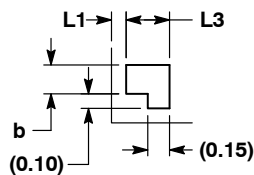


XX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



DETAIL B
OPTIONAL
CONSTRUCTION



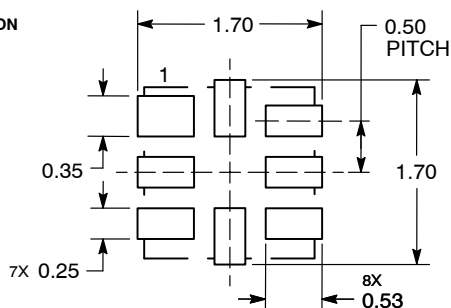
DETAIL A
OPTIONAL
CONSTRUCTION

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.60
A1	0.00	0.05
A3	0.13	REF
b	0.15	0.25
D	1.60	BSC
E	1.60	BSC
e	0.50	BSC
L	0.35	0.45
L1	---	0.15
L3	0.25	0.35

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	UQFN8, 1.60X1.60, 0.50P	PAGE 1 OF 1

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