TPS793-Q1 Ultralow-Noise, High-PSRR, Fast RF 200-mA Low-Dropout Linear Regulators

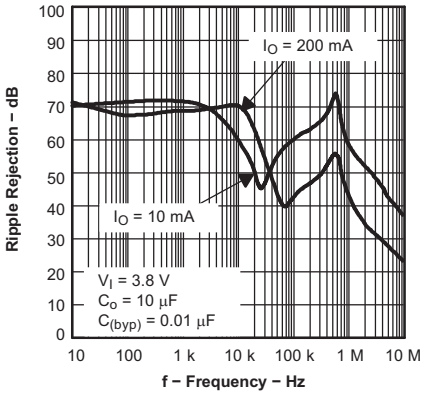
1 Features

- Qualified For Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C
  - Device HBM ESD Classification Level 1C
  - Device CDM ESD Classification Level C2
- 200-mA Low-Dropout Regulator With EN
- Available in 1.8-V, 2.5-V, 2.8-V, 3-V, 3.3-V, 4.75-V, and Adjustable Options
- High PSRR (70 dB at 10 kHz)
- Ultralow Noise (32 μV)
- Fast Start-Up Time (50 μs)
- Stable With a 2.2-μF Ceramic Capacitor
- Excellent Load and Line Transient
- Very Low Dropout Voltage (112 mV at Full Load, TPS79330-Q1)
- 5-Pin SOT-23 (DBV) Package

2 Applications

- VCOs
- RF
- Bluetooth™

TPS79328-Q1 Ripple Rejection vs Frequency



3 Description

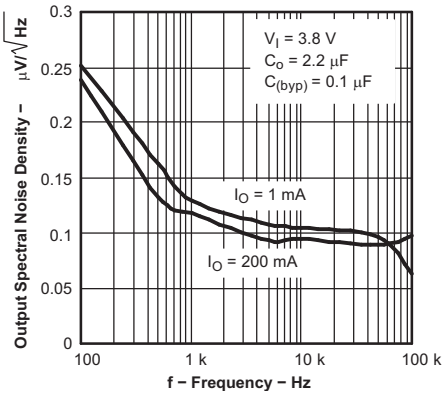
The TPS793xx-Q1 family of low-dropout (LDO) low-power linear voltage regulators features high power-supply rejection ratio (PSRR), ultralow noise, fast start-up, and excellent line and load transient responses in a small-outline SOT-23 package. Each TPS793-Q1 device in the family is stable, with a small 2.2-μF ceramic capacitor on the output. The TPS793xx-Q1 family uses an advanced, proprietary, BiCMOS fabrication process to yield extremely low dropout voltages (for example, 112 mV at 200 mA, TPS79330-Q1). Each device achieves fast start-up times (approximately 50 μs with a 0.001-μF bypass capacitor), while consuming very low quiescent current (170 μA typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than 1 μA. The TPS79328-Q1 exhibits approximately 32 μV_{RMS} of output voltage noise with a 0.1-μF bypass capacitor. Applications with analog components that are noise sensitive, such as portable RF electronics, benefit from the high PSRR and low-noise features, as well as the fast response time.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS793xx-Q1	SOT-23 (6)	2.90 × 2.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

TPS79328-Q1 Output Spectral Noise Density vs Frequency



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (January 2013) to Revision I	Page
• Changed document part numbers to the generic TPS793-Q1	1
• Removed the 2.85-V version from the data sheet	1
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

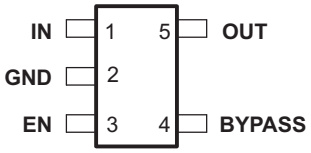
5 Voltage Options

OUTPUT VOLTAGE	ORDERABLE PART NUMBER	SYMBOL
1.2 V to 5.5 V	TPS79301DBVRQ1	PGV1
1.8 V	TPS79318DBVRQ1	PHH1
2.5 V	TPS79325DBVRQ1	PGW1
2.8 V	TPS79328DBVRQ1	PGX1
2.85 V	TPS793285QDBVRQ1	PHI1
3 V	TPS79330QDBVRQ1	PGY1
3.3 V	TPS79333DBVRQ1	PHU1
4.75 V	TPS793475QDBVRQ1(1)	PHJ1

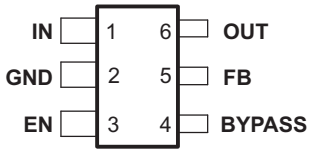
(1) Product Preview

6 Pin Configuration and Functions

Fixed Option: DBV Package
6-Pin SOT-23
Top View



Adjustable Option: DBV Package
6-Pin SOT-23
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	ADJ	FIXED		
BYPASS	4	4	—	An external bypass capacitor, connected to this terminal, in conjunction with an internal resistor, creates a low-pass filter to further reduce regulator noise.
EN	3	3	I	Enable input that enables or shuts down the device. When EN goes to a logic high, the device is enabled. When the device goes to a logic low, the device is in shutdown mode.
FB	5	N/A	I	Feedback input voltage for the adjustable device
GND	2	2	—	Regulator ground
IN	1	1	I	Input to the device
OUT	6	5	O	Regulated output of the device

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
	Input voltage(2)	–0.3	6	V
	Voltage range at EN	–0.3	V_I + 0.3	V
	Voltage on OUT	–0.3	6	V
	Peak output current	Internally limited		
	Continuous total power dissipation	See *Thermal Information*		
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±250	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	2.7		5.5	V
V_{EN}	Enable supply voltage	0		V_{IN}	V
V_{OUT}	Output voltage	V_{FB}		5	V
I_{OUT}	Output current	0		200	mA
T_J	Operating junction temperature	–40		125	°C
C_{IN}	Input capacitor	0.1	1		µF
C_{OUT}	Output capacitor	2.2	10		µF
C_{NR}	Noise reduction capacitor	0	10		nF
C_{FF}	Feed-forward capacitor		15		pF
R_2	Lower feedback resistor		30.1		kΩ

7.4 Thermal Information

THERMAL METRIC(1)		TPS793xx-Q1 DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	225.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over recommended operating free-air temperature range, EN = V_I, T_J = –40 to 125°C, V_I = $V_{O(typ)}$ + 1 V, I_O = 1 mA, C_o = 10 µF, $C_{(byp)}$ = 0.01 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_I Input voltage(1)				2.7		5.5	V
I_O Continuous output current				0		200	mA
T_J Operating junction temperature				–40		125	°C
Output voltage	TPS79301-Q1	0 µA < I_O < 200 mA		V_{FB}		5.5 – $V_{DROPOUT}$	V
	TPS79318-Q1	T_J = 25°C			1.8		
		0 µA < I_O < 200 mA,	2.8 V < V_I < 5.5 V	1.764		1.836	
	TPS79325-Q1	T_J = 25°C			2.5		
		0 µA < I_O < 200 mA,	3.5 V < V_I < 5.5 V	2.45		2.55	
	TPS79328-Q1	T_J = 25°C			2.8		
		0 µA < I_O < 200 mA,	3.8 V < V_I < 5.5 V	2.744		2.856	
	TPS79330-Q1	T_J = 25°C			3		
		0 µA < I_O < 200 mA,	4 V < V_I < 5.5 V	2.94		3.06	
	TPS79333-Q1	T_J = 25°C			3.3		
		0 µA < I_O < 200 mA,	4.3 V < V_I < 5.5 V	3.234		3.366	
	TPS793475-Q1	T_J = 25°C			4.75		
		0 µA < I_O < 200 mA,	5.25 V < V_I < 5.5 V	4.655		4.845	
Quiescent current (GND current)		0 µA < I_O < 200 mA,	T_J = 25°C		170		µA
		0 µA < I_O < 200 mA				220	
Load regulation		0 µA < I_O < 200 mA,	T_J = 25°C		5		mV
Output voltage line regulation ($\Delta V_O/V_O$)		V_O + 1 V < V_I ≤ 5.5 V,	T_J = 25°C		0.05		%/V
		V_O + 1 V < V_I ≤ 5.5 V				0.12	
Output noise voltage	TPS79328-Q1	BW = 200 Hz to 100 kHz, I_O = 200 mA, T_J = 25°C	$C_{(byp)}$ = 0.001 µF		55		μV_{RMS}
			$C_{(byp)}$ = 0.0047 µF		36		
			$C_{(byp)}$ = 0.01 µF		33		
			$C_{(byp)}$ = 0.1 µF		32		
Time, start-up	TPS79328-Q1	R_L = 14 Ω, C_o = 1 µF, T_J = 25°C	$C_{(byp)}$ = 0.001 µF		50		µs
			$C_{(byp)}$ = 0.0047 µF		70		
			$C_{(byp)}$ = 0.01 µF		100		
Output current limit		V_O = 0 V		285		600	mA
Standby current(2)		EN = 0 V,	2.7 V < V_I < 5.5 V		0.07	1	µA
High-level enable input voltage		2.7 V < V_I < 5.5 V		2			V
Low-level enable input voltage		2.7 V < V_I < 5.5 V				0.7	V
Input current (EN)		EN = 0		–1		1	µA
Input current (FB)	TPS79301-Q1	FB = 1.8 V				1	µA
Internal reference, V_{FB}	TPS79301-Q1			1.201	1.225	1.250	V
Power-supply ripple rejection	TPS79328-Q1	f = 100 Hz, T_J = 25°C,	I_O = 10 mA		70		dB
			I_O = 200 mA		68		
		f = 10 kHz, T_J = 25°C,	I_O = 200 mA		70		
		f = 100 kHz, T_J = 25°C,			43		

(1) Minimum V_{IN} is 2.7 V or VOUT + VDO, whichever is greater.
(2) For adjustable versions, this parameter applies only after V_{IN} is applied; then V_{EN} transitions high to low.

Electrical Characteristics (continued)

over recommended operating free-air temperature range, EN = V_I, T_J = –40 to 125°C, V_I = $V_{O(typ)}$ + 1 V, I_O = 1 mA, C_o = 10 µF, $C_{(byp)}$ = 0.01 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Dropout voltage(3)	TPS79328-Q1	I_O = 200 mA,	T_J = 25°C		120		mV
		I_O = 200 mA				200	
	TPS79330-Q1	I_O = 200 mA,	T_J = 25°C		112		
		I_O = 200 mA				200	
	TPS79333-Q1	I_O = 200 mA,	T_J = 25°C		102		
		I_O = 200 mA				180	
	TPS793475-Q1	I_O = 200 mA,	T_J = 25°C		77		
		I_O = 200 mA				125	
UVLO threshold		V_{CC} rising		2.25		2.65	V
UVLO hysteresis		T_J = 25°C	V_{CC} rising		100		mV

(3) Dropout is not measured for the TPS79318-Q1 and TPS79325-Q1 since minimum V_{IN} = 2.7 V.

7.6 Typical Characteristics

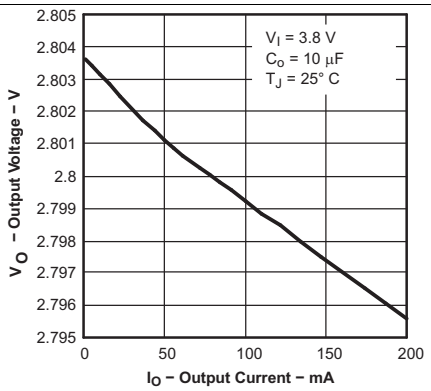


Figure 1. TPS79328-Q1 Output Voltage vs Output Current

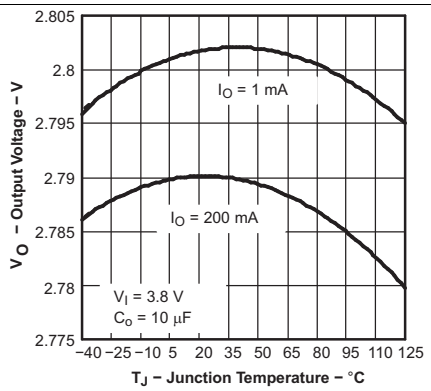


Figure 2. TPS79328-Q1 Output Voltage vs Junction Temperature

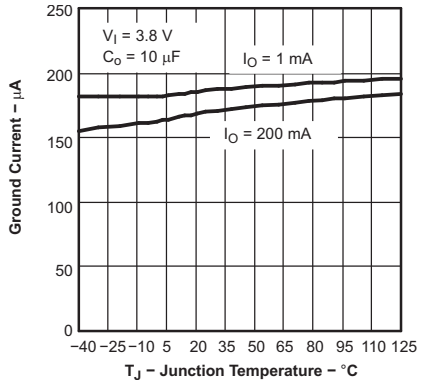


Figure 3. TPS79328-Q1 Ground Current vs Junction Temperature

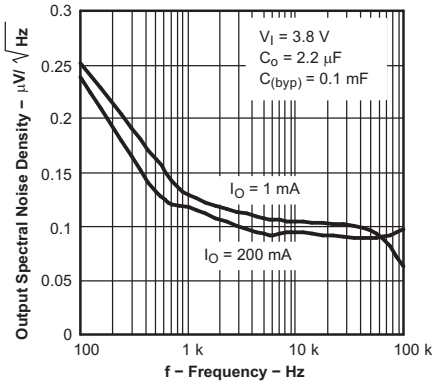


Figure 4. TPS79328-Q1 Output Spectral Noise Density vs Frequency

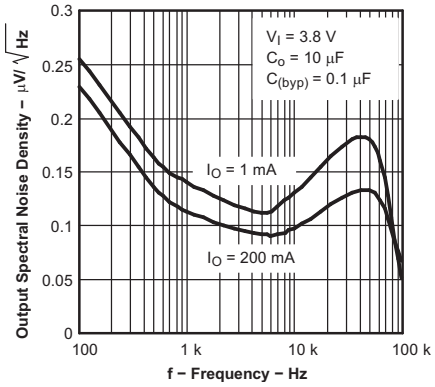


Figure 5. TPS79328-Q1 Output Spectral Noise Density vs Frequency

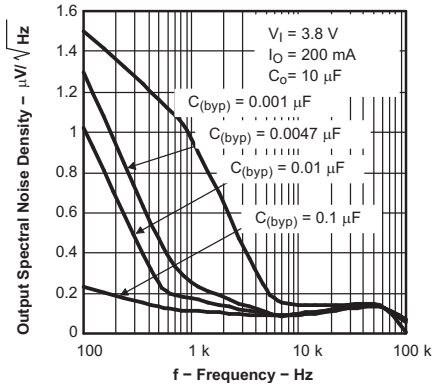


Figure 6. TPS79328-Q1 Output Spectral Noise Density vs Frequency

Typical Characteristics (continued)

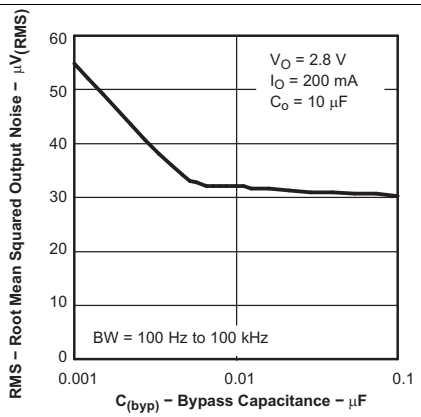


Figure 7. Root Mean Squared Output Noise vs Bypass Capacitance

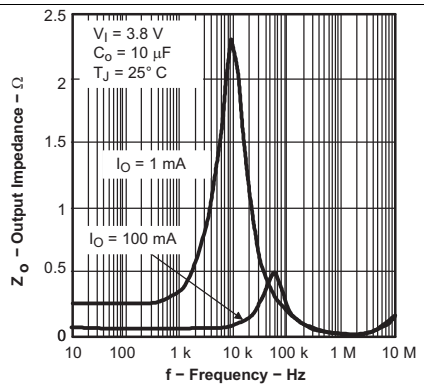


Figure 8. Output Impedance vs Frequency

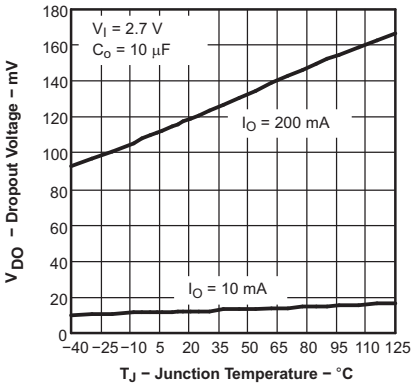


Figure 9. TPS79328-Q1 Dropout Voltage vs Junction Temperature

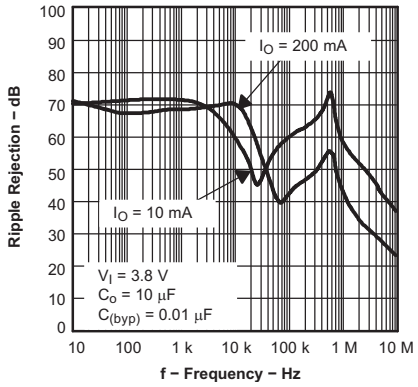


Figure 10. TPS79328-Q1 Ripple Rejection vs Frequency

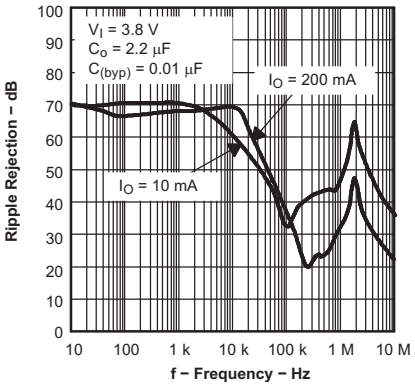


Figure 11. TPS79328-Q1 Ripple Rejection vs Frequency

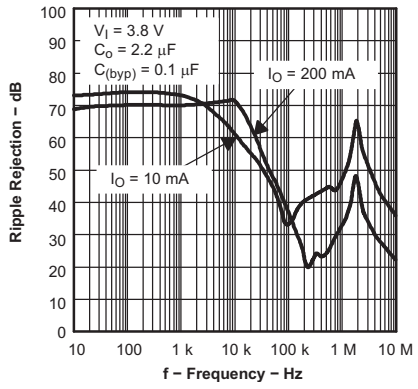


Figure 12. TPS79328-Q1 Ripple Rejection vs Frequency

Typical Characteristics (continued)

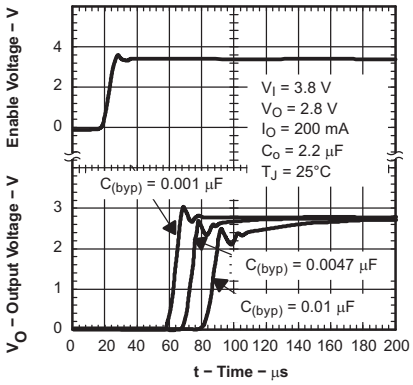


Figure 13. TPS79328-Q1 Output Voltage and Enable Voltage vs Time (Start-Up)

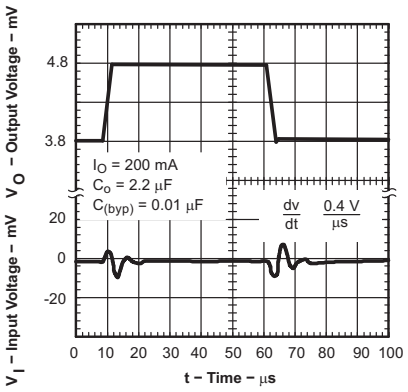


Figure 14. TPS79328-Q1 Line Transient Response

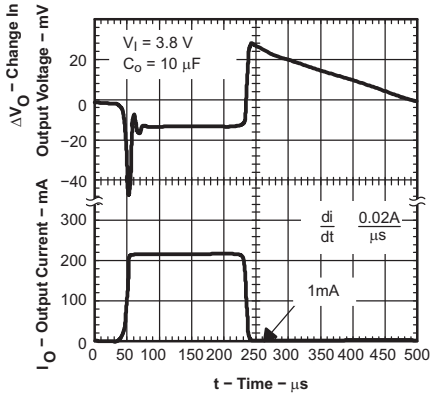


Figure 15. TPS79328-Q1 Load Transient Response

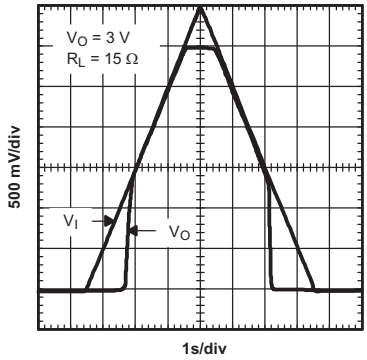


Figure 16. Power Up and Power Down

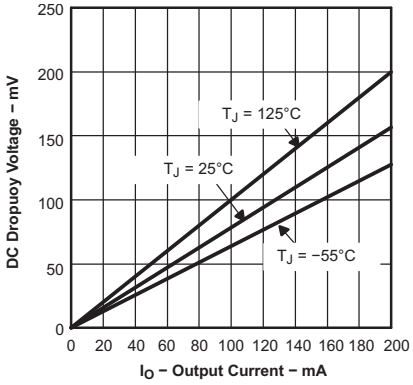


Figure 17. Dropout Voltage vs Output Current

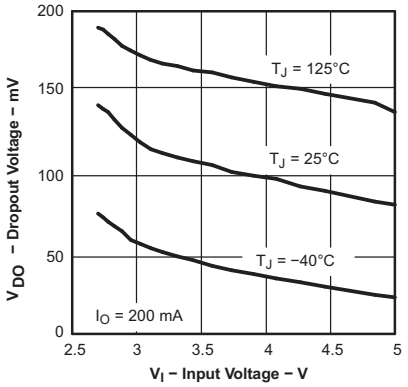


Figure 18. TPS79301-Q1 Dropout Voltage vs Input Voltage

Typical Characteristics (continued)

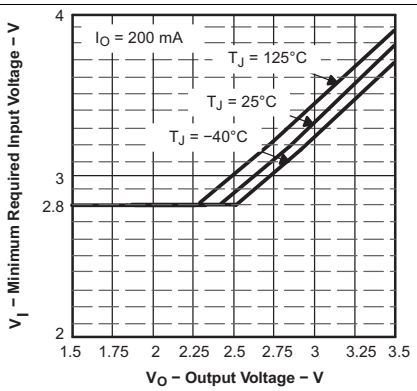


Figure 19. Minimum Required Input Voltage vs Output Voltage

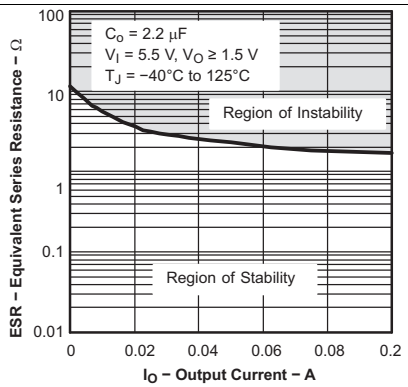


Figure 20. Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

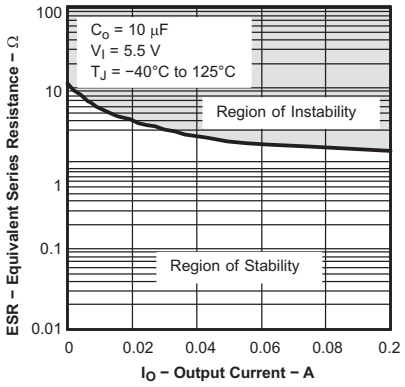


Figure 21. Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

8 Detailed Description

8.1 Overview

The TPS793xx-Q1 family of LDO regulators has been optimized for use in noise-sensitive battery-operated equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current (170 µA typically), and enable-input to reduce supply currents to less than 1 µA when the regulator is turned off.

8.2 Functional Block Diagram

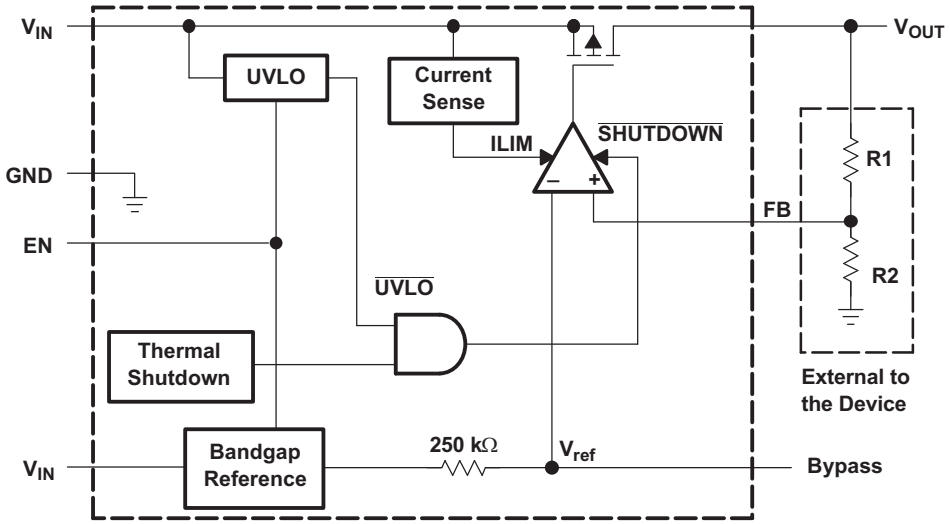


Figure 22. Functional Block Diagram – Adjustable Version

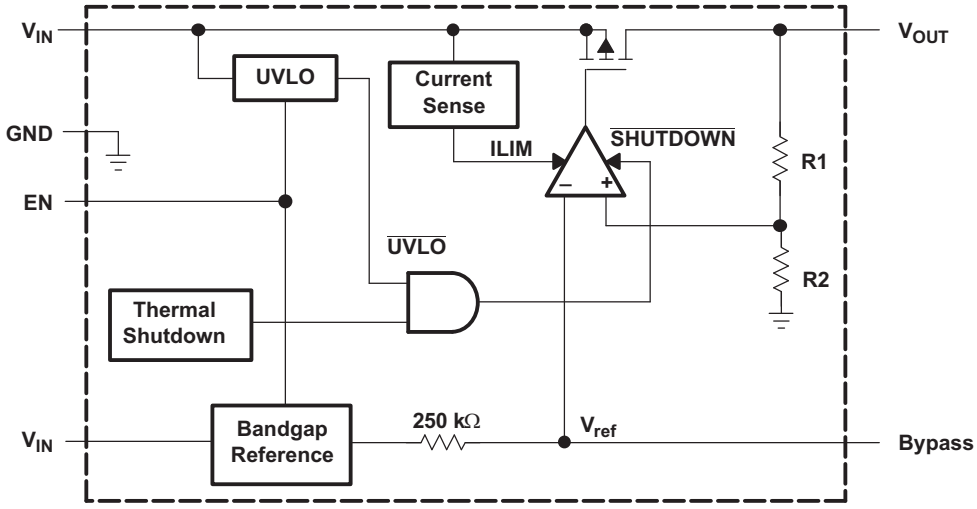


Figure 23. Functional Block Diagram – Fixed Version

8.3 Feature Description

8.3.1 Undervoltage Lockout (UVLO)

The TPS793xx-Q1 uses an undervoltage lockout (UVLO) circuit that disables the output until the input voltage is greater than the rising UVLO voltage. This circuit ensures that the device does not exhibit any unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry, $V_{IN(min)}$.

8.3.2 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed $V_{EN(high)}$ (2 V minimum). Turn off the device by forcing the EN pin to drop below 0.7 V. If shutdown capability is not required, connect EN to IN.

8.3.3 Foldback Current Limit

The TPS793xx-Q1 features internal current limiting and thermal protection. During normal operation, the TPS793xx-Q1 limits output current to approximately 400 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package or the absolute maximum voltage ratings of the device.

8.3.4 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the device from damage as a result of overheating. Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature must be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The TPS793xx-Q1 internal protection circuitry is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TPS793xx-Q1 into thermal shutdown degrades device reliability.

8.3.5 Reverse Current Operation

The TPS793xx-Q1 PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

8.3.6 Regulator Protection

The TPS793xx-Q1 features internal current limiting and thermal protection. During normal operation, the TPS793xx-Q1 limits output current to approximately 400 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package or the absolute maximum voltage ratings of the device. If the temperature of the device exceeds approximately 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately 140°C, regulator operation resumes.

The TPS793xx-Q1 PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

8.4 Device Functional Modes

8.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as $V_{IN(min)}$.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage is greater than $V_{EN(min)}$.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

8.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in the linear region and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

8.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.
- The input voltage is less than $UVLO_{falling}$.

Table 1 lists the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(high)}$	$I_{OUT} < I_{LIM}$	$T_J < 125°C$
Dropout mode	$V_{IN(min)} < VIN < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(high)}$	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	$V_{IN} < UVLO_{falling}$	$V_{EN} < V_{EN(low)}$	—	$T_J > 165°C$ (1)

(1) Approximate value for thermal shutdown

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS793xx-Q1 family of low-dropout (LDO) regulators has been optimized for use in noise-sensitive battery-operated equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current (170 µA typically), and enable-input to reduce supply currents to less than 1 µA when the regulator is turned off.

9.2 Typical Application

A typical application circuit is shown in Figure 24.

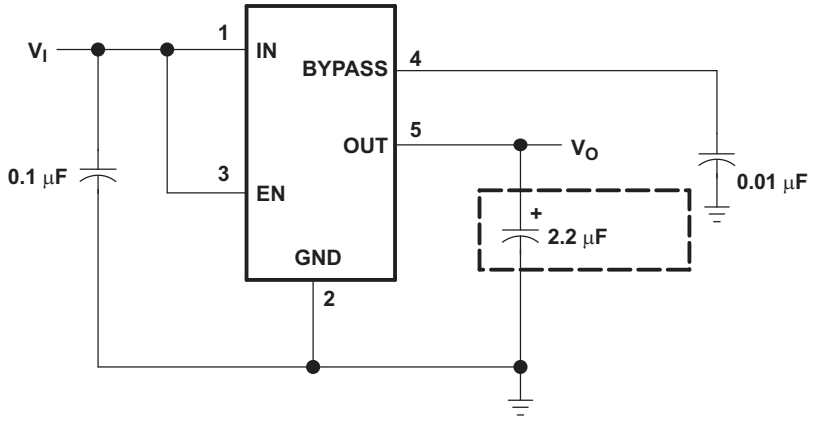


Figure 24. Typical Application Circuit

9.2.1 Design Requirements

Table 2 lists the design requirements.

Table 2. Design Parameters

PARAMETER	DESIGN REQUIREMENTS
Input voltage	3 V – 4 V (Lithium Ion battery)
Output voltage	2.8 V
DC output current	10 mA
Peak output current	75 mA
Maximum ambient temperature	65°C

9.2.2 Detailed Design Procedure

9.2.2.1 External Capacitor Requirements

A 0.1-µF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS793xx-Q1, is required for stability and improves transient response, noise rejection, and ripple rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like all LDOs, the TPS793xx-Q1 requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 2.2-µF. Any 2.2-µF or larger ceramic capacitor is suitable, provided the capacitance does not vary significantly over temperature.

The internal voltage reference is a key source of noise in an LDO regulator. The TPS793xx-Q1 has a BYPASS pin that is connected to the voltage reference through a 250-kΩ internal resistor. The 250-kΩ internal resistor, in conjunction with an external bypass capacitor connected to the BYPASS pin, creates a low pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. For the regulator to operate properly, the current flow out of the BYPASS pin must be at a minimum, because any leakage current creates an IR drop across the internal resistor, thus, creating an output error. Therefore, the bypass capacitor must have minimal leakage current.

For example, the TPS79328-Q1 exhibits only 32 μV_{RMS} of output voltage noise using a 0.1-µF ceramic bypass capacitor and a 2.2-µF ceramic output capacitor. Note that the output starts up slower as the bypass capacitance increases due to the RC time constant at the BYPASS pin that is created by the internal 250-kΩ resistor and external capacitor.

9.2.2.2 Programming the TPS79301-Q1 Adjustable LDO Regulator

The output voltage of the TPS79301-Q1 adjustable regulator is programmed using an external resistor divider as shown in Figure 25. The output voltage is calculated using Equation 1.

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right)$$

where V_{ref} = 1.2246 V typical (the internal reference voltage) (1)

Resistors R1 and R2 should be chosen for approximately 50-µA divider current. Lower-value resistors can be used for improved noise performance, but the solution consumes more power. Higher resistor values should be avoided as leakage current into/out of FB across R1/R2 creates an offset voltage that artificially increases/decreases the feedback voltage and, thus, erroneously decreases or increases V_O. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at 50 µA, C1 = 15 pF for stability, and then calculate R1 using Equation 2.

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \quad (2)$$

To improve the stability of the adjustable version, TI suggests placing a small compensation capacitor between OUT and FB. For voltages <1.8 V, the value of this capacitor should be 100 pF. For voltages >1.8 V, the approximate value of this capacitor can be calculated using Equation 3.

$$C1 = \frac{(3 \times 10^{-7}) \times (R1 + R2)}{(R1 \times R2)} \quad (3)$$

The suggested value of this capacitor for several resistor ratios is shown in the table in Table 3. If this capacitor is not used (such as in a unity-gain configuration) or if an output voltage <1.8 V is chosen, then the minimum recommended output capacitor is 4.7 µF instead of 2.2 µF.

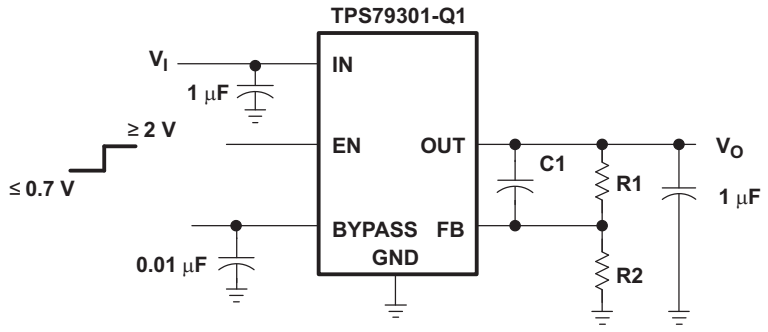


Figure 25. TPS79301-Q1 Adjustable LDO Regulator Programming

Table 3. Output Voltage Programming Guide

OUTPUT VOLTAGE	R1	R2	C1
2.5 V	31.6 kΩ	30.1 kΩ	22 pF
3.3 V	51 kΩ	30.1 kΩ	15 pF
3.6 V	59 kΩ	30.1 kΩ	15 pF

9.2.3 Application Curves

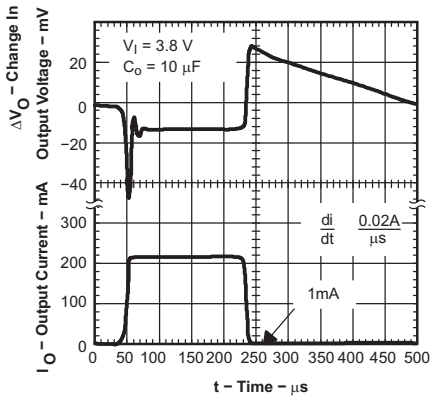


Figure 26. TPS79328-Q1 Load Transient Response

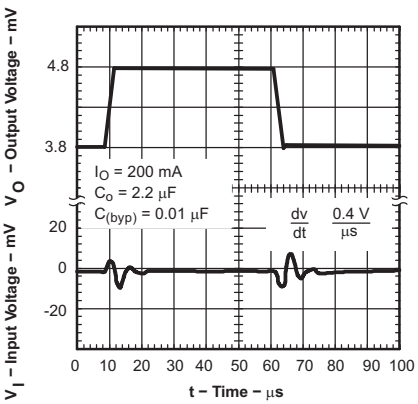


Figure 27. TPS79328-Q1 Line Transient Response

10 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range from 2.7 V to 5.5 V. The input voltage range must provide adequate headroom in order for the device to have a regulated output. This input supply must be well-regulated and stable. A 0.1-µF input capacitor is required for stability; if the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

11 Layout

11.1 Layout Guidelines

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, the IN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with an X5R or X7R dielectric.

Equivalent series inductance (ESL) and equivalent series resistance (ESR) must be minimized to maximize performance and ensure stability. Every capacitor (C_{IN}, C_{OUT}, $C_{NR/SS}$, C_{FF}) must be placed as close as possible to the device and on the same side of the PCB as the regulator itself. Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because these circuits may impact system performance negatively, and even cause instability

11.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve AC measurements like PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for VIN and VOUT, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

11.2 Layout Example

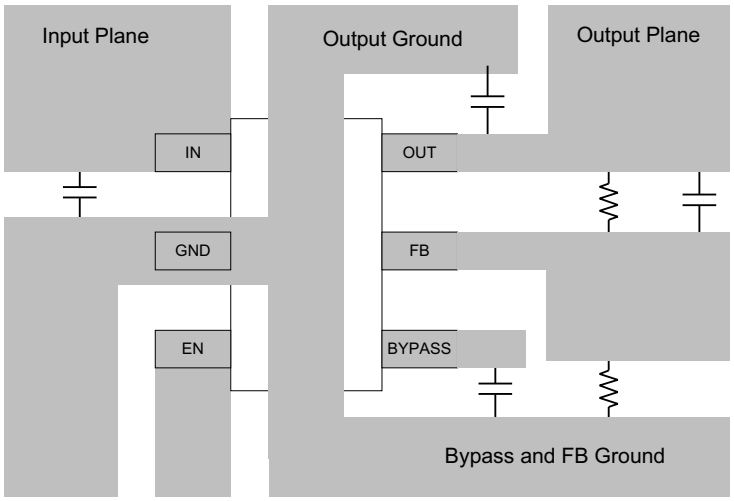


Figure 28. Layout Example (DBV Package)

11.3 Power Dissipation and Junction Temperature

Specified regulator operation is ensured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

Power Dissipation and Junction Temperature (continued)

The maximum power dissipation limit is determined using Equation 4.

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}}$$

Where

- $T_J$max = Maximum allowable junction temperature
- $R_{\theta JA}$ = Thermal resistance, junction to ambient, for the package, see the *Thermal Information* table
- T_A = Ambient temperature (4)

The regulator dissipation is calculated using Equation 5.

$$P_D = (V_I - V_O) \times I_O \quad (5)$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 Evaluation Modules

Seven evaluation modules (EVMs) are available to assist in the initial circuit performance evaluation using the TPS793xx-Q1:

- TPS79301EVM
- TPS793285YEQEVM
- TPS79328EVM

These EVMs can be requested at the Texas Instruments website through the device product folders or purchased directly from the TI eStore.

12.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS793 is available through the product folders under *Tools & Software*.

12.1.2 Device Nomenclature

Table 4. Ordering Information

PRODUCT	V_{OUT}
TPS793**xxyyyz**	**XX(X)** is the nominal output voltage (for example, 28 = 2.8 V; 285 = 2.85 V; 01 = adjustable version). **YYY** is the package designator. **Z** is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces).

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Application note, *Using New Thermal Metrics*, SBVA025
- Application note, *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator*, SBVA042
- *TPS79301EVM, TPS79328EVM LDO Linear Regulator Evaluation Module User's Guide*, SLVU060

12.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
Bluetooth is a trademark of Bluetooth SIG, Inc.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS79301DBVRG4Q1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGV1	Samples
TPS79301DBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGV1	Samples
TPS79318DBVRG4Q1	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 125	PHH1	
TPS79318DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHH1	Samples
TPS79325DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGW1	Samples
TPS79328QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGX1	Samples
TPS79330QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGY1	Samples
TPS79333DBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHU1	Samples
TPS79333DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHU1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS793-Q1 :

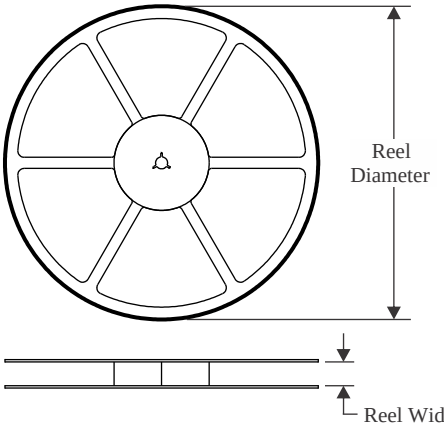
- Catalog : TPS793

NOTE: Qualified Version Definitions:

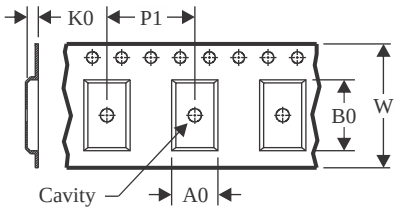
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

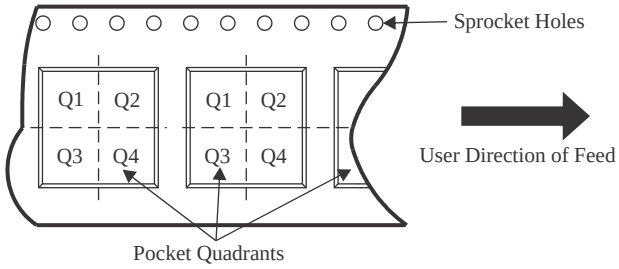


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

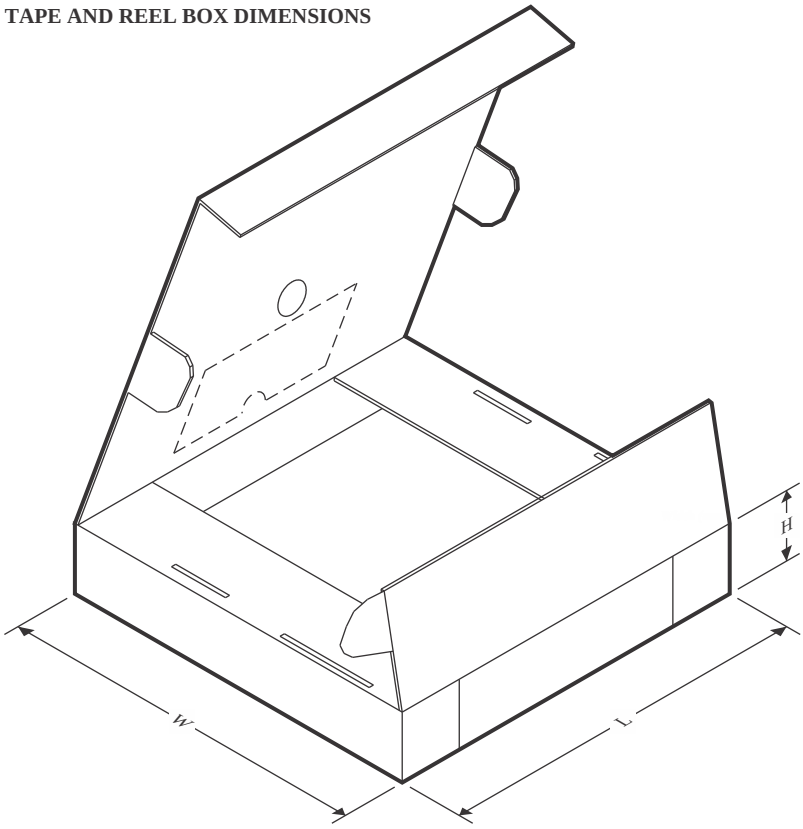
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79301DBVRG4Q1	SOT-23	DBV	6	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS79301DBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS79318DBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS79325DBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS79328QDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79330QDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79333DBVRG4Q1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79333DBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

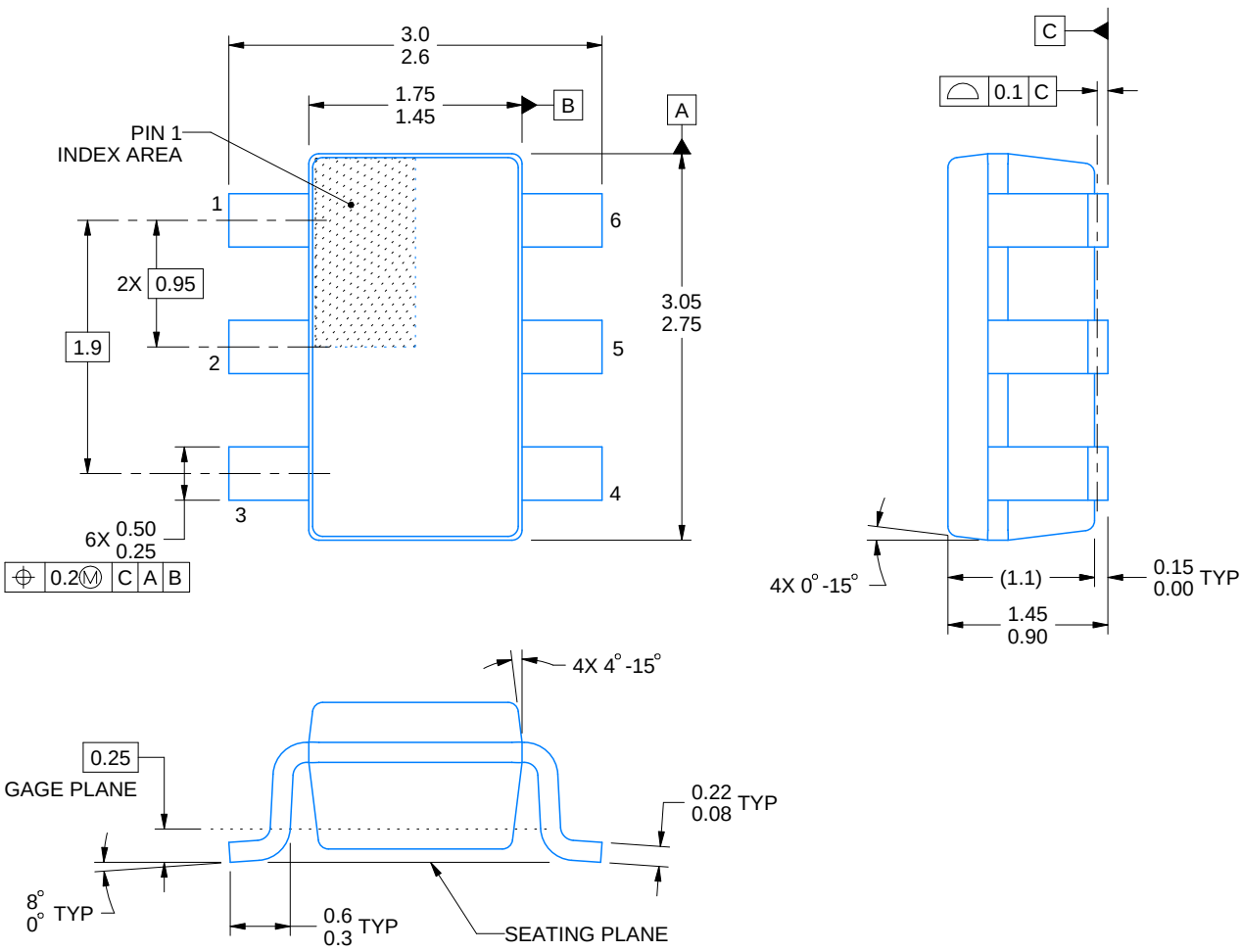
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79301DBVRG4Q1	SOT-23	DBV	6	3000	445.0	220.0	345.0
TPS79301DBVRQ1	SOT-23	DBV	6	3000	445.0	220.0	345.0
TPS79318DBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS79325DBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS79328QDBVRQ1	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS79330QDBVRQ1	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS79333DBVRG4Q1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS79333DBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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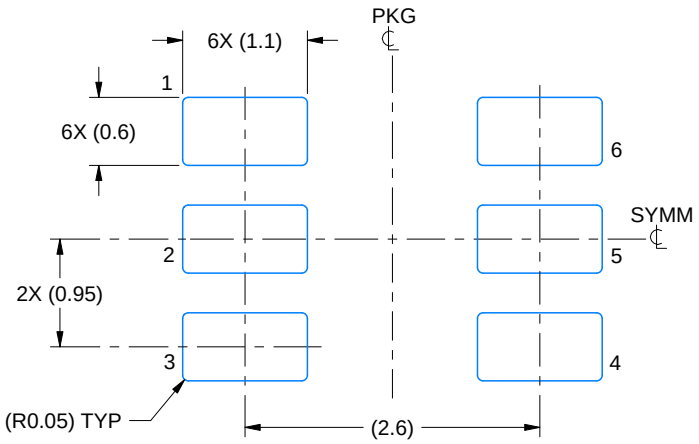
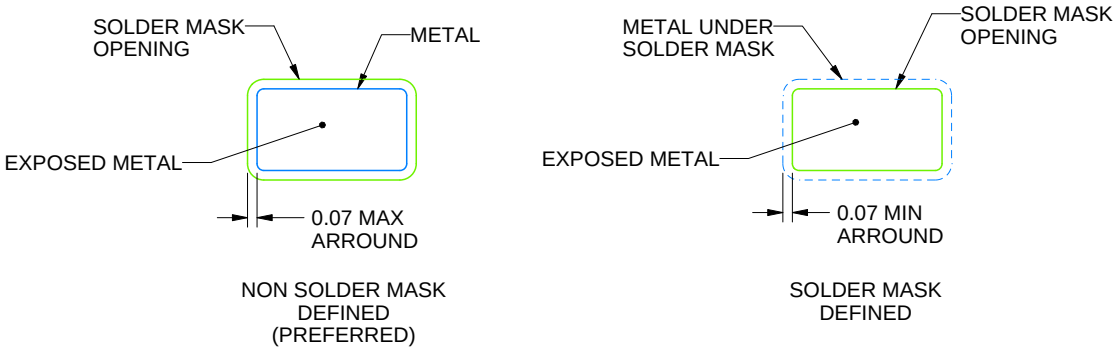
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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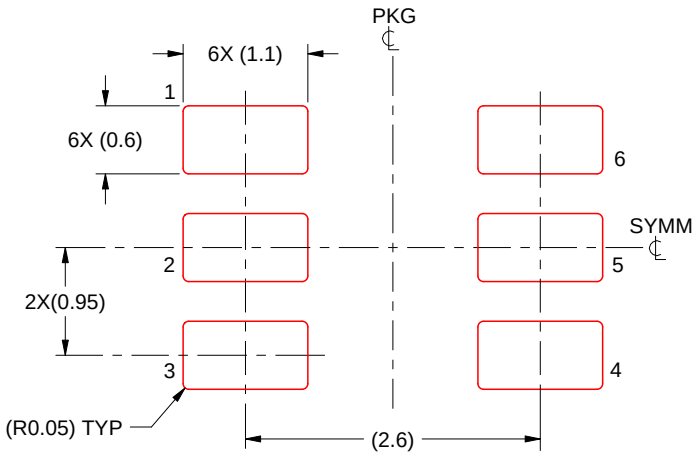
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

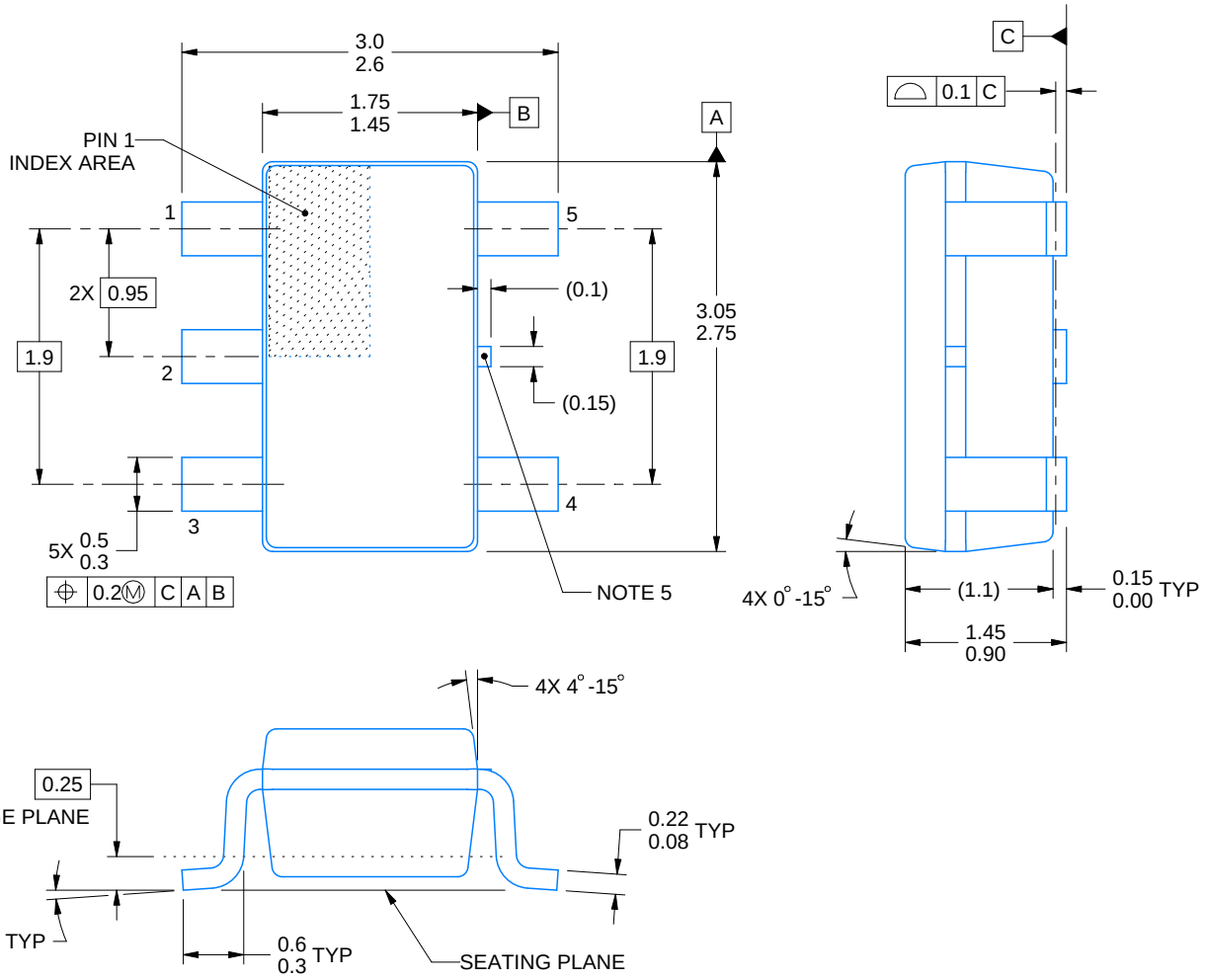
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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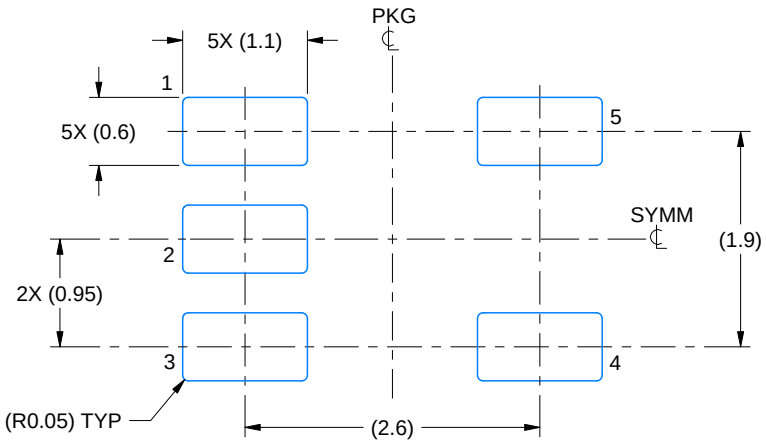
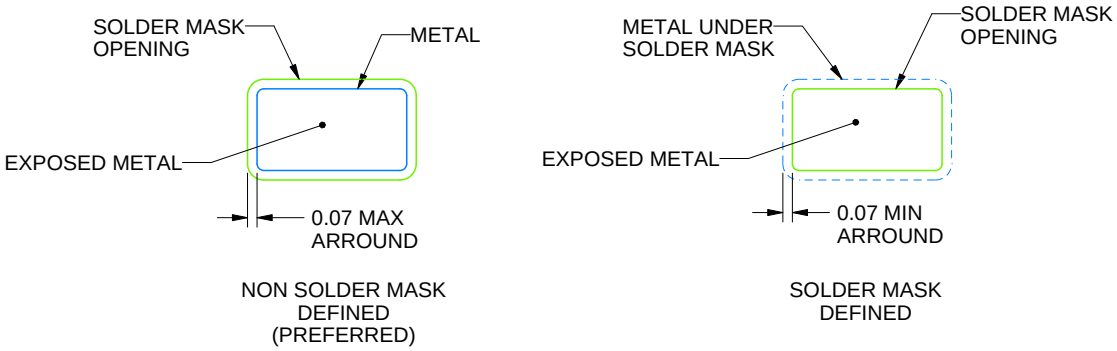
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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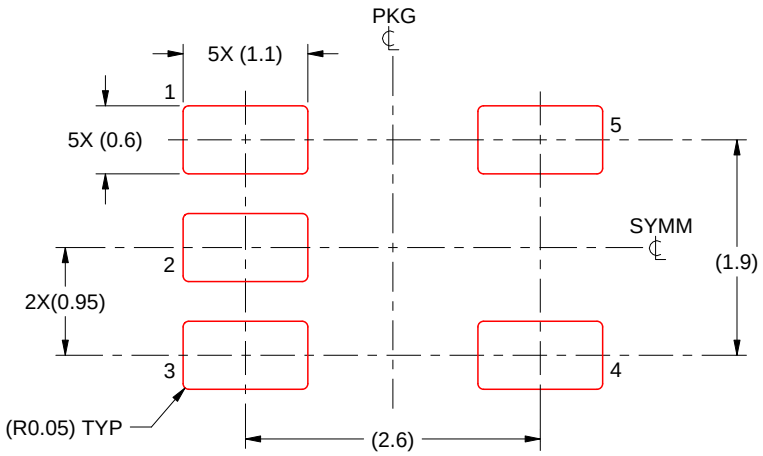
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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