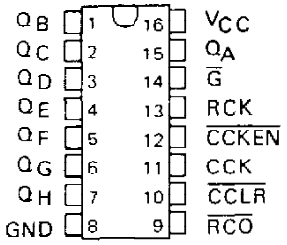
SN54LS590, SN54LS591, SN74LS590, SN74LS591
8-BIT BINARY COUNTERS WITH OUTPUT REGISTERS

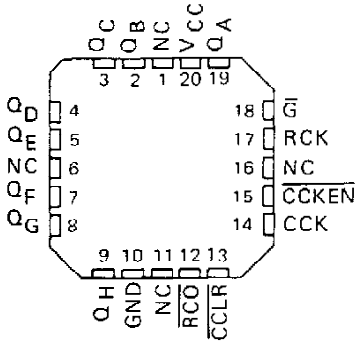
SDLS003 D2632, JANUARY 1981 – REVISED MARCH 1988

- 8-Bit Counter with Register
- Parallel Register Outputs
- Choice of 3-State ('LS590) or Open-Collector ('LS591) Register Outputs
- Guaranteed Counter Frequency: DC to 20 MHz

SN54LS590, SN54LS591 . . . J OR W PACKAGE
SN74LS590, SN74LS591 . . . N PACKAGE
(TOP VIEW)



SN54LS590, SN54LS591 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

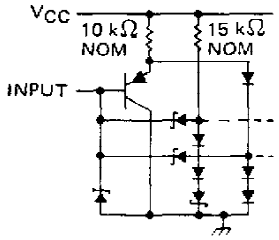
description

These devices each contain an 8-bit binary counter that feeds an 8 bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register. The binary counter features a direct clear input $\overline{CCLR}$ and a count enable input $\overline{CCKEN}$. For cascading, a ripple carry output $\overline{RCO}$ is provided. Expansion is easily accomplished for two stages by connecting $\overline{RCO}$ of the first stage to $\overline{CCKEN}$ of the second stage. Cascading for larger count chains can be accomplished by connecting $\overline{RCO}$ of each stage to CCK of the following stage.

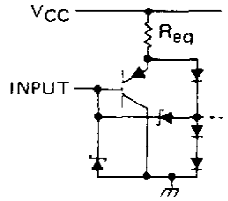
Both the counter and register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the counter state will always be one count ahead of the register. Internal circuitry prevents clocking from the clock enable.

schematics of inputs and outputs

EQUIVALENT OF CCK INPUT

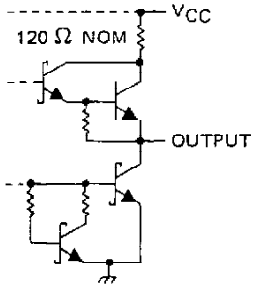


EQUIVALENT OF ALL OTHER INPUTS

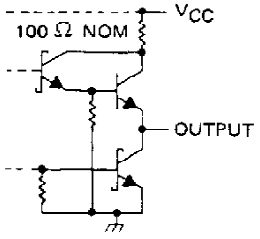


RCK: R_{eq} = 10 kΩ NOM
ALL OTHER: R_{eq} = 13 kΩ NOM

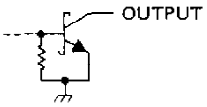
$\overline{RCO}$ OUTPUT



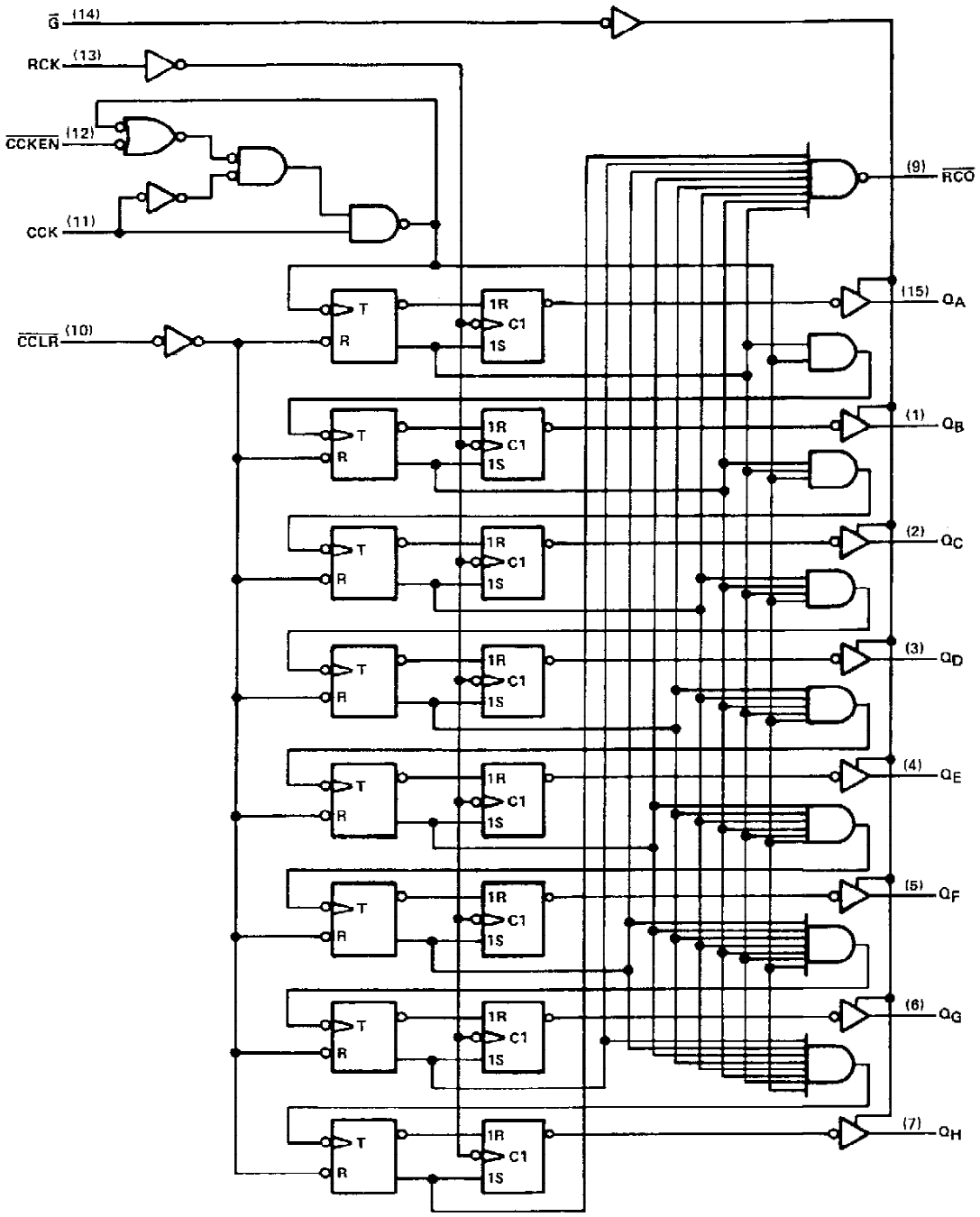
TYPICAL OF Q OUTPUTS ('LS590)



TYPICAL OF Q OUTPUTS ('LS591)

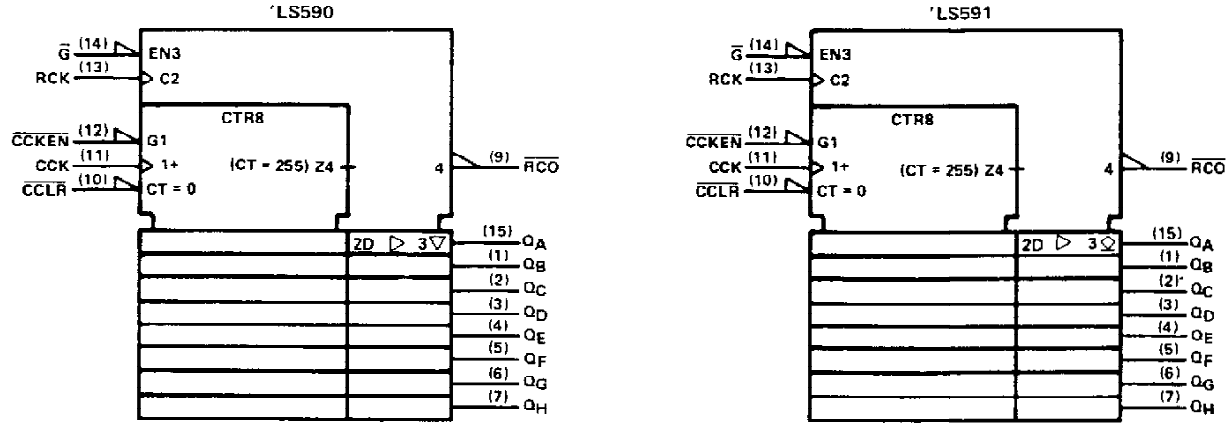


logic diagram (positive logic)



Pin numbers shown are for J, N and W packages.

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for J, N, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS590, SN54LS591 . . . . . −55°C to 125°C
SN74LS590, SN74LS591 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

			SN54LS'			SN74LS'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
V_{OH}	High-level output voltage	Q, 'LS591 only			5.5			5.5	V
I_{OH}	High-level output current	$\overline{RCO}$			−1			−1	mA
		Q, 'LS590 only			−1			−2.6	
I_{OL}	Low-level output current	$\overline{RCO}$			8			16	mA
		Q			12			24	
f_{CCK}	Counter clock frequency		0		20	0		20	MHz
f_{RCK}	Register clock frequency		0		25	0		25	MHz
$t_{w(CCK)}$	Duration of counter clock pulse		25			25			ns
$t_{w(\overline{CCLR})}$	Duration of counter clear pulse		20			20			ns
$t_{w(RCK)}$	Duration of register clock pulse		20			20			ns
t_{su}	Setup time	$\overline{CCKEN}$ low before CCK↑	20			20			ns
		$\overline{CCLR}$ inactive before CCK↑	20			20			
		CCK before RCK↑ (see Note 2)	40			40			
t_h	Hold time	$\overline{CCKEN}$ low after CCK↑	0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

NOTE 2: This setup time ensures the register will see stable data from the counter outputs. The clocks may be tied together in which case the register state will be one clock pulse behind the counter.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			SN54LS'			SN74LS'			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}			V_{CC} = MIN, I_I = −18 mA					−1.5			−1.5	V
V_{OH}	'LS590 Q		V_{CC} = MIN, V_{IH} = 2V, V_{IL} = MAX	I_{OH} = −1 mA		2.4	3.2					V
				I_{OH} = −2.6 mA					2.4	3.1		
	$\overline{RCO}$			I_{OH} = −1 mA		2.4	3.2		2.4	3.2		
I_{OH}	'LS591 Q		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	V_{OH} = 5.5 V,				0.1			0.1	mA
V_{OL}	Q		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OL} = 12 mA			0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA						0.35	0.5	
	$\overline{RCO}$			I_{OL} = 8 mA			0.25	0.4		0.25	0.4	
				I_{OL} = 16 mA						0.35	0.5	
I_{OZH}	'LS590 Q		V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.7 V	V_{IL} = MAX,				20			20	μA
I_{OZL}	'LS590 Q		V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.4 V	V_{IL} = MAX,				−20			−20	μA
I_I			V_{CC} = MAX, V_I = 7 V					0.1			0.1	mA
I_{IH}			V_{CC} = MAX, V_I = 2.7 V					20			20	μA
I_{IL}	CCK		V_{CC} = MAX, V_I = 0.4 V					−0.8			−0.8	mA
	All others							−0.2			−0.2	
I_{OS}§	'LS590 Q		V_{CC} = MAX, V_O = 0 V			−30		−130	−30		−130	mA
	$\overline{RCO}$					−20		−100	−20		−100	
I_{CC}	'LS590	I_{CCH}	V_{CC} = MAX, All possible inputs grounded, All outputs open				33	55		33	55	mA
		I_{CCL}					44	65		44	65	
		I_{CCZ}					46	65		46	65	
	'LS591	I_{CCH}					35	55		35	55	
		I_{CCL}					42	65		42	65	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C
§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		'LS590			'LS591			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	RCK	Q	R_L = 667 Ω,	C_L = 45 pF	20	35		20	35		MHz
t_{PLH}	CCK↑	$\overline{RCO}$	R_L = 1 kΩ,	C_L = 30 pF		14	22		16	24	ns
t_{PHL}	CCK↑	$\overline{RCO}$				20	30		25	38	ns
t_{PLH}	$\overline{CCLR}$↓	$\overline{RCO}$				30	45		32	48	ns
t_{PLH}	RCK↑	Q	R_L = 667 Ω,	C_L = 45 pF		12	18		25	38	ns
t_{PHL}	RCK↑	Q				22	33		28	42	ns
t_{PZH}	$\overline{G}$↓	Q				25	38				ns
t_{PZL}	$\overline{G}$↓	Q				30	45				ns
t_{PHZ}	$\overline{G}$↑	Q	R_L = 667 Ω,	C_L = 5 pF		20	30				ns
t_{PLZ}	$\overline{G}$↑	Q				25	38				ns
t_{PLH}	$\overline{G}$↑	Q	R_L = 667 Ω,	C_L = 45 pF					34	50	ns
t_{PHL}	$\overline{G}$↓	Q							32	48	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-87517012A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-87517012A SNJ54LS590FK	Samples
5962-8751701EA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8751701EA SNJ54LS590J	Samples
5962-8751701EA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8751701EA SNJ54LS590J	Samples
SN54LS590J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS590J	Samples
SN54LS590J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS590J	Samples
SN74LS590D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS590	Samples
SN74LS590D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS590	Samples
SN74LS590N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS590N	Samples
SN74LS590N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS590N	Samples
SN74LS590NSR	ACTIVE	SOP	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS590	Samples
SN74LS590NSR	ACTIVE	SOP	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS590	Samples
SNJ54LS590FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-87517012A SNJ54LS590FK	Samples
SNJ54LS590FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-87517012A SNJ54LS590FK	Samples
SNJ54LS590J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8751701EA SNJ54LS590J	Samples
SNJ54LS590J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8751701EA SNJ54LS590J	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN54LS590, SN74LS590 :

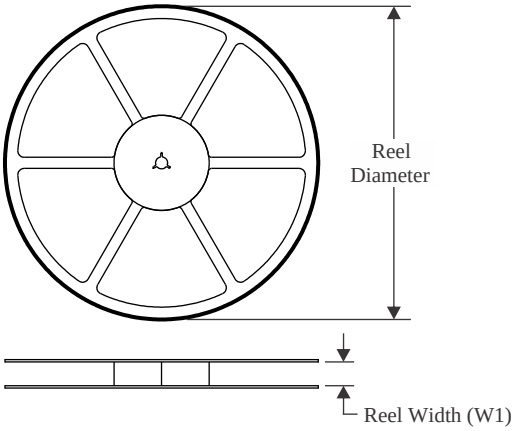
- Catalog : SN74LS590
- Military : SN54LS590

NOTE: Qualified Version Definitions:

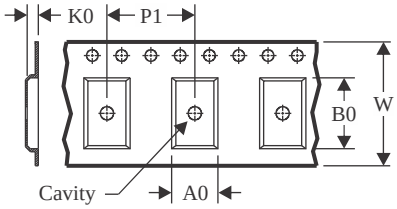
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

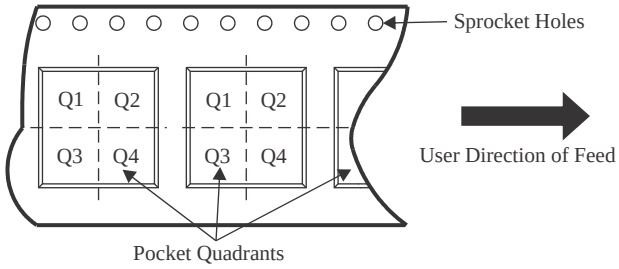


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

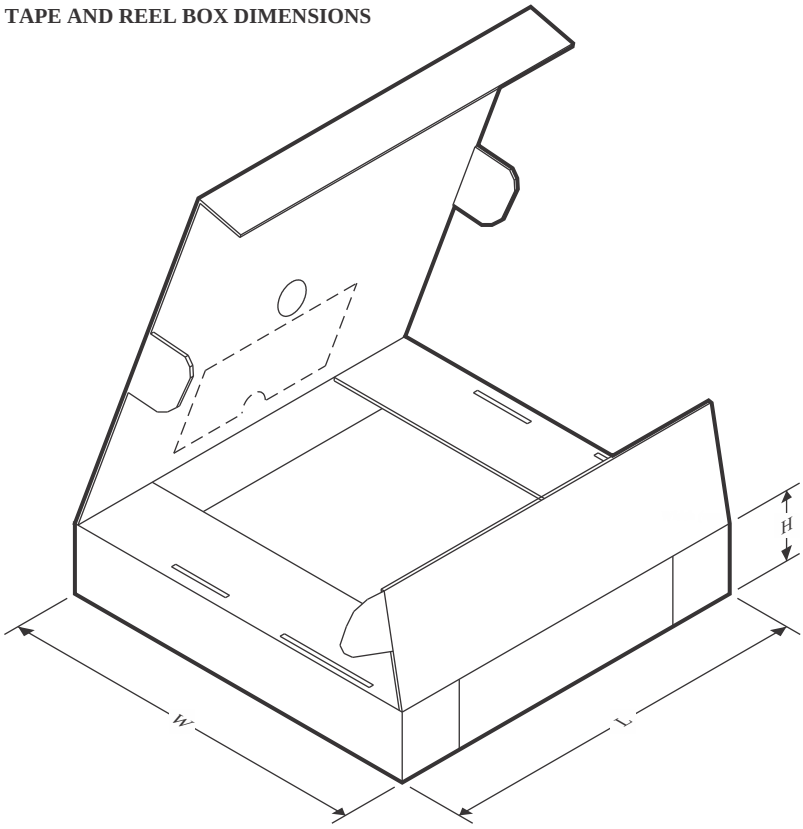
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS590NSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

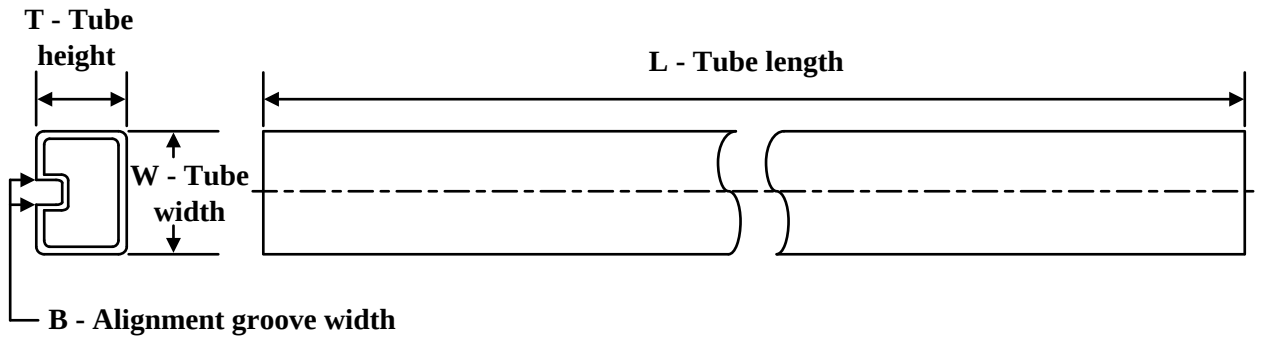
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS590NSR	SOP	NS	16	2000	356.0	356.0	35.0

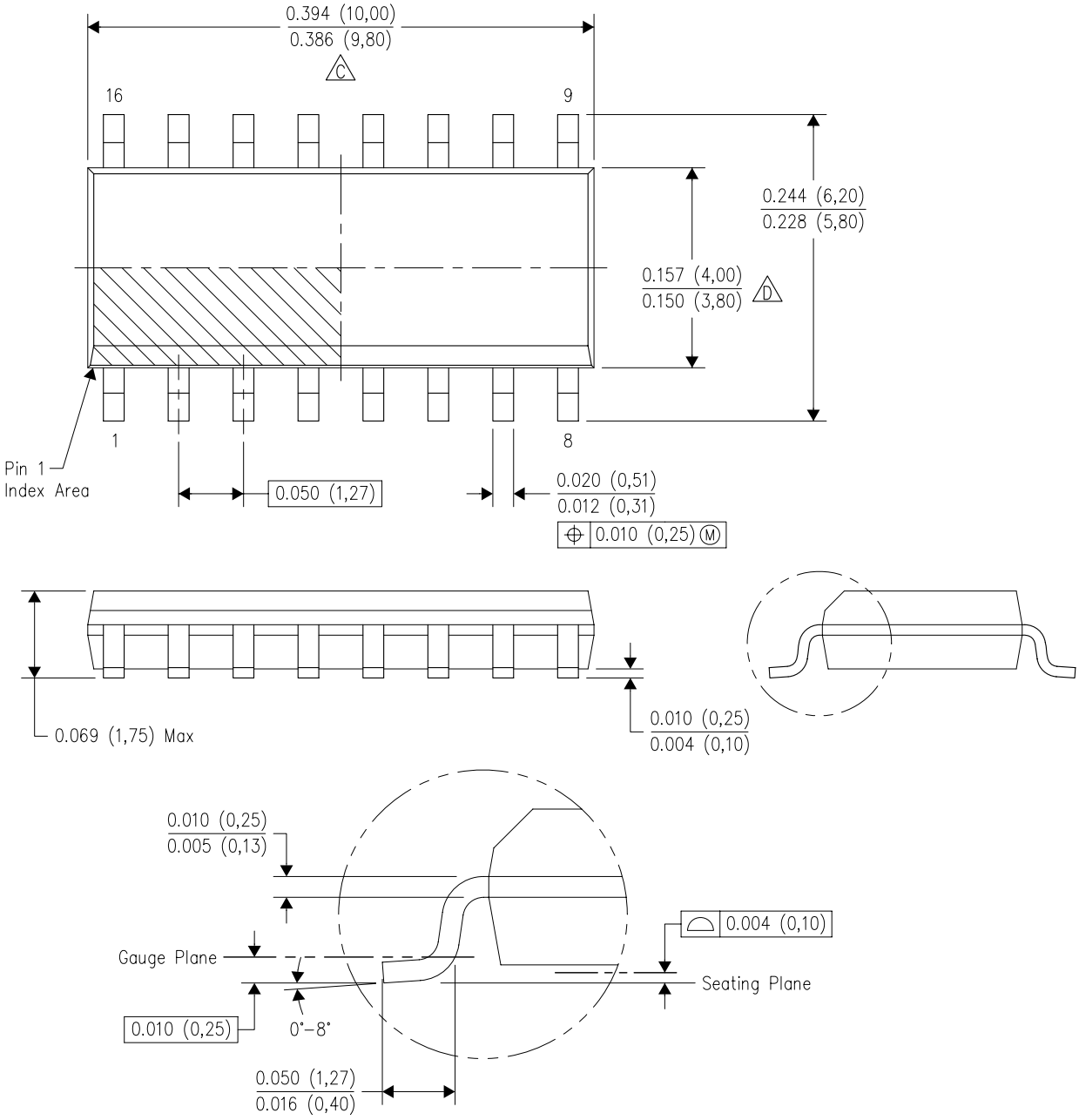
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-87517012A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74LS590D	D	SOIC	16	40	507	8	3940	4.32
SN74LS590N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS590N	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54LS590FK	FK	LCCC	20	55	506.98	12.06	2030	NA

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

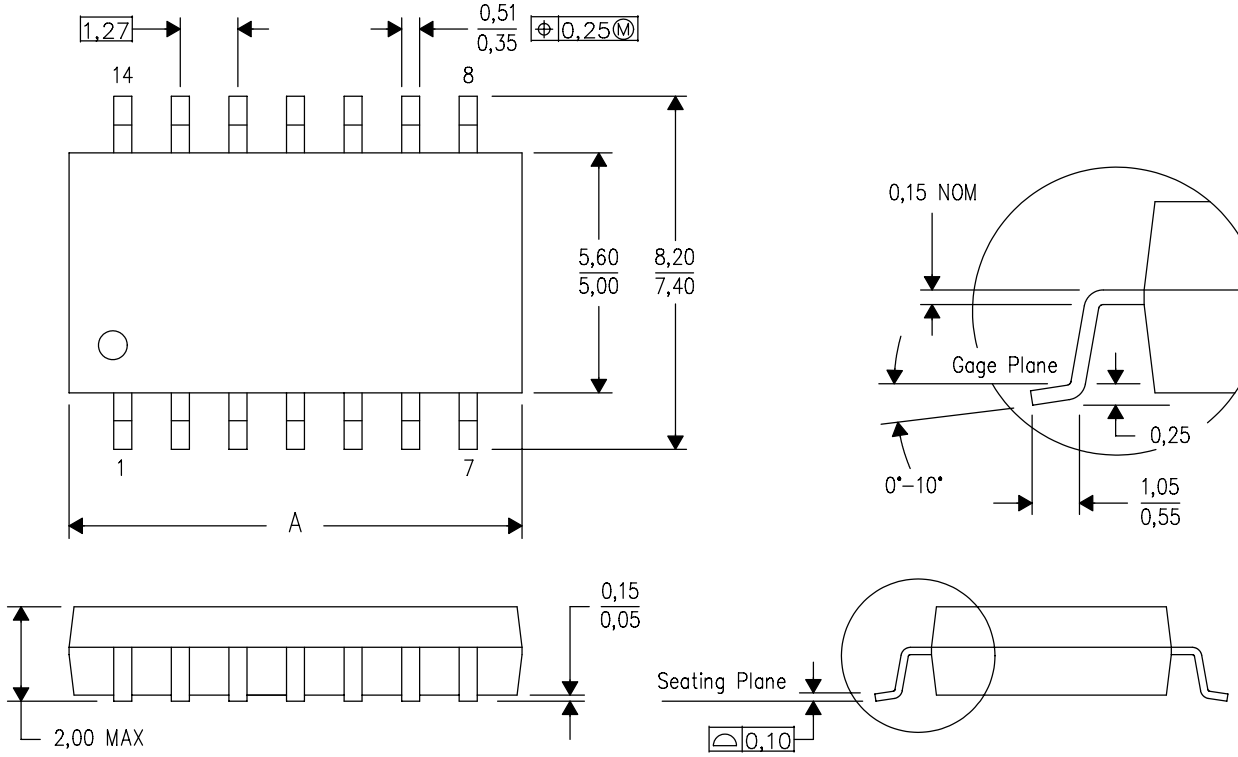


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

GENERIC PACKAGE VIEW

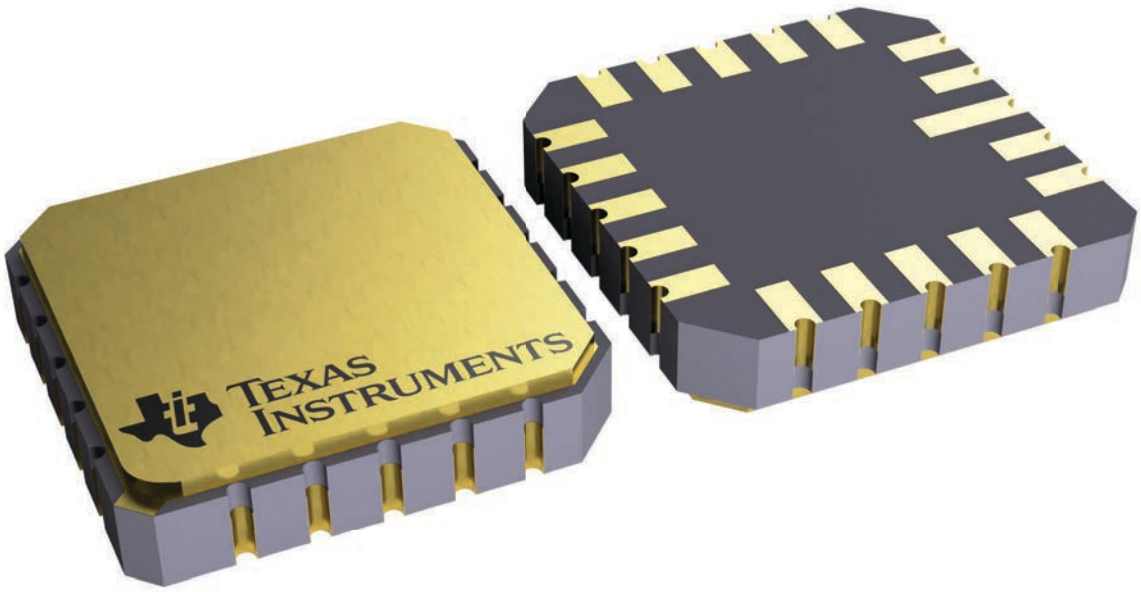
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

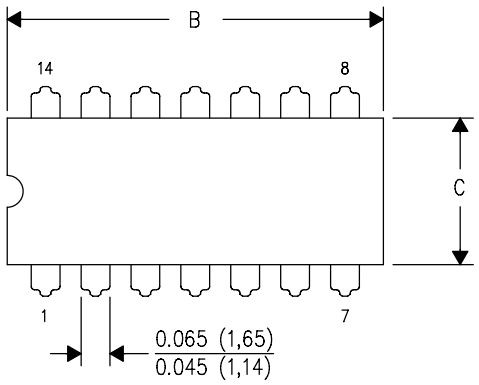


4229370VA\

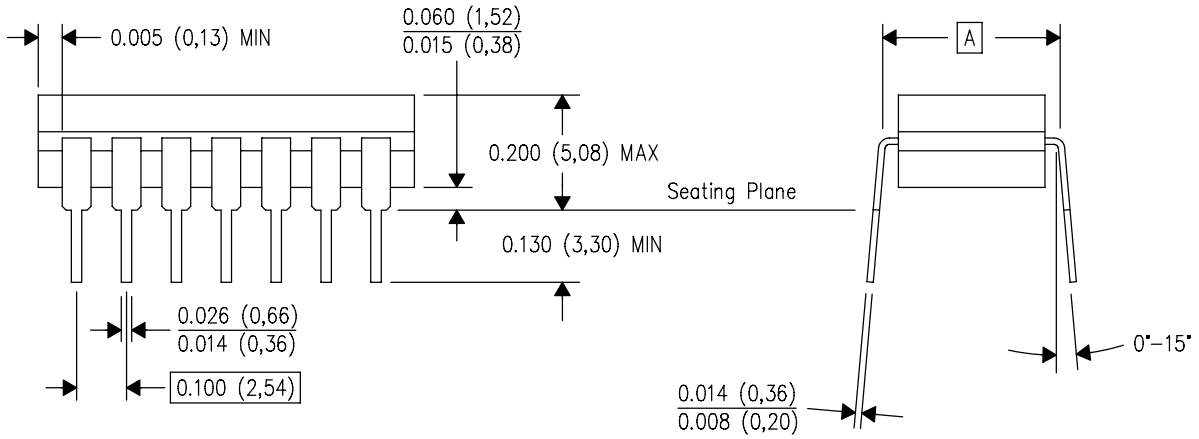
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



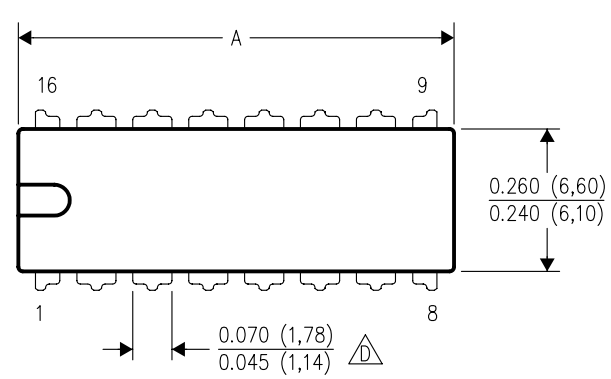
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

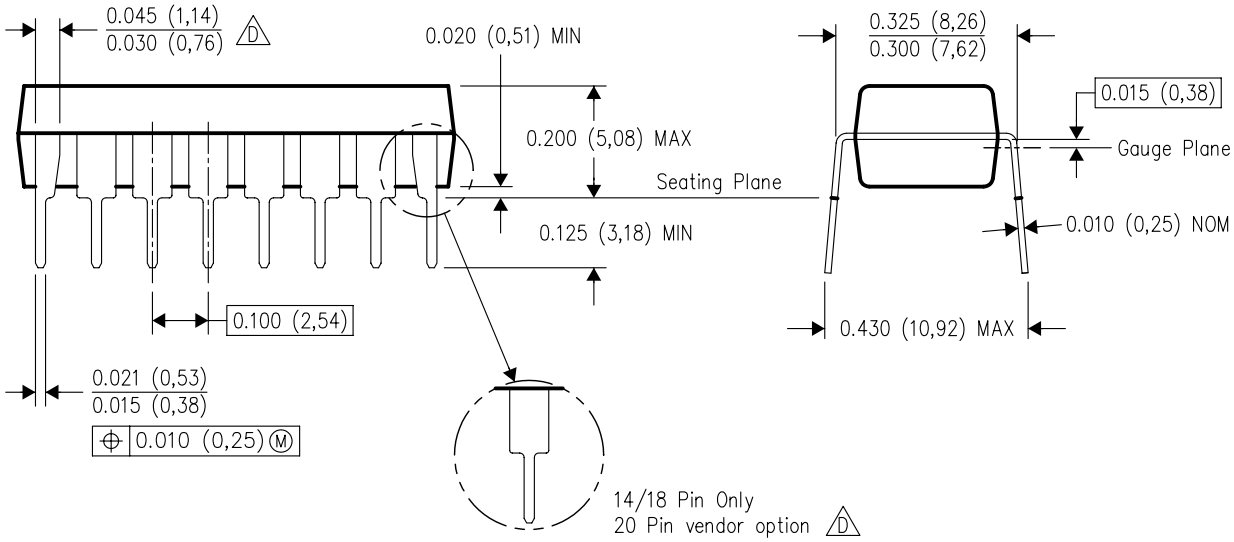
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

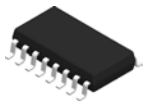


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

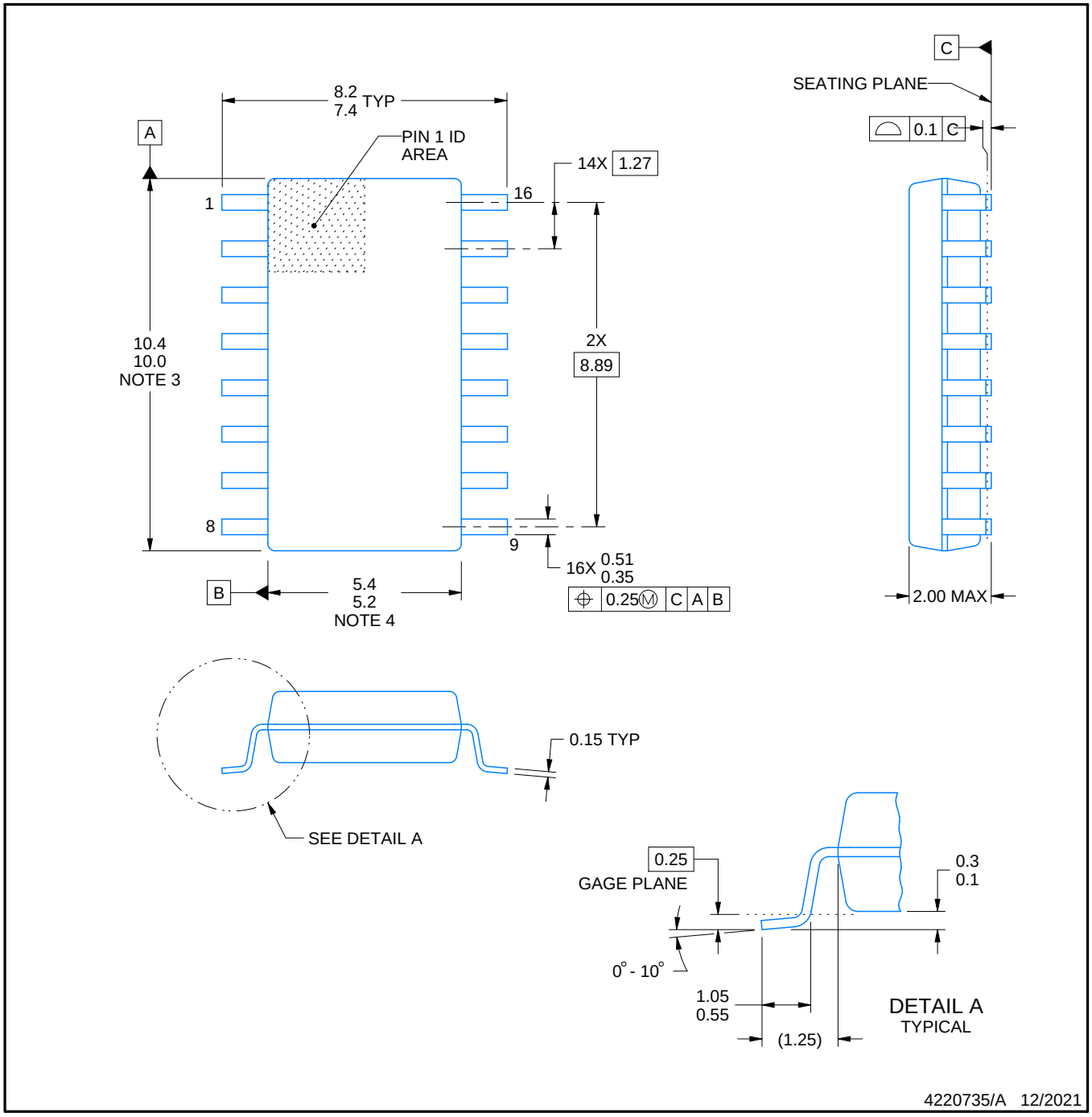


PACKAGE OUTLINE

NS0016A

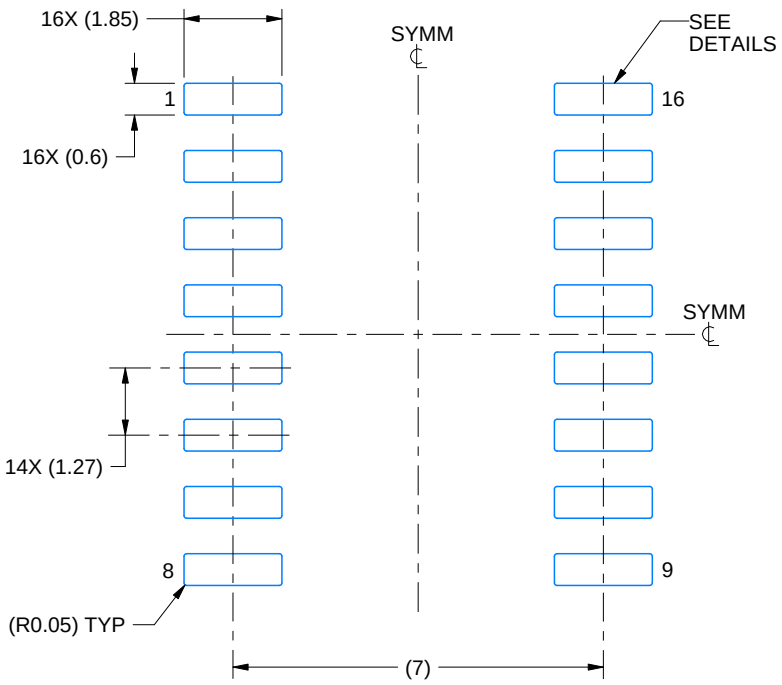
SOP - 2.00 mm max height

SOP

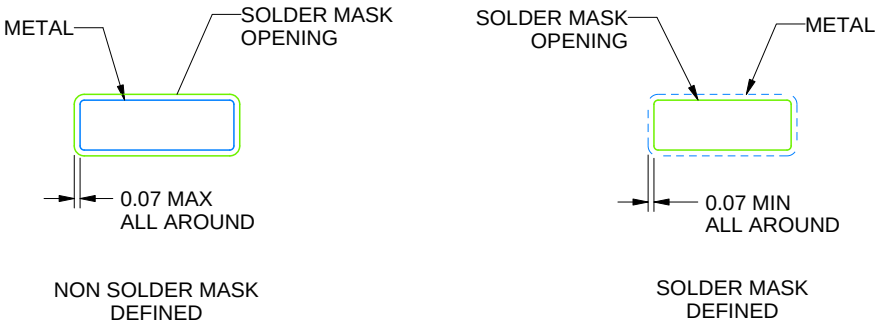


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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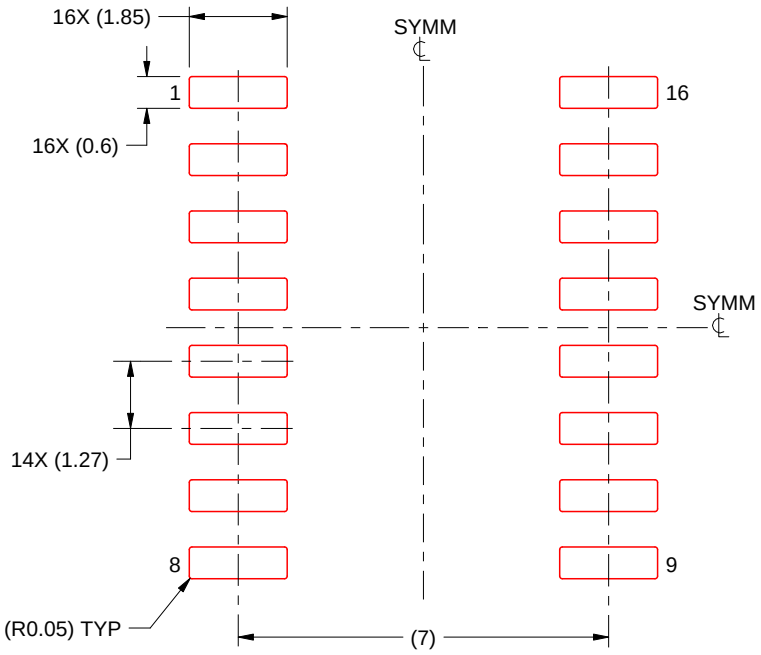
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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