# SN65HVD3x-EP 3.3V Full-Duplex RS-485 Drivers and Receivers

## 1 Features

- 1/8 Unit-load option available (up to 256 nodes on the bus)
- Bus-pin ESD protection exceeds 15kV HBM
- Optional driver output transition times for signaling rates[1] of 1Mbps, 5Mbps, and 25Mbps
- Low-current standby mode: <1µA
- Glitch-free power-up and power-down protection for hot-plugging applications
- 5V Tolerant inputs
- Bus idle, open, and short-circuit fail safe
- Driver current limiting and thermal shutdown
- Meet or exceed the requirements of ANSI TIA/EIA-485-A and RS-422 compatible

## 2 Applications

- Utility meters
- DTE and DCE interfaces
- Industrial, process, and building automation
- Point-of-Sale (POS) terminals and networks
- Controlled baseline
- One assembly and test site
- One fabrication site
- Available in military (–55°C/125°C) temperature range
- Extended product life cycle
- Extended product-change notification
- Product traceability

## 3 Description

The SN65HVD3x-EP devices are 3-state differential line drivers and differential-input line receivers that operate with 3V power supply.

Each driver and receiver has separate input and output pins for full-duplex bus communication designs. They are designed for balanced transmission lines and interoperation with ANSI TIA/EIA-485A, TIA/EIA-422-B, ITU-T v.11, and ISO 8482:1993 standard-compliant devices.

The SN65HVD30 is fully enabled with no external enabling pins.

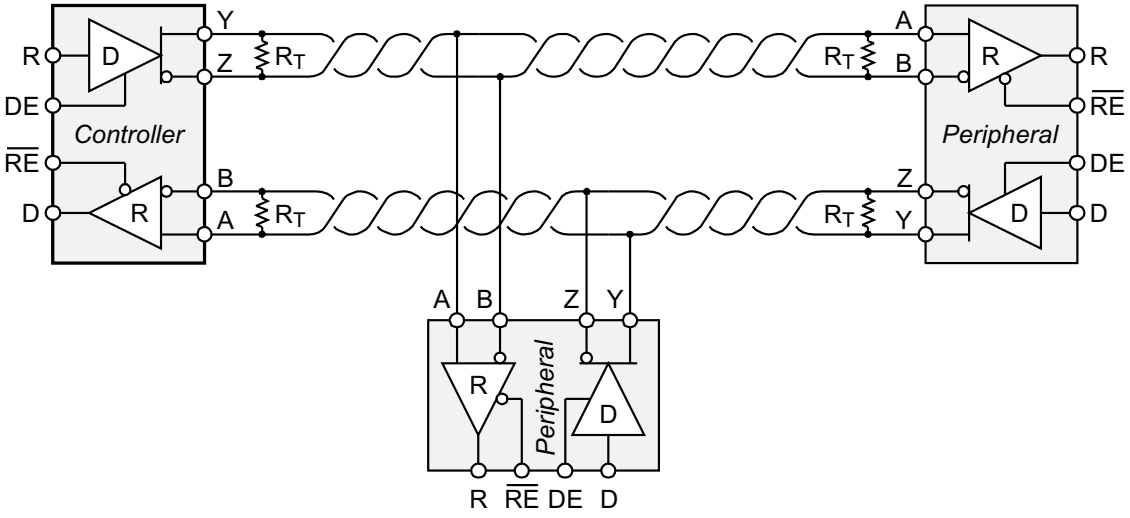
The SN65HVD33 has active-high driver enables and active-low receiver enables. A low (less than 1µA) standby current is achieved by disabling both the driver and receiver.

All devices are characterized for operation from –55°C to 125°C.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) |
|---|---|---|
| SN65HVD3x-EP | SOIC (8) | 4.9mm x 6mm |
| | SOIC (14) | 8.65mm x 6mm |

(1) For more information see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**Typical Application Schematic**

[1] The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

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## 4 Device Comparison

**Table 4-1. Available Options**

| BASE PART NUMBER | SIGNALING RATE | UNIT LOADS | RECEIVER EQUALIZATION | ENABLES | SOIC MARKING(1) |
|---|---|---|---|---|---|
| SN65HVD30MDREP | 25Mbps | 1/2 | No | No | HVD30EP |
| SN65HVD33MDREP | 25Mbps | 1/2 | No | Yes | HVD33EP |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

**Table 4-2. Improved Replacement Parts**

| Part Number | Replace With | Description |
|---|---|---|
| xxx3491<br>xxx3490 | SN65HVD33<br>SN65HVD30 | Better ESD protection (15kV vs 2kV or not specified), higher signaling rate (25Mbps vs 20Mbps), fractional unit load (64 nodes vs 32) |
| MAX3491E<br>MAX3490E | SN65HVD33<br>SN65HVD30 | Higher signaling rate (25Mbps vs 12Mbps), fractional unit load (64 nodes vs 32) |
| MAX3076E<br>MAX3077E | SN65HVD33<br>SN65HVD30 | Higher signaling rate (25Mbps vs 16Mbps), lower standby current (1µA vs 10µA) |

## 5 Pin Configuration and Functions

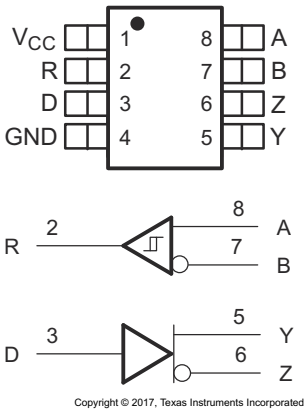



**Figure 5-1. D Package, 8-Pin SOIC (Top View)**

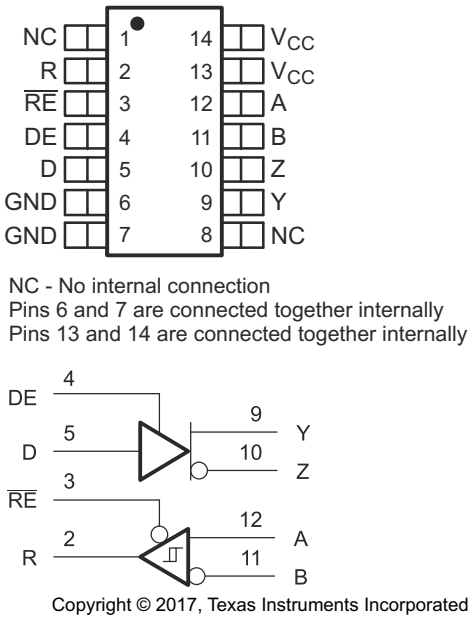



**Figure 5-2. D Package, 14-Pin SOIC (Top View)**

**Table 5-1. Pin Functions**

| PIN | | | TYPE | DESCRIPTION |
|---|---|---|---|---|
| NAME | D (8-PIN) | D (14-PIN) | | |
| A | 8 | 12 | Bus input | Receiver input (complementary to B) |
| B | 7 | 11 | Bus input | Receiver input (complementary to A) |
| D | 3 | 5 | Digital input | Driver data input |
| DE | — | 4 | Digital input | Driver enable, active high |
| GND | 4 | 6, 7 | Reference potential | Local device ground |
| NC | — | 1, 8 | No connect | No connect; must be left floating |
| R | 2 | 2 | Digital output | Receive data output |
| $\overline{RE}$ | — | 3 | Digital output | Receiver enable, active low |
| $V_{CC}$ | 1 | 13, 14 | Supply | 3V to 3.6V supply |
| Y | 5 | 9 | Bus output | Driver output (complementary to Z) |
| Z | 6 | 10 | Bus output | Driver output (complementary to Y) |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | –0.3 | 6 | V |
| $V_{(A)}$, $V_{(B)}$, $V_{(Y)}$, $V_{(Z)}$ | Voltage range at any bus terminal (A, B, Y, Z) | –9 | 14 | V |
| $V_{(TRANS)}$ | Voltage input, transient pulse through 100Ω (see Figure 7-12) (A, B, Y, Z)(3) | –50 | 50 | V |
| $V_I$ | Input voltage range (D, DE, $\overline{RE}$) | –0.5 | 7 | V |
| $P_{D(cont)}$ | Continuous total power dissipation | Internally limited(4) | | |
| $I_O$ | Output current (receiver output only, R) | | 11 | mA |
| $T_J$ | Junction temperature | | 165 | °C |
| $T_{stg}$ | Storage temperature range | –65 | 150 | °C |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) This tests survivability only and the output state of the receiver is not specified.
(4) The thermal shutdown protection circuit internally limits the continuous total power dissipation. Thermal shutdown typically occurs when the junction temperature reaches 165°C.

## 6.2 ESD Ratings

| | | | | MIN | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | Bus pins and GND | ±16000 | V |
| | | | All pins | ±4000 | |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | | ±1000 | |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 3 | | 3.6 | V |
| $V_I$ or $V_{IC}$ | Voltage at any bus terminal (separately or common mode) | | –7(1) | | 12 | V |
| $1/t_{UI}$ | Signaling rate | 'HVD30, 'HVD33 | | | 25 | Mbps |
| $R_L$ | Differential load resistance | | 54 | 60 | | Ω |
| $V_{IH}$ | High-level input voltage | D, DE, $\overline{RE}$ | 2 | | $V_{CC}$ | V |
| $V_{IL}$ | Low-level input voltage | D, DE, $\overline{RE}$ | 0 | | 0.8 | V |
| $V_{ID}$ | Differential input voltage | | –12 | | 12 | V |
| $I_{OH}$ | High-level output current | Driver | –60 | | | mA |
| | | Receiver | –8 | | | |
| $I_{OL}$ | Low-level output current | Driver | | | 60 | mA |
| | | Receiver | | | 8 | |
| $T_A$ | Ambient still-air temperature | | –55 | | 125(2) | °C |

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet.
(2) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

## 6.4 Thermal Information

| THERMAL METRIC(1) | | D (SOIC) 8 PINS | D (SOIC) 14 PINS | UNIT |
|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 135 | 92 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 43 | 59 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 44 | 61 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 12.1 | 5.7 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 49.7 | 30.7 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Dissipation Ratings

| PARAMETER | DEVICE | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $P_D$ | 'HVD30 (25 Mbps) | $R_L$ = 60Ω, $C_L$ = 50pF, Input to D a 50% duty cycle square wave at indicated signaling rate, $T_A$ = 85°C | | 197 | mW |
| | 'HVD33 (25Mbps) | $R_L$ = 60Ω, $C_L$ = 50pF, DE at $V_{CC}$, $\overline{RE}$ at 0V, Input to D a 50% duty cycle square wave at indicated signaling rate, $T_A$ = 85°C | | 197 | mW |

## 6.6 Electrical Characteristics: Driver

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{I(K)}$ | Input clamp voltage | | $I_I$ = –18mA | | –1.5 | | | V |
| $\|V_{OD(SS)}\|$ | Steady-state differential output voltage | | $I_O$ = 0 | | 2.3 | | $V_{CC}$ + 0.1 | V |
| | | | $R_L$ = 54Ω, See Figure 7-1 (RS-485) | | 1.5 | 2 | | |
| | | | $R_L$ = 100Ω, See Figure 7-1 (RS-422) | | 2 | 2.3 | | |
| | | | $V_{test}$ = –7V to 12V, See Figure 7-2 | | 1.5 | | | |
| $\Delta\|V_{OD(SS)}\|$ | Change in magnitude of steady-state differential output voltage between states | | $R_L$ = 54Ω, See Figure 7-1 and Figure 7-2 | | –0.2 | | 0.2 | V |
| $V_{OD(RING)}$ | Differential output voltage overshoot and undershoot | | $R_L$ = 54Ω, $C_L$ = 50pF, See Figure 7-5 and Figure 7-3 | | | | 10%(2) | V |
| $V_{OC(PP)}$ | Peak-to-peak common-mode output voltage | 'HVD30, 'HVD33 | See Figure 7-4 | | | 0.5 | | V |
| $V_{OC(SS)}$ | Steady-state common-mode output voltage | | See Figure 7-4 | | 1.6 | | 2.3 | V |
| $\Delta V_{OC(SS)}$ | Change in steady-state common-mode output voltage | | See Figure 7-4 | | –0.05 | | 0.05 | V |
| $I_{Z(Z)}$ or $I_{Y(Z)}$ | High-impedance state output current | 'HVD30 | $V_{CC}$ = 0V, $V_Z$ or $V_Y$ = 12V, Other input at 0V | | | | 90 | μA |
| | | | $V_{CC}$ = 0V, $V_Z$ or $V_Y$ = –7V, Other input at 0V | | –10 | | | |
| | | 'HVD33 | $V_{CC}$ = 3V or 0V, DE = 0 V, $V_Z$ or $V_Y$ = 12V | Other input at 0V | | | 90 | |
| | | | $V_{CC}$ = 3V or 0V, DE = 0V, $V_Z$ or $V_Y$ = –7V | | –10 | | | |
| $I_{Z(S)}$ or $I_{Y(S)}$ | Short-circuit output current | | $V_Z$ or $V_Y$ = –7V | Other input at 0 V | | ±250 | | mA |
| | | | $V_Z$ or $V_Y$ = 12V | | | | | |
| $I_I$ | Input current | D, DE | | | 0 | | 100 | μA |
| $C_{(OD)}$ | Differential output capacitance | | $V_{OD}$ = 0.4 sin (4E6πt) + 0.5V, DE at 0V | | | 16 | | pF |

(1) All typical values at 25°C with 3.3V supply
(2) 10% of the peak-to-peak differential output voltage swing, per TIA/EIA-485

## 6.7 Electrical Characteristics: Receiver

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IT+}$ | Positive-going differential input threshold voltage | | $I_O$ = –8mA | | | | –0.02 | V |
| $V_{IT–}$ | Negative-going differential input threshold voltage | 'HVD30 | $I_O$ = 8mA | | –0.15 | | | V |
| | | 'HVD33 | | | -0.2 | | | |
| $V_{hys}$ | Hysteresis voltage ($V_{IT+} – V_{IT–}$) | | | | | 50 | | mV |
| $V_{IK}$ | Enable-input clamp voltage | | $I_I$ = –18mA | | –1.5 | | | V |
| $V_O$ | Output voltage | | $V_{ID}$ = 200mV, $I_O$ = –8mA, See Figure 7-8 | | 2.4 | | | V |
| | | | $V_{ID}$ = –200mV, $I_O$ = 8mA, See Figure 7-8 | | | | 0.4 | |
| $I_{O(Z)}$ | High-impedance-state output current | | $V_O$ = 0 or $V_{CC}$, $\overline{RE}$ at $V_{CC}$ | | –1 | | 1 | µA |
| $I_A$ or $I_B$ | Bus input current | 'HVD30, 'HVD33 | $V_A$ or $V_B$ = 12 V | Other input at 0 V | | 0.20 | 0.35 | mA |
| | | | $V_A$ or $V_B$ = 12V, $V_{CC}$ = 0V | | | 0.24 | 0.4 | |
| | | | $V_A$ or $V_B$ = –7V | | –0.35 | –0.18 | | |
| | | | $V_A$ or $V_B$ = –7V, $V_{CC}$ = 0V | | –0.25 | –0.13 | | |
| $I_{IH}$ | Input current, $\overline{RE}$ | | $V_{IH}$ = 0.8V or 2V | | –60 | | | µA |
| $C_{ID}$ | Differential input capacitance | | $V_{ID}$ = 0.4 sin (4E6πt) + 0.5V, DE at 0V | | | 15 | | pF |
| **SUPPLY CURRENT** | | | | | | | | |
| $I_{CC}$ | Supply current | 'HVD30 | D at 0V or $V_{CC}$ and no load | | | | 2.1 | mA |
| | | 'HVD33 | $\overline{RE}$ at 0V, D at 0V or $V_{CC}$, DE at 0V, No load (receiver enabled and driver disabled) | | | | 1.8 | mA |
| | | 'HVD33 | $\overline{RE}$ at $V_{CC}$, D at $V_{CC}$, DE at 0V, No load (receiver disabled and driver disabled) | | | 0.022 | 1.5 | µA |
| | | 'HVD33 | $\overline{RE}$ at 0V, D at 0V or $V_{CC}$, DE at $V_{CC}$, No load (receiver enabled and driver enabled) | | | | 2.1 | mA |
| | | 'HVD33 | $\overline{RE}$ at $V_{CC}$, D at 0V or $V_{CC}$, DE at $V_{CC}$ No load (receiver disabled and driver enabled) | | | | 1.8 | mA |

(1) All typical values at 25°C with 3.3V supply

## 6.8 Switching Characteristics: Driver

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low- to high-level output | 'HVD30, 'HVD33 | $R_L$ = 54 Ω, $C_L$ = 50 pF, See Figure 7-5 | 4 | 10 | 23 | ns |
| $t_{PHL}$ | Propagation delay time, high- to low-level output | 'HVD30, 'HVD33 | | 4 | 9 | 23 | ns |
| $t_r$ | Differential output signal rise time | 'HVD30, 'HVD33 | | 2.5 | 5 | 18 | ns |
| $t_f$ | Differential output signal fall time | 'HVD30, 'HVD33 | | 2.5 | 5 | 18 | ns |
| $t_{sk(p)}$ | Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$) | 'HVD30, 'HVD33 | | | 0.6 | | ns |
| $t_{PZH1}$ | Propagation delay time, high-impedance to high-level output | 'HVD33 | $R_L$ = 110Ω, $\overline{RE}$ at 0V, D = 3V and S1 = Y, or D = 0V and S1 = Z, See Figure 7-6 | | | 45 | ns |
| $t_{PHZ}$ | Propagation delay time, high-level to high-impedance output | 'HVD33 | | | | 25 | ns |
| $t_{PZL1}$ | Propagation delay time, high-impedance to low-level output | 'HVD33 | $R_L$ = 110Ω, $\overline{RE}$ at 0V, D = 3V and S1 = Z, or D = 0V and S1 = Y, See Figure 7-7 | | | 35 | ns |
| $t_{PLZ}$ | Propagation delay time, low-level to high-impedance output | 'HVD33 | | | | 30 | ns |
| $t_{PZH2}$ | Propagation delay time, standby to high-level output | 'HVD30 | $R_L$ = 110Ω, $\overline{RE}$ at 3V, D = 3V and S1 = Y, or D = 0 V and S1 = Z, See Figure 7-6 | | | 4000 | ns |
| | | 'HVD33 | | | | 5000 | |
| $t_{PZL2}$ | Propagation delay time, standby to low-level output | 'HVD30 | $R_L$ = 110Ω, $\overline{RE}$ at 3V, D = 3V and S1 = Z, or D = 0 V and S1 = Y, See Figure 7-7 | | | 4000 | ns |
| | | 'HVD33 | | | | 5000 | |

## 6.9 Switching Characteristics: Receiver

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low- to high-level output | 'HVD30, 'HVD33 | $V_{ID}$ = –1.5V to 1.5V, $C_L$ = 15pF, See Figure 7-9 | | | 26 | 60 | ns |
| $t_{PLH}$ | Propagation delay time, high- to low-level output | 'HVD30, 'HVD33 | | | | 29 | 60 | ns |
| $t_{sk(p)}$ | Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$) | 'HVD30, 'HVD33 | | | | | 12 | ns |
| $t_r$ | Output signal rise time | 'HVD30 | | | | | 10 | ns |
| | | 'HVD33 | | | | | 18 | |
| $t_f$ | Output signal fall time | | | | | | 12.5 | ns |
| $t_{PHZ}$ | Output disable time from high level | | DE at 3V | $C_L$ = 15pF, See Figure 7-10 | | | 20 | ns |
| $t_{PZH1}$ | Output enable time to high level | | | | | | 20 | ns |
| $t_{PZH2}$ | Propagation delay time, standby to high-level output | 'HVD30 | DE at 0V | | | | 4000 | ns |
| | | 'HVD33 | | | | | 5000 | |
| $t_{PLZ}$ | Output disable time from low level | | DE at 3V | $C_L$ = 15pF, See Figure 7-11 | | | 20 | ns |
| $t_{PZL1}$ | Output enable time to low level | | | | | | 20 | ns |
| $t_{PZL2}$ | Propagation delay time, standby to low-level output | 'HVD30 | DE at 0V | | | | 4000 | ns |
| | | 'HVD33 | | | | | 5000 | ns |

## 6.10 Typical Characteristics

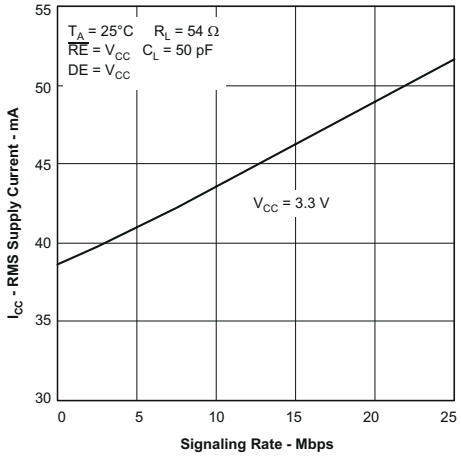



**Figure 6-1. RMS Supply Current Signaling Rate**

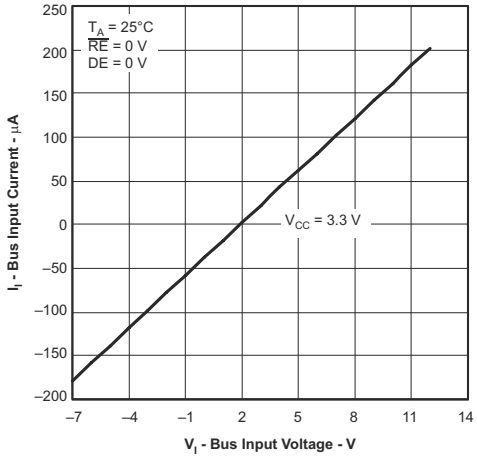



**Figure 6-2. Bus Input Current vs Input Voltage**

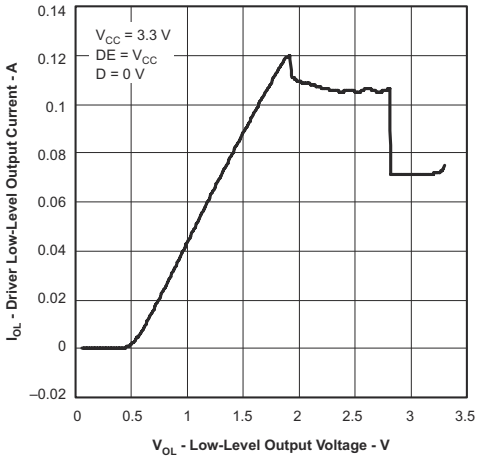



**Figure 6-3. Driver Low-Level Output Current vs Low-Level Output Voltage**

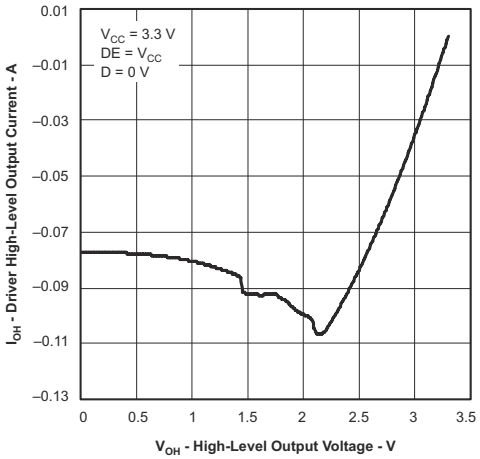



**Figure 6-4. Driver High-Level Output Current vs High-Level Output Voltage**

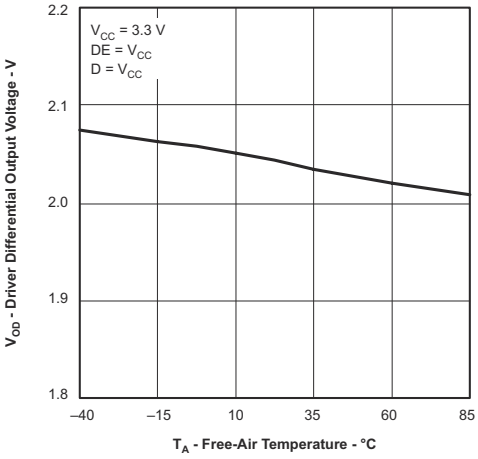



**Figure 6-5. Driver Differential Output Voltage vs Free-Air Temperature**

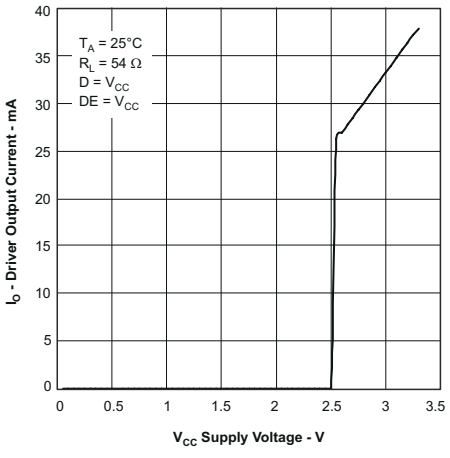



**Figure 6-6. Driver Output Current vs Supply Voltage**

# 7 Parameter Measurement Information

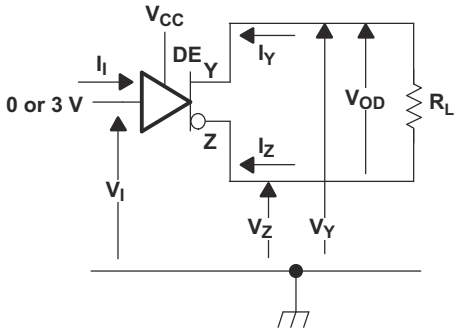



**Figure 7-1. Driver $V_{OD}$ Test Circuit and Voltage and Current Definitions**

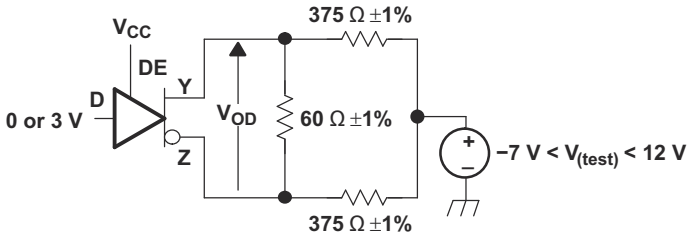



**Figure 7-2. Driver $V_{OD}$ With Common-Mode Loading Test Circuit**

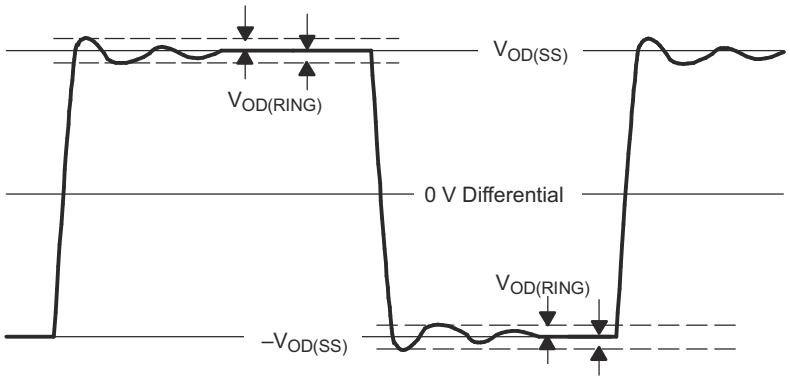
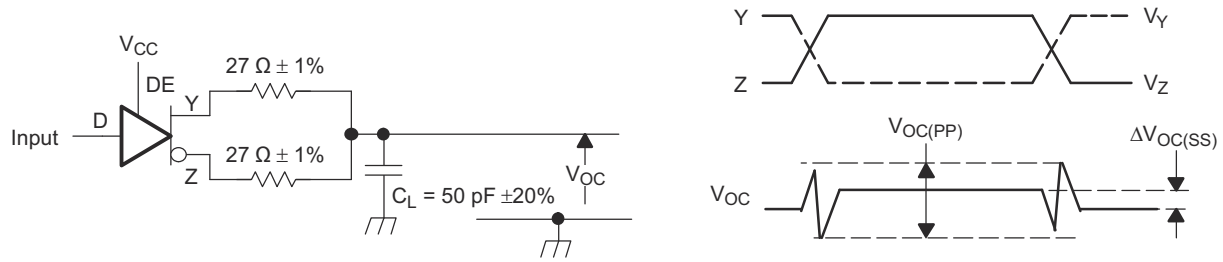


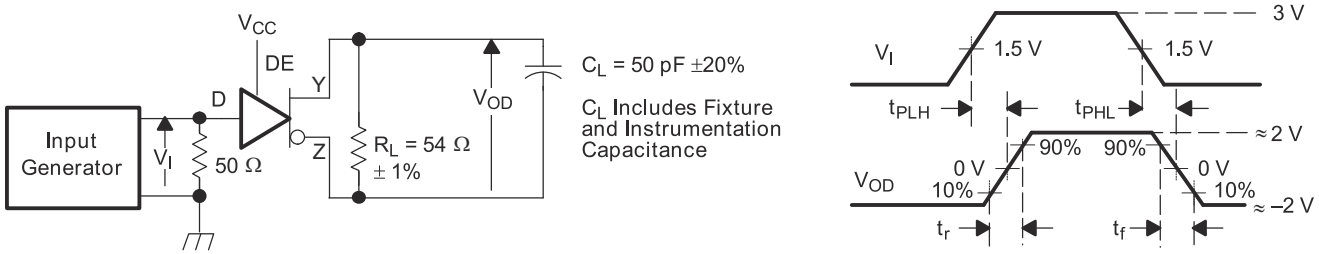

**Figure 7-3. $V_{OD(RING)}$ Waveform and Definitions**

$V_{OD(RING)}$ is measured at four points on the output waveform, corresponding to overshoot and undershoot from the $V_{OD(H)}$ and $V_{OD(L)}$ steady state values.



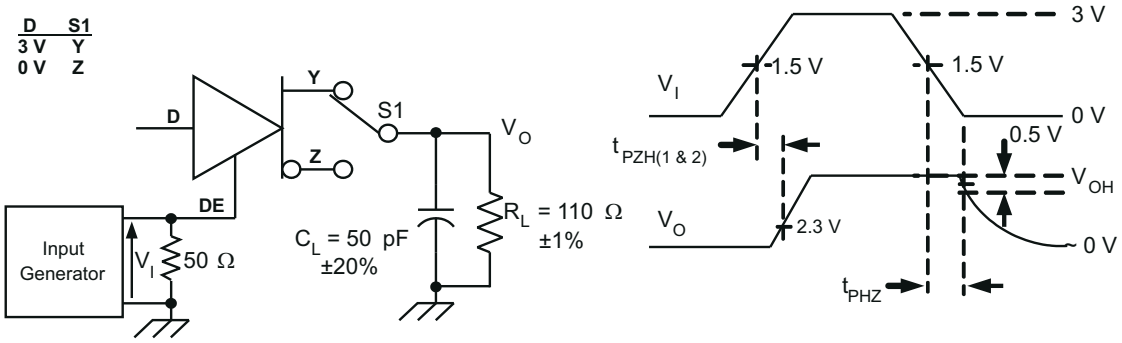

Input: PRR = 500kHz, 50% Duty Cycle, $t_r$ < 6ns, $t_f$ < 6ns, $Z_O$ = 50Ω

**Figure 7-4. Test Circuit and Definitions for Driver Common-Mode Output Voltage**




A. Generator: PRR = 500kHz, 50% Duty Cycle, $t_r$ < 6ns, $t_f$ < 6ns, $Z_O$ = 50Ω

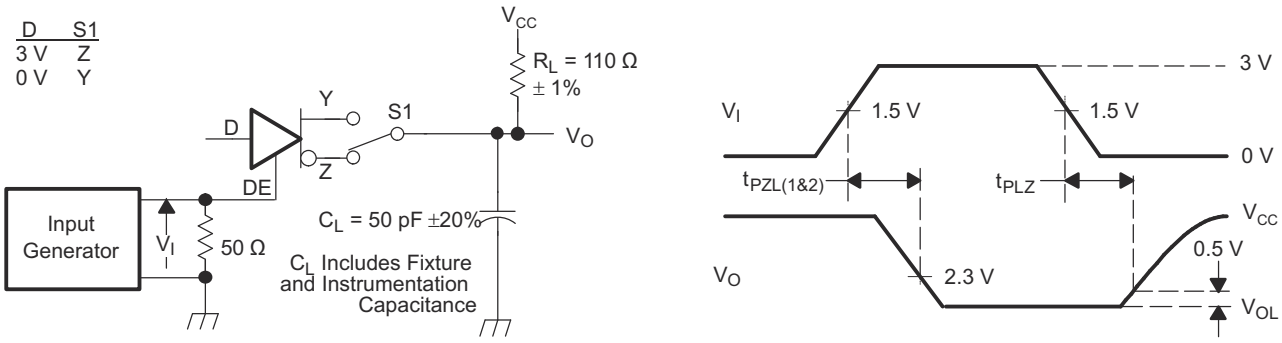
**Figure 7-5. Driver Switching Test Circuit and Voltage Waveforms**




A. Generator: PRR = 500kHz, 50% Duty Cycle, $t_r$ < 6ns, $t_f$ < 6ns, $Z_O$ = 50Ω

B. $C_L$ Includes Fixture and Instrumentation Capacitance

**Figure 7-6. Driver High-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms**




A. Generator: PRR = 500kHz, 50% Duty Cycle, $t_r$ < 6ns, $t_f$ < 6ns, $Z_O$ = 50Ω

**Figure 7-7. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms**

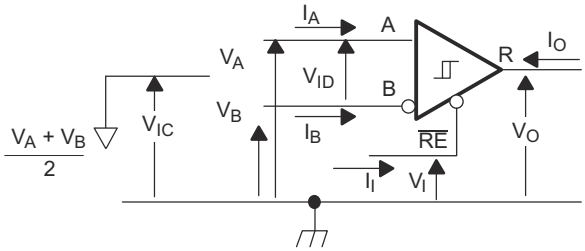
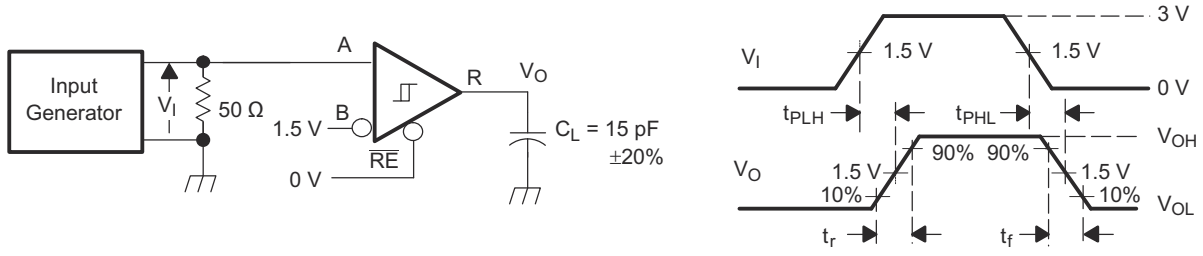
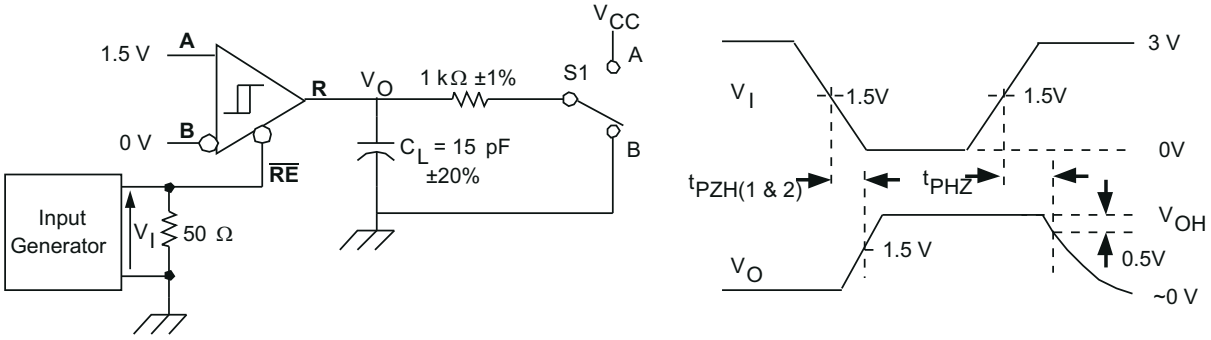



**Figure 7-8. Receiver Voltage and Current Definitions**



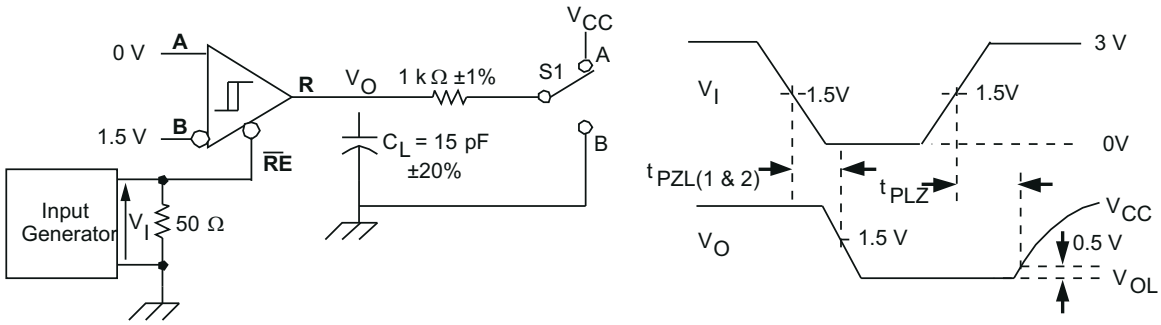

A. $C_L$ Includes Fixture and Instrumentation Capacitance
B. Generator: PRR = 500kHz, 50% Duty Cycle, $t_r$ < 6ns, $t_f$ < 6ns, $Z_O$ = 50Ω

**Figure 7-9. Receiver Switching Test Circuit and Voltage Waveforms**




A. Generator: PRR = 500kHz, 50% Duty Cycle, $t_r$ < 6ns, $t_f$ < 6ns, $Z_O$ = 50Ω

**Figure 7-10. Receiver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms**




A. Generator: PRR = 500kHz, 50% Duty Cycle, $t_r$ < 6ns, $t_f$ < 6ns, $Z_O$ = 50Ω

**Figure 7-11. Receiver Enable Time From Standby (Driver Disabled)**

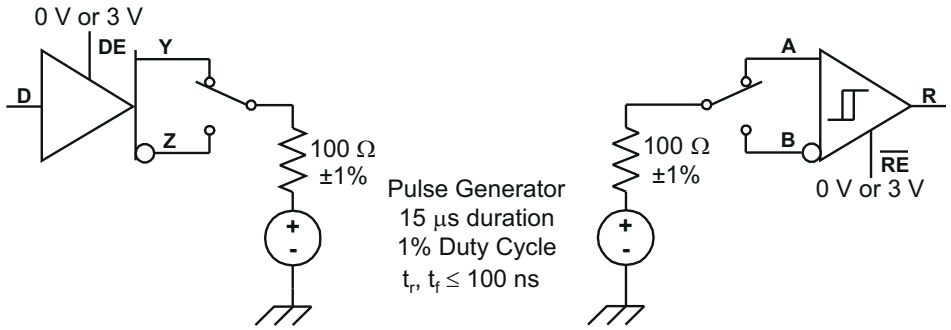



**Figure 7-12. Test Circuit, Transient Over Voltage Test**

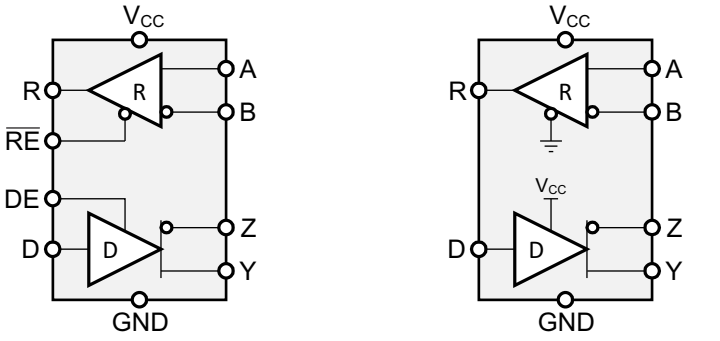
# 8 Detailed Description

## 8.1 Overview

The SN65HVD3x-EP are low-power, full-duplex RS-485 transceivers available in three speed grades suitable for data transmission of 1Mbps, 5Mbps, and 25Mbps.

The SN65HVD30 is fully enabled with no external enabling pins. The SN65HVD33 has an active-high driver enable and active-low receiver enable. A standby current of less than 1µA is achieved by disabling both driver and receiver.

## 8.2 Functional Block Diagram




*a) SN65HVD33, SN65HVD34, SN65HVD35*

*b) SN65HVD30, SN65HVD31, SN65HVD32*



## 8.3 Feature Description

### *8.3.1 Low-Power Standby Mode*

When both the driver and receiver are disabled (DE is low and $\overline{RE}$ is high), the device is in standby mode. If the enable inputs are in this state for less than 60ns, the device does not enter standby mode. This guards against inadvertently entering standby mode during driver or receiver enabling. The device in standby mode only when the enable inputs are held in this state for 300ns or more. In this low-power standby mode, most internal circuitry is powered down, and the supply current is typically less than 1nA. When either the driver or the receiver is re-enabled, the internal circuitry becomes active.

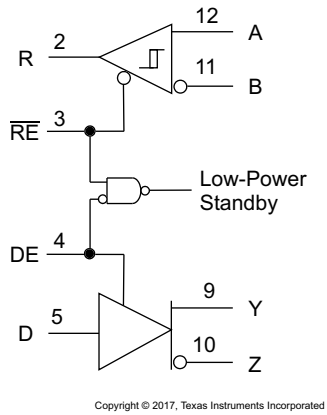



**Figure 8-1. Low-Power Standby Logic Diagram**

If only the driver is re-enabled (DE transitions to high) the driver outputs are driven according to the D input after the enable times given by $t_{PZH2}$ and $t_{PZL2}$ in the driver switching characteristics. If the D input is open when the driver is enabled, the driver output defaults to Y high and Z low, in accordance with the driver-failsafe feature.

If only the receiver is re-enabled ($\overline{RE}$ transitions to low) the receiver output is driven according to the state of the bus inputs (A and B) after the enable times given by $t_{PZH2}$ and $t_{PZL2}$ in the receiver switching characteristics. If there is no valid state on the bus, the receiver responds as described in the failsafe operation section.

If both the receiver and driver are re-enabled simultaneously, the receiver output is driven according to the state of the bus inputs (A and B) and the driver output is driven according to the D input.

**Note**

The state of the active driver affects the inputs to the receiver. Therefore, the receiver outputs are valid as soon as the driver outputs are valid.

### *8.3.2 Driver Output Current Limiting*

The RS-485 standard (ANSI/TIA/EIA-485-A or equivalently ISO 8482) specifies a 250mA driver output current limit to prevent damage caused by data contention on the bus. That applies in the event that two or more transceivers drive the bus to opposing states at the same time. The SN65HVD3x-EP family of devices includes current-limiting circuitry that prevents damage under these conditions.

**Note**

This current limit prevents damage during the bus contention, but the logic state of the bus is indeterminate as specified by the standard, so communication errors can occur.

In a specific combination of circumstances, a condition can occur in which current through the bus pin exceeds the 250mA limit. This combination of conditions is not normally included in RS-485 applications:

- Loading capacitance on the pin is less than 500pF
- The bus pin is directly connected to a voltage more negative than –1V
- The device is supplied with $V_{CC}$ equal to or greater than 3.3V
- The driver is enabled
- The bus pin is driving to the logic high state

In these specific conditions, the normal current-limit circuitry and thermal-shutdown circuitry does not limit or shutdown the current flow. If the current is allowed to continue, the device heats up in a localized area near the driver outputs, and the device can be damaged.

Typical RS-485 twisted-pair cable has a capacitance of approximately 50pF/meter. Therefore, it is expected that 10 meters of cable can provide sufficient capacitance to prevent this latch-up condition.

The –7 to +12V common mode range specified by RS-485 is intended to allow communication between transceivers separated by significant distances when ground offsets occur due to temporary current surges, electrical noise, and so on. Under those circumstances, the inherent cable needed to connect separated transceivers make sure the conditions previously listed do not occur. For a transceiver separated by only a short cable length or backplane applications, a steady-state negative common-mode voltage is unusual. A negative power supply to be shorted to the bus lines due to miswiring or cable damage is possible; however, this is a different root cause fault, and robust devices such as the SN65HVD178x family are used for surviving power supply or miswiring faults.

The 250mA current limit in the RS-485 standard is intended to prevent damage caused by data contention on the bus; that is, in the event that two or more transceivers drive the bus to different states at the same time. These devices are not damaged under these conditions because all RS-485 drivers have output impedance sufficient to prevent the direct connection condition stated previously. Typical RS-485 driver output impedance is on the order of 10Ω to 30Ω.

### *8.3.3 Hot-Plugging*

These devices are designed to operate in *hot swap* or *hot pluggable* applications. Key features for hot-pluggable applications are:

- Power-up

- Power-down glitch-free operation
- Default disabled input/output pins
- Receiver failsafe

As shown in Figure 6-6, an internal power-on reset circuit keeps the driver outputs in a high-impedance state until the supply voltage has reached a level at which the device reliably operates. This makes sure that no spurious bits are transmitted on the bus pin outputs as the power supply turns on or turns off.

As shown in the *Section 8.4*, the enable inputs have the feature of default disable on both the driver enable and receiver enable. This makes sure the device neither drives the bus nor reports data on the R pin until the associated controller actively drives the enable pins.

### *8.3.4 Receiver Failsafe*

The differential receivers of the SN65HVD3x-EP family are failsafe to invalid bus states caused by:

- Open bus conditions such as a disconnected connector
- Shorted bus conditions such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver outputs a failsafe logic high state, so the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the input indeterminate range does not include zero volts differential. In order to comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input $V_{ID}$ is more positive than 200mV, and must output a low when $V_{ID}$ is more negative than –200mV. The receiver parameters which determine the failsafe performance are $V_{IT+}$, $V_{IT–}$, and $V_{HYS}$ (the separation between $V_{IT+}$ and $V_{IT–}$. As shown in the *Section 6.7* table, differential signals more negative than –200mV always cause a low receiver output, and differential signals more positive than 200mV always cause a high receiver output.

When the differential input signal is close to zero, it is still above the $V_{IT+}$ threshold, and the receiver output is high. Only when the differential input is more than $V_{HYS}$ below $V_{IT+}$ does the receiver output transition to a low state. Therefore, the noise immunity of the receiver inputs during a bus fault conditions includes the receiver hysteresis value ($V_{HYS}$) as well as the value of $V_{IT+}$.

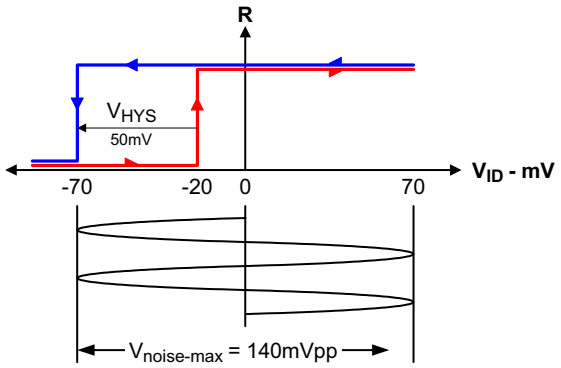



**Figure 8-2. SN65HVD30-35 Noise Immunity Under Bus Fault Conditions**

### *8.3.5 Safe Operation With Bus Contention*

These devices incorporate a driver current limit of 250 mA across the RS-485 common-mode range of –7V to +12V. As stated in the *Application Guidelines for TIA/EIA-485-A* [2], this sets a practical limitation to prevent damage during bus contention events. Contention can occur during system initialization, during system faults, or whenever two or more drivers are active at the same time.

[2] TIA/EIA Telecommunications System Bulletin TSB89, *Application Guidelines for TIA/EIA-485-A*

Figure 8-3 shows a 2-node system to demonstrate bus contention by forcing both drivers to be active in opposing states.

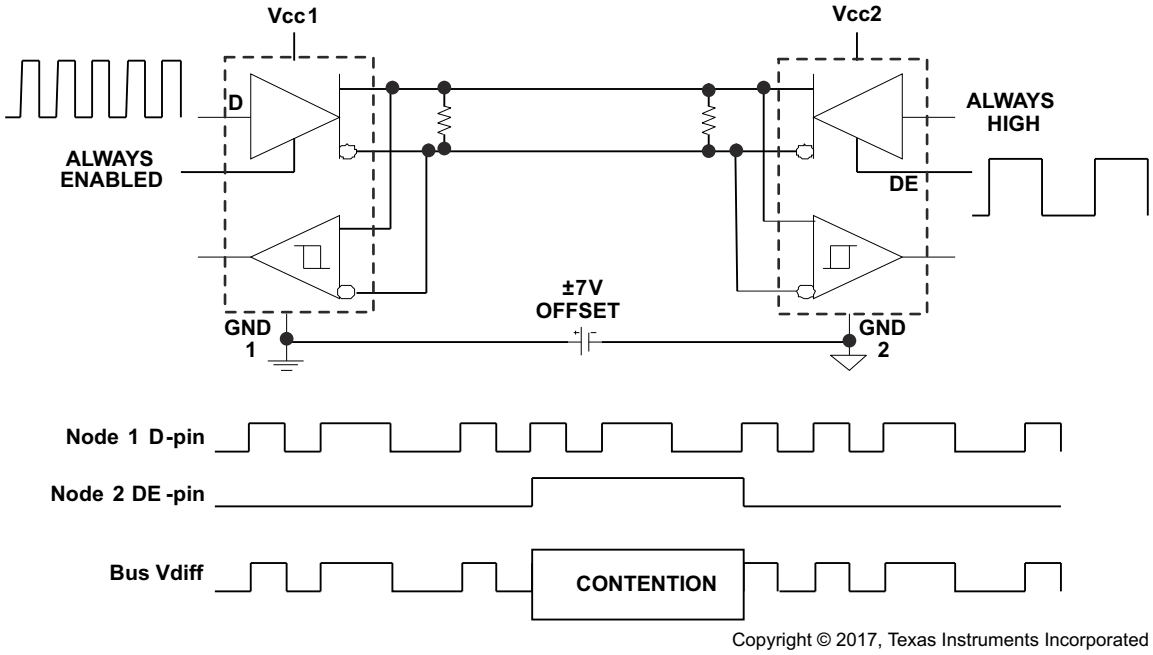





**Figure 8-3. Bus Contention Example**

Figure 8-4 shows typical operation in a bus contention event. The bottom trace illustrates how the SN65HVD33 device at Node 1 continues normal operation after a contention event between the two drivers with a –7V ground offset on Node 2. This illustrates how the SN65HVD3x-EP family of devices operates robustly in spite of bus contention faults, even with large common-mode offsets.

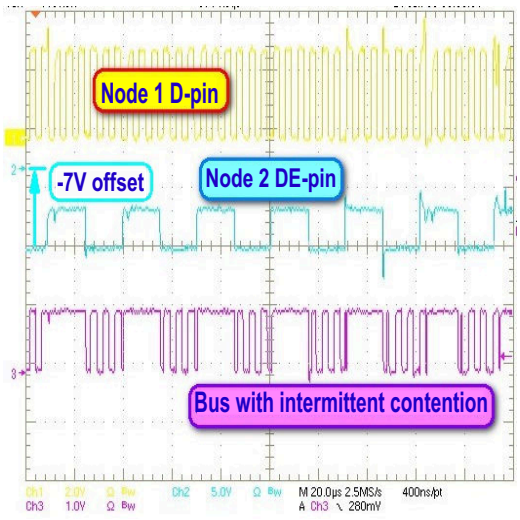



**Figure 8-4. SN65HVD3x-EP Drivers Operate Correctly After Bus Contention Faults**

## 8.4 Device Functional Modes

Table 8-1 through Table 8-4 list the functional modes of the devices.

**Table 8-1. SN65HVD33 Driver**

| INPUTS | | OUTPUTS | |
|---|---|---|---|
| D | DE | Y | Z |
| H | H | H | L |
| L | H | L | H |
| X | L or open | Z | Z |
| Open | H | L | H |

**Table 8-2. SN65HVD33 Receiver**

| DIFFERENTIAL INPUTS $V_{ID} = V_{(A)} – V_{(B)}$ | ENABLE $\overline{RE}$ | OUTPUT R |
|---|---|---|
| $V_{ID} \leq –0.2$ V | L | L |
| $–0.2 V < V_{ID} < –0.02$ V | L | — |
| $–0.02 V \leq V_{ID}$ | L | H |
| X | H or open | Z |
| Open Circuit | L | H |
| Idle circuit | L | H |
| Short Circuit, $V_{(A)} = V_{(B)}$ | L | H |

**Table 8-3. SN65HVD30 Driver**

| INPUT D | OUTPUTS | |
|---|---|---|
| | Y | Z |
| H | H | L |
| L | L | H |
| Open | L | H |

**Table 8-4. SN65HVD30 Receiver**

| DIFFERENTIAL INPUTS $V_{ID} = V_{(A)} – V_{(B)}$ | OUTPUT R |
|---|---|
| $V_{ID} \leq –0.2$ V | L |
| $–0.02 V \leq V_{ID}$ | H |
| Open Circuit | H |
| Idle circuit | H |
| Short Circuit, $V_{(A)} = V_{(B)}$ | H |

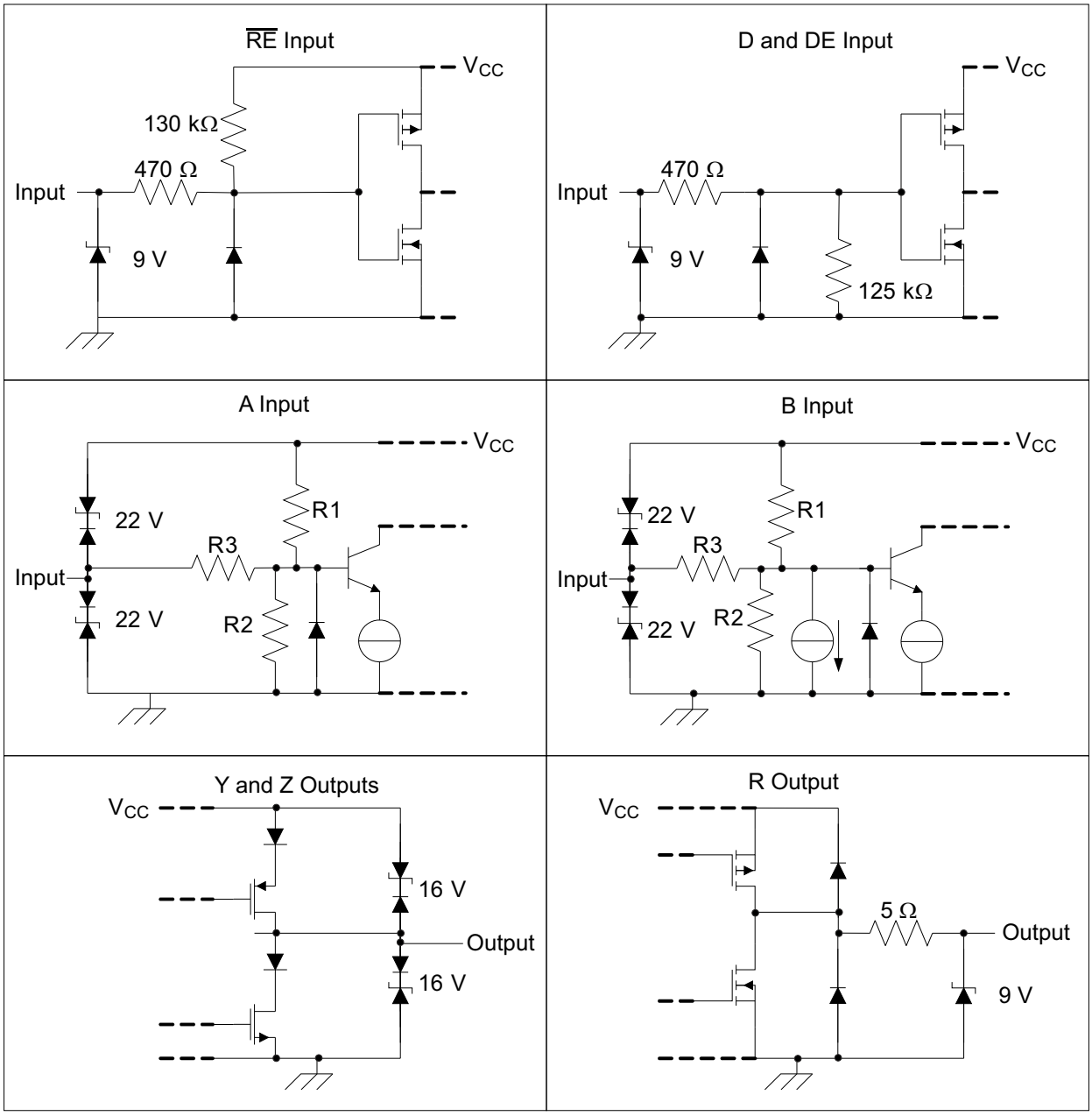





**Figure 8-5. Equivalent Input and Output Schematic Diagrams**

**Table 8-5. Input Attenuator Resistance Values**

| PART NUMBER | R1, R2 | R3 |
|---|---|---|
| SN65HVD30, SN65HVD33 | 9kΩ | 45kΩ |

# 9 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The SN65HVD3x-EP family consists of full-duplex RS-485 transceivers commonly used for asynchronous data transmissions. Full-duplex implementation requires two signal pairs (four wires), and allows each node to transmit data on one pair while simultaneously receiving data on the other pair.

To eliminate line reflections, each cable end is terminated with a termination resistor ($R_T$) whose value matches the characteristic impedance ($Z_0$) of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

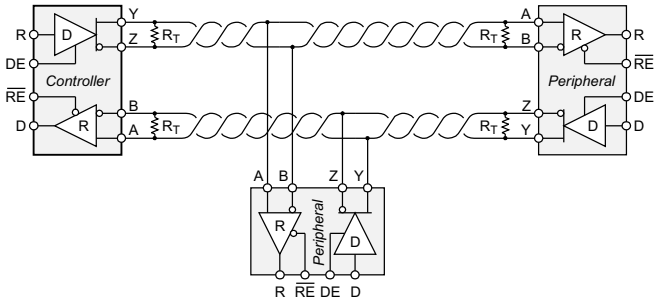
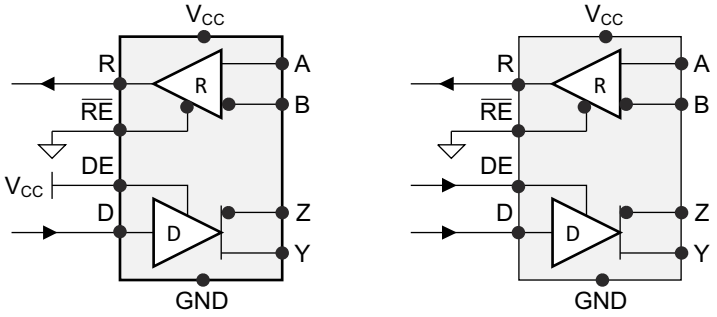



**Figure 9-1. Typical RS-485 Network With Full-Duplex Transceivers**

## 9.2 Typical Application

A full-duplex RS-485 network consists of multiple transceivers connecting in parallel to two bus cables. On one signal pair, a controller driver transmits data to multiple peripheral receivers. The controller driver and peripheral receivers can remain fully enabled at all times. On the other signal pair, multiple peripheral drivers transmit data to the controller receiver. To avoid bus contention, the peripheral drivers must be intermittently enabled and disabled such that only one driver is enabled at any time, as in half-duplex communication. The controller receiver can remain fully enabled at all times.

Because the driver cannot be disabled, connect only one driver to the bus when using the SN65HVD30.




*a) Controller enable control*

*b) Peripheral enable control*

**Figure 9-2. Full-Duplex Transceiver Configurations**

### 9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that is used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

#### 9.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and bus length, meaning the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable can be without introducing data errors. While most RS-485 systems use data rates between 10kbps and 100kbps, some applications require data rates up to 250kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

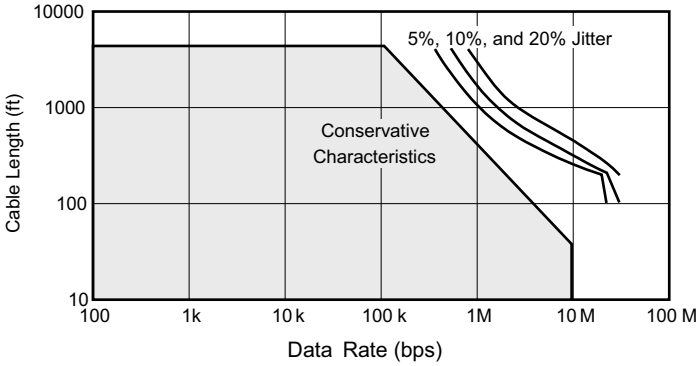



**Figure 9-3. Cable Length vs Data Rate Characteristic**

Even higher data rates are achievable (such as 26Mbps for the SN65HVD30 and SN65HVD33 devices) in cases where the interconnect is short enough, or has suitably low attenuation at signal frequencies, to not degrade the data.

#### 9.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, must be as short as possible. Stubs present a nonterminated piece of bus line that can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub must be less than one-tenth of the rise time of the driver; thus giving a maximum physical stub length as shown in Equation 1.

$$L_{stub} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where:

- $t_r$ is the 10/90 rise time of the driver
- c is the speed of light ($3 \times 10^8$ m/s)
- v is the signal velocity of the cable or trace as a factor of c

Per Equation 1, Table 9-1 shows the maximum cable-stub lengths for the minimum driver output rise times of the SN65HVD3x-EP full-duplex family of transceivers for a signal velocity of 78%.

**Table 9-1. Maximum Stub Length**

| Device | Minimum driver output rise Time (ns) | Maximum Stub Length | |
|---|---|---|---|
| | | (m) | (ft) |
| SN65HVD30 | 4 | 0.1 | 0.3 |
| SN65HVD33 | 4 | 0.1 | 0.3 |

#### 9.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12kΩ. The SN65HVD30 and SN65HVD33 devices are 1/2 UL transceivers, connecting up to 64 receivers to the bus is possible.

### 9.2.2 Detailed Design Procedure

To protect bus nodes against high-energy transients, the implementation of external transient protection devices is necessary (see Figure 9-4).

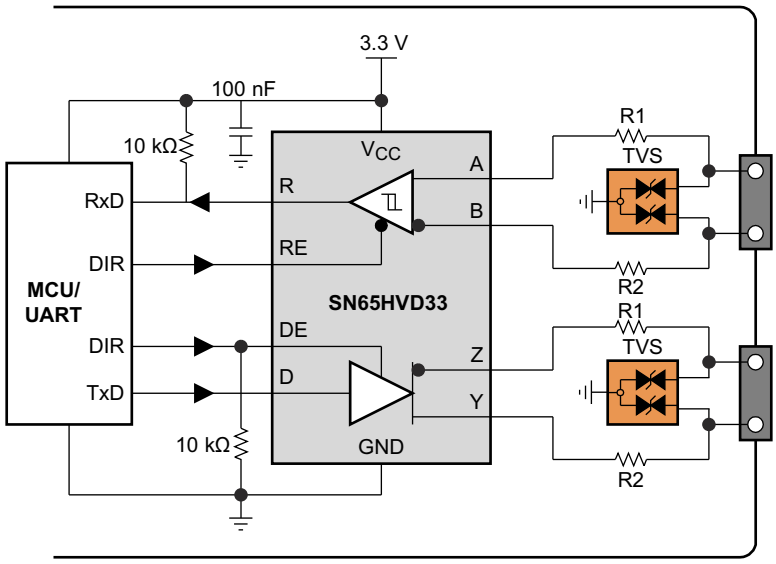




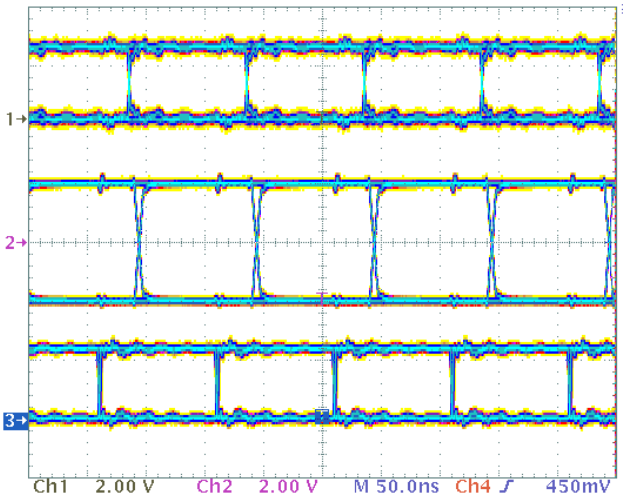

**Figure 9-4. Transient Protection Against ESD, EFT, and Surge Transients**

**Table 9-2. Bill of Materials**

| DEVICE | FUNCTION | ORDER NUMBER | MANUFACTURER(1) |
|---|---|---|---|
| XCVR | 3.3V Full-Duplex RS-485 Transceiver | SN65HVD33 | TI |
| R1, R2 | 10Ω, Pulse-Proof Thick-Film Resistor | CRCW060310RJNEAHP | Vishay |
| TVS | Bidirectional 400W Transient Suppressor | CDSOT23-SM712 | Bourns |

(1) See the Third-Party Products Disclaimer.

### 9.2.3 Application Curve




Signals from top to bottom: D, Y, Z, VOD

**Figure 9-5. SN65HVD33-EP Transient Waveform**

## 9.3 Power Supply Recommendations

For reliable operation at all data rates and supply voltages, each supply must be decoupled with a 100nF ceramic capacitor located as close as possible to the supply pins. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps compensate for the resistance and inductance of the PCB power planes.

## 9.4 Layout

### *9.4.1 Layout Guidelines*

Robust and reliable bus-node design often requires the use of external transient protection devices to protect against EFT and surge transients that can occur in industrial environments. Because these transients have a wide frequency bandwidth (from approximately 3MHz to 3GHz), high-frequency layout techniques must be applied during PCB design.

- Place the protection circuitry close to the bus connector to prevent noise transients from entering the board.
- Use $V_{CC}$ and ground planes to provide low-inductance. High-frequency currents follow the path of least inductance and not the path of least impedance.
- Design the protection components into the direction of the signal path. Do not force the transients currents to divert from the signal path to reach the protection device.
- Apply 100nF to 220nF bypass capacitors as close as possible to the $V_{CC}$ pins of transceiver, UART, and controller ICs on the board.
- Use at least two vias for $V_{CC}$ and ground connections of bypass capacitors and protection devices to minimize effective via inductance.
- Use 1kΩ to 10kΩ pullup or pulldown resistors for enable lines to limit noise currents in these lines during transient events.
- Insert series pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
- While pure TVS protection is sufficient for surge transients up to 1kV, higher transients require metal-oxide varistors (MOVs), which reduces the transients to a few hundred volts of clamping voltage and transient blocking units (TBUs) that limit transient current to 200mA.

### *9.4.2 Layout Example*

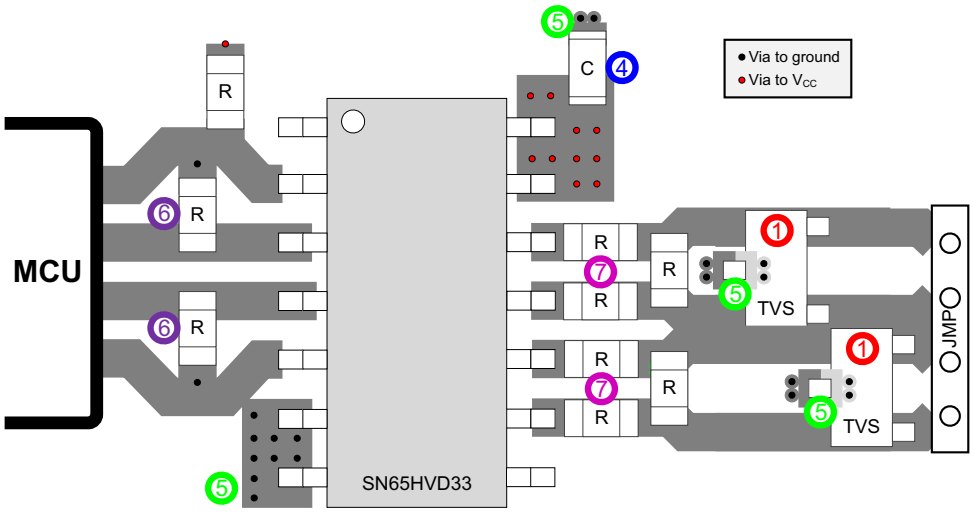



**Figure 9-6. SN65HVD33-EP Layout Example**

# 10 Device and Documentation Support

## 10.1 Third-Party Products Disclaimer

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All trademarks are the property of their respective owners.

## 10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 10.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision E (September 2015) to Revision F (March 2025) | Page |
|---|---|
| • Changed all instances of legacy terminology to controller and peripheral where mentioned | 1 |
| • Changed the Device Information table to the *Package Information* table | 1 |
| • Removed devices SN65HVD31-EP, SN65HVD32-EP, SN65HVD34-EP and SN65HVD35-EP from the data sheet | 1 |
| • Deleted the Receiver Equalization Characteristics table from the *Specifications* | 4 |

| Changes from Revision D (March 2012) to Revision E (September 2015) | Page |
|---|---|
| • Added *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section | 1 |

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65HVD30MDREP | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HVD30EP | Samples |
| SN65HVD30MDREPG4 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HVD30EP | Samples |
| SN65HVD33MDREP | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HVD33EP | Samples |
| V62/06634-01XE | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HVD30EP | Samples |
| V62/06634-04YE | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HVD33EP | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**OTHER QUALIFIED VERSIONS OF SN65HVD30-EP, SN65HVD33-EP :**

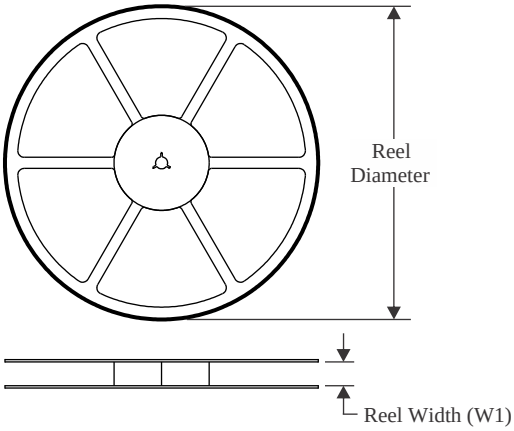
- Catalog : SN65HVD30, SN65HVD33

NOTE: Qualified Version Definitions:

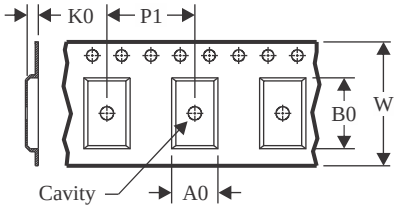
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

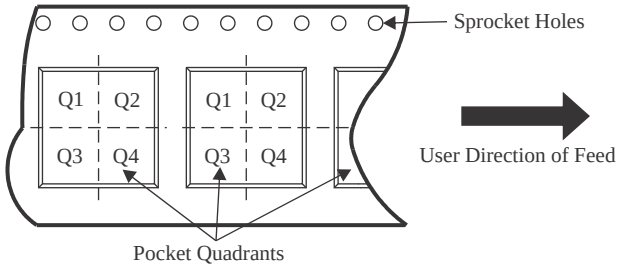



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

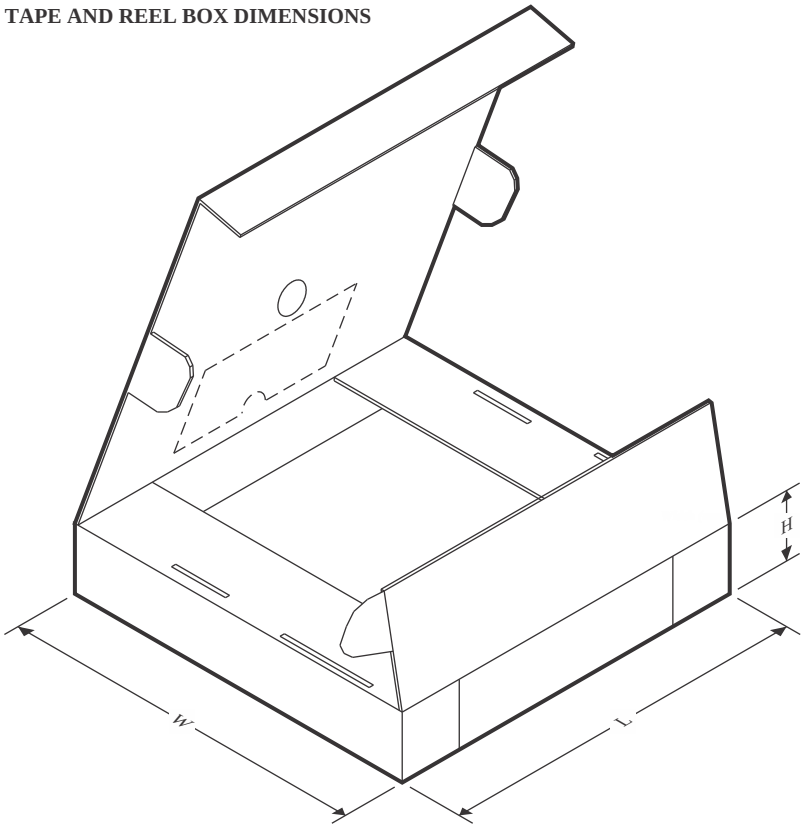
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

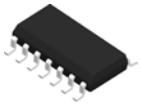
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65HVD30MDREP | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| SN65HVD33MDREP | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN65HVD30MDREP | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| SN65HVD33MDREP | SOIC | D | 14 | 2500 | 340.5 | 336.1 | 32.0 |

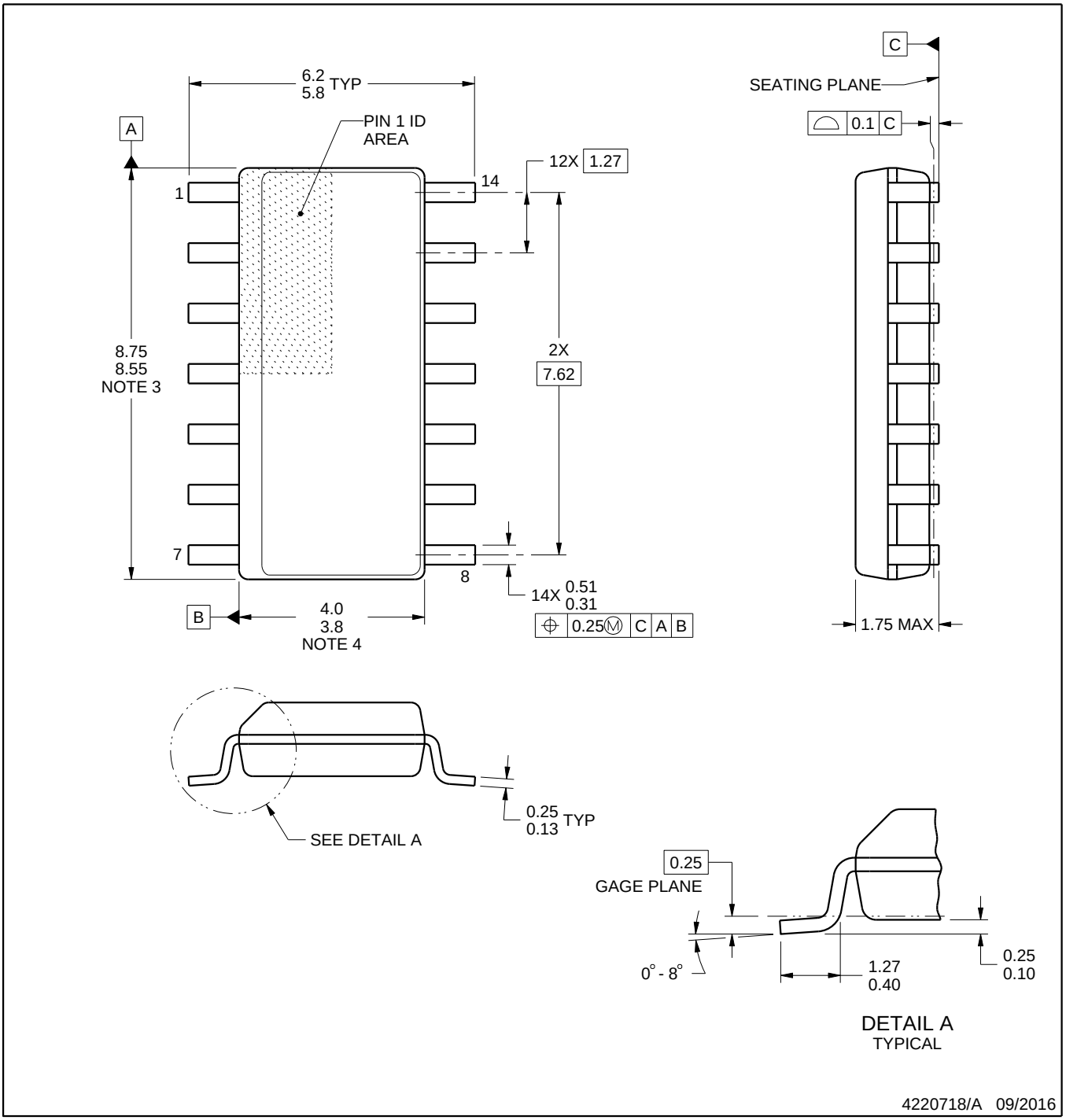


# PACKAGE OUTLINE

## D0014A

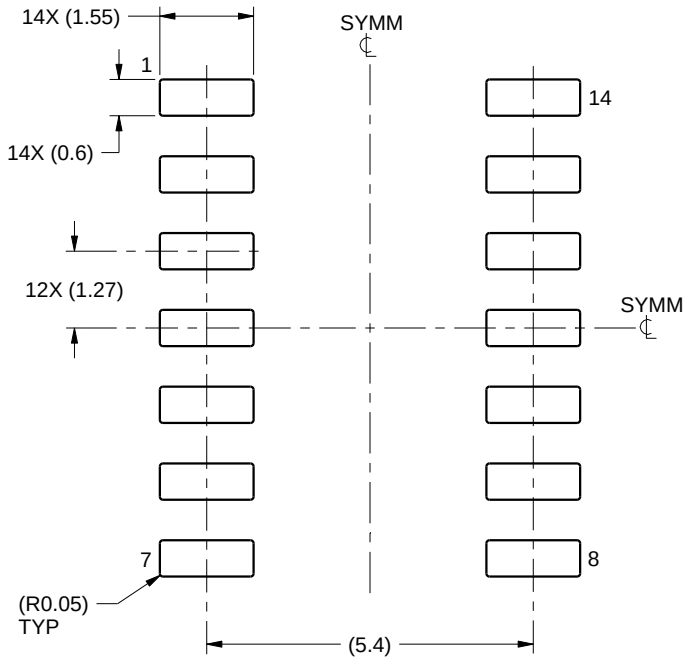
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

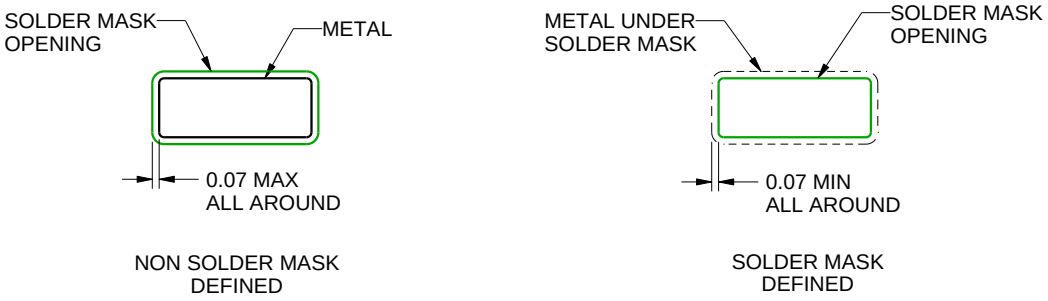



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

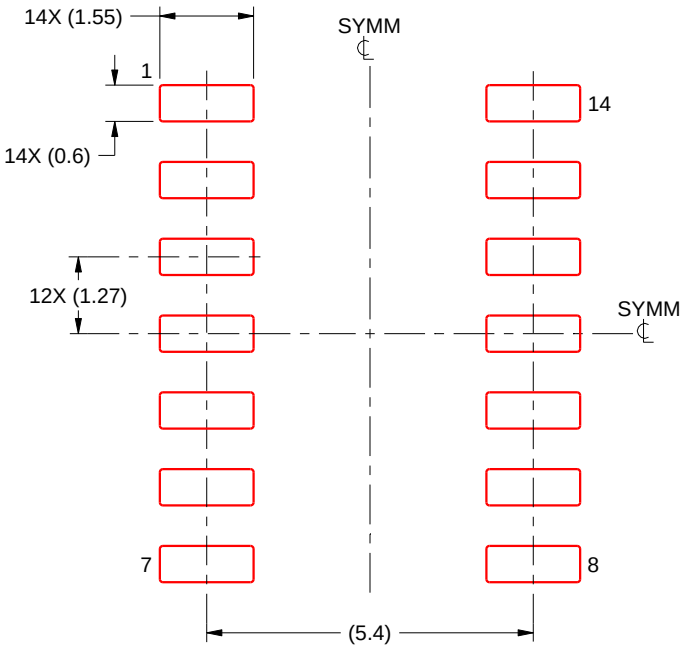
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0014A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

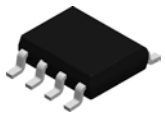



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

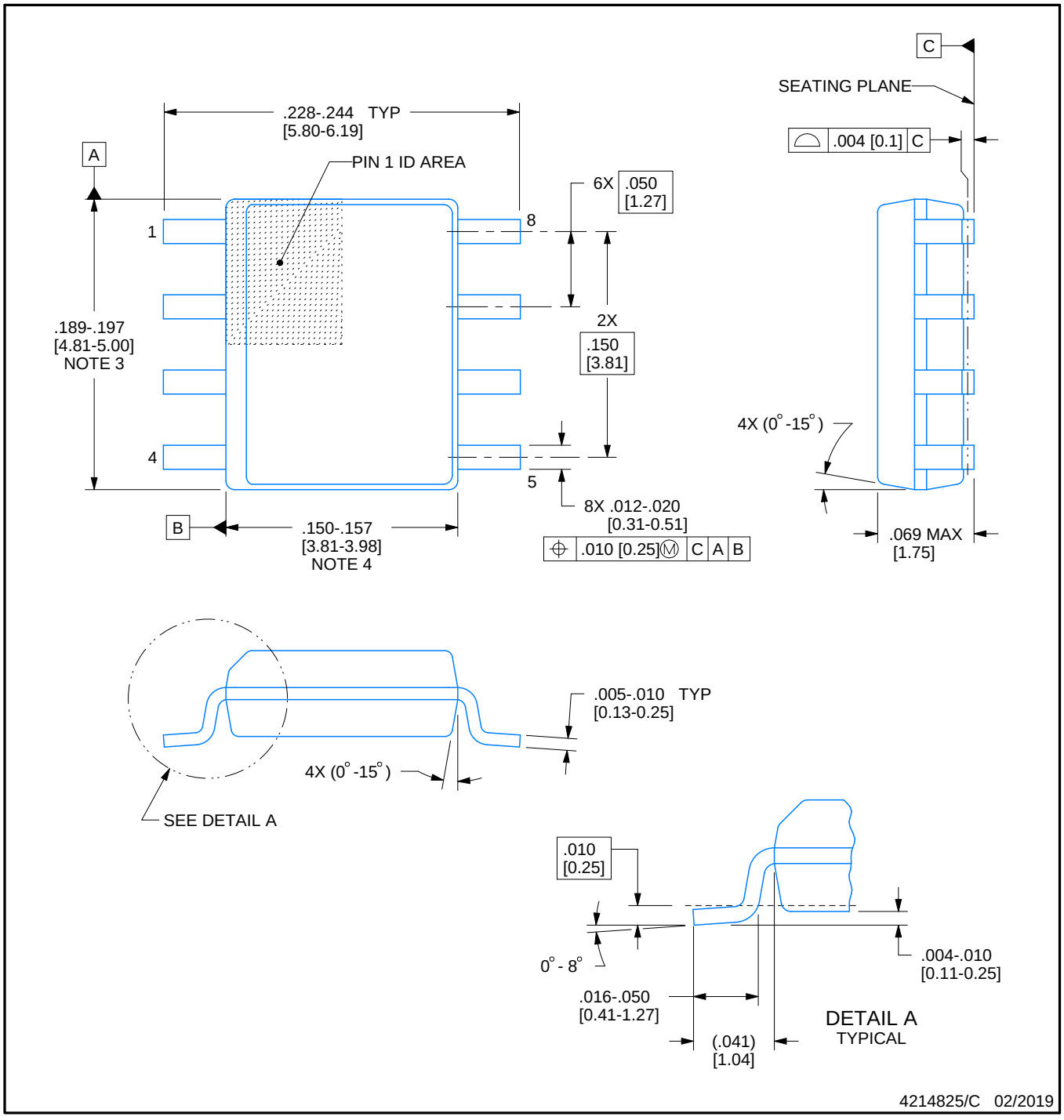


# PACKAGE OUTLINE

## D0008A

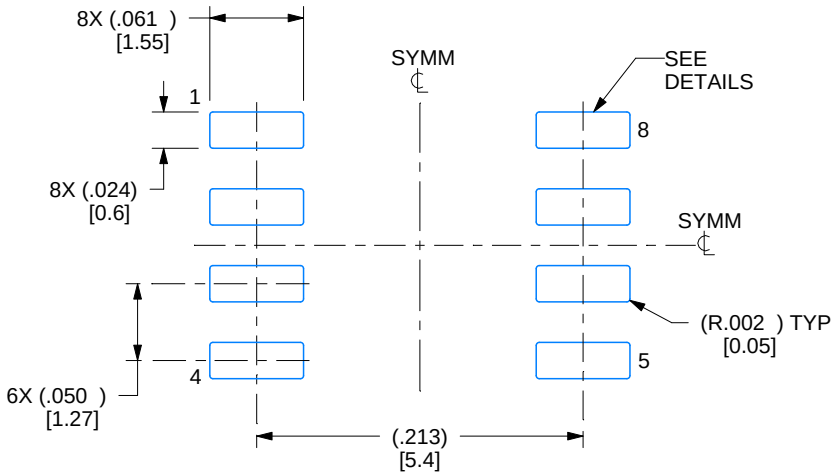
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

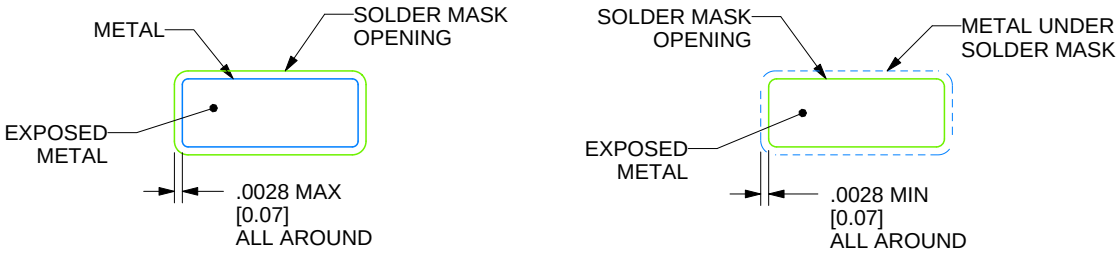



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

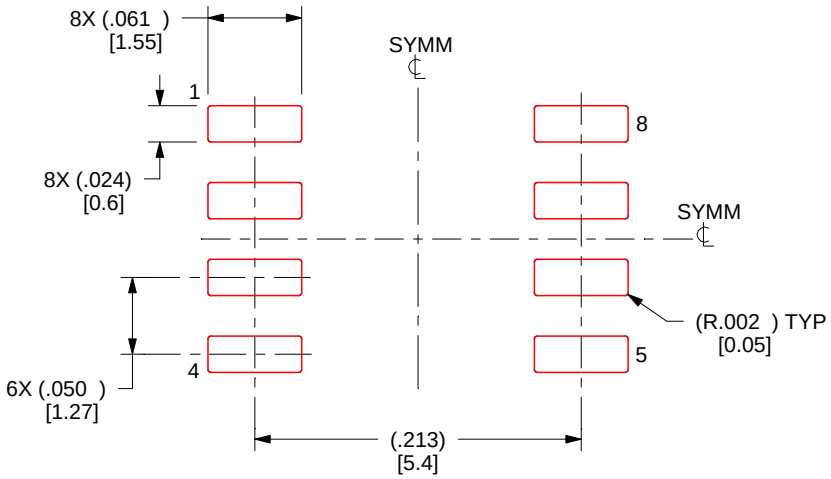
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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