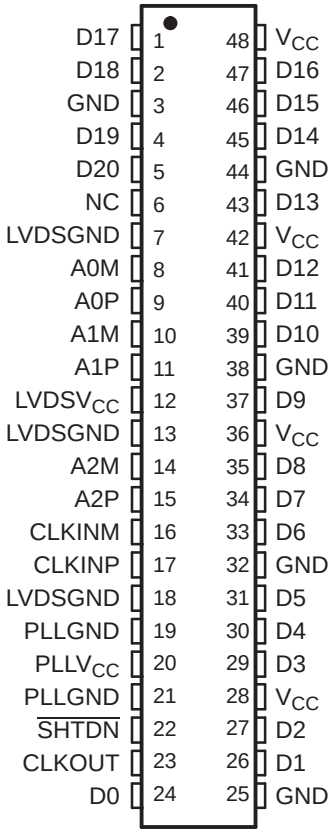
FlatLink™ RECEIVER

Check for Samples: SN65LVDS86A-Q1

FEATURES

- **3:21 Data Channel Expansion at up to 178.5 Mbytes/s Throughput**
- **Suited for SVGA, XGA, or SXGA Display Data Transmission From Controller to Display With Very Low EMI**
- **Three Data Channels and Clock Low-Voltage Differential Channels In and 21 Data and Clock Low-Voltage TTL Channels Out**
- **Operates From a Single 3.3-V Supply**
- **Tolerates 4-kV Human-Body Model (HBM) ESD**
- **Packaged in Thin Shrink Small-Outline Package (TSSOP) With 20-Mil Terminal Pitch**
- **Consumes Less Than 1 mW When Disabled**
- **Wide Phase-Lock Input Frequency Range 31 MHz to 68 MHz**
- **No External Components Required for PLL**
- **Inputs Meet or Exceed the Standard Requirements of ANSI EIA/TIA-644 Standard**
- **Improved Replacement for the SN75LVDS86 and NSC DS90C364**
- **Improved Jitter Tolerance**
- **Qualified for Automotive Applications**

DGG PACKAGE
(TOP VIEW)



NC − Not connected

DESCRIPTION

The SN65LVDS86A FlatLink™ receiver contains three serial-in 7-bit parallel-out shift registers and four low-voltage differential signaling (LVDS) line receivers in a single integrated circuit. These functions allow receipt of synchronous data from a compatible transmitter, such as the SN75LVDS81, '83, '84, or '85, over four balanced-pair conductors and expansion to 21 bits of single-ended low-voltage LVTTL synchronous data at a lower transfer rate.

When receiving, the high-speed LVDS data is received and loaded into registers at seven times the LVDS input clock (CLKIN) rate. The data is then unloaded to a 21-bit wide LVTTL parallel bus at the CLKIN rate. The SN65LVDS86A presents valid data on the falling edge of the output clock (CLKOUT).

The SN65LVDS86A requires only four line-termination resistors for the differential inputs and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the user(s). The only user intervention is the possible use of the shutdown/clear (SHTDN) active-low input to inhibit the clock and shut off the LVDS receivers for lower power consumption. A low level on this signal clears all internal registers to a low level.

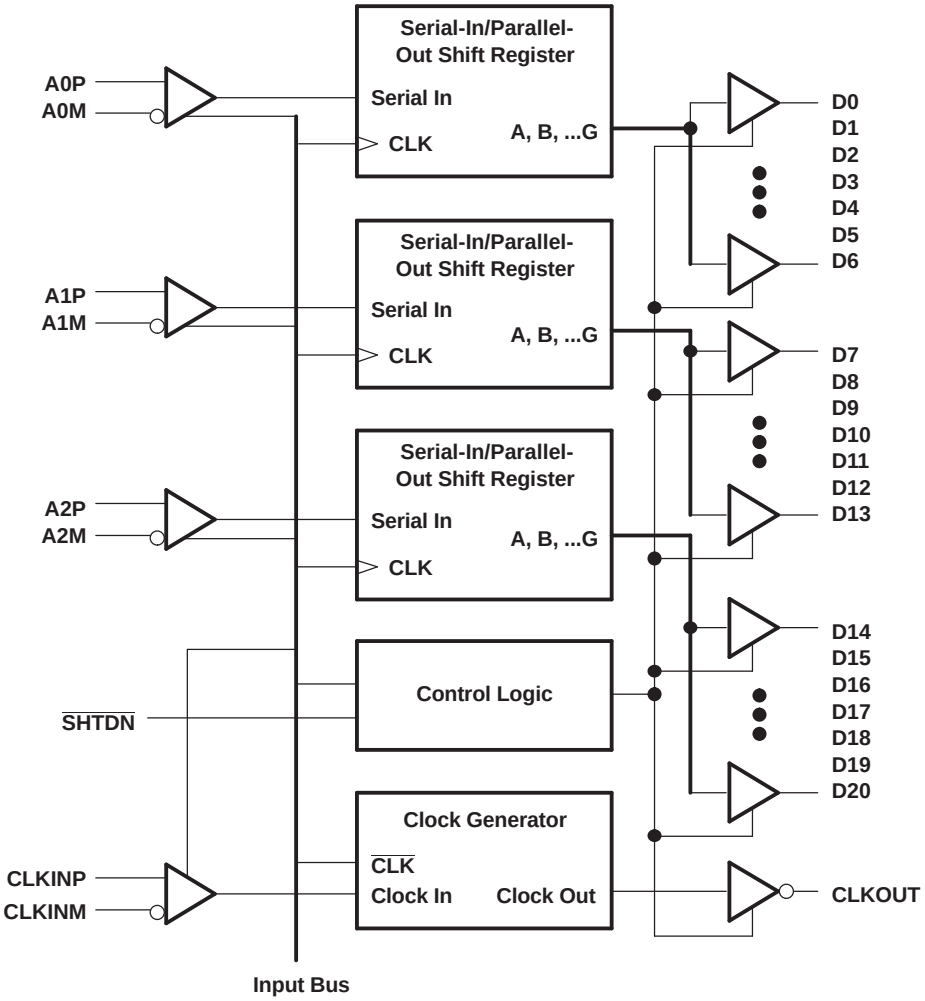
The SN65LVDS86A is characterized for operation over the full automotive temperature range of –40°C to 125°C.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	TSSOP – DGG	Reel of 2000	SN65LVDS86ADGGRQ1	65LVDS86AQ

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTIONAL BLOCK DIAGRAM



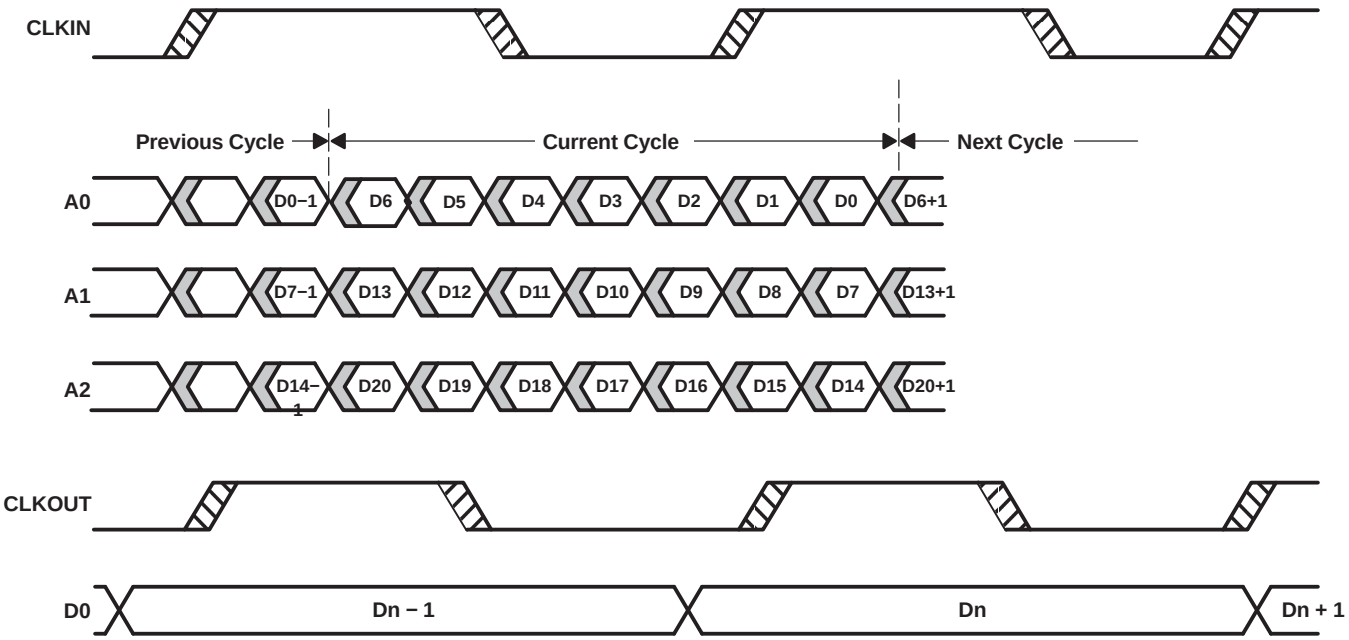
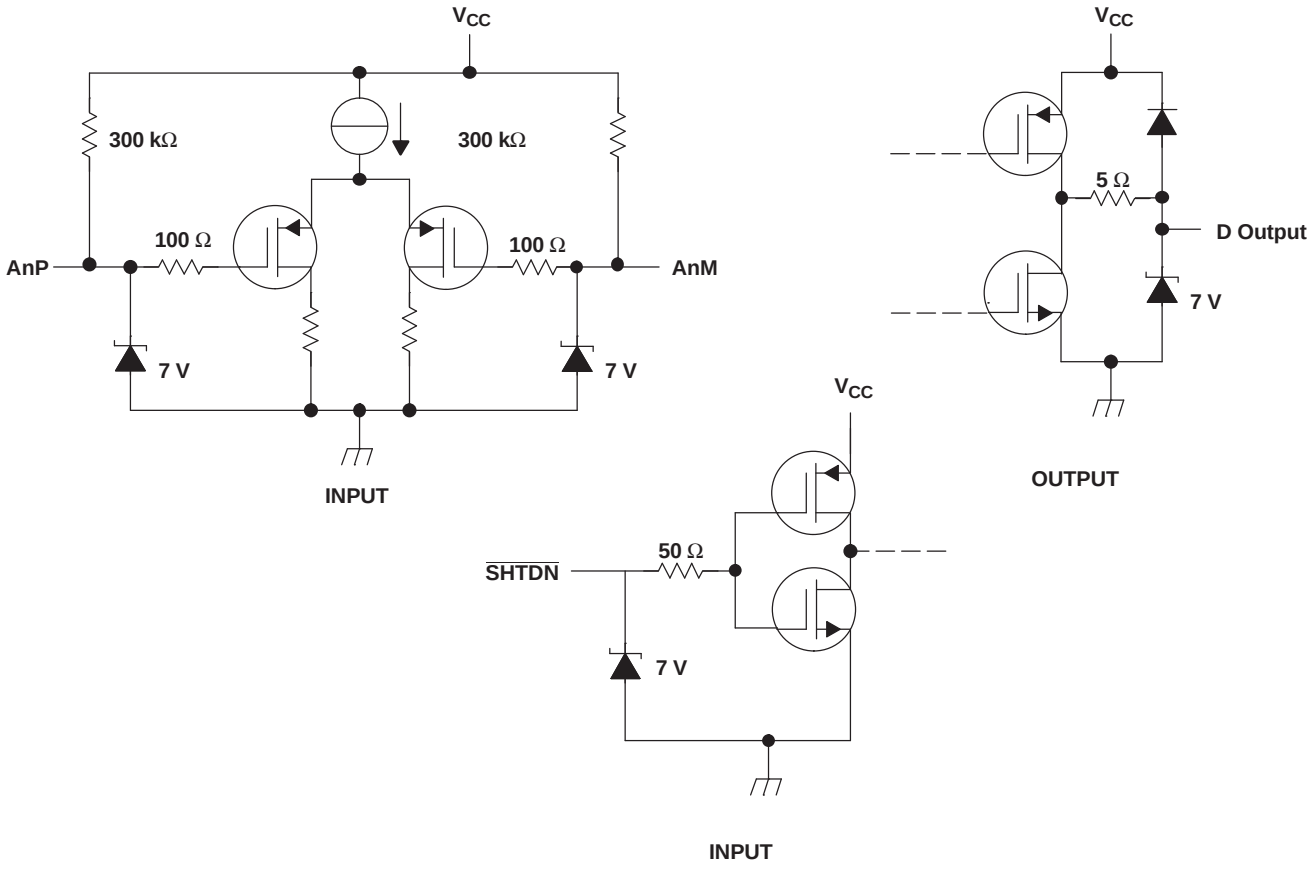


Figure 1. SN65LVDS86A Load and Shift Timing Sequences

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)		–0.5	4	V
	Voltage range at any terminal		–0.5	V_{CC} + 0.5	V
	Electrostatic discharge(3)	All pins (Class 3A)		4	kV
		All pins (Class 2B)		200	V
	Continuous total power dissipation		See Dissipation Rating Table		
T_J	Operating virtual junction temperature range		–40	150	°C
T_{stg}	Storage temperature range		–65	150	°C
	Lead temperature 1,6 mm (1/16 in) from case for 10 s			260	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the GND terminals unless otherwise noted.
(3) This rating is measured using MIL-STD-883C Method, 3015.7.

Dissipation Rating Table

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
DGG	1637 mW	13.1 mW/°C	1048 mW	327 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board mounted and with no air flow.

Recommended Operating Conditions

See Figure 2

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage ($\overline{SHTDN}$)	2			V
V_{IL}	Low-level input voltage ($\overline{SHTDN}$)			0.8	V
$\lvert V_{ID}\rvert$	Magnitude differential input voltage	0.1		0.6	V
V_{IC}	Common-mode input voltage	$\frac{\lvert V_{ID}\rvert}{2}$		$2.4 - \frac{\lvert V_{ID}\rvert}{2}$	V
T_A	Operating free-air temperature	–40		125	°C

Timing Requirements

		MIN	NOM	MAX	UNIT
t_c (1)	Cycle time, input clock	14.7	t_c	32.4	ns

(1) Parameter t_c is defined as the mean duration of a minimum of 32000 clock cycles.

Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going differential input threshold voltage					100	mV
V_{IT-}	Negative-going differential input threshold voltage(2)			–100			mV
V_{OH}	High-level output voltage	I_{OH} = –4 mA		2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA				0.4	V
I_{CC}	Quiescent current (average)	Disabled,	All inputs to GND			280	µA
		Enabled, AnM = 1.4 V,	AnP = 1 V, t_c = 15.38 ns		33	40	mA
		Enabled, Grayscale pattern (see Figure 3),	C_L = 8 pF, t_c = 15.38 ns		43		
		Enabled, Worst-case pattern (see Figure 4),	C_L = 8 pF, t_c = 15.38 ns		68		
I_{IH}	High-level input current ($\overline{SHTDN}$)	$V_{IH} = V_{CC}$				±20	µA
I_{IL}	Low-level input current ($\overline{SHTDN}$)	V_{IL} = 0				±25	µA
I_I	Input current A inputs	0 ≤ V_I ≤ 2.4 V				±20	µA
I_{OZ}	High-impedance output current	V_O = 0 or V_{CC}				±10	µA

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for the negative-going input voltage threshold only.

Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{su}	Setup time, D0–D20 to CLKOUT↓	C_L = 8 pF, See Figure 5	5			ns
t_h	Data hold time, CLKOUT↓ to D0–D20		5			ns
$t_{(RSKM)}$	Receiver input skew margin(2) (see Figure 7)	t_c = 15.38 ns (±0.2%), |Input clock jitter| < 50 ps,(3)	550	700		ps
t_d	Delay time, CLKIN↑ to CLKOUT↓ (see Figure 7)	V_{CC} = 3.3 V, t_c = 15.38 ns (±0.2%), T_A = 25°C	3	5	7	ns
t_{en}	Enable time, $\overline{SHTDN}$ to phase lock	See Figure 7		1		ms
t_{dis}	Disable time, $\overline{SHTDN}$ to off state	See Figure 8		400		ns
t_t	Transition time, output (10% to 90% t_r or t_f) (data only)	C_L = 8 pF		3		ns
t_t	Transition time, output (10% to 90% t_r or t_f) (clock only)	C_L = 8 pF		1.5		ns
t_w	Pulse duration, output clock			0.50 t_c		ns

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) The parameter $t_{(RSKM)}$ is the timing margin available to allocate to the transmitter and interconnection skews and clock jitter. The value of this parameter at clock periods other than 15.38 ns can be calculated from t_{RSKM} = tc/14 – 550 ps.
(3) |Input clock jitter| is the magnitude of the change in input clock period.

PARAMETER MEASUREMENT INFORMATION

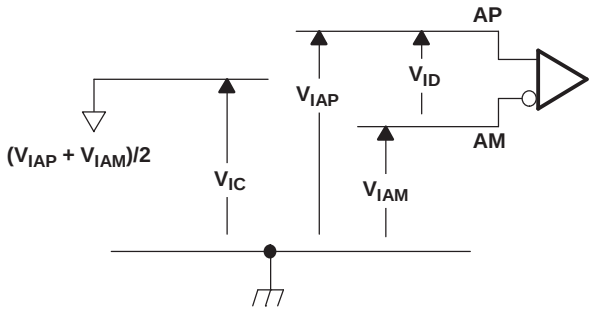
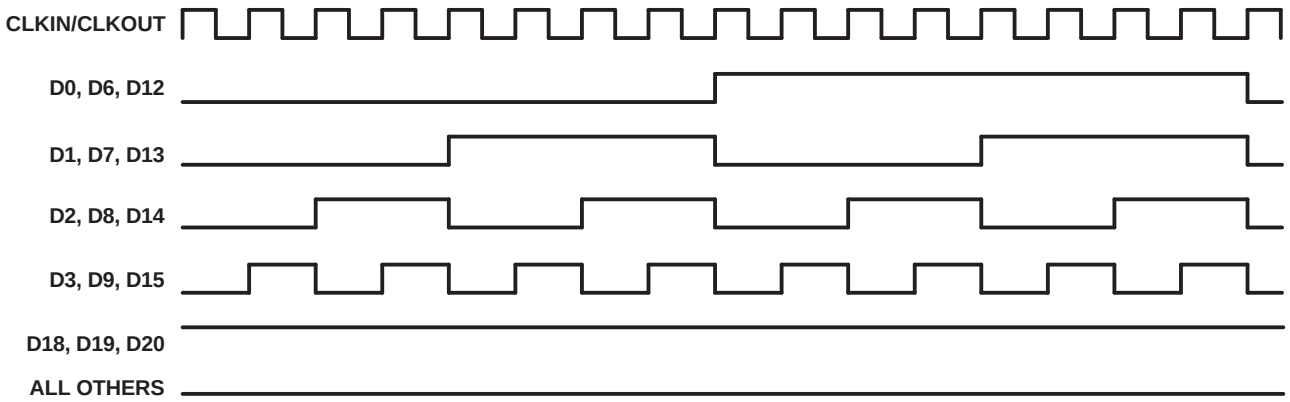
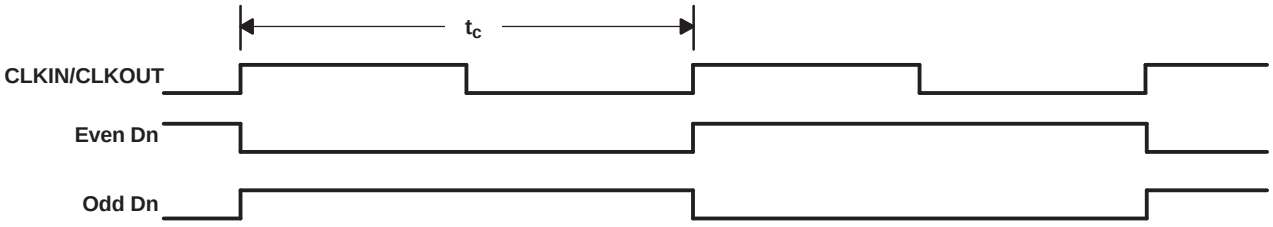


Figure 2. Voltage Definitions



A. The 16-grayscale test-pattern test device power consumption for a typical display pattern.

Figure 3. 16-Grayscale Test-Pattern Waveforms



A. The worst-case test pattern produces nearly the maximum switching frequency for all of the LVTTL outputs.

Figure 4. Worst-Case Test-Pattern Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

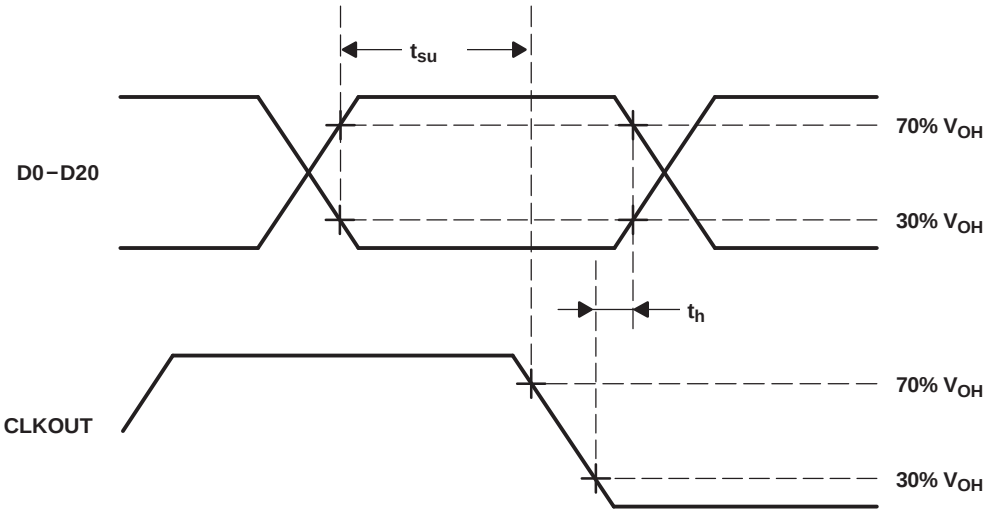
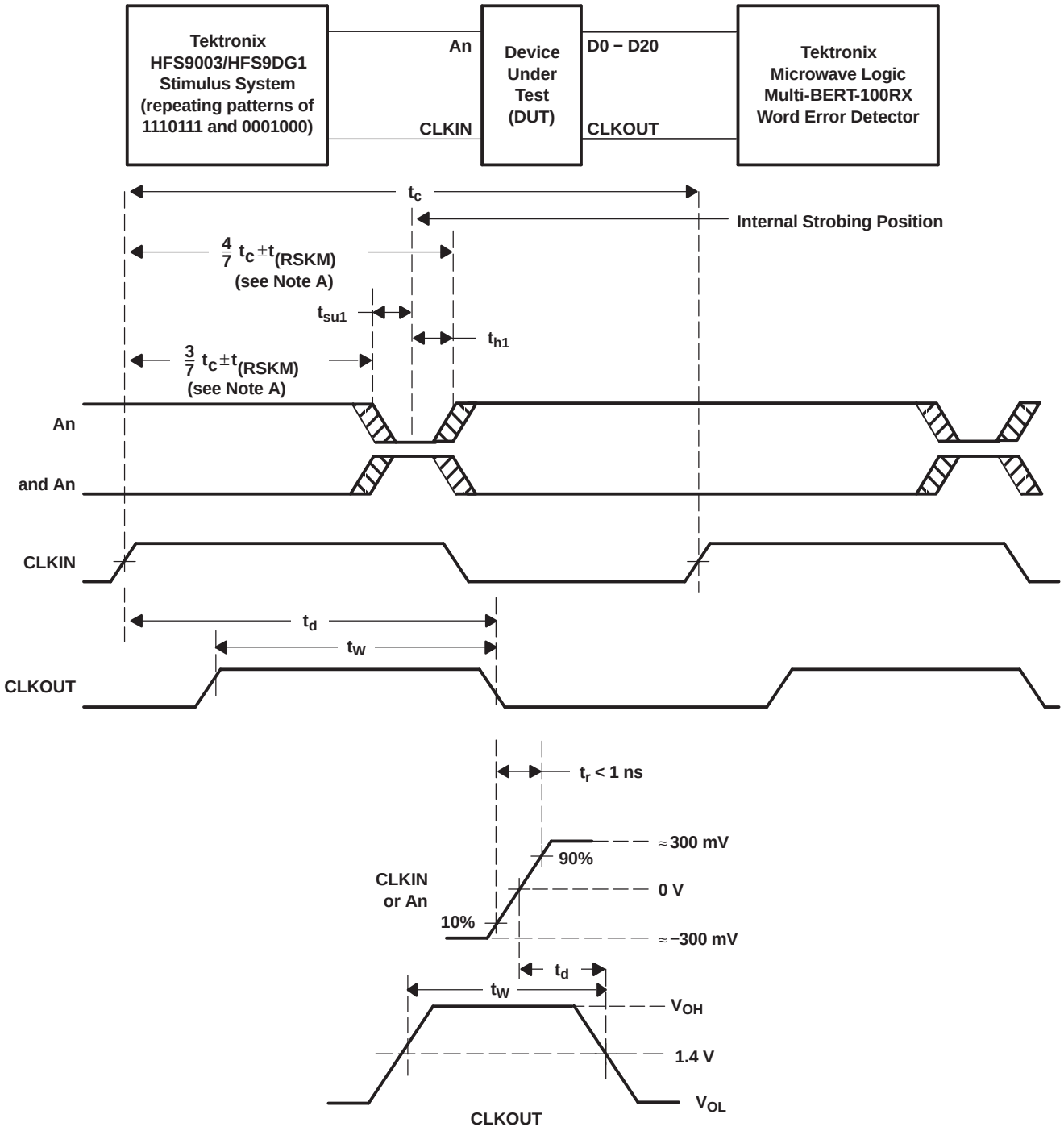


Figure 5. Setup and Hold Time Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



A. CLKIN is advanced or delayed with respect to data until errors are observed at the receiver outputs. The advance or delay is then reduced until there are no data errors observed. The magnitude of the advance or delay is $t_{(RSKM)}$.

Figure 6. Receiver Input Skew Margin, Setup/Hold Time, and Delay Time Definitions

PARAMETER MEASUREMENT INFORMATION (continued)

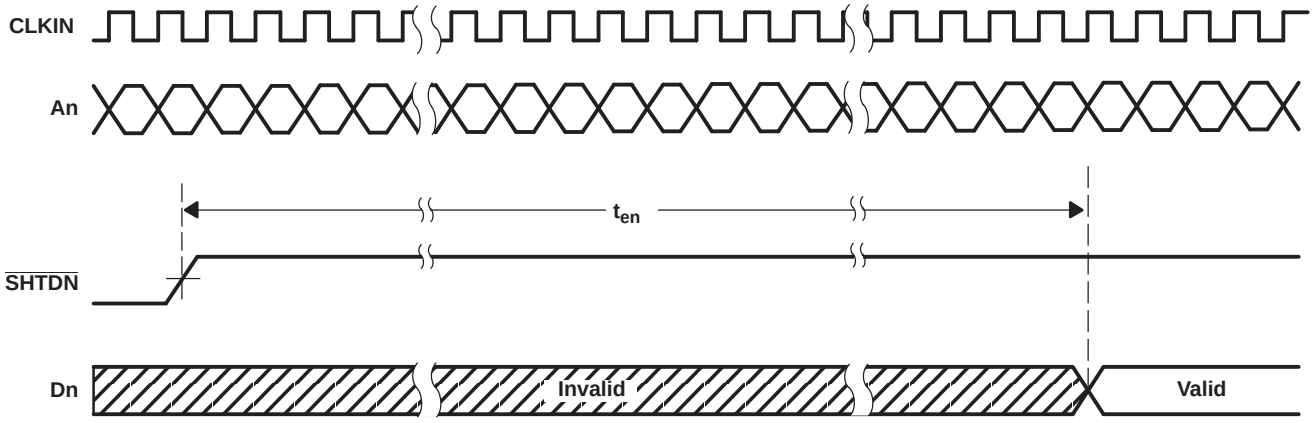


Figure 7. Enable Time Waveforms

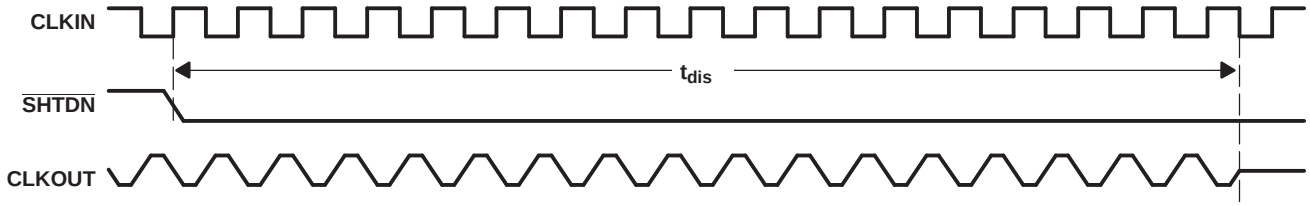


Figure 8. Disable Time Waveforms

TYPICAL CHARACTERISTICS

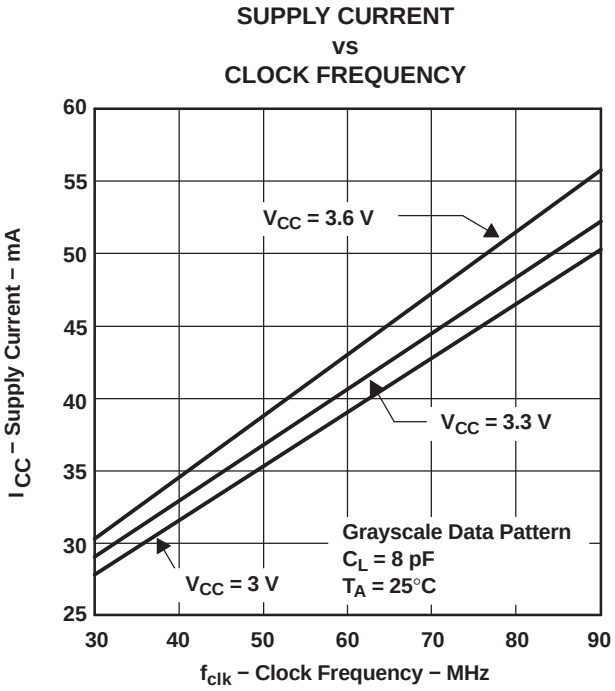
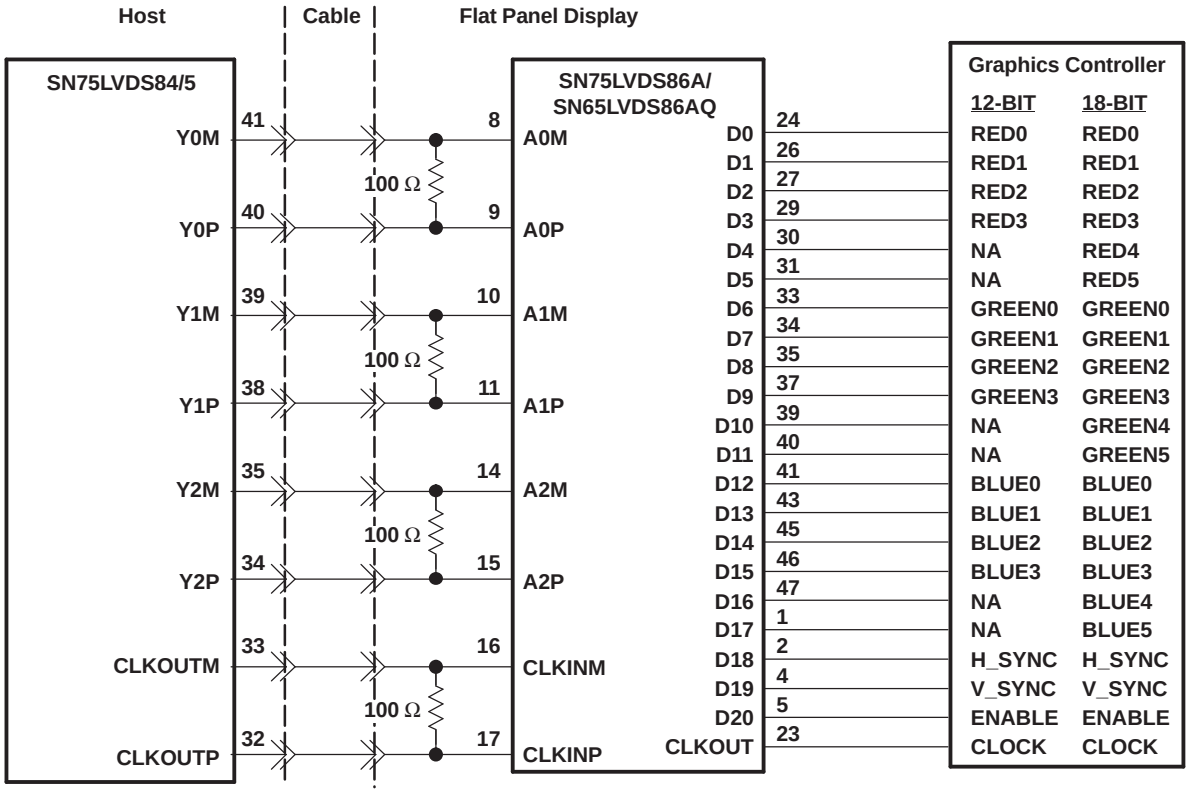


Figure 9. RMS Grayscale I_{CC} vs Clock Frequency

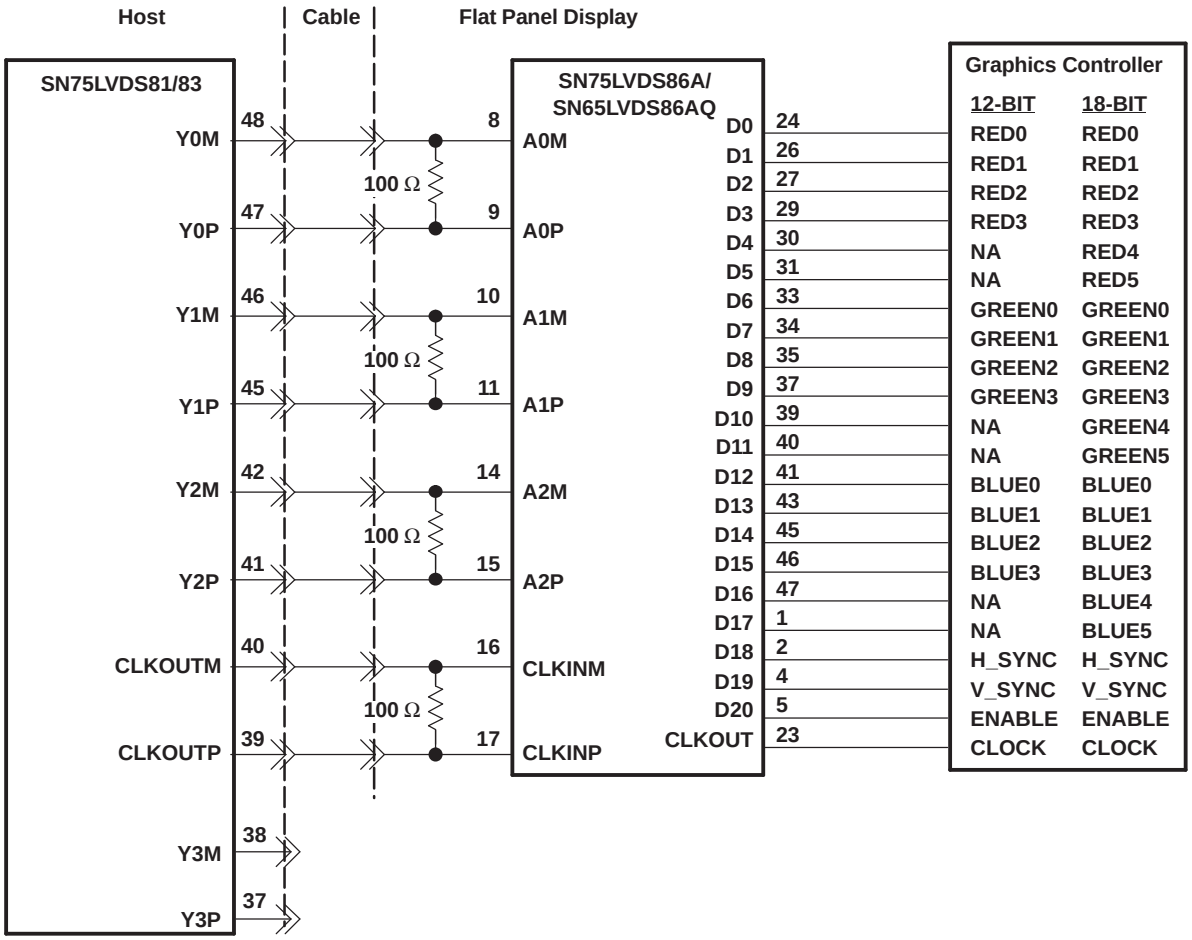
APPLICATION INFORMATION



A. The four 100-Ω terminating resistors are recommended to be 0603 types.

B. NA – not applicable, these unused inputs should be left open.

Figure 10. 18-Bit Color Host to Flat Panel Display Application



A. The four 100-Ω terminating resistors are recommended to be 0603 types.

B. NA – not applicable, these unused inputs should be left open.

Figure 11. 24-Bit Color Host to 18-Bit Color LCD Panel Display Application

See the *FLatLink Designer's Guide* (literature number SLLA012) for more application information.

Changes from Original (August 2006) to Revision A **Page**

- Changed Wide Phase-Lock Input Frequency Range lower limit from 10 MHz to 31 MHz 1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDS86AQDGGG4	ACTIVE	TSSOP	DGG	48	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	65LVDS86AQ	Samples
SN65LVDS86AQDGGRG4	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	65LVDS86AQ	Samples
SN65LVDS86AQDGGRQ1	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	65LVDS86AQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

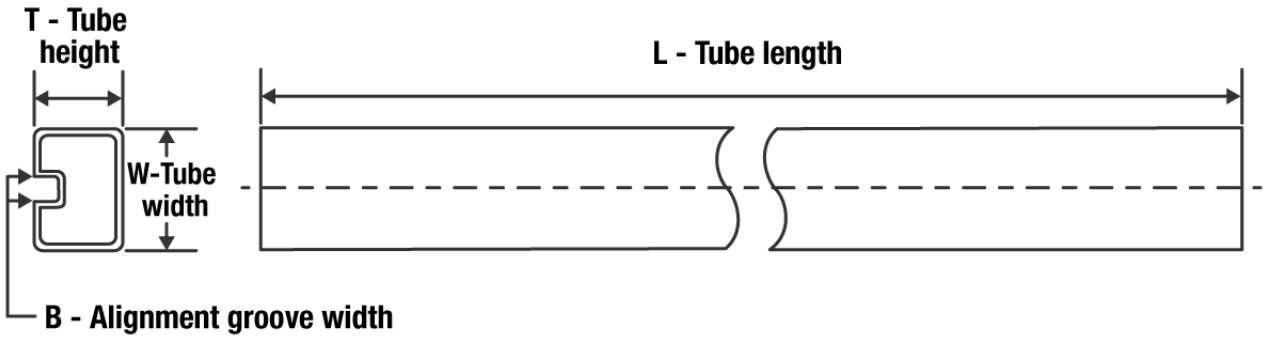
OTHER QUALIFIED VERSIONS OF SN65LVDS86A-Q1 :

- Catalog: SN65LVDS86A

NOTE: Qualified Version Definitions:

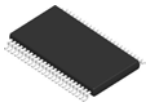
- Catalog - TI's standard catalog product

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LVDS86AQDGGG4	DGG	TSSOP	48	40	530	11.89	3600	4.9

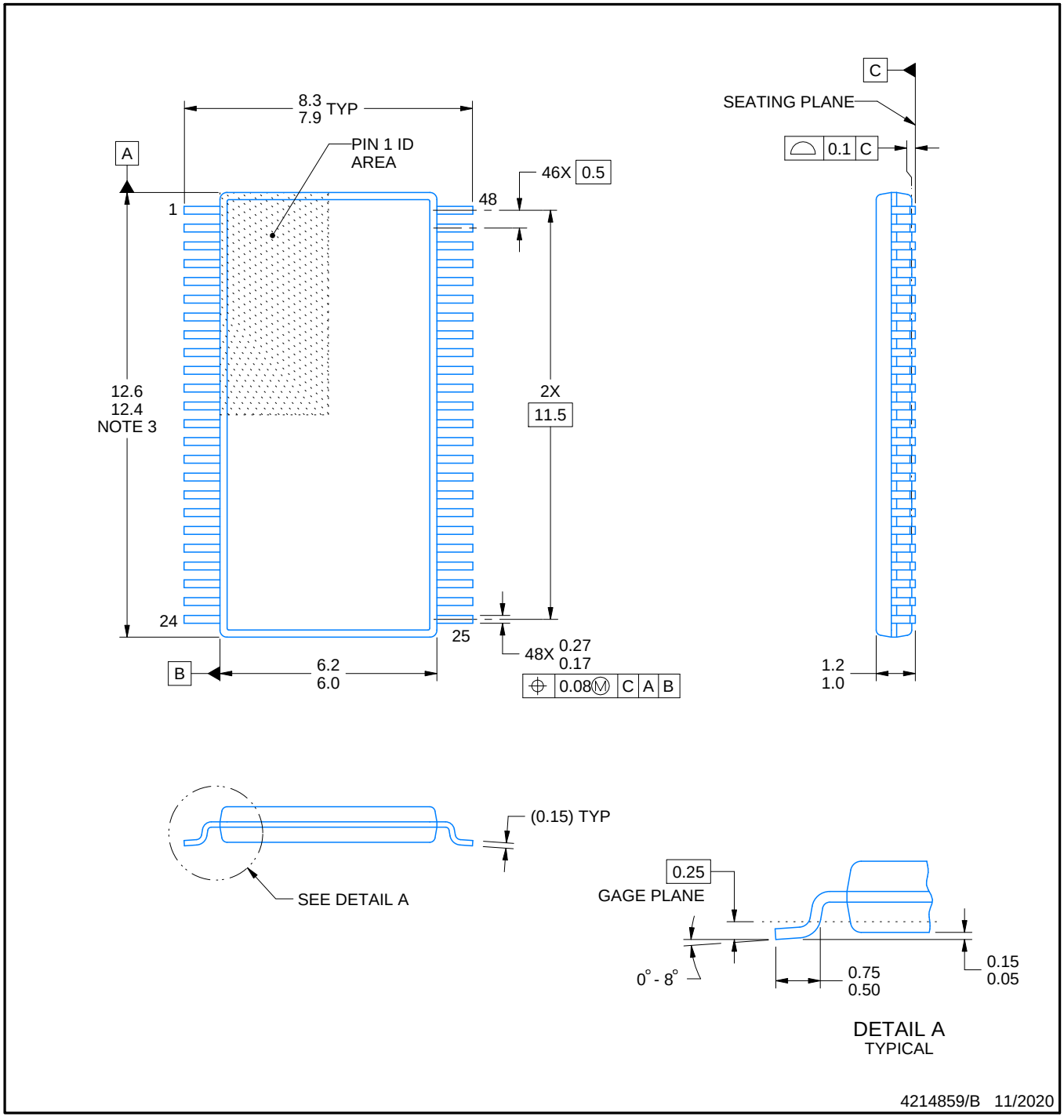


PACKAGE OUTLINE

DGG0048A

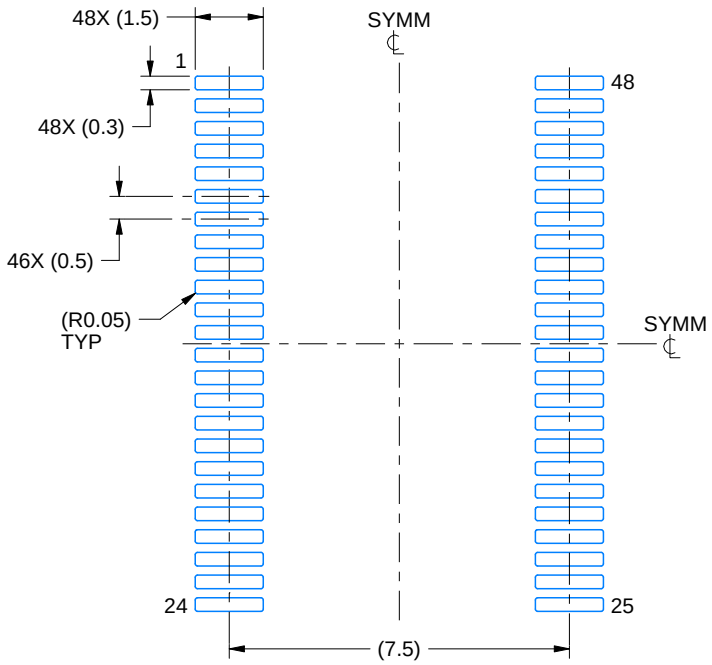
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

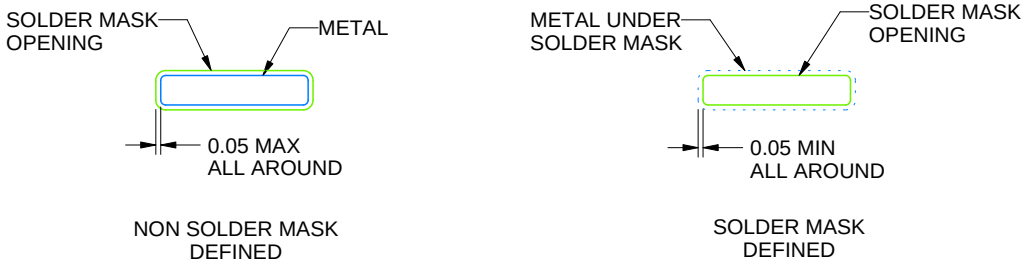


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

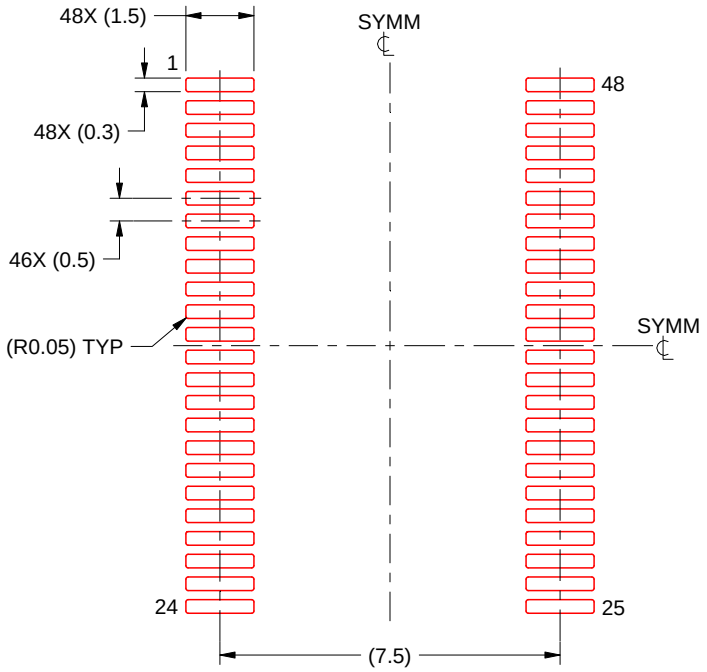


SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

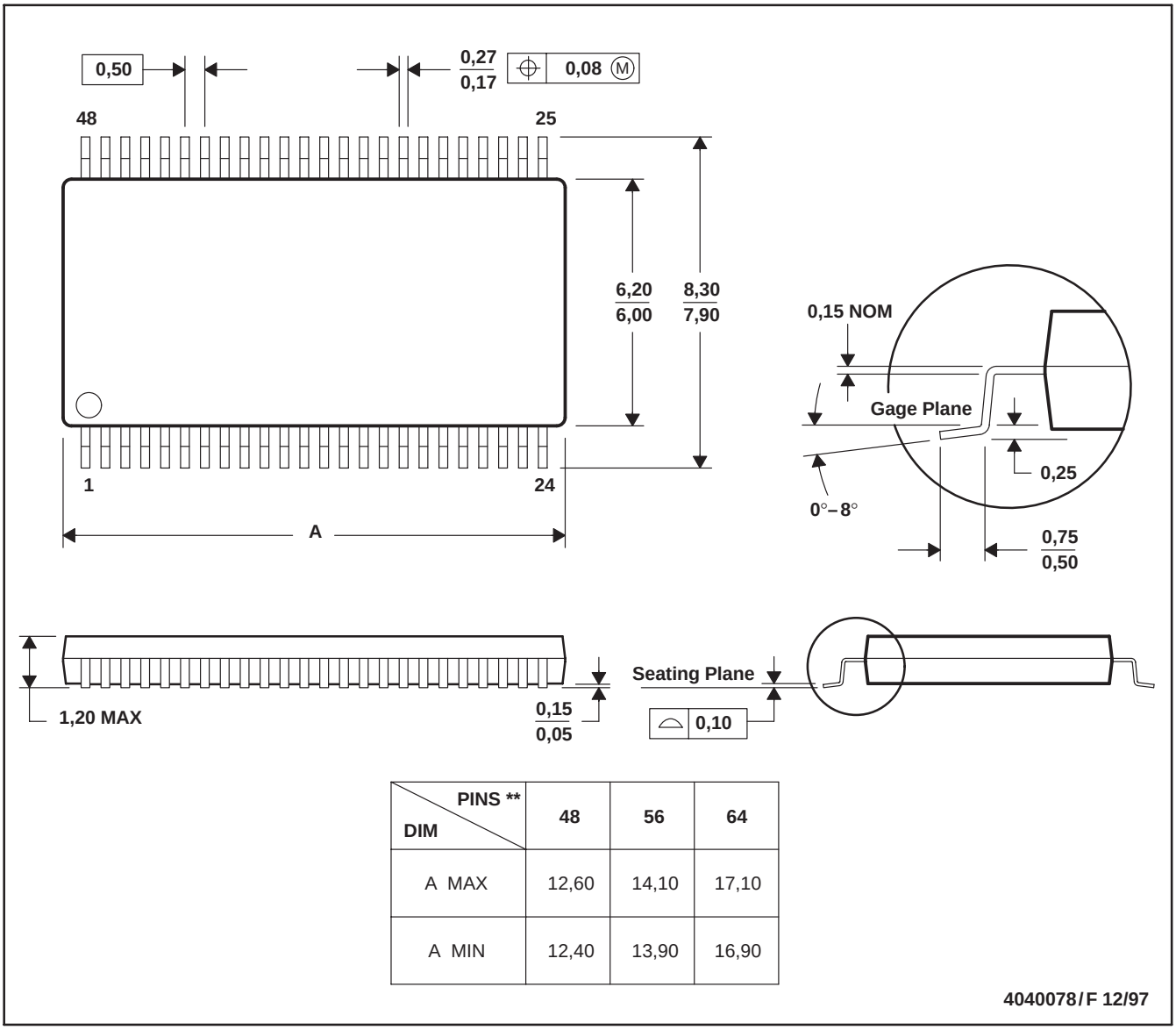
4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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