SNx4AHC157 Quadruple 2-Line To 1-Line Data Selectors/Multiplexers

1 Features

- Operating range 2V to 5.5V
- Latch-up performance exceeds 250mA per JESD 17
- ESD Protection Exceeds JESD 22:
  - 2000V Human-Body Model (A114-A)
  - 200V Machine Model (A115-A
  - 1000V Charged-Device Model (C101)

2 Description

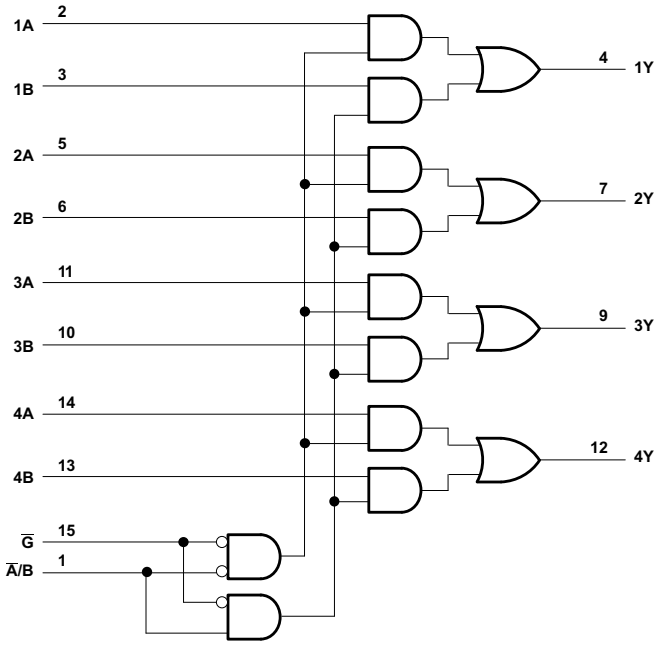
These quadruple 2-line to 1-line data selectors/multiplexers are designed for 2V to 5.5V V_{CC} operation.

The SNx4AHC157 devices feature a common strobe ($\overline{G}$) input. When the strobe is high, all outputs are low. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The devices provide true data.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
SNx4AHC157	D (SOIC, 16)	9.90mm × 6mm	9.90mm × 3.90mm
	DB (SSOP, 16)	6.20mm × 7.8mm	6.20mm × 5.30mm
	N (PDIP, 16)	19.31mm × 9.4mm	19.31mm × 6.35mm
	NS (SOP, 16)	5mm × 6.4mm	5mm × 4.4mm
	PW (TSSOP, 16)	5.00mm × 6.4mm	5.00mm × 4.40mm
	DGV (TVSOP, 16)	3.6mm × 6.4mm	3.6mm × 4.4mm
	RGY (VQFN, 16)	4mm × 3.5mm	4mm × 3.5mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, RGY, and W packages.

Logic Diagram (Positive Logic)

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3 Pin Configuration and Functions

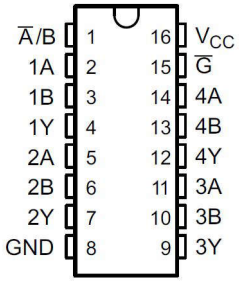


Figure 3-1. SN54AHC157 J or W Package, SN74AHC157 D, DB, DGV, N, NS, or, PW Package (Top View)

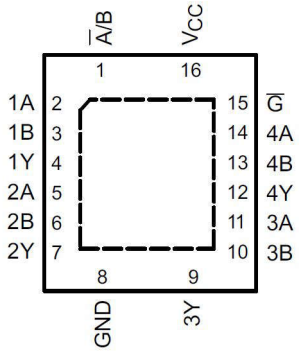
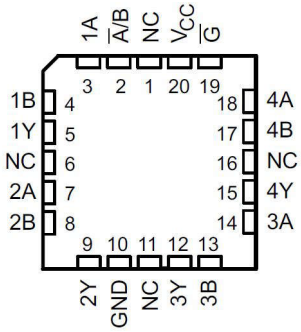


Figure 3-2. SN74AHC157 RGY Package, (Top View)



NC − No internal connection

Figure 3-3. SN54AHC157 FK Package, (Top View)

Table 3-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
$\overline{A}$/B	1	I	Address select
1A	2	I	Channel 1, data input A
1B	3	I	Channel 1, data input B
1Y	4	O	Channel 1, data output
2A	5	I	Channel 2, data input A
2B	6	I	Channel 2, data input B
2Y	7	O	Channel 2, data output
GND	8	G	Ground
3Y	9	O	Channel 3, data output
3B	10	I	Channel 3, data input B
3A	11	I	Channel 3, data input A
4Y	12	O	Channel 4, data output
4B	13	I	Channel 4, data input B
4A	14	I	Channel 4, data input A
$\overline{G}$	15	I	Output strobe, active low
V_{CC}	16	P	Positive supply
Thermal pad[2]		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) Signal Types: I = Input, O = Output, I/O = Input or Output, P = Power, G = Ground.
(2) WBQB package only.

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I (2)	Input voltage range		–0.5	7	V
V_O (2)	Output voltage range		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	(V_I < 0)		–20	mA
I_{OK}	Output clamp current	(V_O < 0 or V_O > V_{CC})		±20	mA
I_O	Continuous output current	(V_O = 0 to V_{CC})		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

4.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101	±1000	

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			SN54AHC157		SN74AHC157		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC}= 2 V	1.5		1.5		V
		V_{CC}= 3V	2.1		2.1		
		V_{CC}= 5.5 V	3.85		3.85		
V_{IL}	Low-level Input voltage	V_{CC}= 2 V		0.5		0.5	V
		V_{CC}= 3 V		0.9		0.9	
		V_{CC}= 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC}= 2 V		–0.05		–0.05	μA
		V_{CC}= 3.3 V ± 0.3 V		–4		–4	
		V_{CC}= 5 V ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC}= 2 V		0.05		0.05	μA
		V_{CC}= 3.3 V ± 0.3 V		4		4	
		V_{CC}= 5 V ± 0.5 V		8		8	
Δt/Δv	Input Transition rise or fall rate	V_{CC}= 3.3 V ± 0.3 V		100		100	ns/V
		V_{CC}= 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

4.4 Thermal Information

THERMAL METRIC[1]		SNx4AHC157							UNIT
		D	DB	DGV	N	NS	PW	RGY	
		16							
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93.8	82	120	67	64	135.9	52.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

4.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			T_A = –55°C TO 125°C		T_A = –40°C TO 85°C		T_A = –40°C TO 125°C Recommended		UNIT
						SN54AHC157		SN74AHC157		SN74AHC157		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 µA	2 V	1.9	2		1.9		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		4.4		
	I_{OH} = –4 mA	3 V	2.58			2.48		2.48		2.48		
	I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		3.8		
V_{OL}	I_{OL} = 50 µA	2 V			0.1		0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1		0.1	
	I_{OH} = 4 mA	3 V			0.36		0.5		0.44		0.5	
	I_{OH} = 8 mA	4.5 V			0.36		0.5		0.44		0.5	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1[1]		±1		±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40		40	µA
C_i	V_I = V_{CC} or GND	5 V		2	10				10			pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at VCC = 0 V.

4.6 Switching Characteristics, V_{CC} = 3.3V ± 0.3V

over recommended operating free-air temperature range, V_{CC} = 3.3V ± 0.3V (unless otherwise noted) (see Load Circuit And Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C		T_A = –55°C TO 125°C		T_A = –40°C TO 85°C		T_A = –40°C TO 125°C Recommended		UNIT
						SN54AHC157		SN74AHC157		SN74AHC157		
				TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	C_L = 15pF	6.2[1]	9.7[1]	1[1]	11.5[1]	1	11.5	1	11.5	ns
t_{PHL}				6.2[1]	9.7[1]	1[1]	11.5[1]	1	11.5	1	11.5	
t_{PLH}	$\overline{A}$/ $\overline{B}$	Y	C_L = 15pF	8.4[1]	13.2[1]	1[1]	15.5[1]	1	15.5	1	15.5	ns
t_{PHL}				8.4[1]	13.2[1]	1[1]	15.5[1]	1	15.5	1	15.5	
t_{PLH}	$\overline{G}$	Y	C_L = 15pF	8.7[1]	13.6[1]	1[1]	16[1]	1	16	1	16	ns
t_{PHL}				8.7[1]	13.6[1]	1[1]	16[1]	1	16	1	16	
t_{PLH}	A or B	Y	C_L = 50pF	8.7	13.2	1	15	1	15	1	15	ns
t_{PHL}				8.7	13.2	1	15	1	15	1	15	
t_{PLH}	$\overline{A}$/ $\overline{B}$	Y	C_L = 50pF	10.9	16.7	1	19	1	19	1	19	ns
t_{PHL}				10.9	16.7	1	19	1	19	1	19	

over recommended operating free-air temperature range, V_{CC} = 3.3V ± 0.3V (unless otherwise noted) (see Load Circuit And Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C		T_A = –55°C TO 125°C		T_A = –40°C TO 85°C		T_A = –40°C TO 125°C Recommended		UNIT
						SN54AHC157		SN74AHC157		SN74AHC157		
				TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	$\overline{G}$	Y	C_L = 50pF	11.2	17.1	1	19.5	1	19.5	1	19.5	ns
t_{PHL}				11.2	17.1	1	19.5	1	19.5	1	19.5	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

4.7 Switching Characteristics, V_{CC} = 5V ± 0.5V

over recommended operating free-air temperature range, V_{CC} = 5V ± 0.5V (unless otherwise noted) (see Load Circuit And Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C		T_A = –55°C TO 125°C		T_A = –40°C TO 85°C		T_A = –40°C TO 125°C Recommended		UNIT
						SN54AHC157		SN74AHC157		SN74AHC157		
				TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	C_L = 15pF	4.1(1)	6.4(1)	1(1)	7.5(1)	1	7.5	1	7.5	ns
t_{PHL}				4.1(1)	6.4(1)	1(1)	7.5(1)	1	7.5	1	7.5	
t_{PLH}	$\overline{A}$/ $\overline{B}$	Y	C_L = 15pF	5.3(1)	8.1(1)	1(1)	9.5(1)	1	9.5	1	9.5	ns
t_{PHL}				5.3(1)	8.1(1)	1(1)	9.5(1)	1	9.5	1	9.5	
t_{PLH}	$\overline{G}$	Y	C_L = 15pF	5.6(1)	8.6(1)	1(1)	10(1)	1	10	1	10	ns
t_{PHL}				5.6(1)	8.6(1)	1(1)	10(1)	1	10	1	10	
t_{PLH}	A or B	Y	C_L = 50pF	5.6(1)	8.4(1)	1(1)	9.5(1)	1	9.5	1	9.5	ns
t_{PHL}				5.6(1)	8.4(1)	1(1)	9.5(1)	1	9.5	1	9.5	
t_{PLH}	$\overline{A}$/ $\overline{B}$	Y	C_L = 50pF	6.8(1)	10.1(1)	1(1)	11.5(1)	1	11.5	1	11.5	ns
t_{PHL}				6.8(1)	10.1(1)	1(1)	11.5(1)	1	11.5	1	11.5	
t_{PLH}	$\overline{G}$	Y	C_L = 50pF	7.1(1)	10.6(1)	1(1)	12(1)	1	12	1	12	ns
t_{PHL}				7.1(1)	10.6(1)	1(1)	12(1)	1	12	1	12	

4.8 Noise Characteristics

V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C(1)

PARAMETER		SN74AHC157			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}			–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.8		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

(1) Characteristics are for surface-mount packages only.

4.9 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	11	pF

4.10 Typical Characteristics

T_A = 25°C (unless otherwise noted)

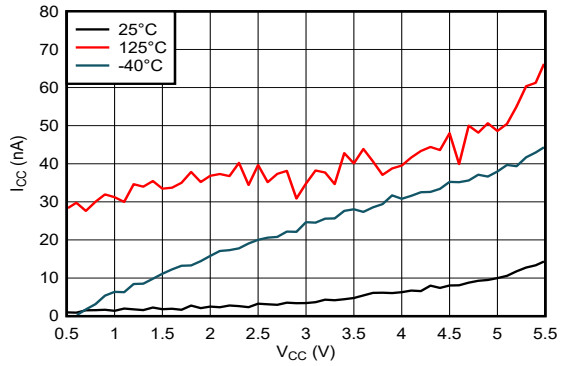


Figure 4-1. Supply Current Across Supply Voltage

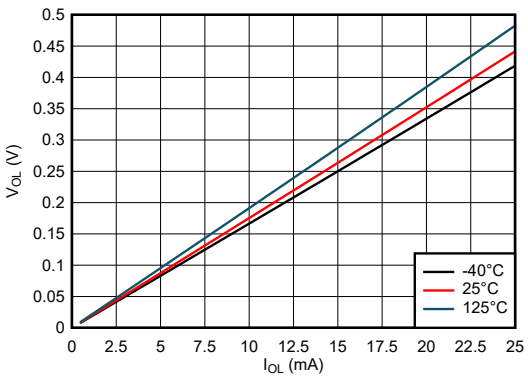


Figure 4-2. Output Voltage vs Current in LOW State; 5V Supply

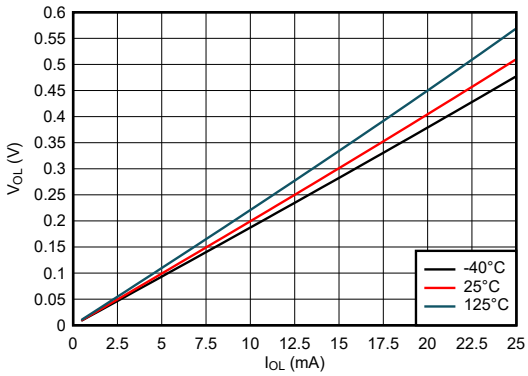


Figure 4-3. Output Voltage vs Current in LOW State; 3.3V Supply

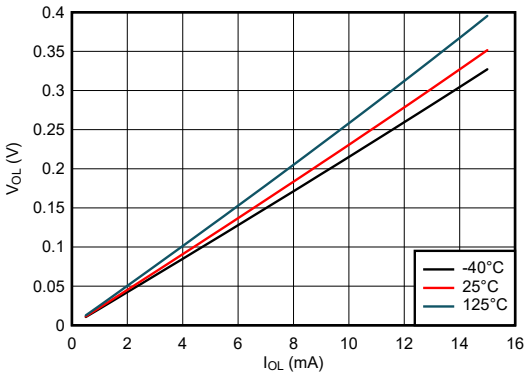
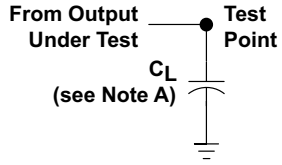
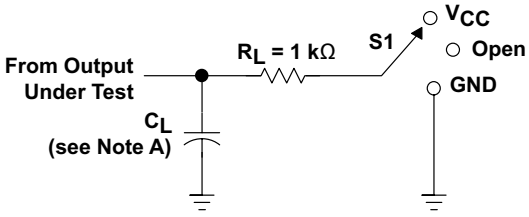


Figure 4-4. Output Voltage vs Current in LOW State; 2.5V Supply

5 Parameter Measurement Information

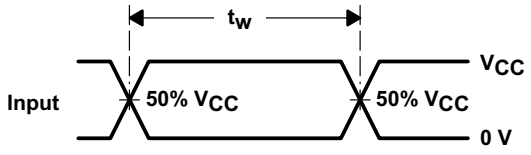


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

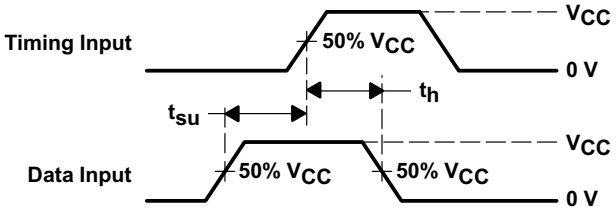


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

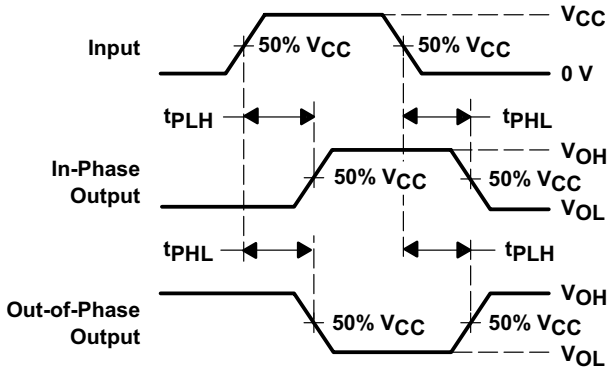
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



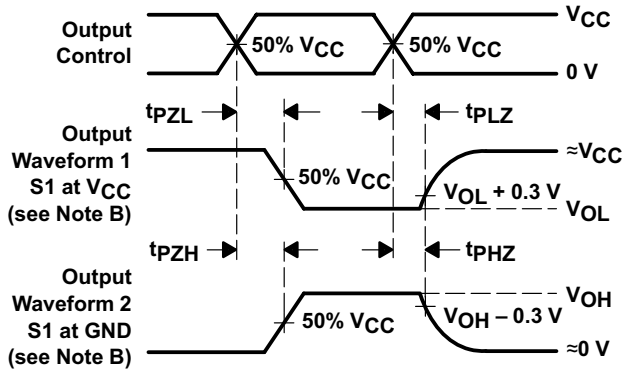
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



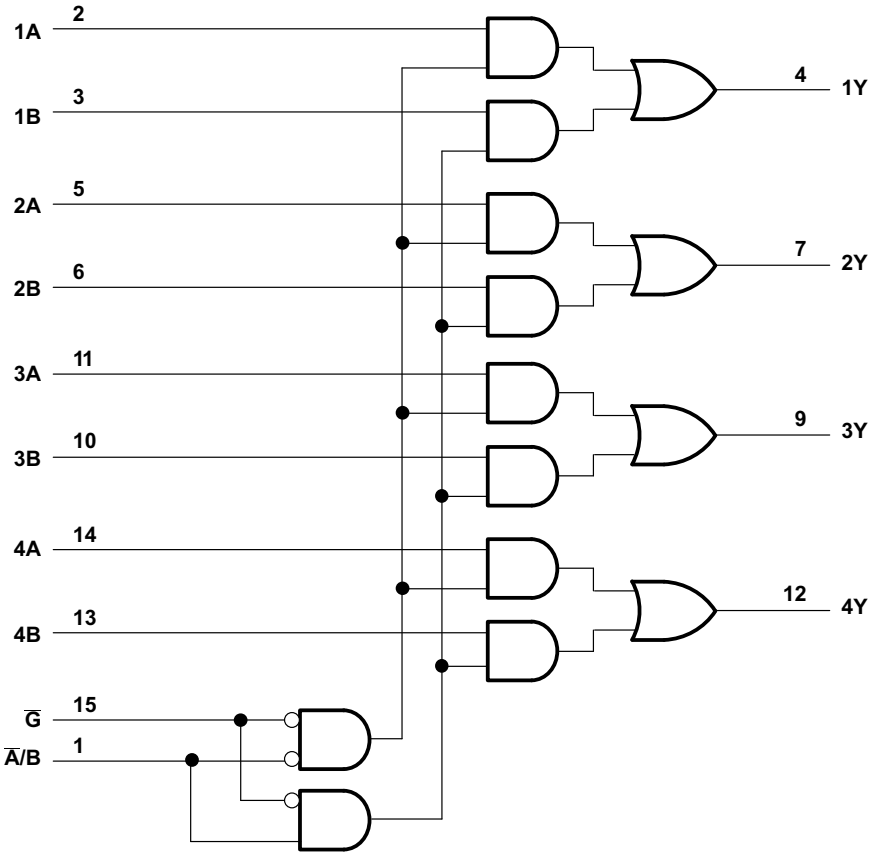
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 5-1. Load Circuit And Voltage Waveforms

6 Detailed Description

6.1 Functional Block Diagram



Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, RGY, and W packages.

Figure 6-1. Logic Diagram (Positive Logic)

6.2 Device Functional Modes

Table 6-1. Function Table

INPUTS				OUTPUT
$\overline{G}$	$\overline{A}$/B	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Section 4.3* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1µf is recommended; if there are multiple V_{CC} pins, then 0.01µf or 0.022 µf is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1µf and a 1µf are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in Layout Diagram are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

7.2.2 Layout Example

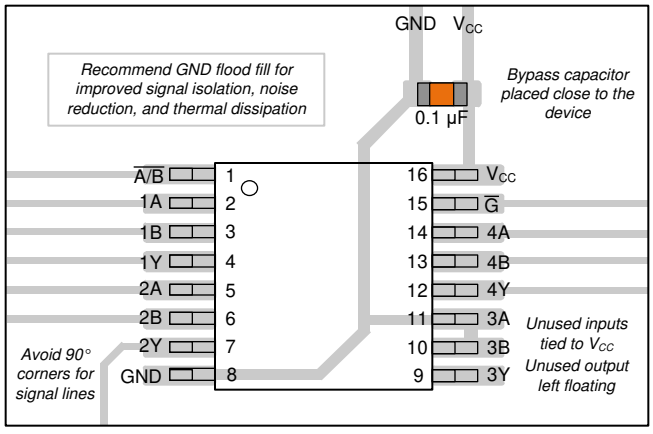


Figure 7-1. Example Layout for the SNx4AHC157

8 Device and Documentation Support

8.1 Documentation Support (Analog)

8.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AHC157	Click here	Click here	Click here	Click here	Click here
SN74AHC157	Click here	Click here	Click here	Click here	Click here

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision K (April 2024) to Revision L (July 2024) — **Page**

- Updated thermal values for RθJA: D = 73 to 93.8, RGY = 39 to 52.9, all values in °C/W 6

Changes from Revision J (June 2013) to Revision K (April 2024) — **Page**

- Added *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Device Functional Modes,*Application and Implementation section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Changed I_{OH} maximums from -50 mA to -0.05 µA 5
- Changed mA (milliamps) to µA (microamps) for I_{OH} and I_{OL} on *Recommended Operating Conditions* table.... 5
- Changed I_{OL} maximums from 50 mA to 0.05 µA 5

- Updated thermal values for PW package from RθJA = 108 to 135.9, all values in °C/W.....6

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9764201Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9764201Q2A SNJ54AHC 157FK	Samples
5962-9764201QEA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9764201QEA SNJ54AHC157J	Samples
5962-9764201QFA	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9764201QFA SNJ54AHC157W	Samples
SN74AHC157D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 125	AHC157	
SN74AHC157DBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA157	Samples
SN74AHC157DGVR	ACTIVE	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA157	Samples
SN74AHC157DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC157	Samples
SN74AHC157N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHC157N	Samples
SN74AHC157NSR	ACTIVE	SOP	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC157	Samples
SN74AHC157PW	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 125	HA157	
SN74AHC157PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	HA157	Samples
SN74AHC157PWRG3	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	HA157	Samples
SN74AHC157RGYR	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA157	Samples
SNJ54AHC157FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9764201Q2A SNJ54AHC 157FK	Samples
SNJ54AHC157J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9764201QEA SNJ54AHC157J	Samples
SNJ54AHC157W	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9764201QFA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										SNJ54AHC157W	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN54AHC157, SN74AHC157 :

- Catalog : SN74AHC157

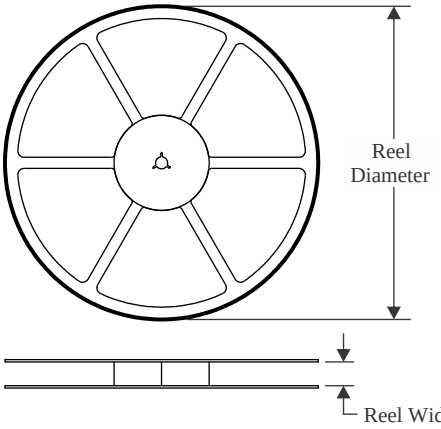
- Automotive : SN74AHC157-Q1, SN74AHC157-Q1
- Military : SN54AHC157

NOTE: Qualified Version Definitions:

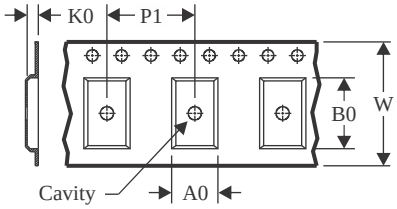
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

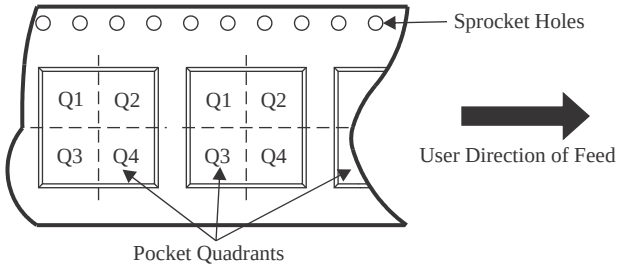


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

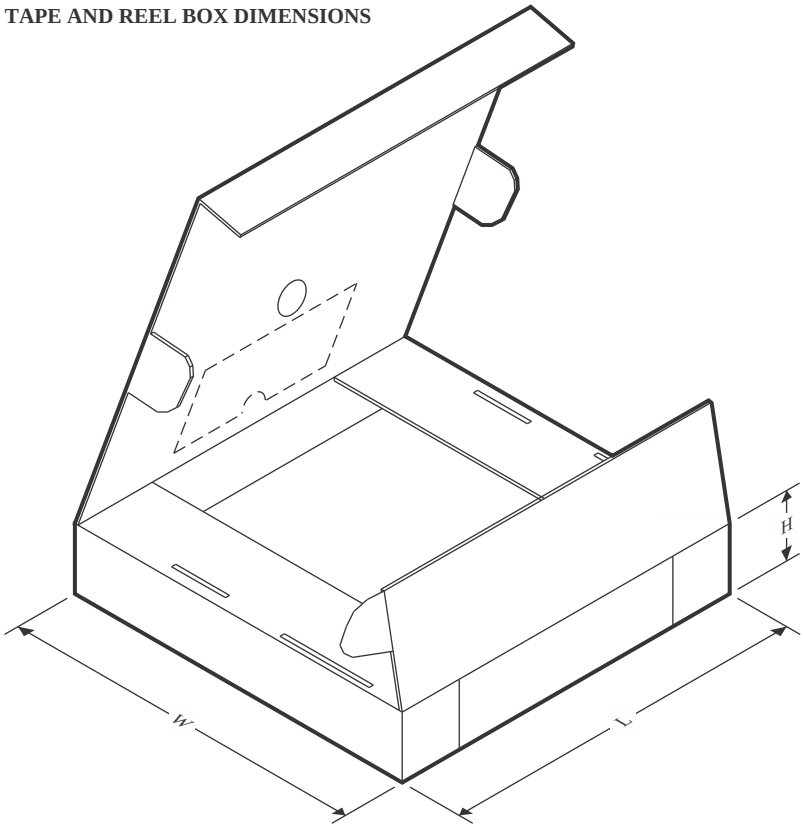
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC157DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC157DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC157DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHC157DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHC157DR	SOIC	D	16	2500	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74AHC157NSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHC157PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC157PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC157PWRG3	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC157RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

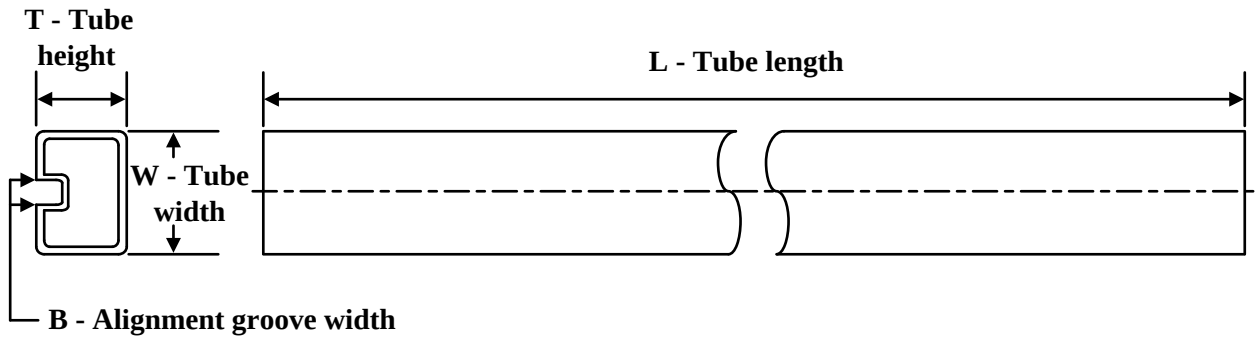
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

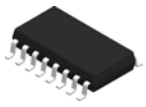
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC157DBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN74AHC157DGVR	TVSOP	DGV	16	2000	356.0	356.0	35.0
SN74AHC157DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74AHC157DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74AHC157DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74AHC157NSR	SOP	NS	16	2000	356.0	356.0	35.0
SN74AHC157PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74AHC157PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74AHC157PWRG3	TSSOP	PW	16	2000	364.0	364.0	27.0
SN74AHC157RGYR	VQFN	RGY	16	3000	360.0	360.0	36.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9764201Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9764201QFA	W	CFP	16	25	506.98	26.16	6220	NA
SN74AHC157N	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHC157N	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54AHC157FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHC157W	W	CFP	16	25	506.98	26.16	6220	NA

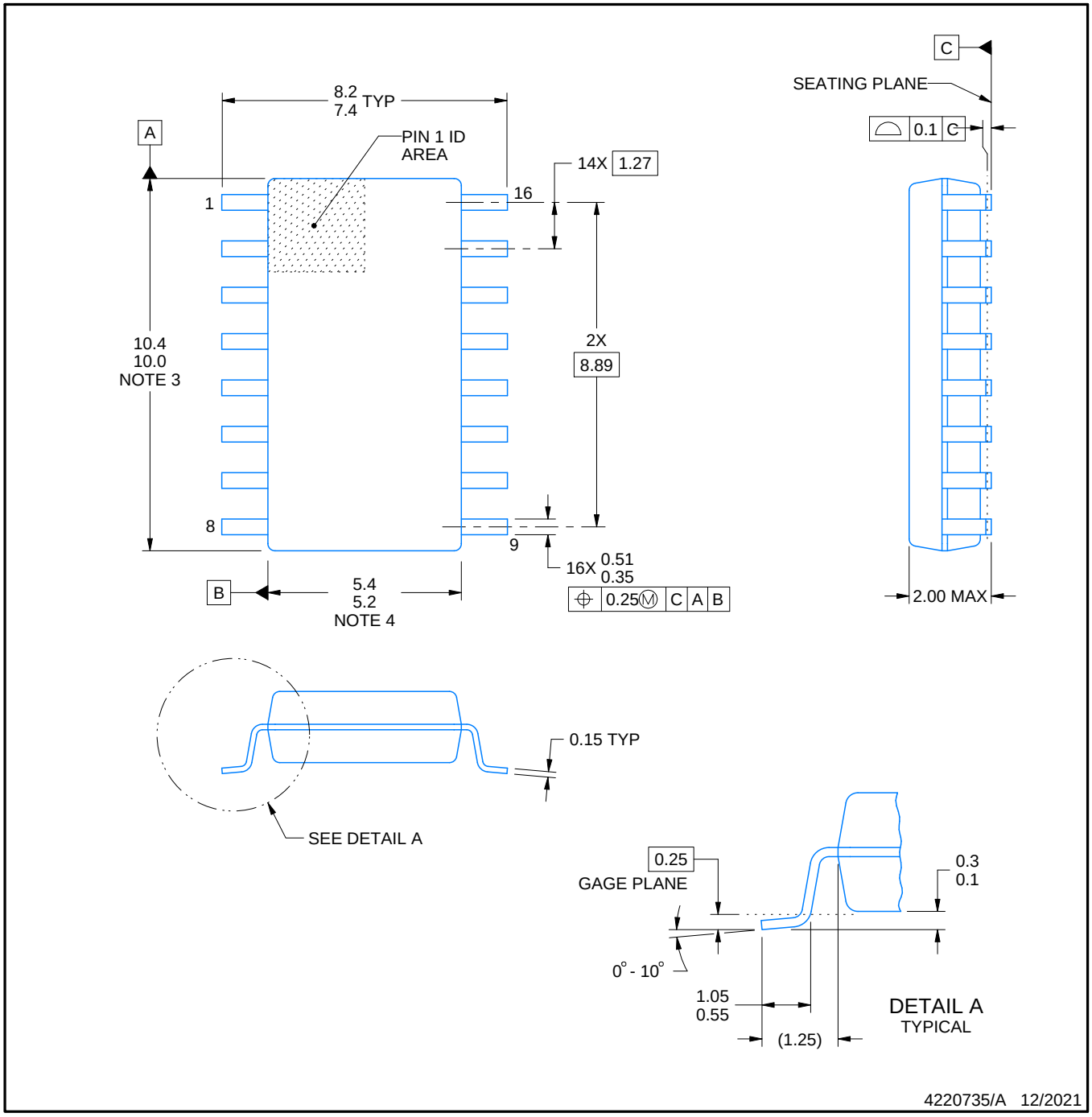


PACKAGE OUTLINE

NS0016A

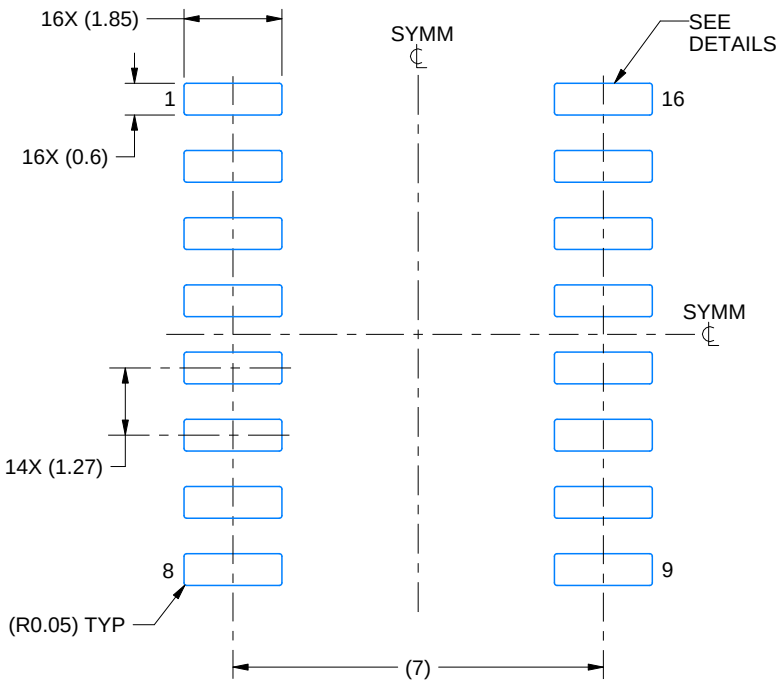
SOP - 2.00 mm max height

SOP

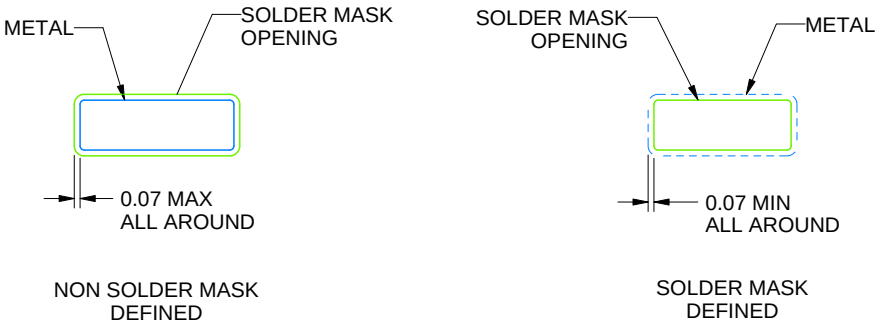


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

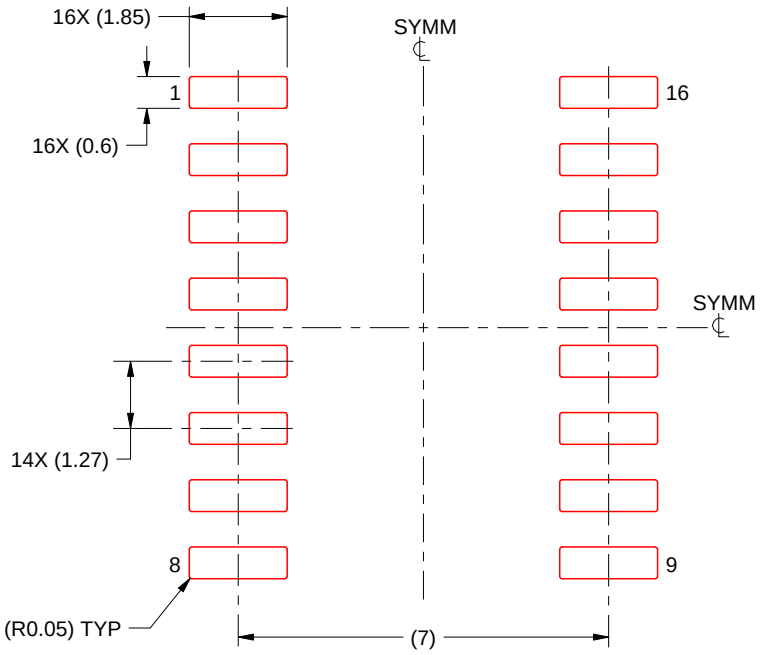
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



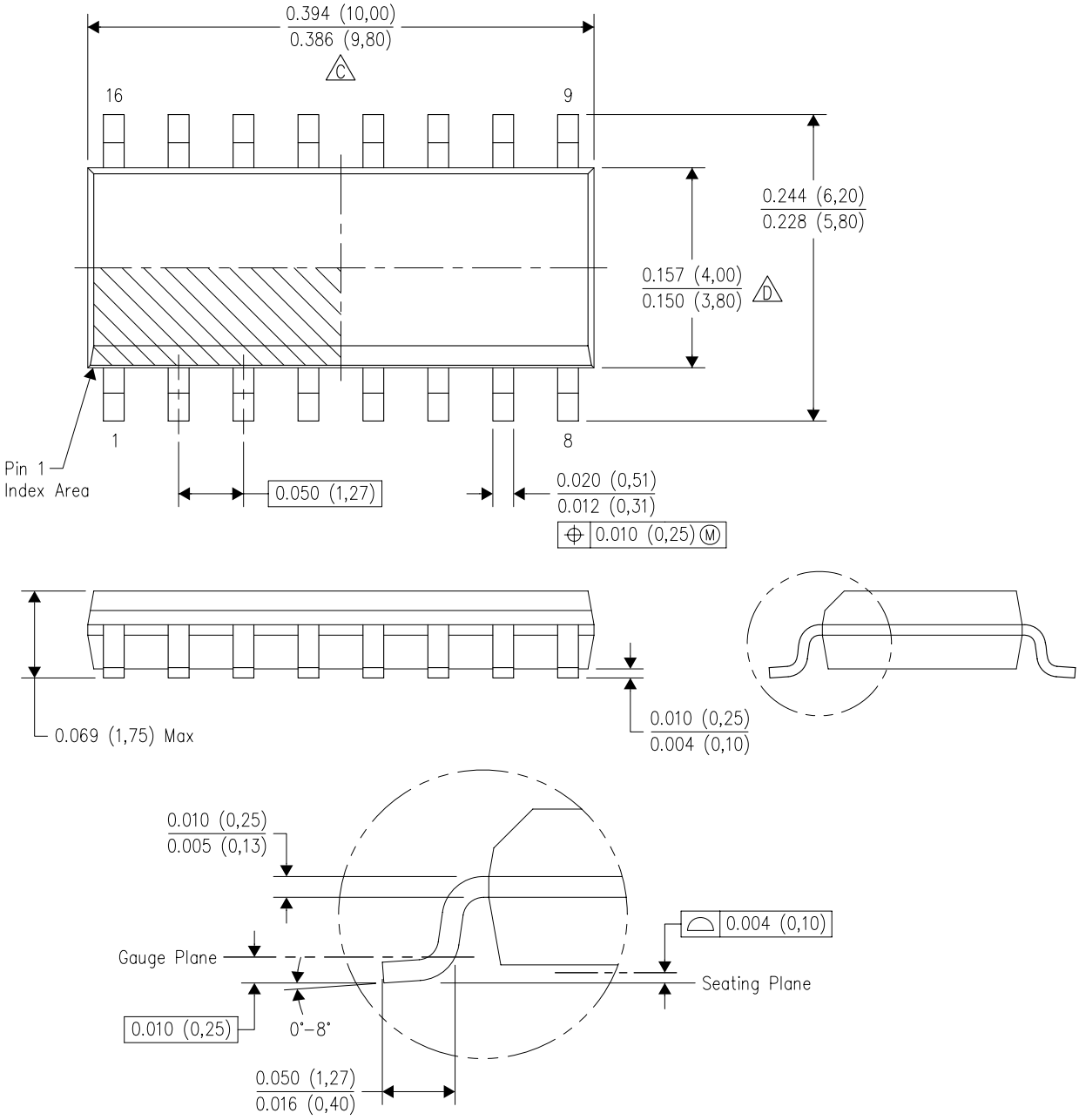
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



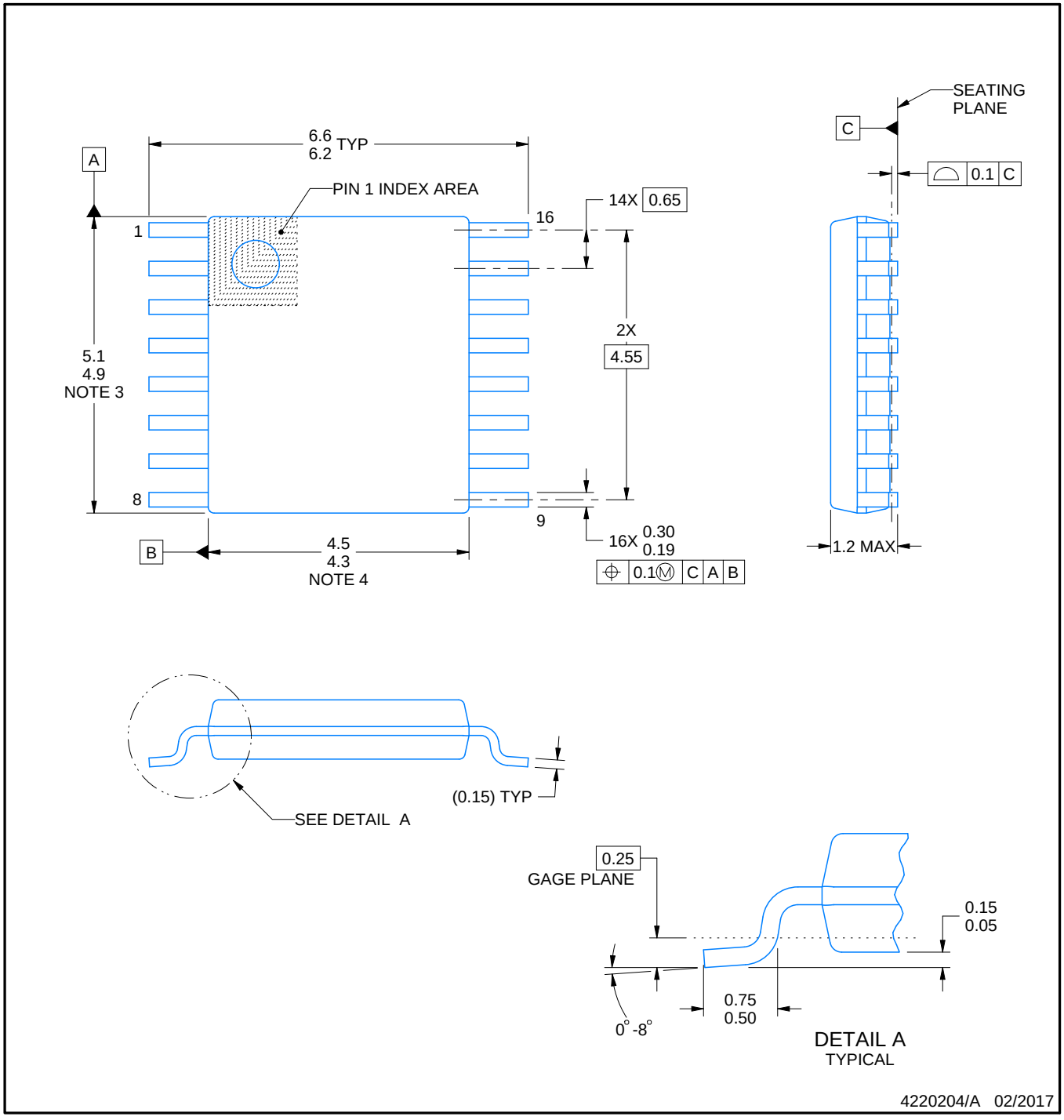
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0016A

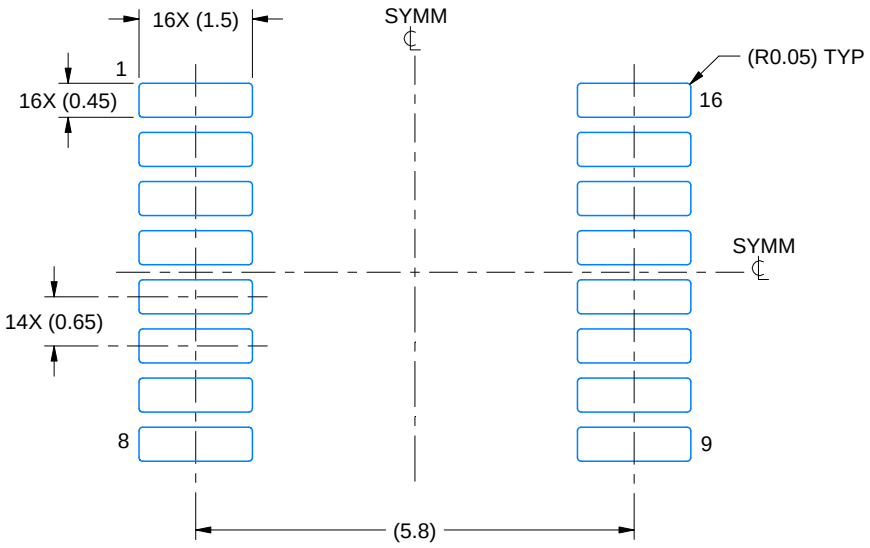
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

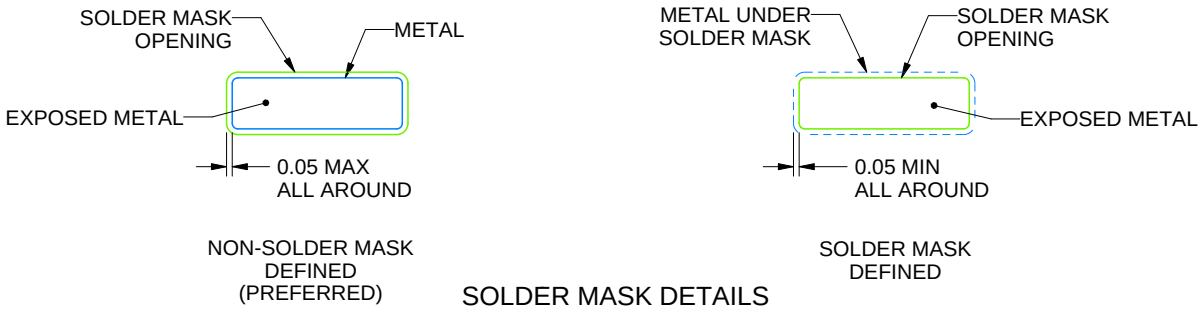


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

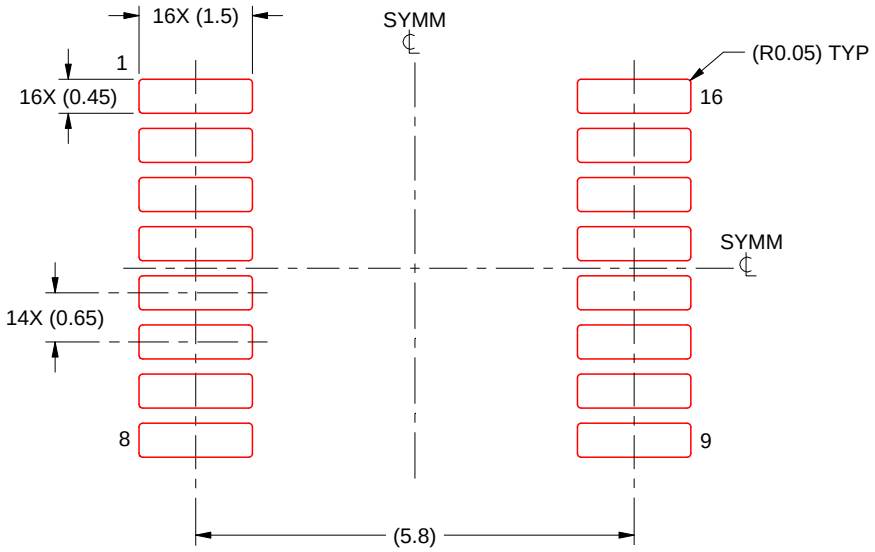


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

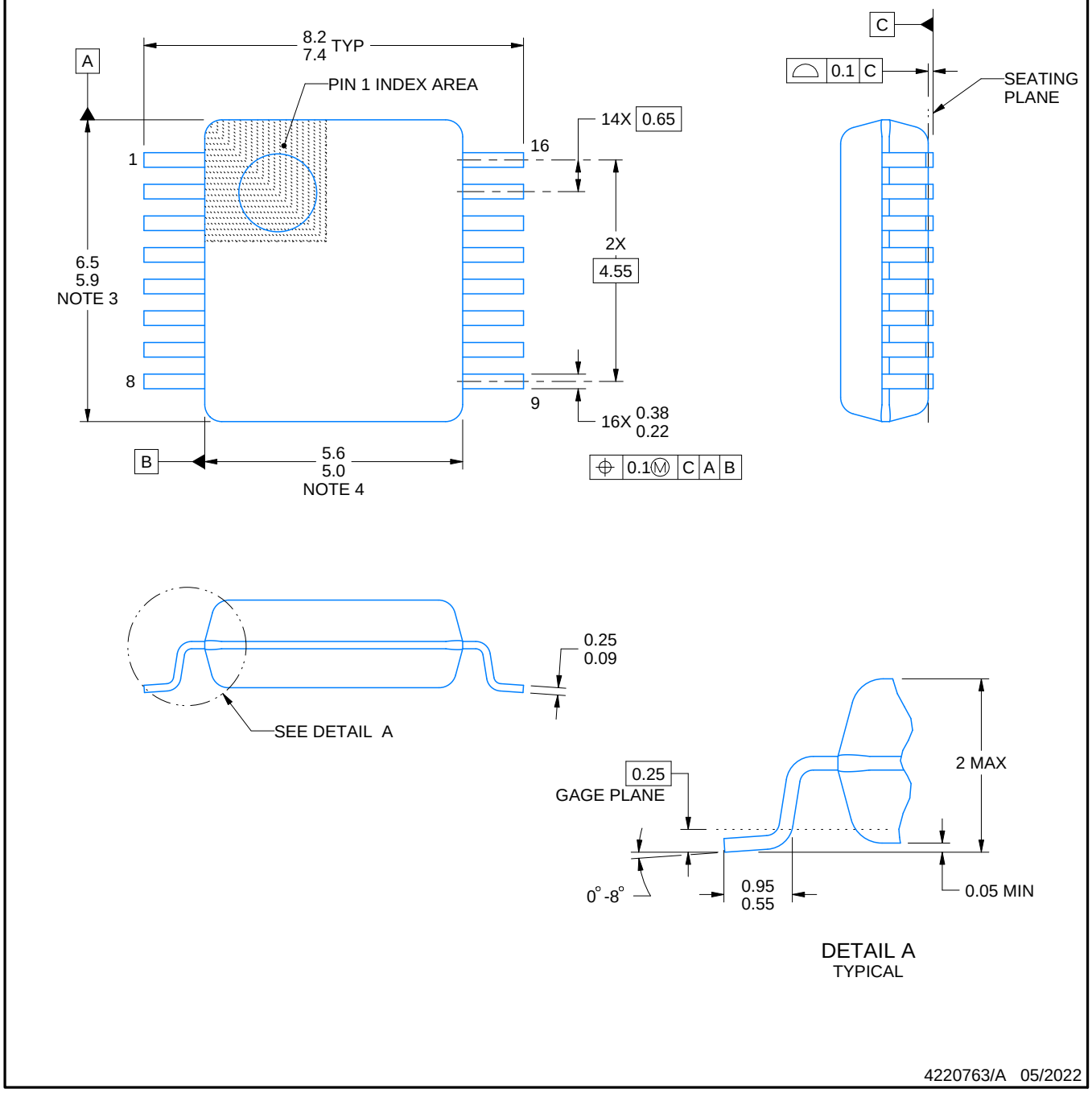
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DB0016A

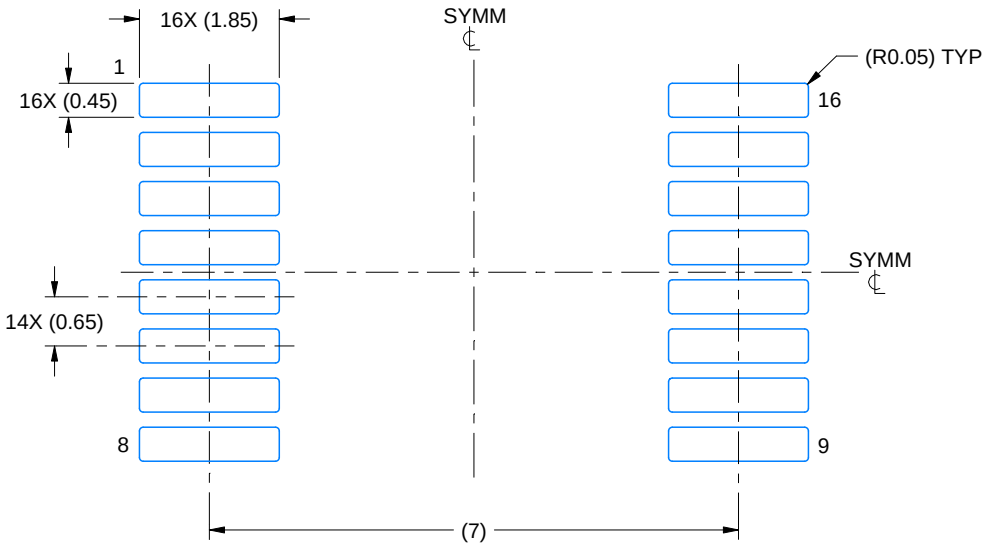
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

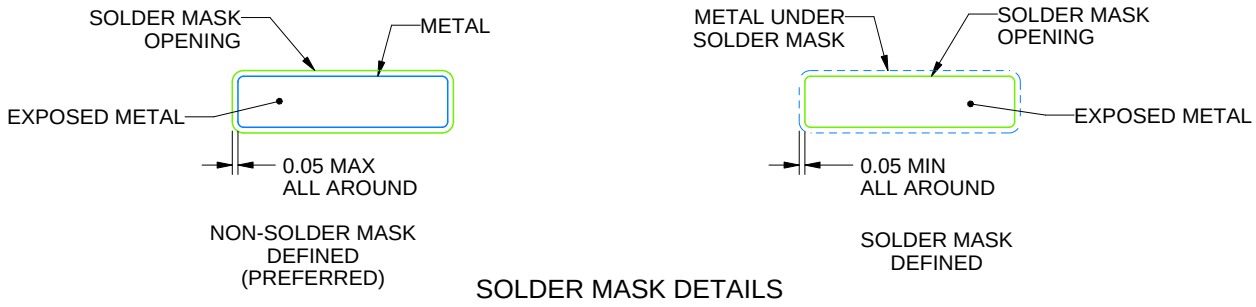


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

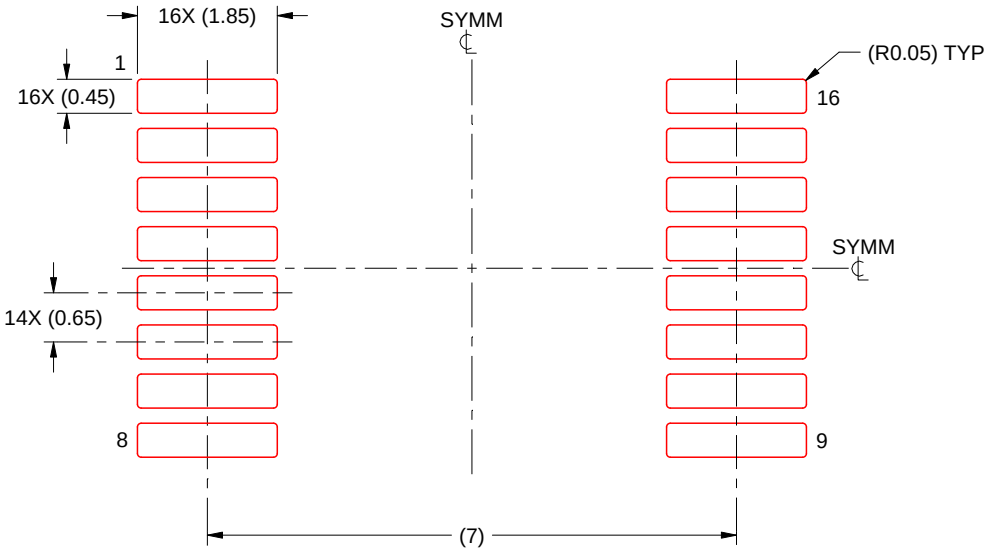


SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

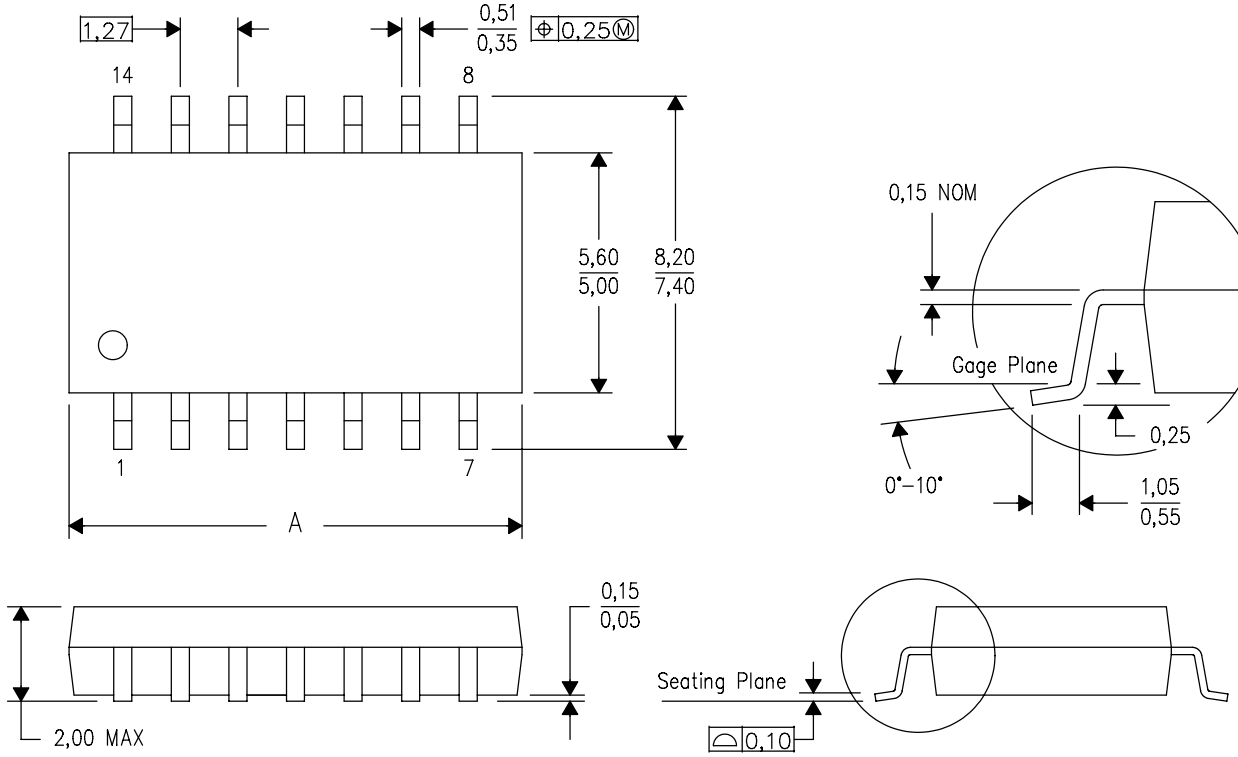
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



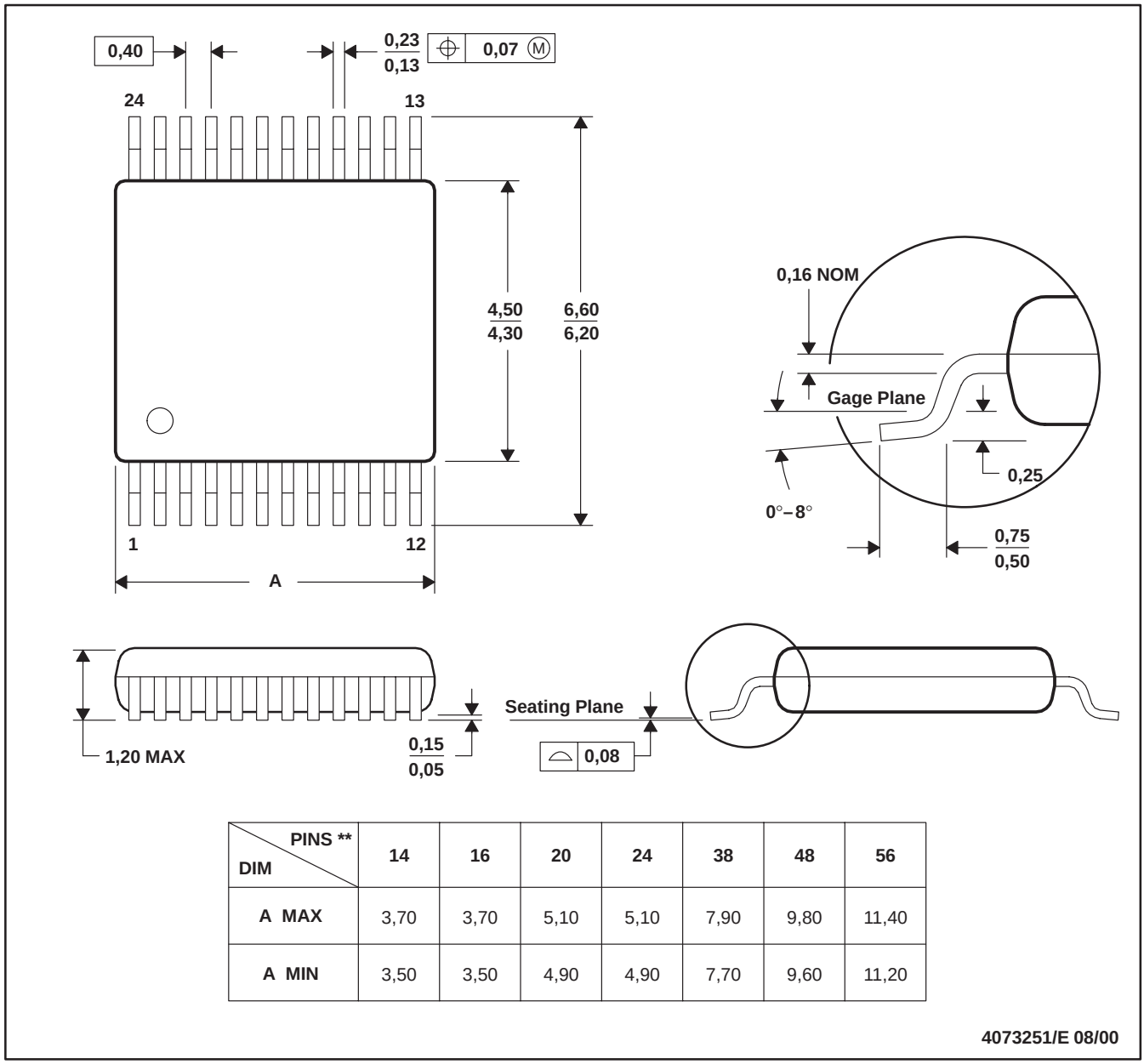
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

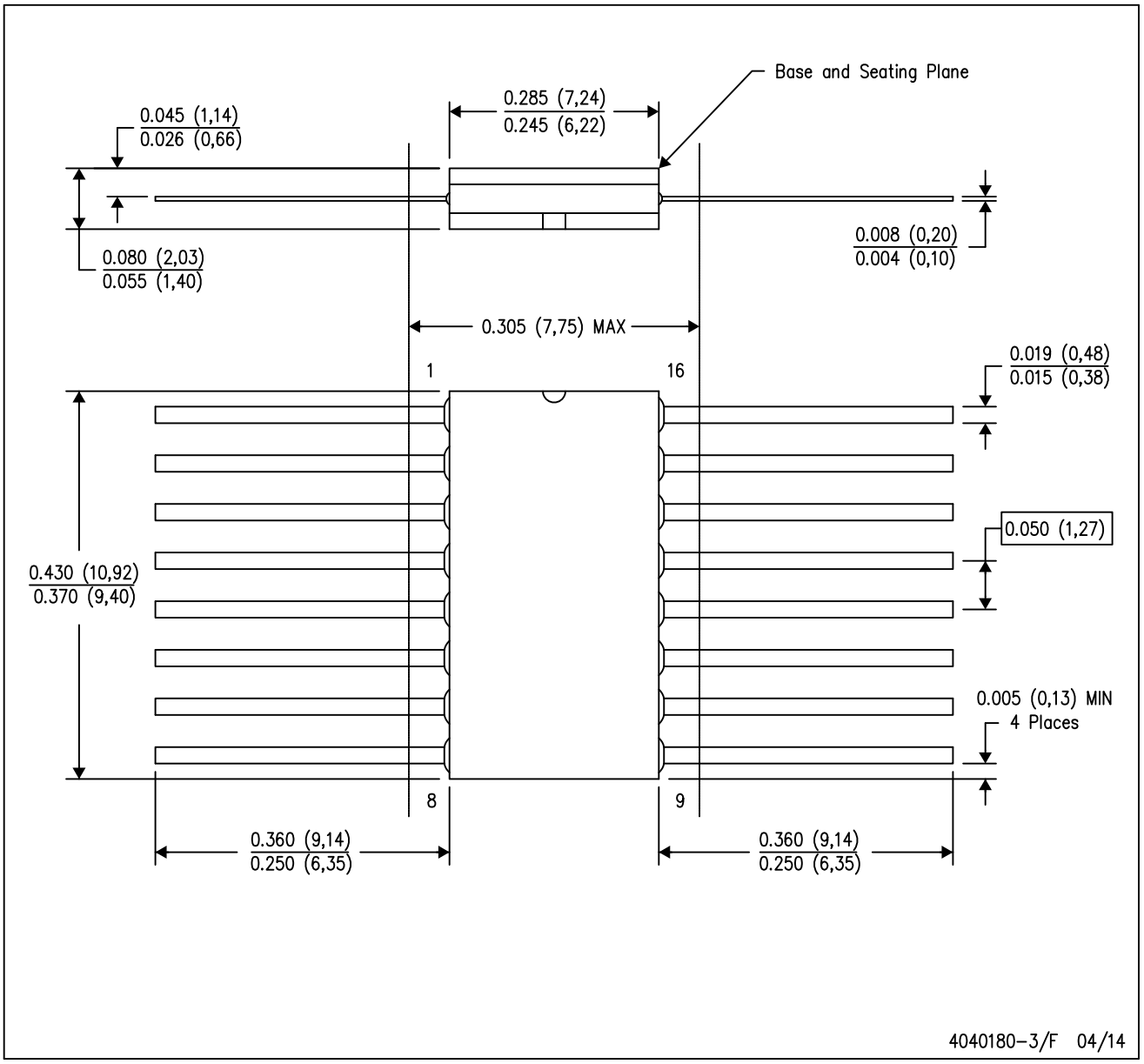


DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

W (R–GDFP–F16) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

GENERIC PACKAGE VIEW

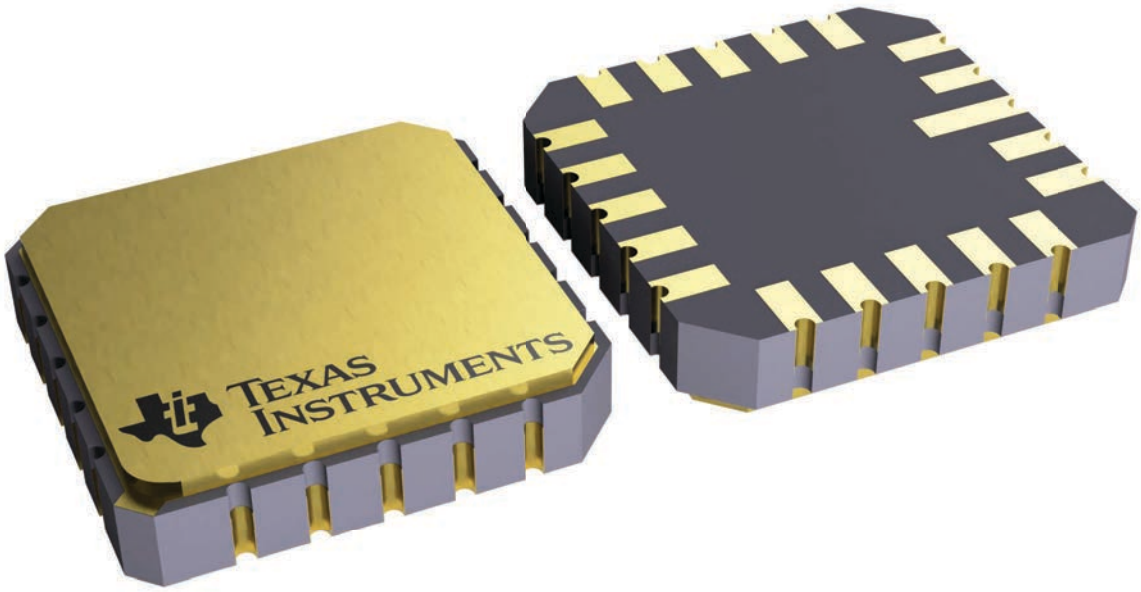
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

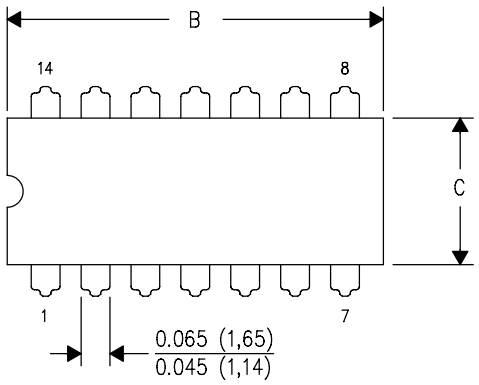


4229370VA\

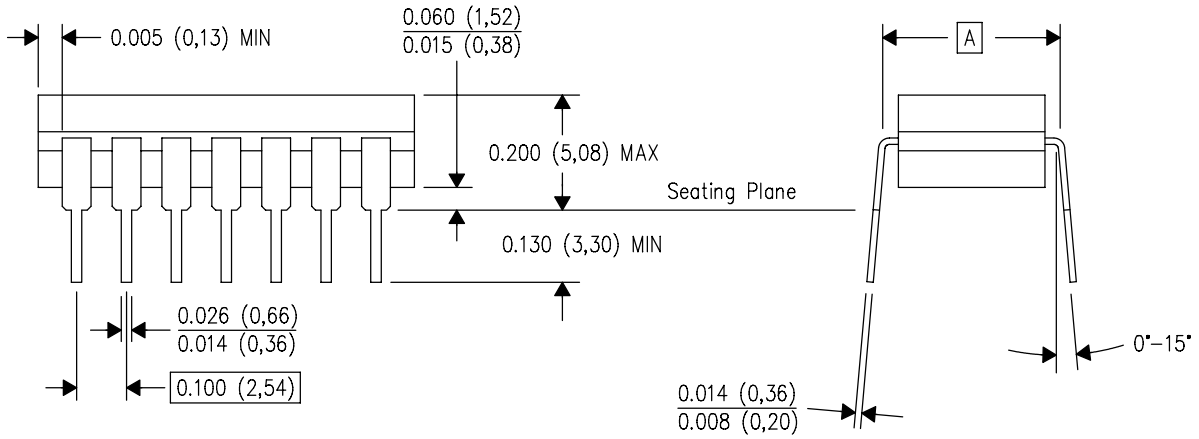
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



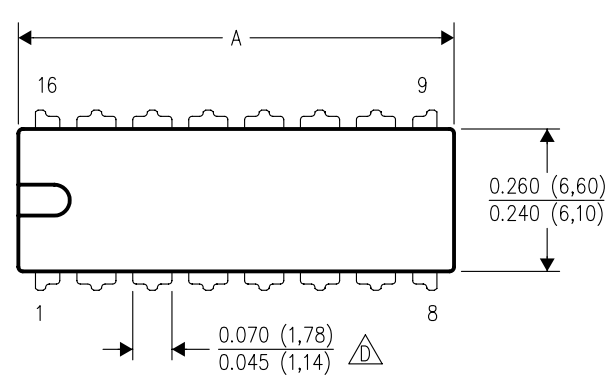
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

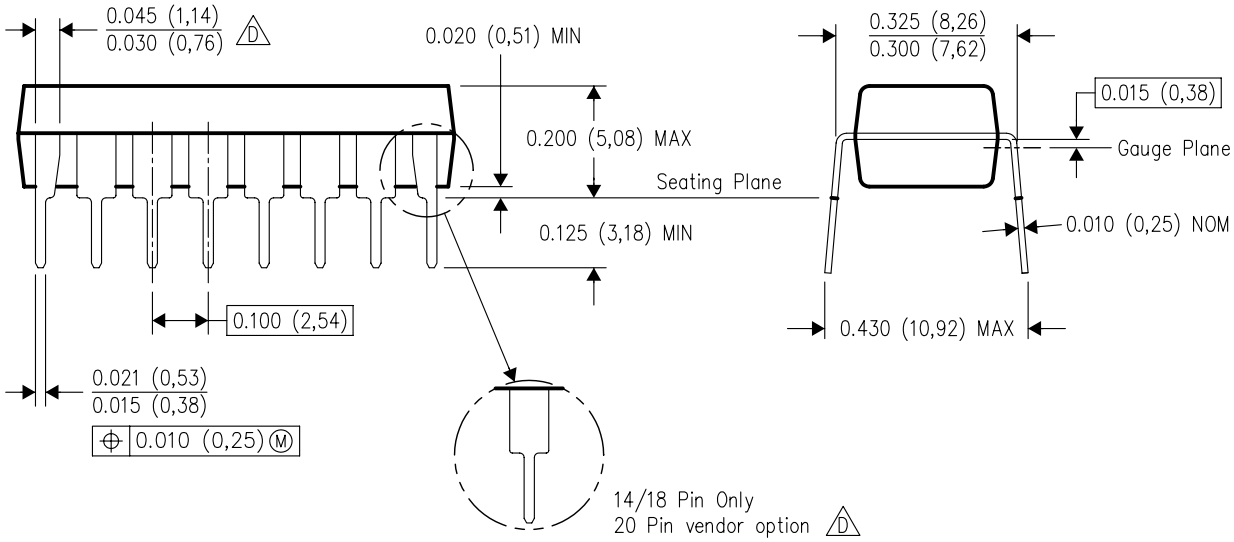
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



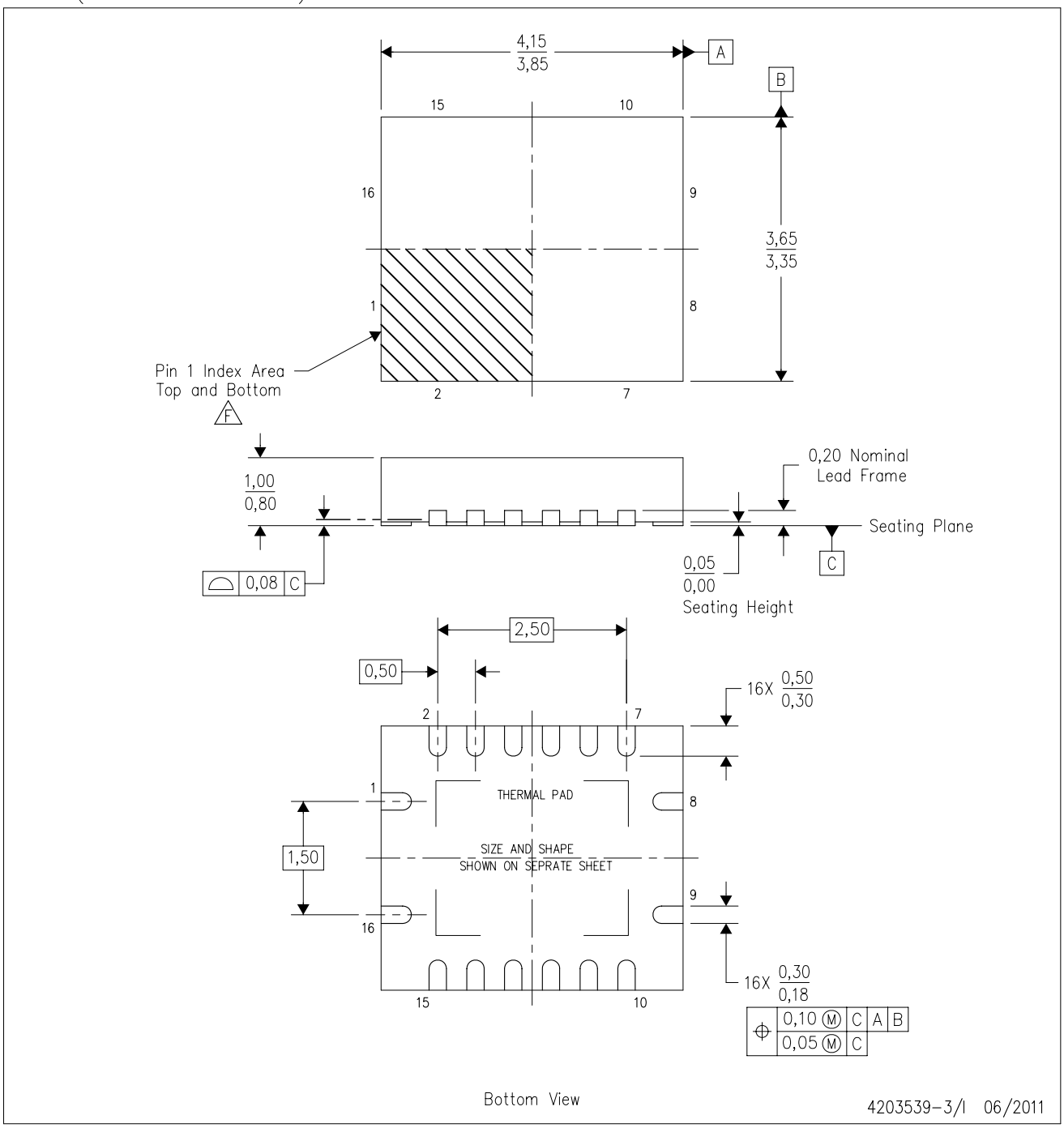
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

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