SNx4AHCT126 Quadruple Bus Buffer Gates With 3-State Outputs

1 Features

- Inputs are TTL-voltage compatible
- Latch-up performance exceeds 250mA per JESD 17
- ESD protection exceeds JESD 22:
  - 2000V Human-Body Model (A114-A)
  - 200V Machine Model (A115-A)
- On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

2 Applications

- Servers
- PCs and notebooks
- Network switches
- Wearable health and fitness devices
- Telecom infrastructures
- Electronic points-of-sale

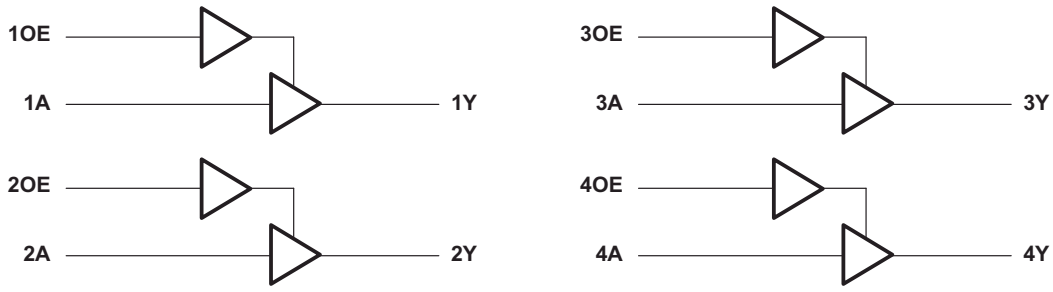
3 Description

The SNxAHCT126 devices are quadruple-bus buffer gates featuring independent line drivers with 3-state outputs.

Device Information

PART NUMBER	RATING	PACKAGE SIZE(1)
SN54AHCT126	Military	D (SOIC, 14)
		DB (SSOP, 14)
		DGV (TVSOP, 14)
SN74AHCT126	Commercial	NS (PDIP, 14)
		N (SOP, 14)
		PW (TSSOP, 14)
		J (CDIP, 14)
		W (CFP, 14)
		BQA (WQFN, 14)
		FK (LCCC, 20)

(1) For more information, see Section 11.



Simplified Schematic

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4 Pin Configuration and Functions

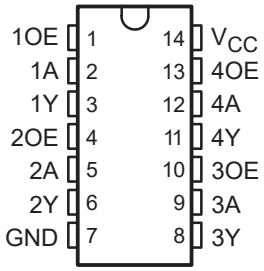
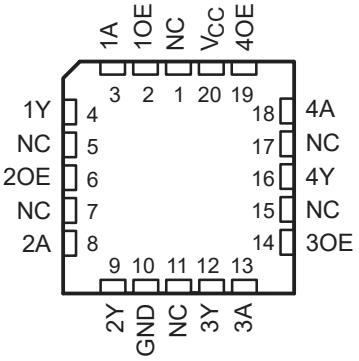


Figure 4-1. SN54AHCT126 J or W Packages, CDIP or CFP SN74AHCT126 D, DB, DGV, N, NS, or PW Packages, 14-Pin SOIC, SSOP, TVSOP, PDIP, SOP or TSSOP (Top View)



NC – No internal connection

Figure 4-2. SN54AHCT126 FK Package, 20-Pin LCCC (Top View)

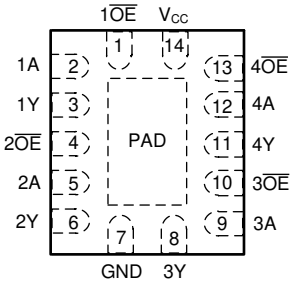


Figure 4-3. SNx4AHCT126 BQA Package, 14-Pin WQFN (Top View)

Table 4-1. Pin Functions

PIN				TYPE[1]	DESCRIPTION
NAME	SN74AHCT126	SN54AHCT126			
	D, DB, DGV, N, NS, PW, BQA	J, W	FK		
1A	2	2	3	I	1A Input
1OE	1	1	2	I	Output Enable 1
1Y	3	3	4	O	1Y Output
2A	5	5	8	I	2A Input
2OE	4	4	6	I	Output Enable 2
2Y	6	6	9	O	2Y Output
3A	9	9	13	I	3A Input
3OE	10	10	14	I	Output Enable 3
3Y	8	8	12	O	3Y Output
4A	12	12	18	I	4A Input
4OE	13	13	19	I	Output Enable 4
4Y	11	11	16	O	4Y Output
GND	7	7	10	—	Ground Pin

Table 4-1. Pin Functions (continued)

PIN				TYPE[1]	DESCRIPTION
NAME	SN74AHCT126	SN54AHCT126			
	D, DB, DGV, N, NS, PW, BQA	J, W	FK		
NC		—	1	—	No Connection
			5		
			7		
			11		
			15		
			17		
V_{CC}	14	14	20	—	Power Pin
Thermal Pad[2]				—	Thermal Pad

(1) I = input, O = output
(2) For BQA package only

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range(2)		–0.5	7	V
V_O	Output voltage range(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0 or V_O > V_{CC}		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	0	2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(2)

		SN54AHCT126(1)		SN74AHCT126		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
Δt/Δv	Input transition rise or fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	125	°C

(1) Product Preview.
(2) All unused inputs of the device must be held at V_{CC} or GND for proper device operation. Refer to the TI Application Report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

5.4 Thermal Information

THERMAL METRIC[1]		SN74AHCT126							UNIT
		D	DB	DGV	N	NS	PW	BQA	
		14 PINS							
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124.5	107.1	129.0	57.4	120.9	147.7	88.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.8	59.6	52.1	44.9	78.2	77.4	90.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	81	54.4	62.0	37.2	81.6	90.9	56.8	
ψ_{JT}	Junction-to-top characterization parameter	37	20.5	6.5	30.1	42.8	27.2	9.9	
ψ_{JB}	Junction-to-board characterization parameter	80.6	53.8	61.3	37.1	81.1	90.2	56.7	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	N/A	33.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT126		SN74AHCT126		SN74AHCT126 –40 to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 µA	4.5 V	4.4	4.5		4.4		4.4		4.4		V
	I_{OH} = –8 mA		3.94			3.8		3.8		3.8		
V_{OL}	I_{OL} = 50 µA	4.5 V			0.1		0.1		0.1		0.1	V
	I_{OL} = 8 mA				0.36		0.44		0.44		0.44	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1[1]		±1		±1	µA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.25		±2.5		±2.5		±2.5	µA
I_{CC}	V_I = V_{CC} or GND I_O = 0	5.5 V			2		20		20		20	µA
ΔI_{CC} [2]	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5		1.5	mA
C_i	V_I = V_{CC} or GND	5 V		4	10				10			pF
C_o	V_O = V_{CC} or GND	5 V		15								pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.
(2) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

5.6 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6-1)

PARAMETER	FROM (OUTPUT)	TO (INPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHCT126 –55°C to 125°C		SN74AHCT126 –40°C to 85°C		SN74AHCT126 –40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 15 pF		3.8[1]	5.5[1]	1[1]	6.5[1]	1	6.5	1	7	ns
t_{PHL}					3.8[1]	5.5[1]	1[1]	6.5[1]	1	6.5	1	7	
t_{PZH}	OE	Y	C_L = 15 pF		3.6[1]	5.1[1]	1[1]	6[1]	1	6	1	6.5	ns
t_{PZL}					3.6[1]	5.1[1]	1[1]	6[1]	1	6	1	6.5	
t_{PHZ}	OE	Y	C_L = 15 pF		4.6[1]	6.8[1]	1[1]	8[1]	1	8	1	8.5	ns
t_{PLZ}					4.6[1]	6.8[1]	1[1]	8[1]	1	8	1	8.5	
t_{PLH}	A	Y	C_L = 50 pF		5.3	7.5	1	8.5	1	8.5	1	9.5	ns
t_{PHL}					5.3	7.5	1	8.5	1	8.5	1	9.5	
t_{PZH}	OE	Y	C_L = 50 pF		5.1	7.1	1	8	1	8	1	9	ns
t_{PZL}					5.1	7.1	1	8	1	8	1	9	
t_{PHZ}	OE	Y	C_L = 50 pF		6.1	8.8	1	10	1	10	1	11	ns
t_{PLZ}					6.1	8.8	1	10	1	10	1	11	
$t_{sk(o)}$			C_L = 50 pF			1[2]				1		1	ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

5.7 Noise Characteristics

V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C[1]

PARAMETER		SN74AHCT126		UNIT
		MIN	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.4		V
$V_{IH(D)}$	High-level dynamic input voltage	2		V
$V_{IL(D)}$	Low-level dynamic input voltage		0.8	V

(1) Characteristics are for surface-mount packages only.

5.8 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	14	pF

5.9 Typical Characteristics

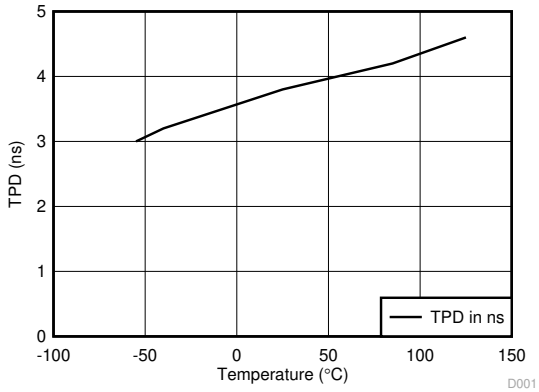
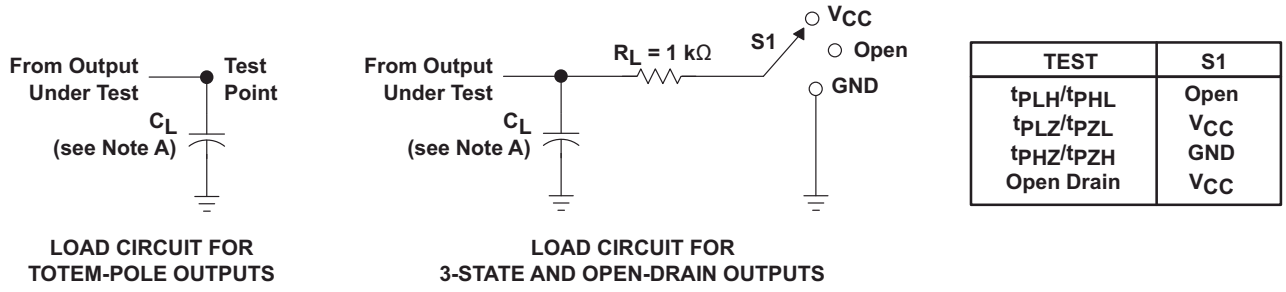


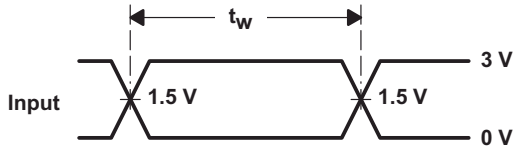
Figure 5-1. TPD vs Temperature

6 Parameter Measurement Information

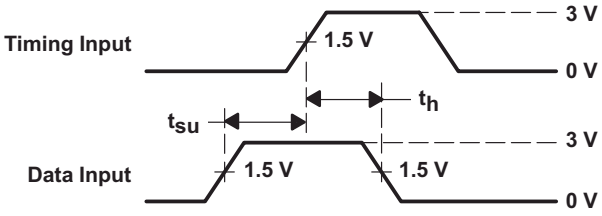


LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

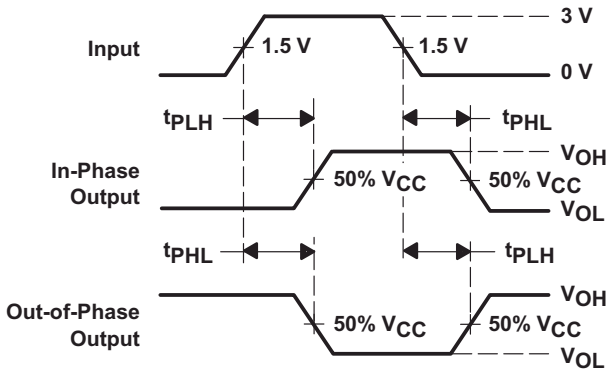
LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS



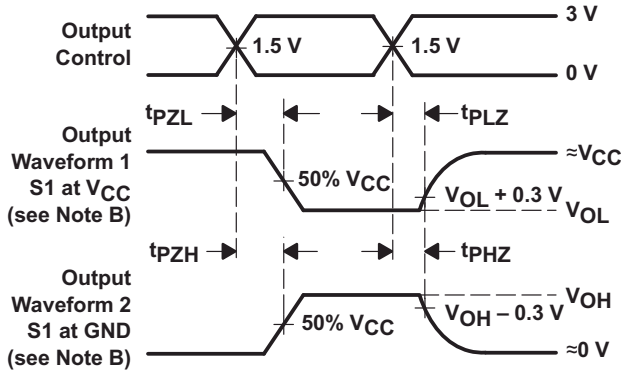
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage and Waveforms

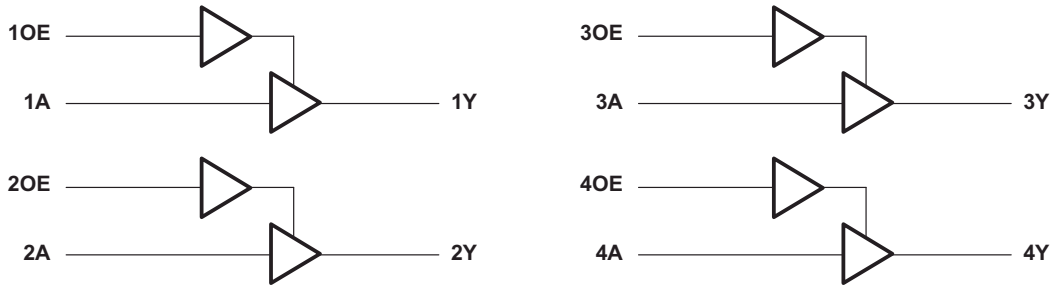
7 Detailed Description

7.1 Overview

The SNxAHCT126 devices are quadruple-bus buffer gates featuring independent line drivers with 3-state outputs.

Each output is disabled when the associated output-enable (OE) input is low. When OE is high, the respective gate passes the data from the A input to the Y output. For the high-impedance state during power up or power down, tie OE to GND through a pull-down resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

7.2 Functional Block Diagram



7.3 Feature Description

- TTL inputs
  - Lowered switching threshold allows up translation from 3.3 V to 5 V
- Slow edges reduce output ringing

7.4 Device Functional Modes

Table 7-1. Function Table (Each Buffer)

INPUTS		OUTPUT Y
OE	A	
H	H	H
H	L	L
L	X	Z

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SNx4AHCT126 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The input switching levels have been lowered to accommodate TTL inputs of 0.8-V V_{IL} and 2-V V_{IH}. This feature makes it ideal for translating up from 3.3 V to 5 V. Figure 8-2 shows this type of translation.

8.2 Typical Application

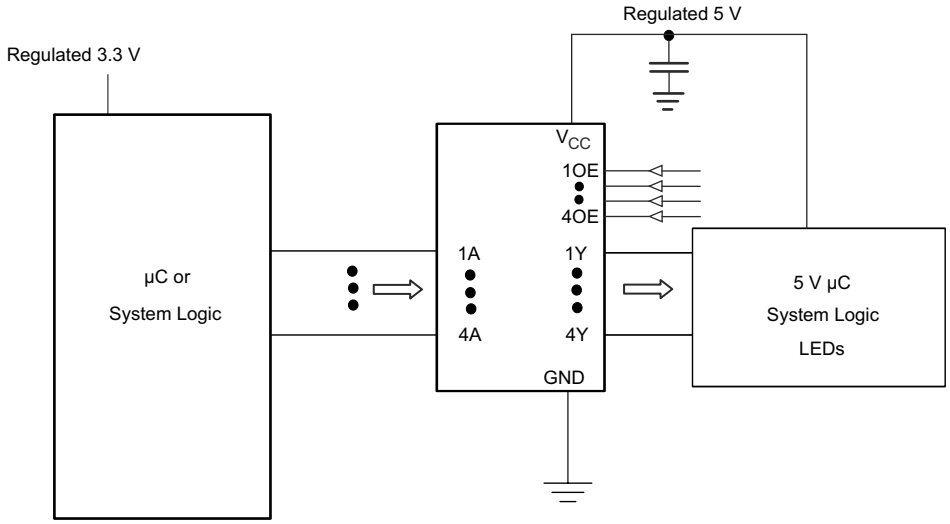


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads; therefore, routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

1. Recommended input conditions:
   - Rise time and fall time specs: See (Δt/ΔV) in the *Recommended Operating Conditions* table.
   - Specified High and low levels: See (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}
2. Recommended output conditions:
   - Load currents should not exceed 25 mA per output and 50 mA total for the part
   - Outputs should not be pulled above V_{CC}

8.2.3 Application Curves

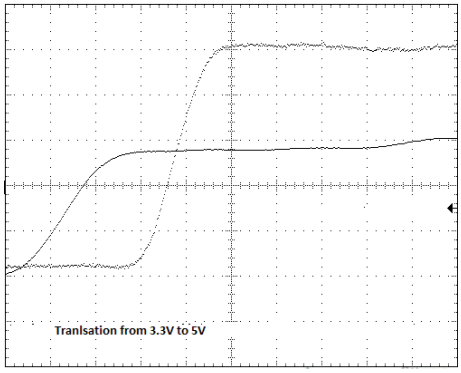


Figure 8-2. Up Translation

8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended. If there are multiple V_{CC} pins, 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Figure 8-3 shows the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}; whichever makes more sense or is more convenient. It is generally acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the IO's so they cannot float when disabled.

8.4.2 Layout Example

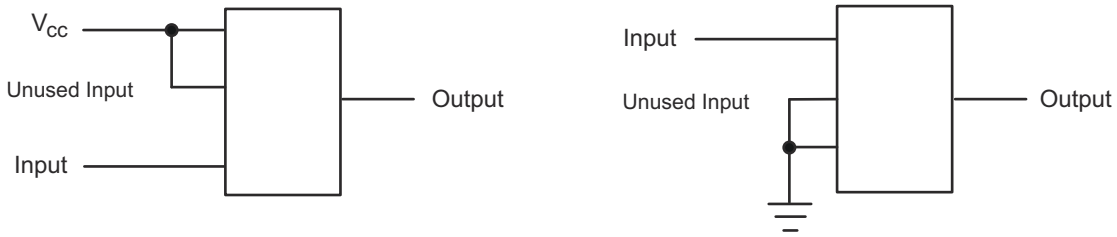


Figure 8-3. Layout Diagram

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision R (October 2023) to Revision S (February 2024)	Page
• Updated thermal values for NS package from RθJA = 90.7 to 120.9, RθJC(top) = 48.3 to 78.2, RθJB = 49.4 to 81.6, ΨJT = 14.6 to 42.8, ΨJB = 49.1 to 81.1, RθJC(bot) = N/A, all values in °C/W	6

Changes from Revision Q (May 2023) to Revision R (October 2023)	Page
• Updated RθJA values: D = 90.6 to 124.5, PW = 122.6 to 147.7; Updated D and PW packages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in °C/W	6

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9686301QDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686301QD A SNJ54AHCT126W	Samples
SN74AHCT126BQAR	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHT126	Samples
SN74AHCT126D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	AHCT126	
SN74AHCT126DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB126	Samples
SN74AHCT126DGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB126	Samples
SN74AHCT126DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT126	Samples
SN74AHCT126N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHCT126N	Samples
SN74AHCT126NSR	ACTIVE	SOP	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT126	Samples
SN74AHCT126PW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125	HB126	
SN74AHCT126PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	HB126	Samples
SNJ54AHCT126W	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686301QD A SNJ54AHCT126W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN54AHCT126, SN74AHCT126 :

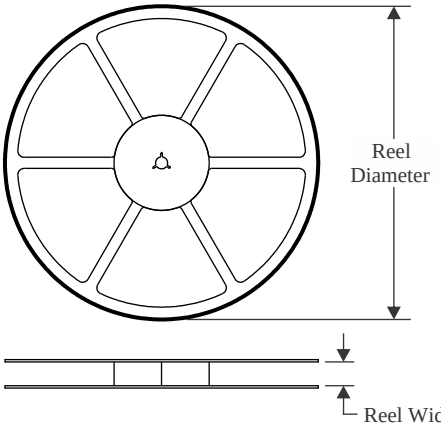
- Catalog : SN74AHCT126
- Automotive : SN74AHCT126-Q1, SN74AHCT126-Q1
- Enhanced Product : SN74AHCT126-EP, SN74AHCT126-EP
- Military : SN54AHCT126

NOTE: Qualified Version Definitions:

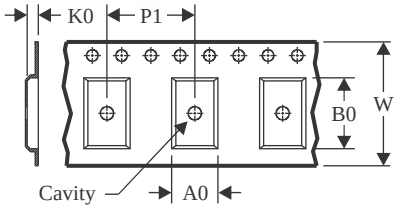
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

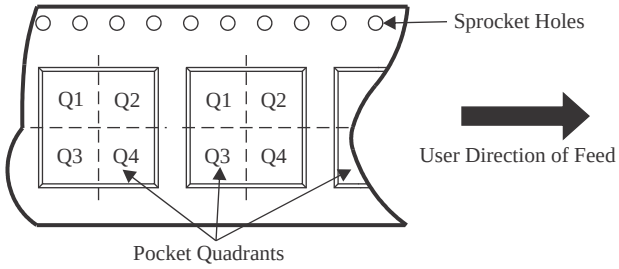


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

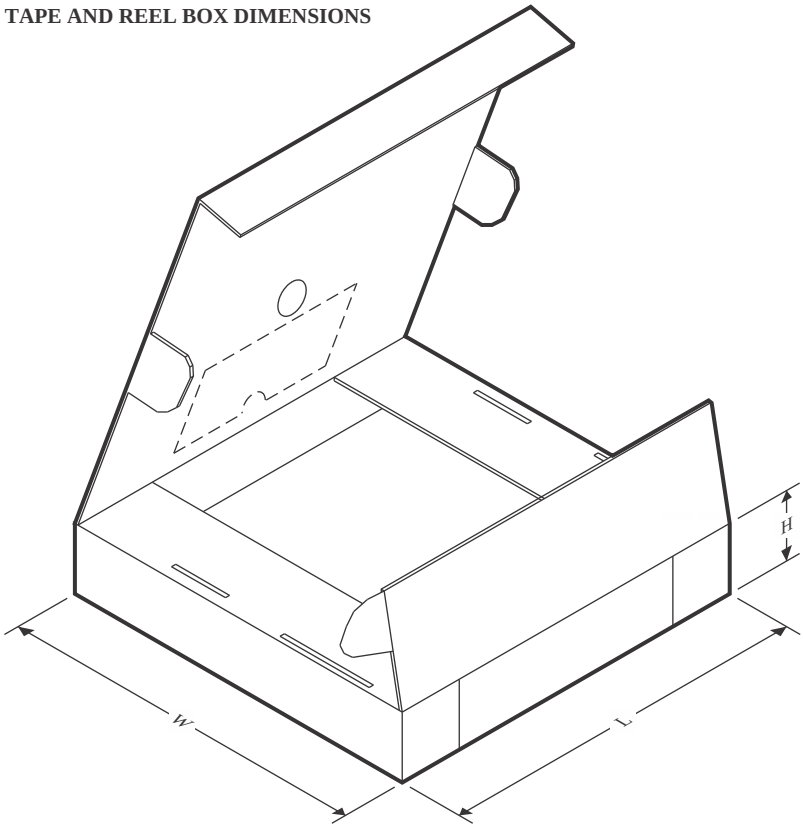
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT126BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74AHCT126DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHCT126DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHCT126DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHCT126NSR	SOP	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHCT126NSR	SOP	NS	14	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
SN74AHCT126PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHCT126PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

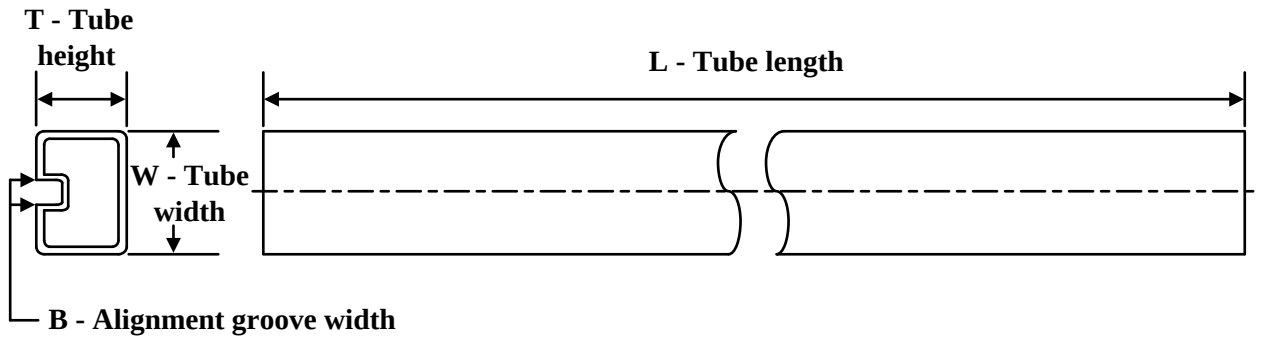
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT126BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74AHCT126DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74AHCT126DGVR	TVSOP	DGV	14	2000	356.0	356.0	35.0
SN74AHCT126DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74AHCT126NSR	SOP	NS	14	2000	367.0	367.0	38.0
SN74AHCT126NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74AHCT126PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHCT126PWR	TSSOP	PW	14	2000	356.0	356.0	35.0

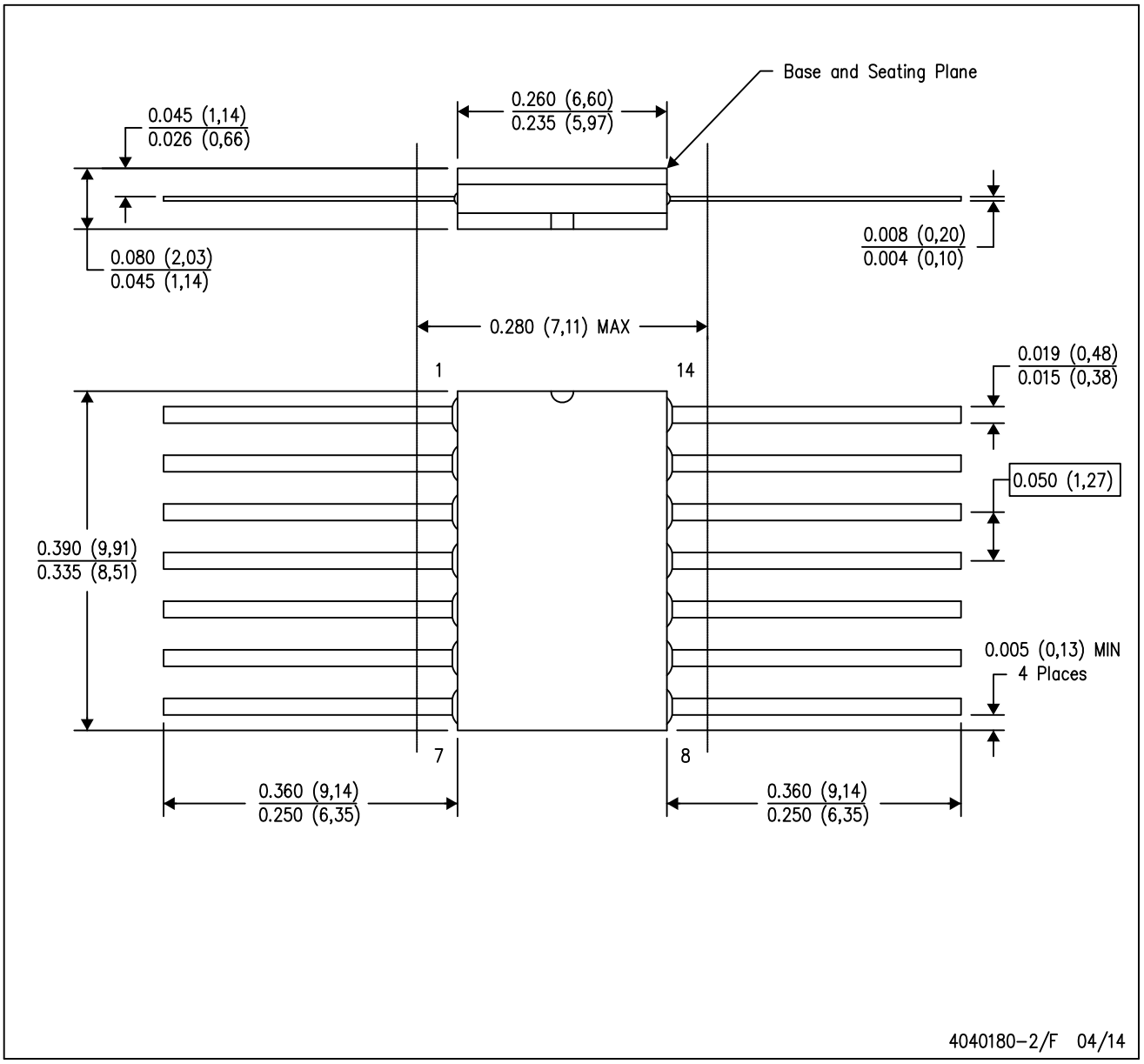
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9686301QDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74AHCT126N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHCT126N	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54AHCT126W	W	CFP	14	25	506.98	26.16	6220	NA

W (R–GDFP–F14) CERAMIC DUAL FLATPACK



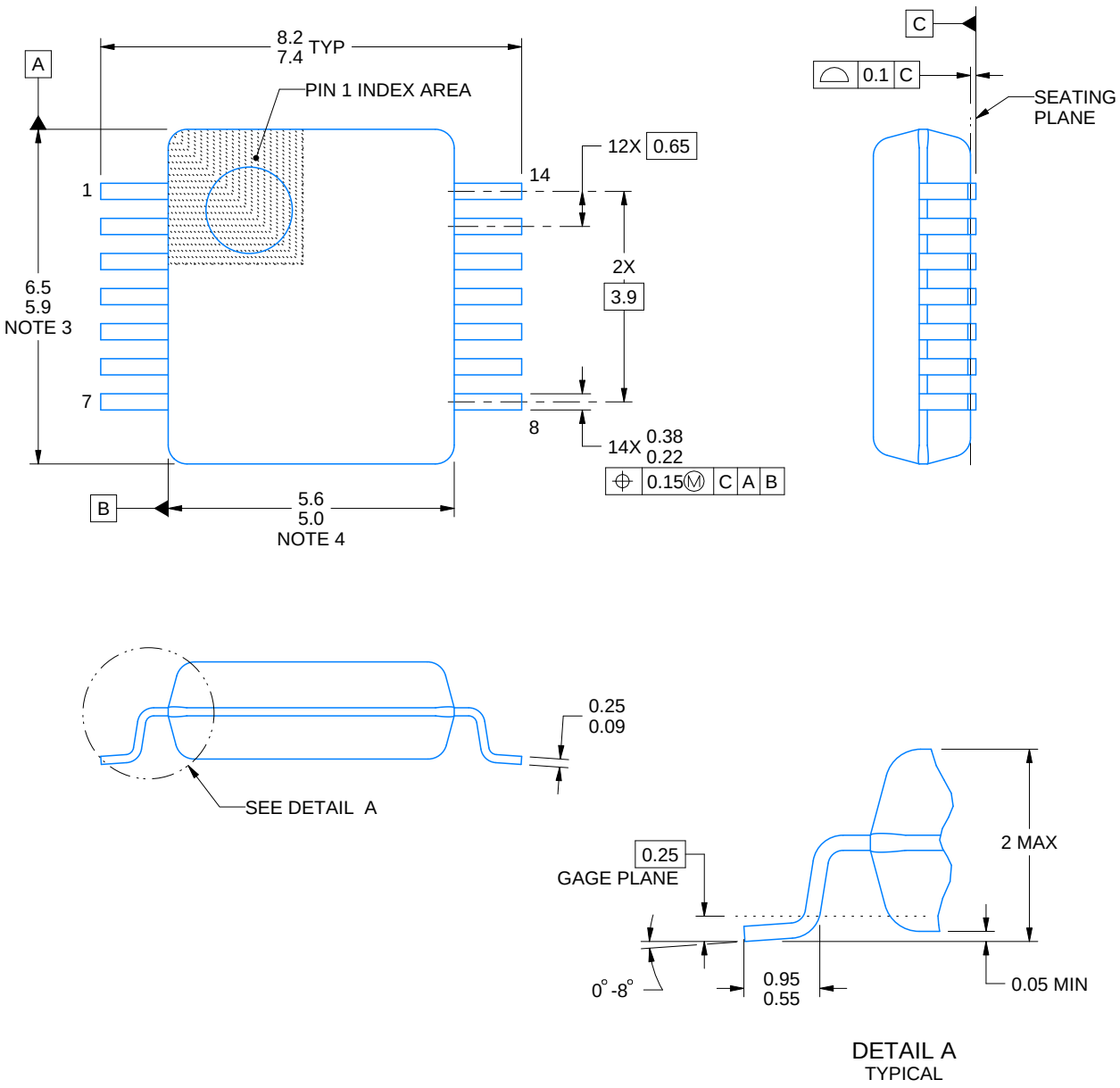
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

PACKAGE OUTLINE

DB0014A

SSOP - 2 mm max height

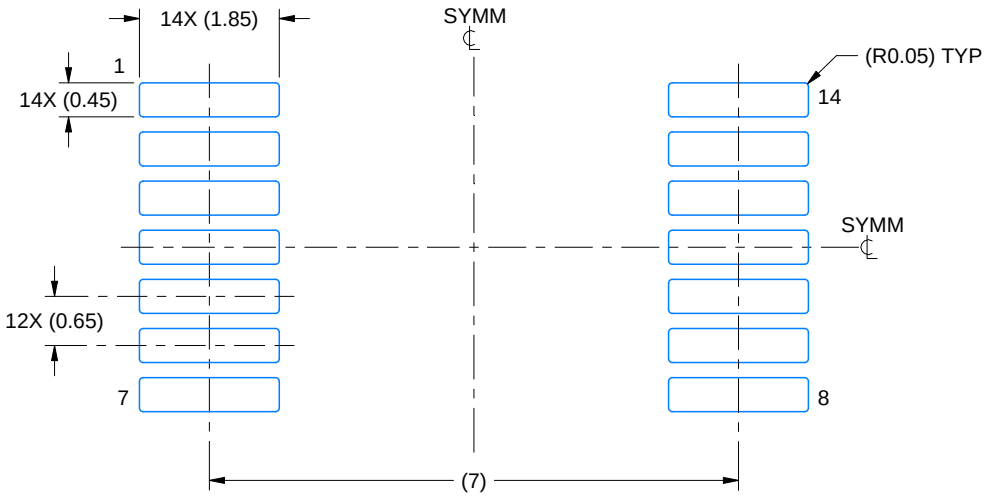
SMALL OUTLINE PACKAGE



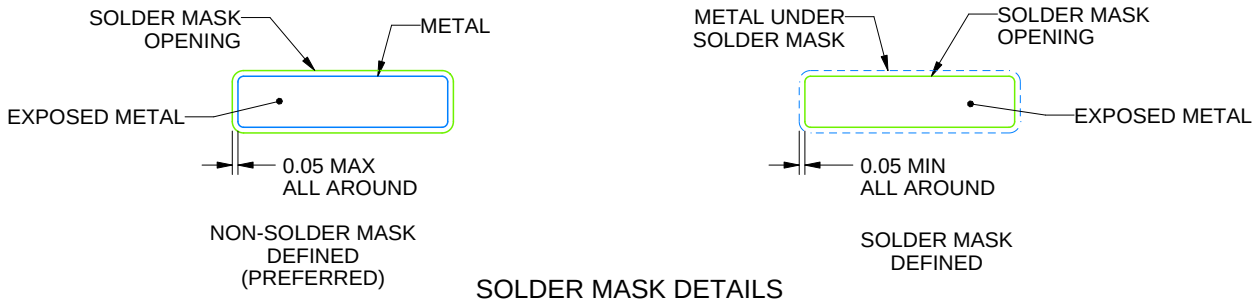
4220762/A 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

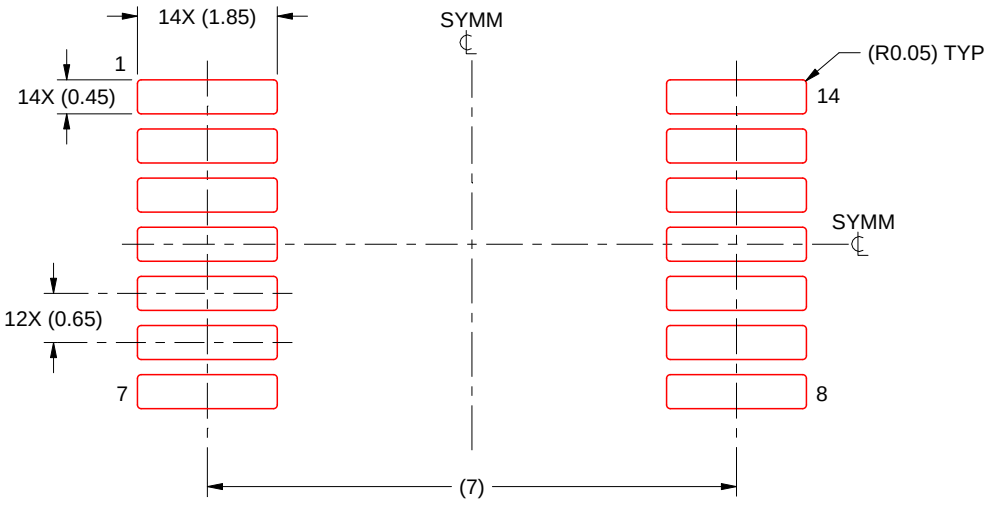


SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

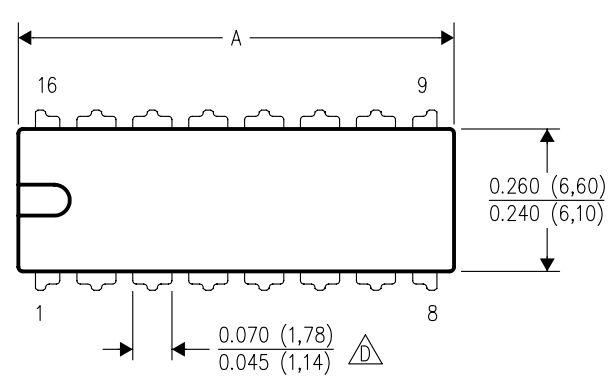
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

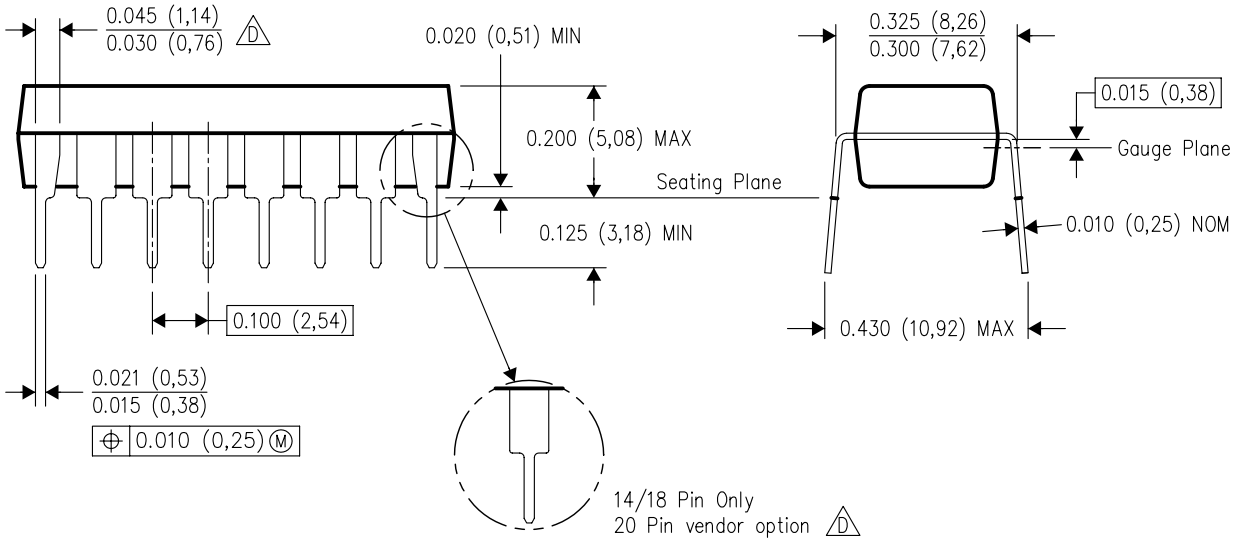
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

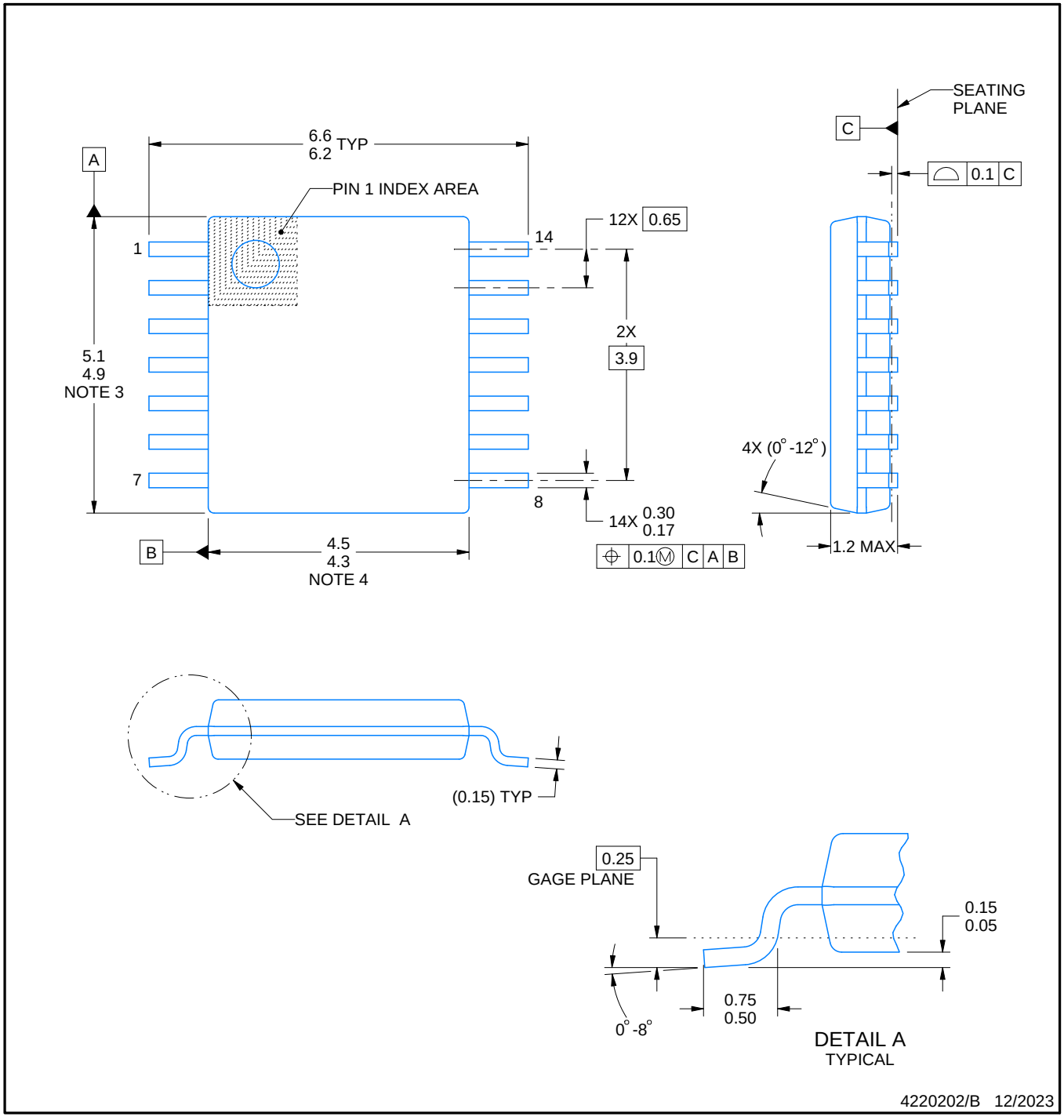
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0014A

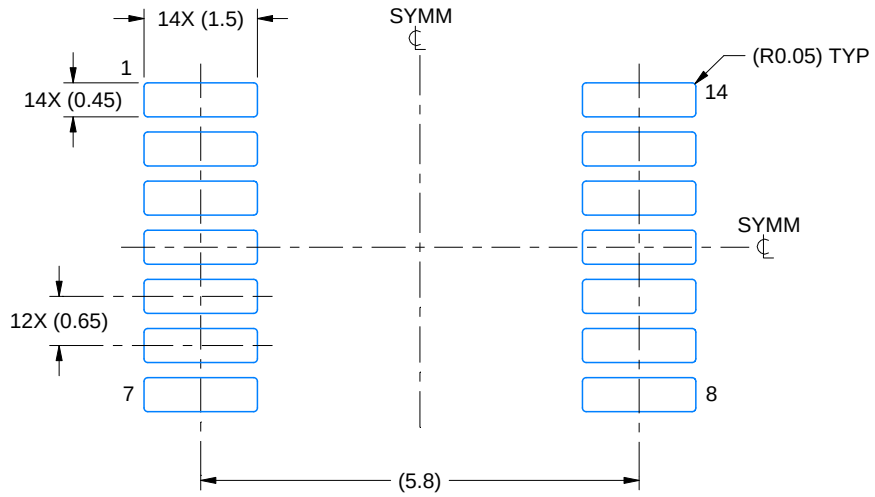
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

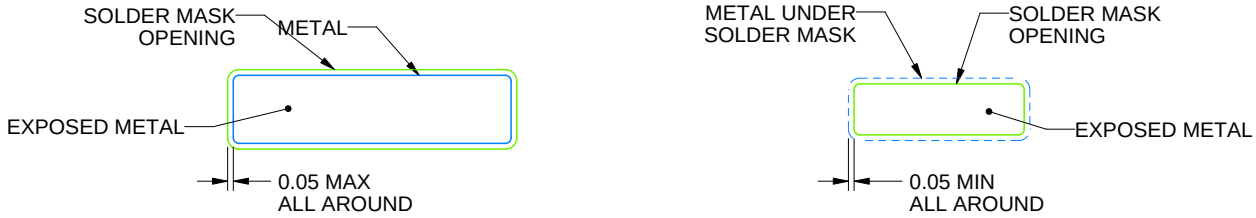


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

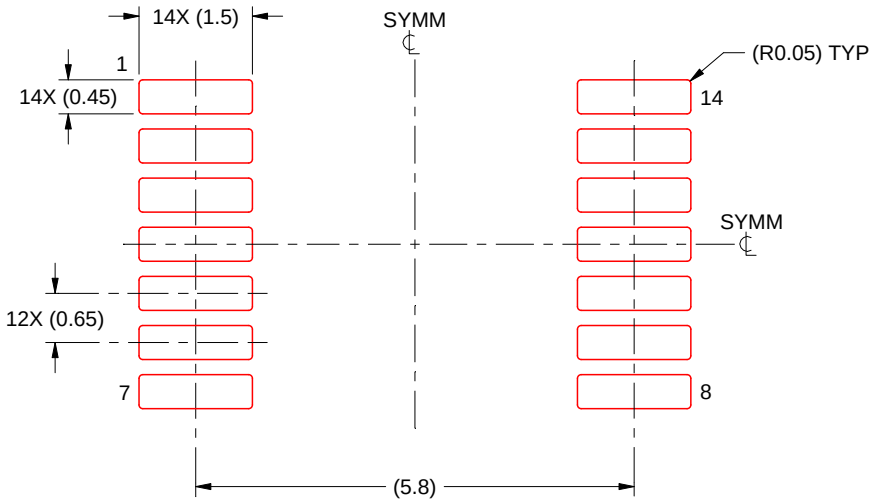


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

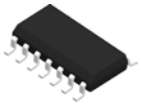


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

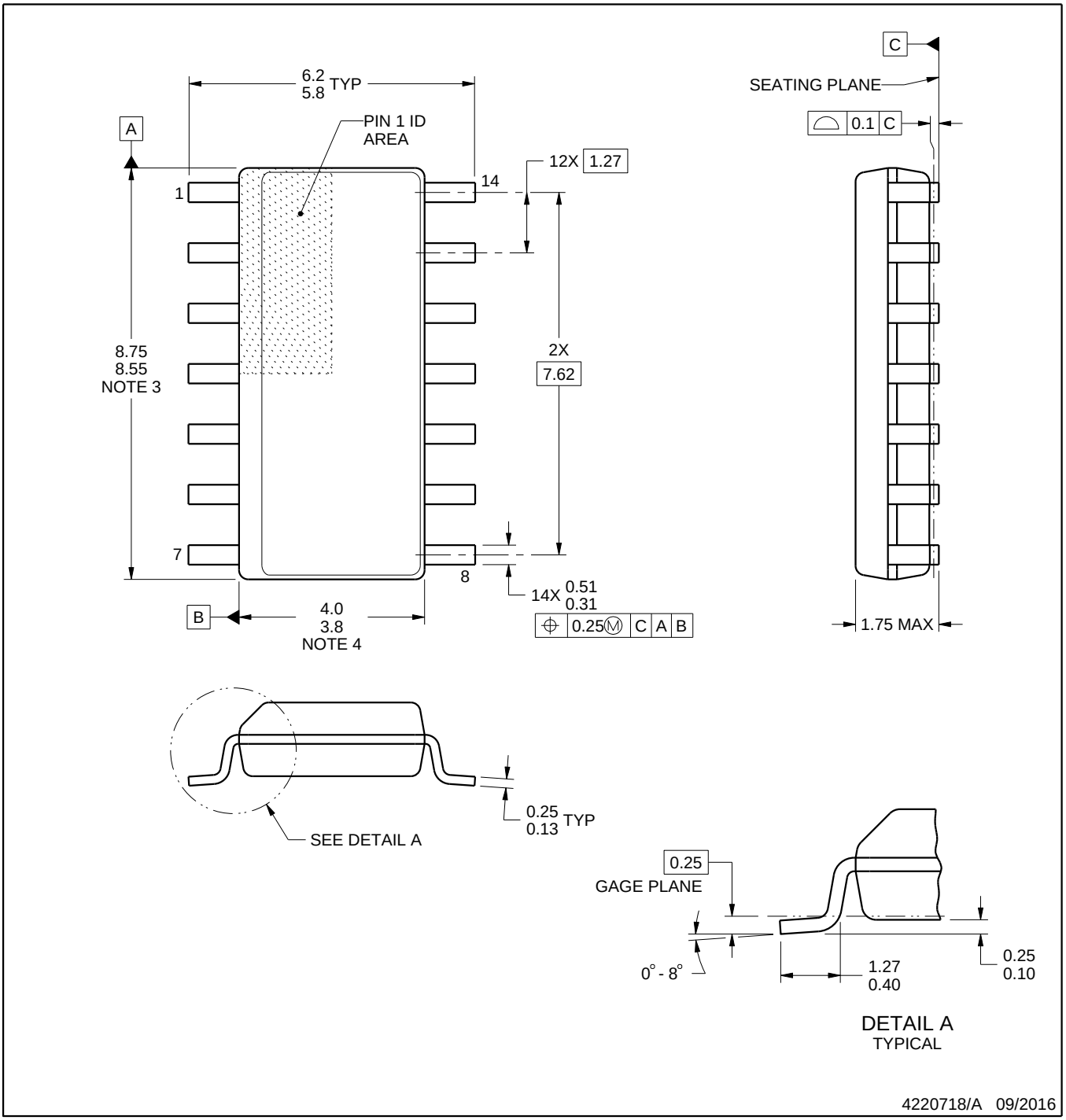


PACKAGE OUTLINE

D0014A

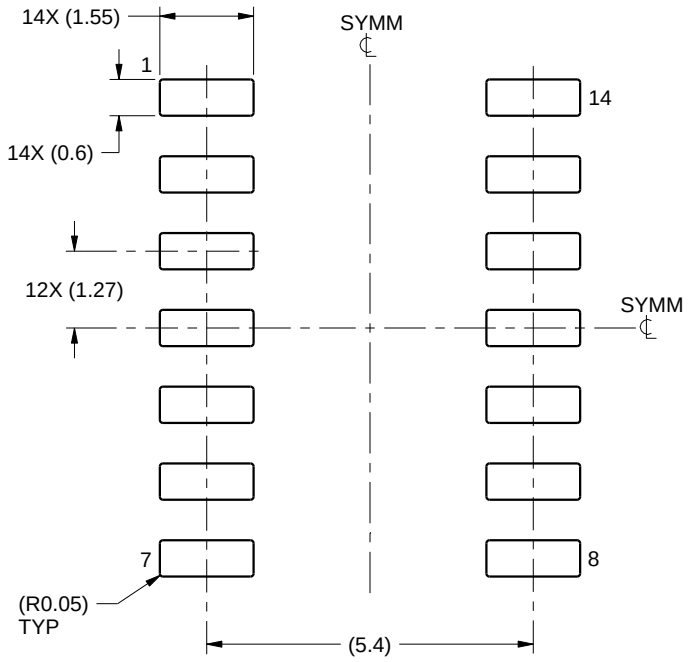
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

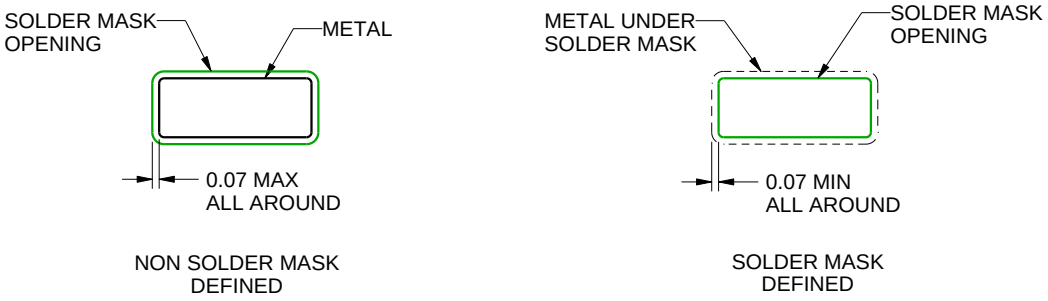


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

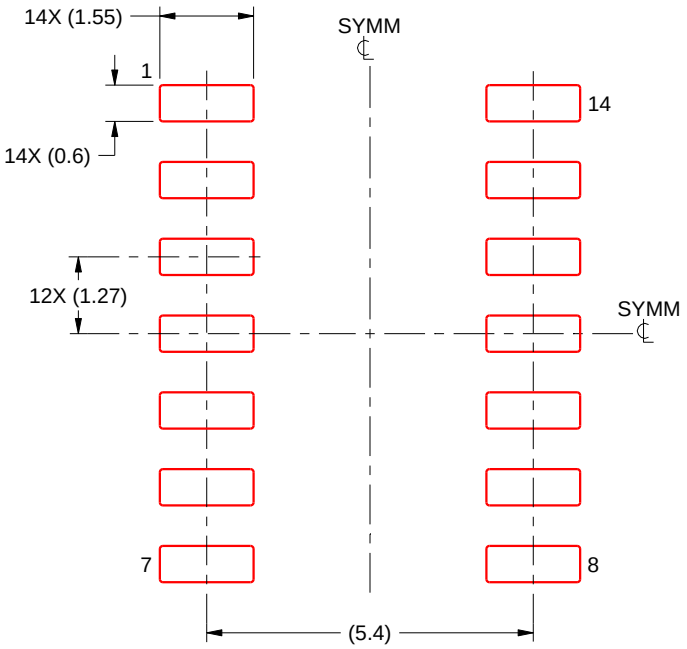
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

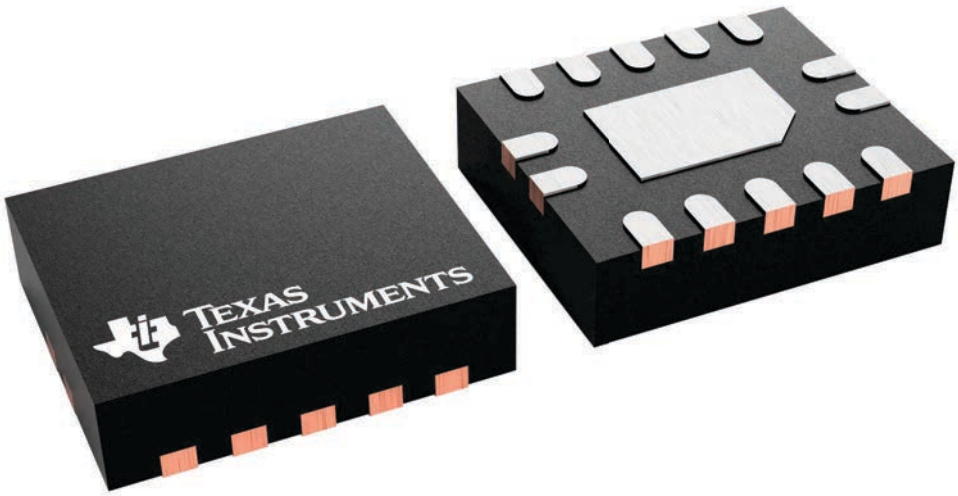
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

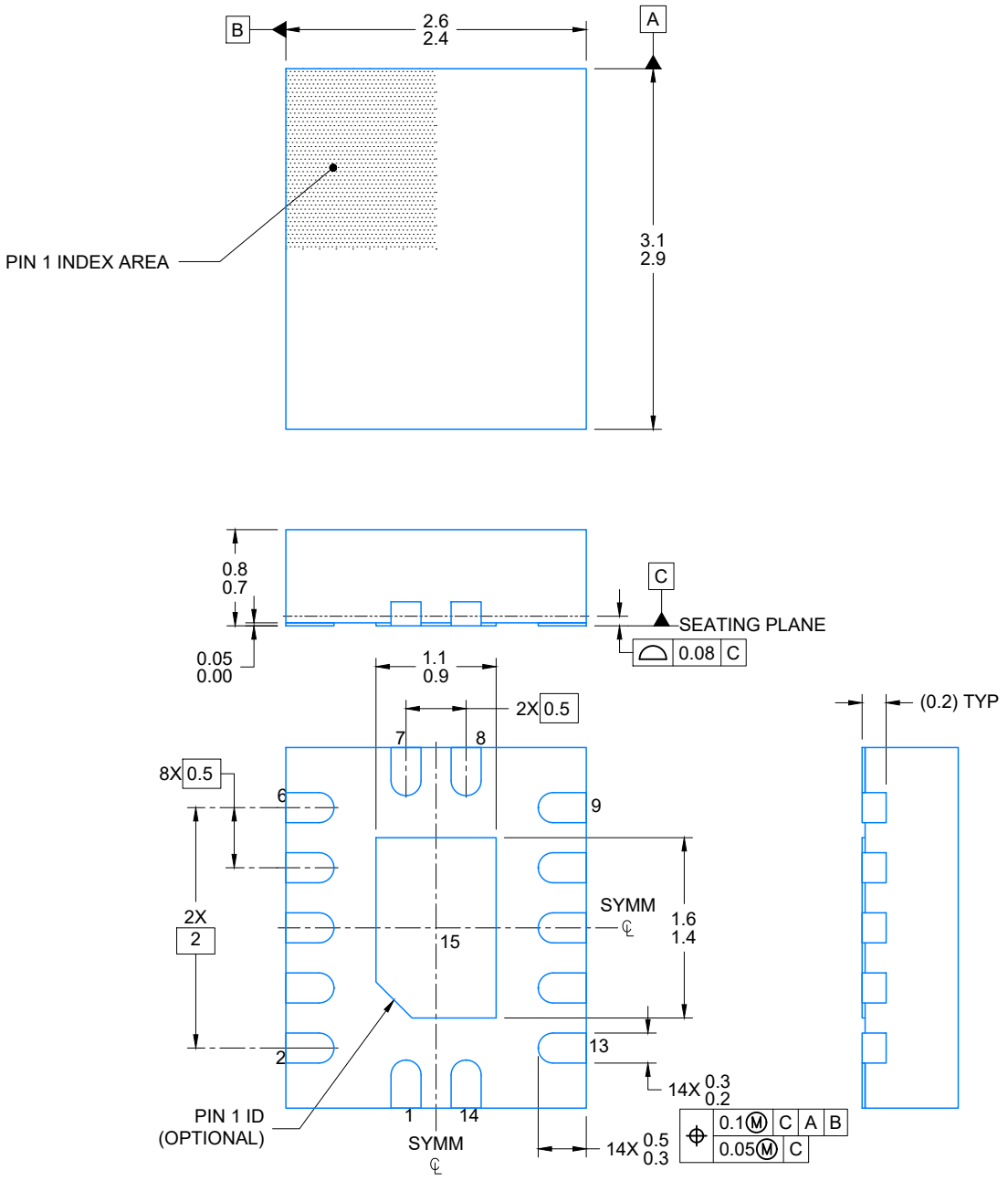


PACKAGE OUTLINE

BQA0014A

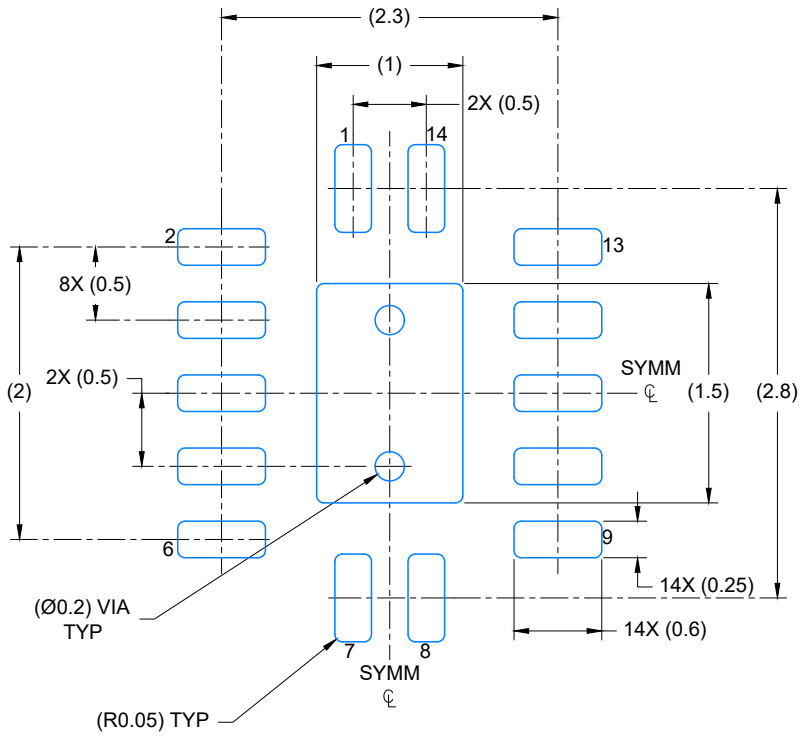
WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

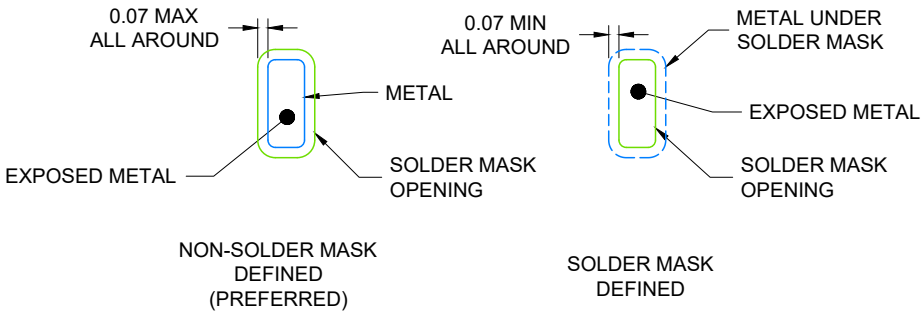


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



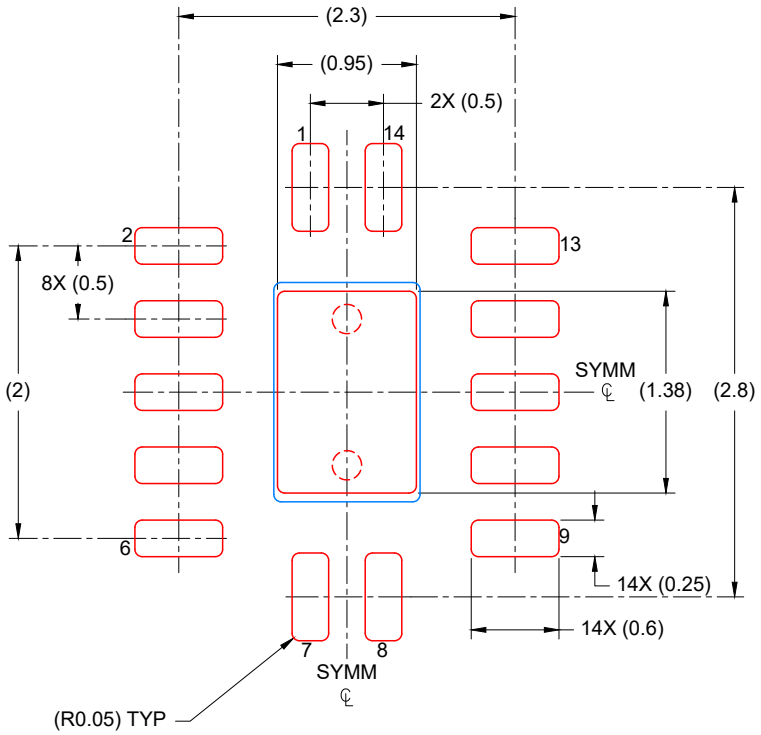
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

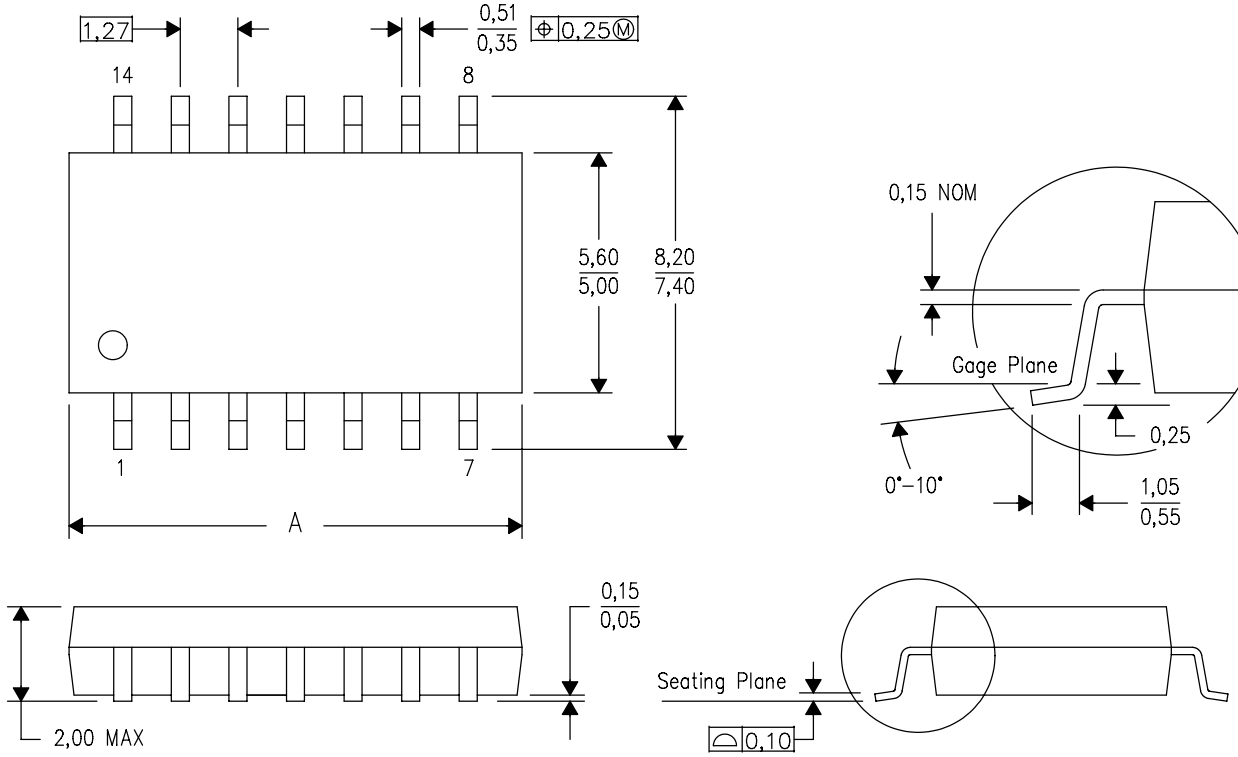
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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