

SN74AHCT244Q Octal Buffer/driver with 3-State Outputs

1 Features

- Q devices meet automotive performance requirements
- Customer-specific configuration control can be supported along with major-change approval
- EPIC™ (Enhanced-Performance Implanted CMOS) process
- Inputs are TTL-Voltage compatible Latch-Up performance exceeds 250 mA per JESD 17

2 Description

This octal buffer/driver is designed specifically to improve both the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

Package Information

| PART NUMBER | PACKAGE ¹ | BODY SIZE (NOM) |
|--------------|----------------------|--------------------|
| SN74AHCT244Q | DW (SOIC, 20) | 12.80 mm × 7.50 mm |
| | PW (TSSOP, 20) | 6.5 mm × 4.4 mm |

1. For all available packages, see the orderable addendum at the end of the data sheet.

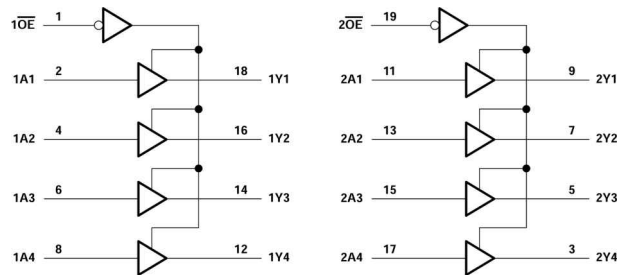


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3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision * (February 2002) to Revision A (May 2023) | Page |
|---|----------|
| • Added <i>Package Information</i> table, <i>Pin Functions</i> table, and <i>Thermal Information</i> table..... | 1 |

4 Pin Configuration and Functions

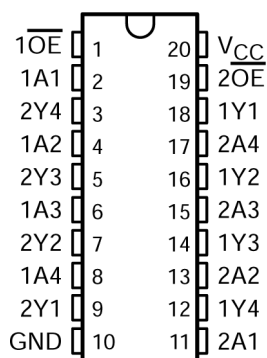


Figure 4-1. DW or PW Package (Top View)

Pin Functions

| PIN | | I/O1 | DESCRIPTION |
|-----------------|-----|------|-----------------------------------|
| Name | NO. | | |
| 1OE | 1 | I | Bank 1, output enable, active low |
| 1A1 | 2 | I | Bank 1, channel 1 input |
| 2Y4 | 3 | O | Bank 2, channel 4 output |
| 1A2 | 4 | I | Bank 1, channel 2 input |
| 2Y3 | 5 | O | Bank 2, channel 3 output |
| 1A3 | 6 | I | Bank 1, channel 3 input |
| 2Y2 | 7 | O | Bank 2, channel 2 output |
| 1A4 | 8 | I | Bank 1, channel 4 input |
| 2Y1 | 9 | O | Bank 2, channel 1 output |
| GND | 10 | — | Ground |
| 2A1 | 11 | I | Bank 2, channel 1 input |
| 1Y4 | 12 | O | Bank 1, channel 4 output |
| 2A2 | 13 | I | Bank 2, channel 2 input |
| 1Y3 | 14 | O | Bank 1, channel 3 output |
| 2A3 | 15 | I | Bank 2, channel 3 input |
| 1Y2 | 16 | O | Bank 1, channel 2 output |
| 2A4 | 17 | I | Bank 2, channel 4 input |
| 1Y1 | 18 | O | Bank 1, channel 1 output |
| 2OE | 19 | I | Bank 2, output enable, active low |
| V _{CC} | 20 | — | Positive supply |

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | | MIN | MAX | UNIT |
|---|---------------------------|---|------|-----------------------|------|
| V _{CC} | Supply voltage range | | −0.5 | 7 | V |
| V _I ⁽¹⁾ | Input voltage range | | −0.5 | 7 | V |
| V _O ⁽¹⁾ | Output voltage range | | −0.5 | V _{CC} + 0.5 | V |
| I _{IK} | Input clamp current | (V _I < 0) | −20 | | mA |
| I _{OK} | Output clamp current | (V _O < 0 or V _O > V _{CC}) | ±20 | | mA |
| I _O | Continuous output current | (V _O = 0 to V _{CC}) | ±25 | | mA |
| Continuous current through V _{CC} or GND | | | ±75 | | mA |
| T _{stg} | Storage temperature range | | −65 | 150 | °C |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions

(see [Note 1](#))

| | | MIN | MAX | UNIT |
|----------|--------------------------------|-----|----------|------|
| V_{CC} | Supply voltage | 4.5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | V |
| V_{IL} | Low-level input voltage | | 0.8 | V |
| V_I | Input voltage | 0 | 5.5 | V |
| V_O | Output voltage | 0 | V_{CC} | V |
| I_{OH} | High-level output current | | –8 | mA |
| I_{OL} | Low-level output current | | 8 | mA |
| T_A | Operating free-air temperature | –40 | 125 | °C |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5.3 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | SN74AHCT244Q | | UNIT |
|-------------------------------|--|--------------|------------|------|
| | | DW (SOIC) | PW (TSSOP) | |
| | | 20 PINS | 20 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 58 | 83 | °C/W |

- (1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | MIN | MAX | UNIT |
|---------------------------------|---|-----------------|-----------------------|-----|-------|-----|------|------|
| | | | MIN | TYP | MAX | | | |
| V _{OH} | I _{OH} = -50 µA | 4.5 V | 4.4 | 4.5 | | 4.4 | | V |
| | I _{OH} = -8 mA | | 3.94 | | | 3.8 | | |
| V _{OL} | I _{OL} = 50 µA | 4.5 V | | | 0.1 | | 0.1 | V |
| | I _{OL} = 8 mA | | | | 0.36 | | 0.44 | |
| I _{OZ} | V _O = V _{CC} or GND | 5.5 V | | | ±0.25 | | ±2.5 | µA |
| I _I | V _I = 5.5 V or GND | 0 V to 5.5 V | | | ±0.1 | | ±1 | µA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | | | 4 | | 40 | µA |
| ΔI _{CC} ⁽¹⁾ | One input at 3.4 V, Other inputs at V _{CC} or GND | 5.5 V | | | 1.35 | | 1.5 | mA |
| C _i | V _I = V _{CC} or GND | 5 V | | 2.5 | 10 | | | pF |
| C _O | V _O = V _{CC} or gnd | 5 V | | 3 | | | | pF |

(1) This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

5.5 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see [Figure 6-1](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | T _A = 25°C | | | MIN | MAX | UNIT |
|--------------------|-----------------|-------------|------------------------|-----------------------|-----|------|-----|-----|------|
| | | | | MIN | TYP | MAX | | | |
| t _{PLH} | A | Y | C _L = 15 pF | | 5.4 | 7.4 | 1 | 8.5 | ns |
| t _{PHL} | | | | | 5.4 | 7.4 | 1 | 8.5 | |
| t _{PZH} | \overline{OE} | Y | C _L = 15 pF | | 7.7 | 10.4 | 1 | 12 | ns |
| t _{PZL} | | | | | 7.7 | 10.4 | 1 | 12 | |
| t _{PHZ} | \overline{OE} | Y | C _L = 15 pF | | 5 | 9.4 | 1 | 10 | ns |
| t _{PLZ} | | | | | 5 | 9.4 | 1 | 10 | |
| t _{PLH} | A | Y | C _L = 50 pF | | 5.9 | 8.4 | 1 | 9.5 | ns |
| t _{PHL} | | | | | 5.9 | 8.4 | 1 | 9.5 | |
| t _{PZH} | \overline{OE} | Y | C _L = 50 pF | | 8.2 | 11.4 | 1 | 13 | ns |
| t _{PZL} | | | | | 8.2 | 11.4 | 1 | 13 | |
| t _{PHZ} | \overline{OE} | Y | C _L = 50 pF | | 8.8 | 11.4 | 1 | 13 | ns |
| t _{PLZ} | | | | | 8.8 | 11.4 | 1 | 13 | |
| t _{sk(o)} | | | C _L = 50 pF | | | 1 | | | ns |

5.6 Noise Characteristics

$V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see [Note 1](#))

| PARAMETER | | MIN | TYP | MAX | UNIT |
|-------------|--|-----|-----|-----|------|
| $V_{OH(V)}$ | Quiet output, minimum dynamic V_{OH} | | 4.1 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.8 | V |

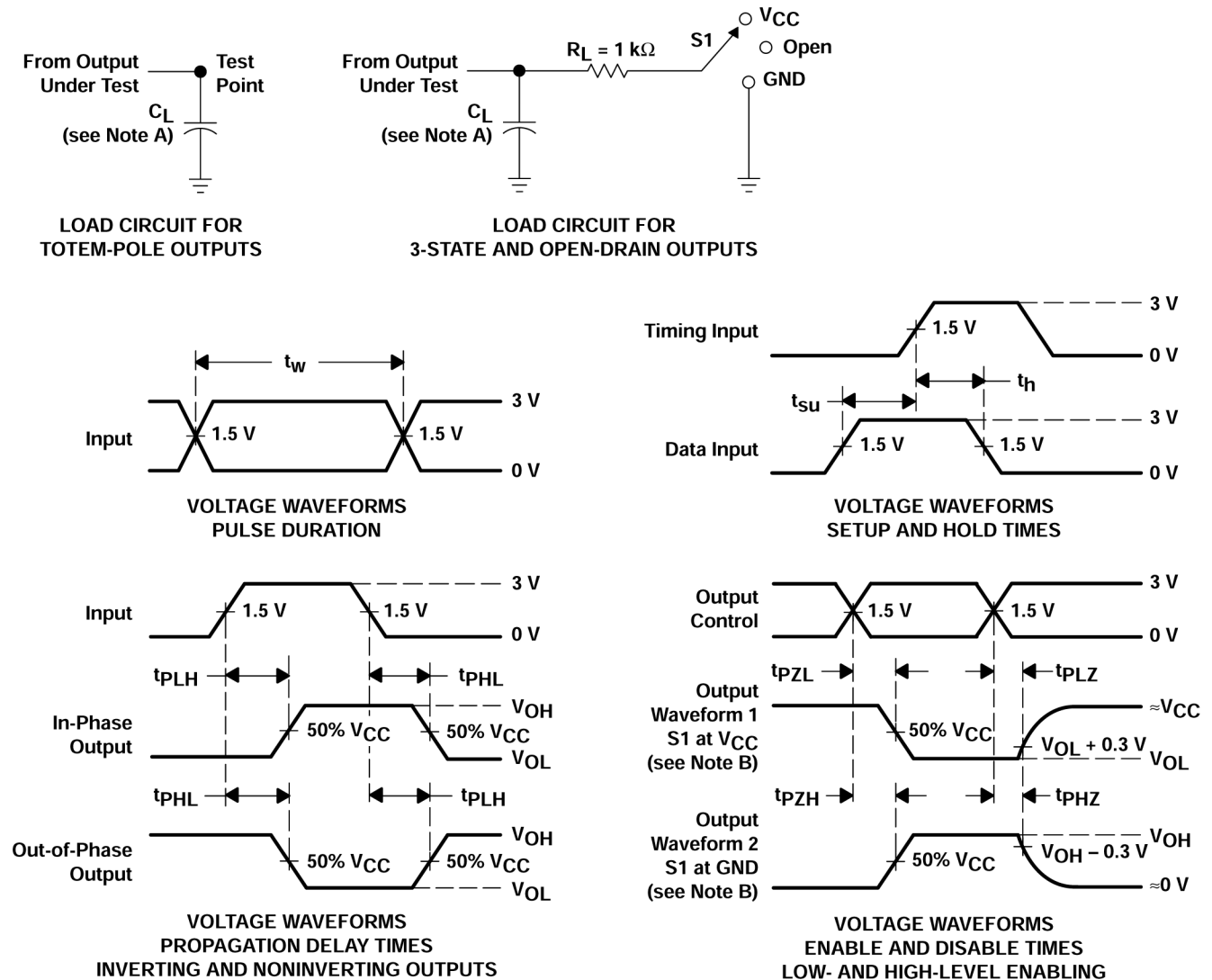
(1) Characteristics are for surface-mount packages only.

5.7 Operating Characteristics

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|-----------|-------------------------------|-----------------------------|-----|------|
| C_{pd} | Power dissipation capacitance | No load, $f = 1\text{ MHz}$ | 8.2 | pF |

6 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 6-1. Load Circuit and Voltage Waveforms

| TEST | S1 |
|-------------------|----------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{CC} |
| t_{PHZ}/t_{PZH} | GND |
| Open Drain | V_{CC} |

7 Detailed Description

7.1 Overview

The SN74AHCT244Q is organized as two 4-bit buffers/line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagram

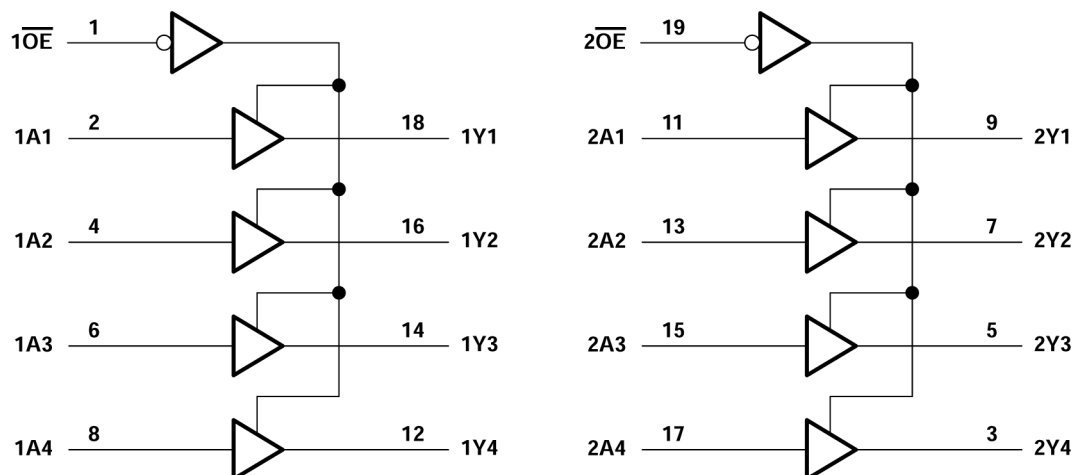


Figure 7-1. Logic Diagram (Positive Logic)

This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

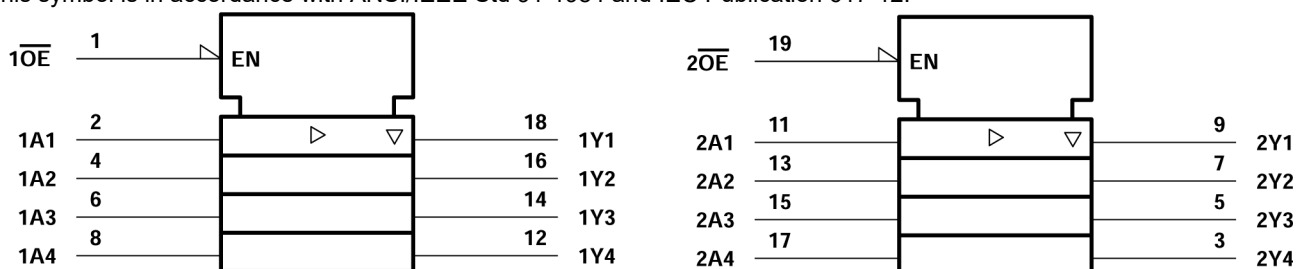


Figure 7-2. Logic Symbol

7.3 Device Functional Modes

Table 7-1. Function Table (Each 4-Bit Buffer/driver)

| INPUTS | | OUTPUT Y |
|-----------------|---|----------|
| \overline{OE} | A | |
| L | H | H |
| L | L | L |
| H | X | Z |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74AHCT244QDWR | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHCT244Q | Samples |
| SN74AHCT244QPWR | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HB244Q | Samples |
| SN74AHCT244QPWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | | HB244Q | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AHCT244QDWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74AHCT244QPWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74AHCT244QPWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| SN74AHCT244QPWRG4 | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AHCT244QDWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74AHCT244QPWR | TSSOP | PW | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74AHCT244QPWR | TSSOP | PW | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74AHCT244QPWRG4 | TSSOP | PW | 20 | 2000 | 356.0 | 356.0 | 35.0 |

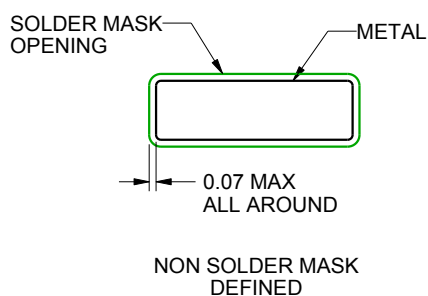
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC

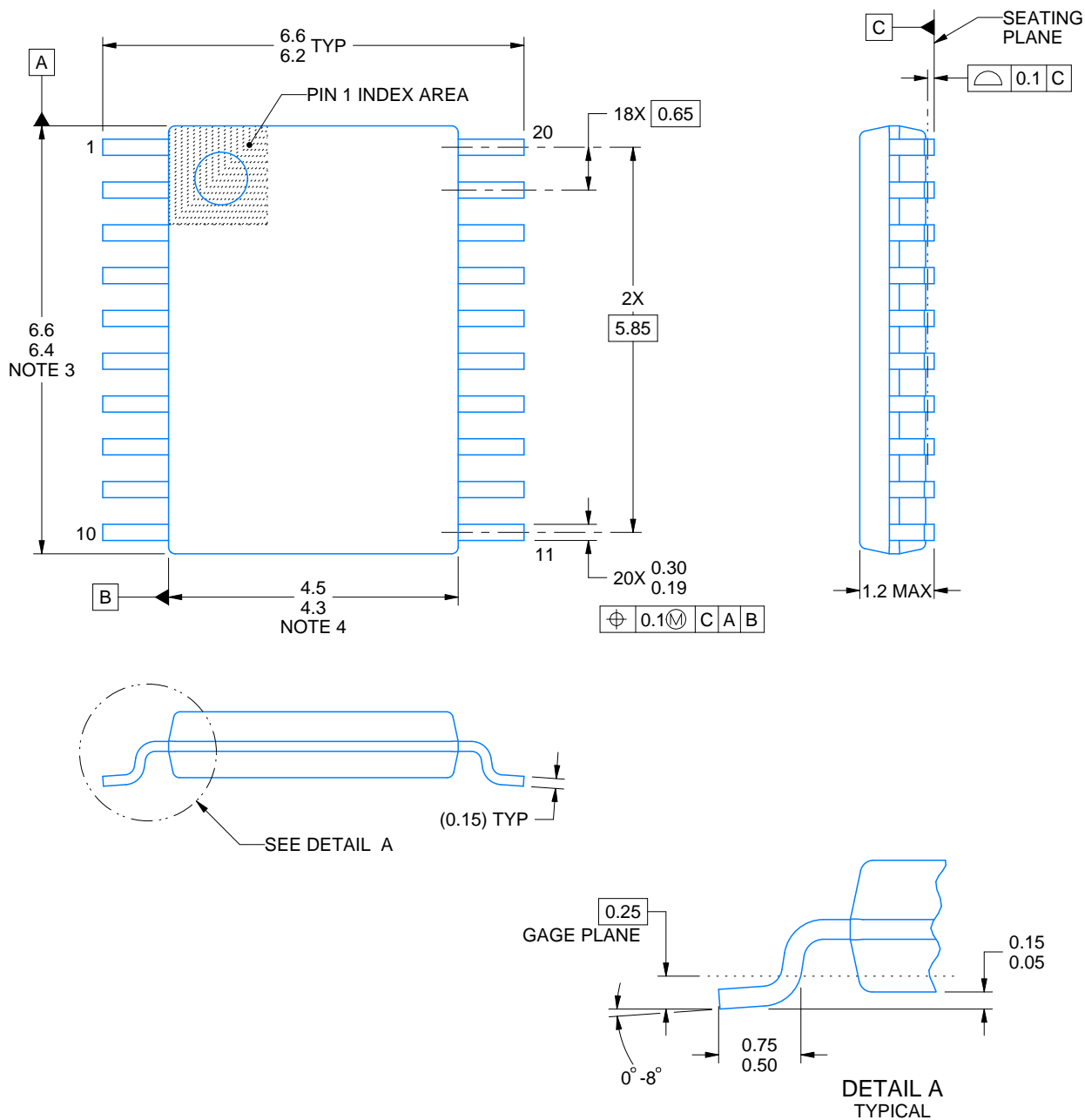
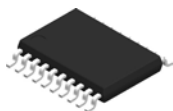


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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