life.augmented

STPMIC25

Datasheet

Highly integrated power management IC for microprocessor units

Maturity status link
STPMIC25

Device summary	
Order code	STPMIC25APQR
	STPMIC25BPQR
	STPMIC25DPQR
Packing	WFQFN 56L (6.5 x 6.5 x 0.9 mm)

Features

- Input voltage range from 2.8 V to 5.5 V
- 7 buck SMPS converters with adaptive constant on-time (COT) topology
- 6 adjustable general purpose LDOs
- 1 LDO for DDR3L/DDR4 termination (sink-source), bypass mode for lpDDR or as a general purpose LDO
- 1 LDO for USB PHY supply with automatic power source detection
- 1 reference voltage VREFDDR LDO for DDR memory
- 2 MHz switching frequency buck converters with forced PWM and spread spectrum function
- User programmable non-volatile memory (NVM), enabling scalability to support a wide range of applications
- Immediate output alternate settings toggle by dedicated power control pins
- Programmable output voltages turn ON/OFF sequences
- I²C and digital I/O control interfaces
- WFQFN 56L (6.5 x 6.5 x 0.9 mm)

Applications

- Power management for embedded microprocessor units
- Wearable and IoT
- Portable devices
- Man-machine interfaces
- Smart home
- Power management unit companion chip of the STM32MP2 MPU

Description

The STPMIC25 is a fully integrated power management IC designed for the STM32MP2x MPU's family applications requiring low power and high efficiency.

The device integrates advanced low power features controlled by a host processor via I²C and IO interfaces.

The STPMIC25 regulators are designed to supply power to the application processor as well as to the external system peripherals such as: DDR, flash memories, and other system devices.

Seven buck SMPS are optimized to provide an excellent transient response and output voltage precision for a wide range of operating conditions. Very high efficiency in the full output load range is achieved due to low power mode (LPM) and high power mode (HPM) selection. All the buck converters are capable of a smooth transition from LPM to HPM. The converters use an advanced PWM phase shift synchronization technique with integrated PLL and a programmable spread spectrum frequency modulation to reduce EMI.

1 Device configuration table

The STPMIC25 has a non-volatile memory (NVM) that enables scalability to support a wide range of applications:

- Default output voltage, POWER_UP/POWER_DOWN sequence, protection behavior, auto turn-on functionality, and an I²C slave address.
- The STPMIC25A, STPMIC25B and STPMIC25D are preprogrammed devices to support the STM32MP2 series application processor versions.
- Straightforward NVM reprogramming via I²C to facilitate mass production directly in target applications.
- Possibility to lock NVM content to prevent further reprogramming by writing LOCK_NVM bit.

Table 1. Default configuration table

	Default configuration table								
	STPMIC25A			STPMIC25B			STPMIC25D		
	Default output voltage	Default output current	Rank	Default output voltage	Default output current	Rank	Default output voltage	Default output current	Rank
LDO1	1.80 V	20 mA OCP level1	1	1.80 V	20 mA OCP level1	1	1.80 V	20 mA OCP level1	1
LDO2	3.30 V	0.4 A OCP level0	4	2.90 V	0.4 A OCP level0	4	3.30 V	0.4 A OCP level0	4
LDO3	-	-	0	-	-	0	-	-	0
LDO4	3.30 V	40 mA OCP Level0	5	3.30 V	40 mA OCP Level0	5	3.30 V	40 mA OCP Level0	5
LDO5	-	-	0	-	-	0	-	-	0
LDO6	-	-	0	-	-	0	-	-	0
LDO7	-	-	0	-	-	0	Bypass	0.4 A OCP Level0	4
LDO8	-	-	0	-	-	0	Bypass	0.15 A OCP Level0	4
VREFDDR	-	-	0	-	-	0	-	-	0
BUCK1	0.80 V	1.0 A OCP Level1	3	0.80 V	1.0 A OCP Level1	3	0.80 V	1.0 A OCP Level1	3
BUCK2	0.82 V	2.0 A OCP Level1	2	0.82 V	2.0 A OCP Level1	2	0.82 V	2.0 A OCP Level1	2
BUCK3	-	-	0	-	-	0	-	-	0
BUCK4	3.30 V	0.5 A OCP Level1	1	1.80 V	0.5 A OCP Level1	1	3.30 V	0.5 A OCP Level1	1
BUCK5	1.80 V	0.5 A OCP Level1	3	1.80 V	0.5 A OCP Level1	3	1.80 V	0.5 A OCP Level1	3
BUCK6	-	-	0	-	-	0	-	-	0
BUCK7	3.30 V	2.5 A OCP Level0	4	3.30 V	2.5 A OCP Level0	4	3.30 V	2.5 A OCP Level0	4
VINOK_Rise	4.0 V		-	3.3V		-	4.0 V		-
VINOK_Fall	3.5V		-	2.8V		-	3.5V		-

All output voltages with Rank = 0 are, by default, programmed with 0 Dec, (refer to Table 19 and Table 20.

The startup sequence is split into four steps (Rank0 to Rank5).

Each BUCK converter or LDO regulator can be programmed to be automatically turned ON in one of these phases. Each rank phase is separated by a delay (1.5 ms, 3 ms, 4.5 ms, or 6 ms) programmed in the NVM:

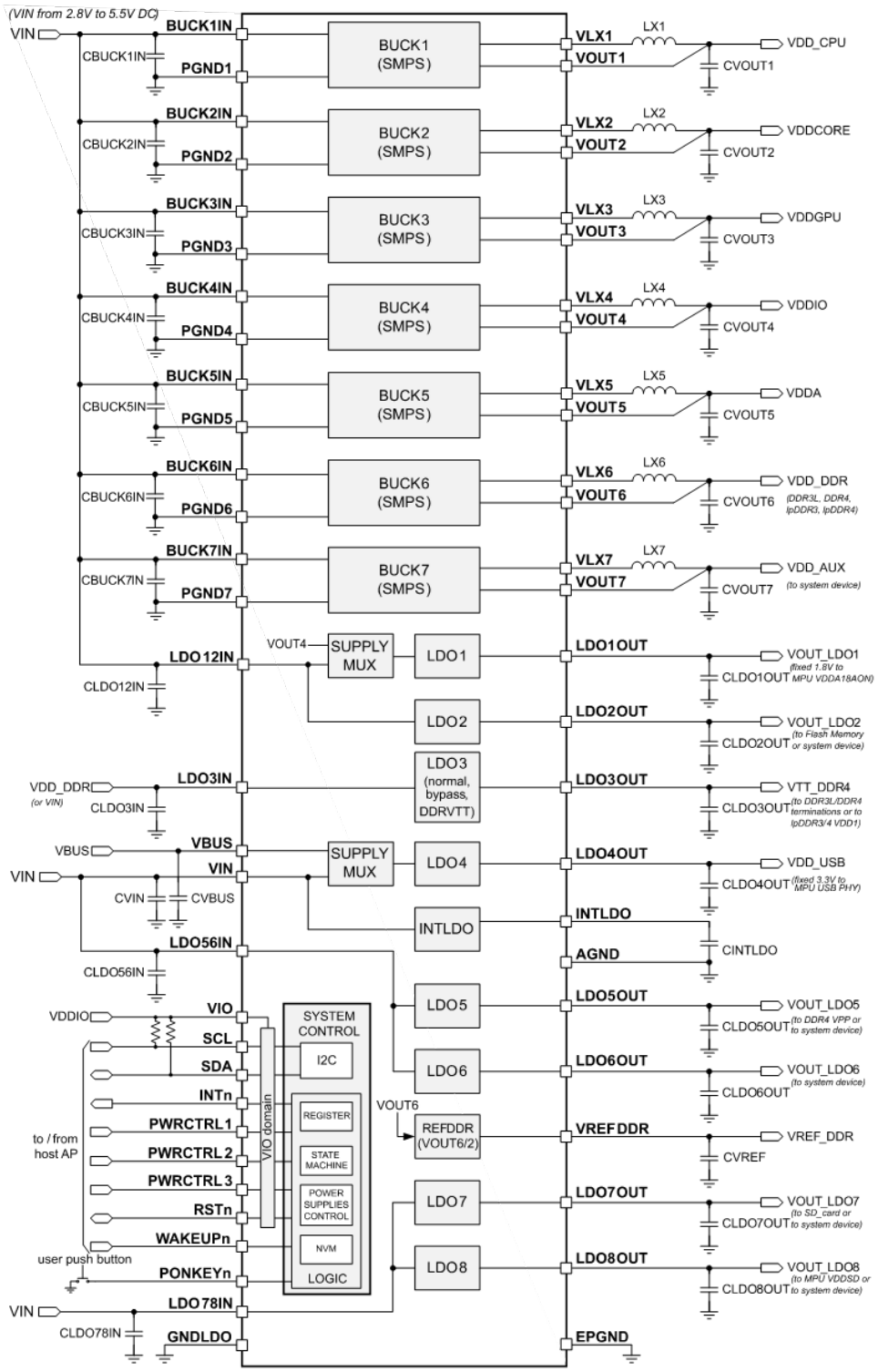
- Rank = 0: rail not turned ON automatically, no output voltage appears after POWER-UP
- Rank = 1: rail automatically turned ON after 7 ms following a turn_ON condition
- Rank = 2: rail automatically turned ON after a further 1.5 ms (by default)
- Rank = 3: rail automatically turned ON after a further 1.5 ms (by default)
- Rank = 4: rail automatically turned ON after a further 1.5 ms (by default)
- Rank = 5: rail automatically turned ON after a further 1.5 ms (by default)

Whatever the STPMIC25 version, the AUTO_TURN_ON option is set.

For complete default NVM configuration table refer to AN6198 application note

2 Typical application schematic

Figure 1. **Typical application schematic**



2.1 Recommended external components

Table 2. Passive components

Component	Manufacturer	Part number	Value	Size
CVIN, CLDO1OUT, CLDO2OUT, CLDO4OUT, CLDO5OUT, CLDO6OUT, CLDO7OUT, CLDO8OUT, CINTLDO	MURATA	GRM155R60J475ME47D	4.7 µF, 6.3 V	0402
CBUCK1IN, BUCK2IN, CBUCK3IN, CBUCK4IN, CBUCK5IN, CBUCK6IN, CBUCK7IN		GRM188R61A106ME69D	10 µF, 10 V	0603
CVOUT1, CVOUT6		GRM188R60J226MEA0D	3 x 22 µF, 6.3 V	0603
CVOUT2, CVOUT3			4 x 22 µF, 6.3 V	
CVOUT4, CVOUT5		GRM21BR61A226ME51L	3 x 22 µF, 10 V	0805
CVOUT7			4 x 22 µF, 10 V	
CLDO12IN, CLDO56IN, CLDO78IN, CVREF		GRM155R61E105KA12D	1 µF, 25 V	0402
CLDO3IN, CLDO3OUT (1)		GRM155R60J106ME05D	10 µF, 6.3 V	0402
CVBUS		GRM188R61C475KE11D	4.7 µF, 16 V	0603
LX1, LX6, LX7		DFE201610E-R68M=P2	0.68 µH	0806
LX2, LX3		DFE252012F-R68M=P2	0.68 µH	1008
LX4, LX5		DFE201610E-2R2M=P2	2.2 µH	0806

1. *4.7 µF normal mode - 10 µF sink/source mode.*

Note: All the components above refer to a typical application working in an environment up to +85 °C ambient temperature. The operation of the device is not limited to the choice of these external components. For different environment application needs, see the forthcoming application note.

2.2 Pinout and pin description

Figure 2. **Pin configuration WFQFN 56L top view**

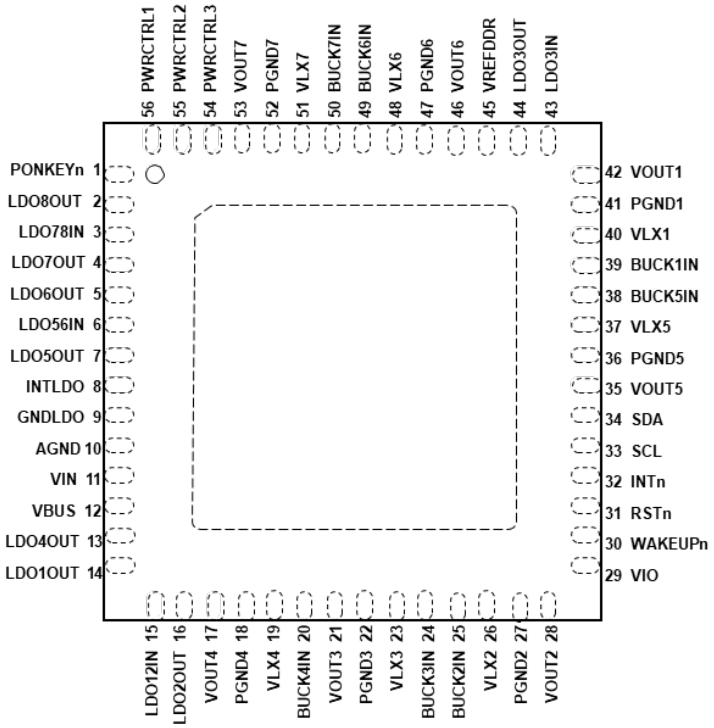


Table 3. **Pin description**

Pin name	A/D [1]	I/O [1]	Location	Description (default configuration)	Not used pin connection
PONKEYn	D	I	1	User power ON key (active low with internal pull-up)	Floating
LDO8OUT	A	O	2	Output voltage LDO8	Floating
LDO78IN	A	I	3	Power input LDO7 and LDO8	VIN
LDO7OUT	A	O	4	Output voltage LDO7	Floating
LDO6OUT	A	O	5	Output voltage LDO6	Floating
LDO56IN	A	I	6	Power input LDO5 and LDO6	VIN
LDO5OUT	A	O	7	Output voltage LDO5	Floating
INTLDO	A	O	8	Internal LDO	4.7 µF capacitor
GNDLDO	A	-	9	LDO GND	GND
AGND	A	-	10	Main analog ground	GND
VIN	A	I	11	Main power input - power input LDO4, VREF	VIN
VBUS	A	I	12	USB input voltage	Floating
LDO4OUT	A	O	13	Output voltage LDO4	Floating
LDO1OUT	A	O	14	Output voltage LDO1	Floating
LDO12IN	A	I	15	Power input LDO1 and LDO2	VIN
LDO2OUT	A	O	16	Output voltage LDO2	Floating
VOUT4	A	I	17	Input feedback signal buck converter 4	GND
PGND4	A	-	18	Power ground buck converter 4	GND

Pin name	A/D [1]	I/O [1]	Location	Description (default configuration)	Not used pin connection
VLX4	A	O	19	LX node buck converter 4	Floating
BUCK4IN	A	I	20	Power input buck converter 4	VIN
VOUT3	A	I	21	Input feedback signal buck converter 3	GND
PGND3	A	-	22	Power ground buck converter 3	GND
VLX3	A	O	23	LX node buck converter 3	Floating
BUCK3IN	A	I	24	Power input buck converter 3	VIN
BUCK2IN	A	I	25	Power input buck converter 2	VIN
VLX2	A	O	26	LX node buck converter 2	Floating
PGND2	A	-	27	Power ground buck converter 2	GND
VOUT2	A	I	28	Input feedback signal buck converter 2	GND
VIO	A	I	29	I/O voltage (for all digital signals except WAKEUP and PONKEYn)	VIO
WAKEUPn	D	I	30	Power-ON from host processor (active low with internal pull-up)	Floating
RSTn	D	I/O	31	Bidirectional reset (active low with internal pull-up)	Floating
INTn	D	O	32	Interrupt (active low with internal pull-up)	Floating
SCL	D	I	33	I²C serial clock	VIO
SDA	D	I/O	34	I²C serial data	VIO
VOUT5	A	I	35	Input feedback signal buck converter 5	GND
PGND5	A	-	36	Power ground buck converter 5	GND
VLX5	A	O	37	LX node buck converter 5	Floating
BUCK5IN	A	I	38	Power input buck converter 5	VIN
BUCK1IN	A	I	39	Power input buck converter 1	VIN
VLX1	A	O	40	LX node buck converter 1	Floating
PGND1	A	-	41	Power ground buck converter 1	GND
VOUT1	A	I	42	Input feedback signal buck converter 1	GND
LDO3IN	A	I	43	Power input LDO3	VIN
LDO3OUT	A	O	44	Output voltage LDO3	VIN
VREFDDR	A	O	45	DDR VREF output voltage	Floating
VOUT6	A	I	46	Input feedback signal buck converter 6	GND
PGND6	A	-	47	Power ground buck converter 6	GND
VLX6	A	O	48	LX node buck converter 6	Floating
BUCK6IN	A	I	49	Power input buck converter 6	VIN
BUCK7IN	A	I	50	Power input buck converter 7	VIN
VLX7	A	O	51	LX node buck converter 7	Floating
PGND7	A	-	52	Power ground buck converter 7	GND
VOUT7	A	I	53	Input feedback signal buck converter 7	GND
PWRCTRL3	D	I	54	Power control 3 mode (pull-up and pull-down, active by default pull-up)	VIO or GND
PWRCTRL2	D	I	55	Power control 2 mode (pull-up and pull-down, active by default pull-up)	VIO or GND
PWRCTRL1	D	I	56	Power control 1 mode (pull-up and pull-down, active by default pull-up)	VIO or GND
EPGND	A	-	ePad	Exposed pad to be connected to ground	GND

1. *A: analog; D: digital; I/O: input/Output*

3 Electrical and timing characteristics

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Parameter	Min.	Unit
VIN, BUCKxIN, VLXx, LDO3IN, LDOxIN, PONKEYn, VBUS	-0.5 to +6.5	V
VIO, SDA, SCL, RSTn, PWRCTRLx, INTn, WAKEUPn	-0.5 to +4.2	
INTLDO	-0.5 to +2	
VOUT1, VOUT2, VOUT3, VOUT6	-0.5 to +3	
VOUT4, VOUT5, VOUT7, LDOxOUT, VREFDDR	-0.5 to +5	
Storage temperature range	-65 to +150	°C
ESD HBM	±1000	V
ESD CDM	±500	

Note: Stressing the device above the absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

3.2 Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Value	Unit
T_j	Absolute maximum junction temperature	-40 to +150	°C
T_A	Operating ambient temperature	-40 to +105	
Θ_{JC}	Junction-case package thermal resistance	6	°C/W
Θ_{JA}	Junction-ambient package thermal resistance	32	

3.3 Consumption in typical application scenarios

STPMIC25 V_{IN} input current consumption (all supply pins connected to V_{IN}, V_{IN} = 3.6 V, V_{IO} = 1.8 V (from V_{OUT4}), T_j = +25 °C, unless otherwise specified.

Table 6. Consumption in typical application scenarios

Application mode	Application description	Conditions	Typ.	Unit
OFF	AP and peripherals are powered OFF, waiting for a turn-on event to start.	PMIC in OFF state. Turn-on from PONKEYn, WAKEUPn, and VBUS I²C inactive. All regulators OFF.	35 (1)	µA
STANDBY	AP is in STANDBY NO-RETENTION. All peripherals are powered OFF.	PMIC in POWER_ON STANDBY, state IRQ from PONKEYn, WAKEUPn, and VBUS PWRCTRLx active. BUCK4 ON_ LP, VOUT4=1.8 V (VDD) LDO1ON, VLDO1OUT=1.8 V (VDD18AON) All other regulators OFF. All outputs without load. No activity on I²C.	120	
STOP	AP is in STOP2-LPLV (Core ON, CPU & GPU OFF) lpDDR4 is in self-refresh. All peripherals are powered OFF.	PMIC in POWER_ON RUN state. IRQ from PONKEYn, WAKEUPn, and VBUS PWRCTRLx active. BUCK2 ON_ LP, VOUT2=0.63 V (VDDCORE) BUCK4 ON_ LP, VOUT4=1.8 V (VDD) BUCK5 ON_ LP, VOUT5=1.8 V (VDDA1V8) BUCK6 ON_ LP, VOUT6=1.2 V (VDD_DDR) LDO1 ON, VLDOOUT=1.8 V (VDD18AON) LDO3 ON, VLDOOUT=1.8 V (VDD_DDR) All other regulators OFF. All outputs without load. No activity on I²C	420	
RUN	Application is in RUN_IOT_UI (Core, CPU, GPU on) lpDDR4 is running.	PMIC in POWER_ON RUN state. IRQ from PONKEYn, WAKEUPn, and VBUS. PWRCTRLx active. BUCK1 ON_HP, VOUT1=0.92 V (VDDCPU) BUCK2 ON_ HP, VOUT2=0.85 V (VDDCORE) BUCK3 ON_HP, VOUT3=0.90 V (VDDGPU) BUCK4 ON_ HP, VOUT4=1.8 V (VDD) BUCK5 ON_ HP, VOUT5=1.8 V (VDDA1V8) BUCK6 ON_ HP, VOUT6=1.1 V (VDD_DDR) LDO1 ON, VLDOOUT=1.8 V (VDD18AON) LDO3 ON, VLDOOUT=1.8 V (VDD_DDR) LDO4 ON, VLDOOUT=3.3 V (VDD3V3_USB) All other regulators OFF. All outputs without load. No activity on I²C.	2	mA

1. *Current consumption, 100 µA max at Tj = -40 °C to +105 °C*

3.4 Electrical and timing parameter specifications

All parameters are specified at V_{IN} = $V_{BUCKxIN}$ = V_{LDOxIN} = 5 V, V_{OUT1} = 0.85 V, V_{OUT2} = 0.85 V, V_{OUT3} = 0.85 V, V_{OUT4} = 3.3 V, V_{OUT5} = 1.8 V, V_{OUT6} = 1.1 V, V_{OUT7} = 3.3 V, $V_{LDO1OUT}$ = 1.8 V, $V_{LDO2OUT}$ = $V_{LDO5OUT}$ = $V_{LDO6OUT}$ = $V_{LDO7OUT}$ = $V_{LDO8OUT}$ = 2.9 V, $V_{LDO3OUT}$ = 1.8 V, $V_{LDO4OUT}$ = 3.3 V, V_{IO} = V_{OUT4}, T_j = -40 °C to +125 °C, with recommended BOM, unless otherwise specified.

3.4.1 General section

Table 7. Electrical and timing parameter specifications (general section)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
General section						
V_{IN}	Input voltage range		2.8	3.6 or 5	5.5	V
V_{INPOR_Rise}	$V_{IN\ POR}$ rising threshold		2.2	2.3	2.4	V
V_{INPOR_Fall}	$V_{IN\ POR}$ falling threshold			2.1	2.2	V
V_{INOK_Rise}	V_{INOK} rising threshold	Programmable value defined in the NVM register	3	3.1	3.2	V
			3.2	3.3	3.4	
			3.35	3.5	3.6	
			3.8	4.0	4.1	
V_{INOK_HYST}	V_{INOK} hysteresis	Programmable value defined in the NVM register		200 300 400 500		mV
V_{INOK_Fall}	V_{INOK} falling threshold	Defined indirectly by V_{INOK_Rise} and V_{INOK_HYST} settings		V_{INOK_Rise} - V_{INOK_HYST}		mV
t_{VINOK_Fall}	V_{INOK} falling delay	When V_{IN} is crossing V_{INOK_Fall}, PMIC power-down then cannot restart before t_{VINOK_Fall} delay, even if V_{IN} > V_{INOK_Rise}		100		ms
V_{INLOW_Rise}	(*)V_{INLOW} rising threshold	Programmable value defined in register V_{INLOW_CR} VINLOW_Rise is guaranteed as the sum of VINOK_Fall + OFFSET values here reported.	+20 +300	+50 to +400	+80 +500	mV
V_{INLOW_HYST}	V_{INLOW} hysteresis	Programmable value defined in register V_{INLOW_CR}	90	100	110	mV
			180	200	220	
			270	300	330	
			360	400	440	
V_{INLOW_Fall}	V_{INLOW} falling threshold	Defined indirectly by V_{INLOW_Rise} and V_{INLOW_HYST} settings		V_{INLOW_Rise} + V_{INLOW_HYST}		mV
V_{BUS_Rise}	V_{BUS} rising threshold		3.6	3.8	4.0	V
V_{BUS_Fall}	V_{BUS} falling threshold		2.0	2.2	2.4	V
t_{VBUSDB}	V_{BUS} debounce filter duration			30		ms
T_{WRN_Rise}	Warning temperature rising		115	125	135	°C

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{WRN_Fall}	Warning temperature falling		95	105	120	°C
T_{SHDN_Rise}	Shutdown temperature rising		140	150	160	°C
T_{SHDN_Fall}	Shutdown temperature falling		105	115	130	°C
t_{TSHDN_DLY}	Shutdown temperature falling delay			3		s
t_{OCPDB_LDO}	LDO OCP turn-off delay			5		ms
t_{OCPDB_BUCK}	BUCK OCP turn-off delay			5		ms
t_{HICCUP_DLY}	Hiccup mode OFF delay	Programmable value defined in NVM_BUCKS_IOUT_SHR2 NVM register		0 100 500 1000		ms
t_{WD}	Watchdog timer	Programmable value defined in the register		1 to 256		s
		Timer programming step		1		
NVM_{END}	NVM write cycles endurance	Recommended maximum writing cycles (1)			10	Cycle
V_{NVM_PROG}	NVM min voltage for write operation		3.8			V

1. *NVM writing procedures must be performed under controlled electrical/environmental values.*

3.4.2 Digital interface

Table 8. Electrical and timing parameter specifications (digital interface)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Digital interface						
V_{IO}	V_{IO} input voltage for IO signal		1.7	1.8 or 3.3	3.6	V
V_{IL}	PONKEYn input low voltage		0		0.3 x V_{IN}	
	WAKEUPn input low voltage		0		0.3 x V_{INTLDO}	
	RSTn, PWRCTRL1, PWRCTRL2, PWRCTRL3, input low voltage	Tj = 25°C	0		0.3 x V_{IO}	
	SDA, SCL input low voltage	Tj = 25°C	0		0.3 x V_{IO}	
V_{IH}	PONKEYn input high voltage		0.7 x V_{IN}		V_{IN}	
	WAKEUPn input high voltage		0.7 x V_{INTLDO}		V_{INTLDO}	
	RSTn, PWRCTRL1, PWRCTRL2, PWRCTRL3, input high voltage		0.7 x V_{IO}		V_{IO}	
	SDA, SCL input high voltage		0.7 x V_{IO}		V_{IO}	
V_{HYST}	PONKEYn input hysteresis			0.1 x V_{IN}		
	WAKEUPn input hysteresis			0.1 x V_{INTLDO}		
	RSTn, PWRCTRL1, PWRCTRL2, PWRCTRL3, input hysteresis			0.1 x V_{IO}		
	SDA, SCL input hysteresis			0.1 x V_{IO}		
V_{OL}	RSTn output low voltage	I_{IO} = 4 mA, Tj = 25°C	-		0.4	
	INTn output low voltage	I_{IO} = 4 mA, Tj = 25°C	-		0.4	
	SDA, SCL output low voltage	I_{IO} = 4 mA, Tj = 25°C	-		0.4	
R_{PD}	PWRCTRL1, PWRCTRL2, and PWRCTRL3 pins pull-down resistor	Internally connected to GND	60	90	140	KΩ
R_{PU}	PWRCTRL1, PWRCTRL2, and PWRCTRL3 pins pull-up resistor	Internally connected to V_{IO}	50	80	120	
	WAKEUPn pin pull-up resistor	Internally connected to V_{INTLDO}	2500	4000	5500	
	RSTn pin pull-up resistor	Internally connected to V_{IO}	50	80	120	
	INTn pin pull-up resistor	Internally connected to V_{IO}	50	80	120	
	PONKEYn pin pullup resistor	Internally connected to V_{IN}	80	110	140	
$t_{PONKEYnDB}$	PONKEYn debounce filter duration			30		ms
$t_{WAKEUPnAS}$	WAKEUPn assertion time (1)		20			µs
t_{RSTnAS}	RSTn assertion time (2)		20			

1. *WAKEUPn has no debounce filter. PMIC detects a pulse smaller than $t_{WAKEUPnAS}$ duration. PMIC must detect a pulse equal to or longer than $t_{WAKEUPnAS}$ duration.*
2. *RSTn has no debounce filter. PMIC detects a pulse smaller than t_{RSTnAS} duration. PMIC must detect a pulse equal to or longer than t_{RSTnAS} duration.*

3.4.3 LDO1 (VDDA18AON)

Table 9. Electrical and timing parameter specifications (LDO1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
LDO1						
V_{LDOIN}	Main input voltage range		2.8		5.5	V
V_{LDOOUT}	Output voltage			1.8		
$V_{LDOOUT-ACC}$	Output voltage accuracy	2.8 V < V_{LDOIN} < 5.5 V, 10 µA < I_{LDOOUT} < 20 mA	-4		+4	%
I_{LDOLIM}	Output current limitation	2.8 V < V_{LDOIN} < 5.5 V	20	30		mA
I_{LDO12Q}	Total quiescent current	I_{LDOOUT} = 0 mA Measured from the related common input pin, LDO12IN			10	µA
$I_{LDO12IN\_LKG}$	Input leakage current	LDO1 output disabled, Tj = 25 °C Measured from common input pin, LDO12IN			2	
$V_{LDOOUT-LO}$	Load transient regulation	I_{LDOOUT} = 10 µA to 10 mA, t_R = t_F = 1 µs		10		mV
$V_{LDOOUT-LI}$	Line transient regulation	V_{LDOIN} = 3.0 V to 3.6 V, I_{LDOOUT} = 0, t_R = t_F = 10 µs		5		
$PSRR_{LDO}$	Power supply rejection ratio	ΔV_{LDOIN} = 300 mV_{PP}, f = [0.1:20] kHz, T_j = 25 °C, I_{LDOOUT} = 10 mA		50		dB
		Δ_{VLDOIN} = 300 mV_{PP}, f = [20:100] kHz, T_j = 25 °C, I_{LDOOUT} = 10 mA		45		
N	Output noise	I_{LDOOUT} = 10 µA to 10 mA, f = 10 Hz to 5 MHz, T_j = 25 °C, all bucks enabled		250		μV_{RMS}
t_{SSLDO}	Soft-start duration	2.8 V < V_{LDOIN} < 5.5 V, 0 < I_{LDOOUT} < 1 mA, C_{OUT} = 4.7 µF		230		µs
$V_{LDOOUT-SO}$	Startup overshoot	2.8 V < V_{LDOIN} < 5.5 V, I_{LDOOUT} < 10 µA		1		%
t_{SDLDO}	Shutdown duration	Pull-down enabled, V_{LDOOUT}= 1.8 V to V_{LDOOUT} = 0.2 V, I_{LDOOUT} = no load			1.5	ms

3.4.4 LDO2, LDO5, LDO6, LDO7

Table 10. Electrical and timing parameter specifications (LDO2/5/6/7)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
LDO2, LDO5, LDO6, LDO7 (normal mode)						
V_{LDOIN}	Main input voltage range		2.8		5.5	V
V_{LDOOUT}	Output voltage	V_{LDOIN} > V_{LDOOUT}+$V_{LDODROP}$ Programmable value.		0.9 to 4.0		V
		Voltage programming step		100		mV
$V_{LDOOUT-ACC}$	Output voltage accuracy	V_{LDOIN} = 3.6 V or 5.0 V 1.7 V < V_{LDOOUT} < 3.3 V 100 µA < I_{LDOOUT} < 350 mA	-2		2	%
I_{LDOLIM}	Output current limitation	2.8 V < V_{LDOIN} < 5.5 V I_{LDOLIM} programmable in NVM_$L_{DOS_IOUT_SHR}$ Ref. Section 1 NVM setting A and B versions	50 100 200 400		75 150 300 600	mA
I_{LDOxxQ}	Total quiescent current	I_{LDOOUT} = 0 mA, V_{LDOIN} = 5 V Measured from the related common input pin, L_{DOxxIN}		4	20	µA
$I_{LDOxxIN\_LKG}$	Input leakage current	LDOx output disabled Measured from the related common input pin, L_{DOxxIN}			2	
$V_{LDODROP}$	Dropout voltage	V_{LDOOUT} = 2.9 V, I_{LDOOUT} = 350 mA		180	300	mV
$V_{LDOOUT-LO}$	Load transient regulation	I_{LDOOUT} = 1 mA to 180 mA, t_R = t_F = 1 µs		35		
$V_{LDOOUT-LI}$	Line transient regulation	V_{LDOIN} = 3.0 V to 3.6 V, t_R = t_F = 10 µs		10		
$PSRR_{LDO}$	Power supply rejection ratio	ΔV_{LDOIN} = 300 mV_{PP}, f = [0.1:20] kHz, Tj = 25 °C, I_{LDOOUT} = 200 mA		43		dB
		ΔV_{LDOIN} = 300 mV_{PP}, f = [20:100] kHz, Tj = 25 °C, I_{LDOOUT} = 200 mA		37		
t_{SSLDO}	Soft-start duration	2.8 V < V_{LDOIN} < 5.5 V, 0 < I_{LDOOUT} < 1 mA C_{OUT} = 4.7 µF, V_{LDOOUT} = 1.2 V		160		µs
$V_{LDOOUT-SO}$	Startup overshoot	2.8 V < V_{LDOIN} < 5.5 V, 1.7 V < V_{LDOOUT} < 3.3 V I_{LDOOUT} < 10 µA		1		%
t_{SDLDO}	Shutdown duration	Pull-down enabled, V_{LDOOUT} = from 3.3 V to 0.2 V, I_{LDOOUT} = no load			1.5	ms
LDO2, LDO5, LDO6, LDO7 (bypass mode)						
$V_{LDOIN-BP}$	Main input voltage range		2.8		5.5	V
$R_{DSONLDO-BP}$	Bypass on resistance	2.8 V < V_{LDOIN} < 5.5 V			340	mΩ
$I_{LDOLIM-BP}$	Output current limitation (1)	Note: use the same range than in normal mode. Programmable value	200 400		300 600	mA
$t_{SSLDO-BP}$	Soft-start duration	2.8 V < V_{LDOIN} < 5.5 V, 0 < I_{LDOOUT} < 1 mA C_{OUT} = 4.7 µF, I_{LDOLIM} = 400 mA,		120		µs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{SDLDO-BP}$	Shutdown duration	Pull-down enabled, V_{LDOOUT} from 3.6 V to 0.2 V, I_{LDOOUT} = no load			1.5	ms

1. *If LDO is in bypass mode and 50 or 100 mA is set in the NVM, then 200 mA is used*

3.4.5 LDO8

Table 11. . Electrical and timing parameter specifications (LDO8)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
LDO8 normal mode						
V_{LDOIN}	Main input voltage range		2.8		5.5	V
V_{LDOOUT}	Output voltage	V_{LDOIN} > V_{LDOOUT} + $V_{LDODROP}$, programmable value		0.9 to 4.0		V
		Voltage programming step		100		mV
$V_{LDOOUT-ACC}$	Output voltage accuracy	V_{LDOIN} = 3.6 V or 5.0 V, 0.9 V < V_{LDOOUT} < 3.3 V 100 µA < I_{LDOOUT} < 150 mA	-2		+2	%
I_{LDOLIM}	Output current limitation	2.8 V < V_{LDOIN} < 5.5 V	150	200	350	mA
I_{LDO78Q}	Total quiescent current	I_{LDOOUT} = 0 mA Measured from the related common input pin, L_{DO78IN}		4	10	µA
$I_{LDO78IN\_LKG}$	Input leakage current	LDO output disable, Tj = +25 °C Measured from the related common input pin, L_{DO78IN}			2	
$V_{LDODROP}$	Dropout voltage	V_{LDOOUT} = 2.9 V, I_{LDOOUT} = 150 mA		160	300	mV
$V_{LDOOUT-LO}$	Load transient regulation	I_{LDOOUT} = 1 to 75 mA, t_R = t_F = 1 µs		20		
$V_{LDOOUT-LI}$	Line transient regulation	V_{LDOIN} = 3.0 V to 3.6 V, t_R = t_F = 10 µs		10		
$PSRR_{LDO}$	Power supply rejection ratio	ΔV_{LDOIN} = 300 mV_{PP}, f = [0.1:20] kHz, T_j = 25 °C, I_{LDOOUT} = 75 mA		55		dB
		ΔV_{LDOIN} = 300 mV_{PP}, f = [20:100] kHz, T_j = 25 °C, I_{LDOOUT} = 75 mA		40		
t_{SSLDO}	Soft-start duration	2.8 V < V_{LDOIN} < 5.5 V, 0 < I_{LDOOUT} < 1 mA, C_{OUT} = 4.7 µF, V_{OUT} = 1.8 V		160		µs
$V_{LDOOUT-SO}$	Startup overshoot	2.8 V < V_{LDOIN} < 5.5 V, 0.9 V < V_{LDOOUT} < 3.3 V I_{LDOOUT} < 10 µA		1		%
t_{SDLDO}	Shutdown duration	Pull-down enabled, V_{LDOOUT} = 3.3 V to V_{LDOOUT} = 0.2 V I_{LDOOUT} = no load			1.5	ms
LDO8 bypass mode						
$V_{LDOIN-BP}$	Main input voltage range		2.8		5.5	V
$R_{DSONLDO-BP}$	Bypass on resistance	V_{LDOIN} = 2.8 V to 5.5 V			600	mΩ
$I_{LDOLIM-BP}$	Output current limitation	Note: use the same value as in normal mode	150			mA
$t_{SSLDO-BP}$	Soft-start duration	2.8 V < V_{LDOIN} < 5.5 V, 0 < I_{LDOOUT} < 1 mA, C_{OUT} = 4.7 µF I_{LDOLIM} = 400 mA		120		µs
$t_{SDLDO-BP}$	Shutdown duration	Pull-down enabled, V_{LDOOUT} = 3.6 V to V_{LDOOUT} = 0.2 V I_{LDOOUT} = no load			1.5	ms

3.4.6 LDO3

Table 12. Electrical and timing parameter specifications (LDO3)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
LDO3 normal mode (general purpose or lpDDR VDD1 backup)						
V_{LDOIN}	Main input voltage range		2.8		5.5	V
V_{LDOOUT}	Output voltage	V_{LDOIN} > V_{LDOOUT} + $V_{LDODROP}$ programmable value.		0.9 to 4.0		V
		Voltage programming step		100		mV
$V_{LDOOUT-ACC}$	Output voltage accuracy	V_{LDOIN} = 2.8 V or 5.0 V, 1.7 V < V_{LDOOUT} < 3.3 V 100 µA < I_{LDOOUT} < 120 mA	-2		+2	%
I_{LDOLIM}	Output current limitation	2.8 V < V_{LDOIN} < 5.5 V	120		180	mA
I_{LDOQ}	Total quiescent current	I_{LDOOUT} = 0 mA measured from LDO3IN pin		4	20	µA
I_{LDOIN_LKG}	Input leakage current	LDO output disabled, Tj=25 °C		1	3	
$V_{LDODROP}$	Dropout voltage	V_{LDOOUT} = 2.9 V, I_{LDOOUT} = 100 mA		120	200	mV
$V_{LDOOUT-LO}$	Load transient regulation	I_{LDOOUT} = 100 µA to 50 mA, t_R = t_F = 1 µs		20		
$V_{LDOOUT-LI}$	Line transient regulation	V_{LDOIN} = 3.0 V to 3.6 V, t_R = t_F = 10 µs		5		
$PSRR_{LDO}$	Power supply rejection ratio	ΔV_{LDOIN} = 300 mV_{PP}, f = [0.1:20] kHz, Tj = 25 °C, I_{LDOOUT} = 50 mA		45		dB
		ΔV_{LDOIN} = 300 mV_{PP}, f = [20:100] kHz, Tj = 25 °C, I_{LDOOUT} = 50 mA		40		
t_{SSLDO}	Soft-start duration	2.8 V < V_{LDOIN} < 5.5 V, 0 < I_{LDOOUT} < 1 mA C_{OUT} = 4.7 µF, V_{OUT} = 1.8 V		160		µs
$V_{LDOOUT-SO}$	Startup overshoot	2.8 V < V_{LDOIN} < 5.5 V, 1.7 V < V_{LDOOUT} < 3.3 V I_{LDOOUT} < 10 µA		1		%
t_{SDLDO}	Shutdown duration	Pull-down enabled, V_{LDOOUT} = 3.3 V to V_{LDOOUT} = 0.2 V, I_{LDOOUT} = no load			1.5	ms
LDO3 sink-source mode (DDR VTT supply)						
V_{LDOIN} = V_{OUT6} = 1.2 V, V_{IN} = 5.0 V, $V_{BUCK6IN}$ = 5.0 V, V_{LDOOUT} = V_{REFDDR} = $V_{OUT6/2}$, Tj = -40 °C to +125 °C, recommended BOM, unless otherwise specified						
$V_{LDOIN-SS}$	Input voltage range		1.1	1.2	1.6	V
$V_{LDOOUT-SS}$	Output voltage			VREFDDR		
$V_{LDOOUT-ACC-SS}$	Output voltage accuracy	1.1 V < V_{LDOIN} < 1.6 V, -215 mA < I_{LDOOUT} < +215 mA	-1.5		+1.5	%
$I_{LDOOUT-SS}$	Continuous output current	1.1 V < V_{LDOIN} < 1.6 V			120	mA_{RMS}
$I_{LDOLIM-SS}$	Output current limitation	V_{LDOIN} = 2.8 V to 5.5 V	±230		±500	mA
$I_{LDOQ-SS}$	Total quiescent current	I_{LDOOUT} = 0 mA measured from LDO3IN pin		4	20	µA
$V_{LDOOUT-LO-SS}$	Load transient regulation	I_{LDOOUT} = ± [0:50] mA, t_R = t_F = 250 ns		30		mV
$V_{LDOOUT-LI-SS}$	Line transient regulation	V_{LDOIN} = V_{OUT6} = 1.2 V ±30 mV, t_R = t_F = 10 µs		5		
$t_{SSLDO-SS}$	Soft-start duration	1.1 V < V_{LDOIN} < 1.6 V, $\|I_{LDOOUT}\|$ < 1 mA, C_{OUT} = 10 µF		20	40	µs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{LDOOUT-SO-SS}$	Startup overshoot	1.1 V < V_{LDOIN} < 1.6 V, V_{LDOOUT} = VREFDDR, I_{LDOOUT} = 10 µA			4	%
$t_{SDLDO-SS}$	Shutdown duration	Pull-down enabled, V_{LDOOUT} = VREFDDR to V_{LDOOUT} = 0.2 V, I_{LDOOUT} = no load			1.5	ms
LDO3 bypass mode (IpDDR V_{DD1} supply)						
V_{LDOIN} = 1.8 V, V_{LDOOUT} = ~1.8 V, Tj = -40 °C to +125 °C, recommended BOM, unless otherwise specified						
$V_{LDOIN-BP}$	Input voltage range		1.7		2	V
$I_{LDOOUT-BP}$	Continuous output current	1.7 V < V_{LDOIN} < 2 V (no overcurrent protection in bypass mode TBV)	80			mA
$R_{DSONLDO-BP}$	Bypass on resistance	1.7 V < V_{LDOIN} < 2 V, I_{LDOOUT} = 40 mA			360	mΩ
$t_{SSLDO-BP}$	Soft-start duration	1.7 V < V_{LDOIN} < 2 V, 0 < I_{LDOOUT} < 1 mA C_{OUT} = 4.7 µF,		100		µs
$t_{SDLDO-BP}$	Shutdown duration	Pull-down enabled, V_{LDOOUT} = 1.8 V to V_{LDOOUT} = 0.2 V, I_{LDOOUT} = no load			1.5	ms

3.4.7 LDO4

Table 13. Electrical and timing parameter specifications (LDO4)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
LDO4						
V_{LDOIN}	Main input voltage range	V_{LDOIN} from V_{IN} or V_{BUS} pins	2.8		5.5	V
$V_{LDOOUT-ACC}$	Output voltage accuracy	V_{LDOIN} = 3.6 V to 5.0 V, 100 µA < I_{LDOOUT} < 30 mA	3.23	3.3	3.40	V
I_{LDOLIM}	Output current limitation	V_{LDOIN} = 3.6 V to 5.5 V	40		80	mA
I_{LDOQ}	Quiescent current	I_{LDOOUT} = 0 mA		20	25	µA
$V_{LDODROP}$	Dropout voltage from VIN pin	I_{LDOOUT} = 30 mA		45	90	mV
$V_{LDOOUT-LO}$	Load transient regulation	I_{LDOOUT} = 1 to 30 mA, t_R = t_F = 1 µs		40		mV
$V_{LDOOUT-LI}$	Line transient regulation	V_{IN} = 3.6 V, V_{BUS} = from 0 V to 5 V (internal mux), I_{LDOOUT} = 10 mA		10		mV
$PSRR_{LDO}$	Power supply rejection ratio	ΔV_{LDOIN} = 300 mV_{PP}, f = [0.1:20] kHz, T_j = 25 °C, I_{LDOOUT} = 25 mA		55		dB
		ΔV_{LDOIN} = 300 mV_{PP}, f = [20:100] kHz, T_j = 25 °C, I_{LDOOUT} = 25 mA		40		dB
t_{SSLDO}	Soft-start duration	3.6 V < V_{LDOIN} < 5.5 V, 0 < I_{LDOOUT} < 1 mA, C_{OUT} = 4.7 µF		100		µs
$V_{LDOOUT-SO}$	Startup overshoot	3.6 V < V_{LDOIN} < 5.5 V, I_{LDOOUT} < 10 µA		1		%
t_{SDLDO}	Shutdown duration	Pull-down enabled, V_{LDOOUT} = 3.3 V to V_{LDOOUT} = 0.2 V, I_{LDOOUT} = no load			1.5	ms

3.4.8 REFDDR (DDR_VREF)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
REFDDR (sink-source)						
V_{REFOUT}	Output voltage			$V_{OUT6}/2$		V
$V_{VREF-ACC}$	Output voltage accuracy	1.1 V < V_{OUT6} < 1.5 V, 100 μA_{rms} < I_{LDOOUT} < 5 mA_{rms}	-1		+1	%
I_{REFOUT}	Continuous output current		5			mA_{RMS}
I_{REFLIM}	Output current limitation		±10	±25	±50	mA
I_{REFQ}	Quiescent current	I_{REFOUT} = 0 mA		25	35	µA
t_{SSREF}	Soft-start duration	0 < I_{REFOUT} < 1 mA		100		µs
t_{SDREF}	Shutdown duration	Pull-down enabled, V_{REFOUT} = 0.6 V to V_{REFOUT}= 0.2 V, I_{LDOOUT} = no load			1.5	ms

3.4.9 BUCK1, BUCK6

Table 14. Electrical and timing parameter specifications (BUCK1, BUCK6)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BUCK1, BUCK6						
V_{BUCKIN}	Main input voltage range		2.8		5.5	V
V_{OUT}	Output voltage	Programmable value		0.5 to 1.5		V
		Voltage programming step		10		mV
$V_{OUT-ACC}$	Output voltage error amplifier accuracy	BUCK1 HP mode 0.5 V < V_{OUT} < 1.5 V	-1.5		+1.5	%
		BUCK6 HP mode 0.5 V < VOUT6 < 1.5 V	-1.5		+1.5	
		BUCK1, BUCK6 LP mode 0 < I_{OUT} < 50 mA	-4		+4	
		BUCK6 LP mode VOUT6 = 1.1 V 0 < I_{OUT} < 50 mA	-3		+3	
$V_{OUT-REG}$	Output load regulation (4)	BUCK1, BUCK6 HP mode, CCM mode 1 mA < I_{OUT} < 1.5 A	-1		+1	
$V_{OUT-RIPP}$	Output voltage ripple (2)	HP mode 3.0 V < V_{BUCKIN} < 5.5 V, 5 mA < I_{OUT} < 1500 mA 0.7 V < V_{OUTBK1} < 1.0 V 1.0 V < V_{OUTBK6} < 1.35 V		10		mV_{PP}

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{OUT-RIPP}$	Output voltage ripple (2)	HP mode, I_{OUT} = 750 mA		3		mV_{PP}
		LP mode, 0.5 mA < IOUTBK6 < 50 mA 3.0 V < VBUCKIN < 4.2 V VOUT6 = 1.110 V		10 (2)		
$I_{OUT\_LP\_PEAK}$	Peak output current in LP mode	2.8 V < V_{BUCKIN} < 5.5 V, tPEAK < 1 ms	200			mA
I_{BCKLIM}	Inductor peak current limit (with typical BoM list)	Programmable value in NVM_BUCKS_IOUT_SHR Ref. Section 1: Device configuration table NVM setting A and B version Max output current steps (0.5 A, 1 A, 1.5 A, 2 A) can be defined based on the selected inductor peak current limit level		1.5 2.1 2.8 3.3		A
I_{OUT}	Max output current (4)	HP mode, 2.8 V < V_{BUCKIN} < 5.5 V Programmable value in NVM_BUCKS_IOUT_SHR	500 1000 1500 2000			mA
f_{REFCLK}	Reference switching frequency	CCM mode		2		MHz
I_{Q_BCK}	Total quiescent current	I_{OUT} = 0 mA, HP mode		115	300	µA
		I_{OUT} = 0 mA, LP mode		30	80	
I_{BUCKIN_LKG}	Input leakage current	BUCK OFF, Tj = 25 °C		1	1.5	
EFF_{BCK}	Efficiency	V_{BUCKIN} = 5 V, V_{OUT} = 0.9 V, HP mode				%
		I_{OUT} = 10 mA		78		
		I_{OUT} = 100 mA		80		
		I_{OUT} = 300 mA (best efficiency load)		80		
		I_{OUT} = 1000 mA		79		
		I_{OUT} = 1500 mA		76		
V_{OUT-LO}	Load transient regulation (4)	HP mode 3.0 V < VBUCKIN < 5.5 V 5 mA < I_{OUT}< 1.5 A ΔI_{OUT} = 560 mA, t_R = t_F ~500 ns			30	mV
		LP mode, 0 < I_{OUT} < 50 mA ΔI_{OUT} = 50 mA, t_R = t_F ~500 ns			30	
		LP mode, 3.0 V < VBUCKIN < 5.5 V, V_{OUTBK6} = 1.110 V ΔI_{OUT} = 10 mA, t_R = t_F ~500 ns			15	
V_{OUT-LI}	Line transient regulation	ΔVBKIN = 600 mV, ΔI_{OUT} = 500 mA tR = tF~10 µs, HP mode		2		
$V_{OUT-OVR}$	Power-up overshoot	2.8 V < VBKIN < 5.5 V, I_{OUT}~1 mA TA = +25 °C, 0.5 V < V_{OUT} < 1.5 V		5		
$t_{LP-HP-BCK}$	Recovery time from LP to HP mode	V_{OUT_LP} = V_{OUT_HP}			60(4)	µs
t_{SU_BCK}	Startup delay (delay before voltage starts to rise)	Delay time from PWRCTRL signal (PWRCTRL_DLY = 0)		25 (3)	40. (4)	µs
t_{SS_BCK}	Soft-start duration			235	400	µs
SR_{BCK}	Output voltage slew rate	Slew rate during startup	3.7	6.3		mV/µs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
SR_{BCK}	Output voltage slew rate	DVS slew rate of a voltage programmed change low to high or high to low, from V_{OUT} = 0.5 V to 1.5 V	1	3.1		mV/µs
t_{SD_BCK}	Shutdown duration	From V_{OUT} =1.5 V to V_{OUT} < 0.2 V, 2.8 V < VBUCKIN < 5.5 V, I_{OUT} < 1 mA slow PD			1.5	ms
		From V_{OUT} = 1.5 V to V_{OUT} < 0.2 V, 2.8 V < VBUCKIN < 5.5 V, I_{OUT} < 1 mA Fast PD	1		0.3	

1. *Guaranteed by design - not tested in production. Load transient performances are strongly impacted by the external passive component characteristics. The load transient is also influenced by the parasitic elements of the PCB layout. For more info see the forthcomingAN.*
2. *Output ripple voltage is the result of the inductor ripple current flowing through the output capacitor and depends on the capacitance value, ESR, and ESL. The actual output ripple voltage is also influenced by the parasitic elements of the PCB layout.*
3. *See 1: startup sequence*
4. *Guaranteed by design - not tested in production*

3.4.10 BUCK2, BUCK3

Table 15. Electrical and timing parameter specifications (BUCK2, BUCK3)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BUCK2, BUCK3						
V_{BUCKIN}	Main input voltage range		2.8		5.5	V
V_{OUT}	Output voltage	Programmable value		0.5 to 1.5		V
		Voltage programming step		10		mV
$V_{OUT-ACC}$	Output voltage open loop accuracy	HP mode 0.5 V < V_{OUT} < 1.5 V	-1.5		+1.5	%
		LP mode	-4		+4	
$V_{OUT-REG}$	Output load regulation (4)	HP mode, CCM mode 1 mA < I_{OUT} < 1.5 A	-1		+1	
$V_{OUT-RIPP}$	Output voltage ripple (2)	HP mode 3.0 V < VBUCKIN < 5.5 V 0.7 V < V_{OUT} < 1.0 V 5 mA < I_{OUT} < 2000 mA		10		mV_{PP}
		HP mode, I_{OUT} = 1000 mA		3	20	
		LP mode, 3.0 V < VBUCKIN < 5.5 V 0.6 V < V_{OUT} < 0.9 V 1 mA < I_{OUT} < 50 mA		10		
$I_{OUT\_LP\_PEAK}$	Peak output current in LP mode	2.8 V < VBUCKIN < 5.5 V, t_{PEAK} up to 1 ms	200			mA
I_{BCKLIM}	Inductor peak current limit (with typical BoM list)	Programmable value in NVM_BUCKS_IOUT_SHR Ref. Section 1 NVM setting A and B version. Max output current steps (0.5 A, 1 A, 1.5 A, 2 A) can be defined based on the selected inductor peak current limit level		1.5 2.1 2.8 3.3		A
I_{OUT}	Max output current (4)	Hp mode, 2.8 V < 5.5 V Programmable value in NVM_BUCKS_IOUT_SHR	500 1000 1500 2000			mA
f_{REFCLK}	Reference switching frequency	CCM mode		2		MHz
I_{Q_BCK}	Total quiescent current	I_{OUT} = 0 mA, HP mode		115	300	µA
		I_{OUT} = 0 mA, LP mode		30	80	
I_{BUCKIN_LKG}	Input leakage current	BUCK output disabled, T_j = 25 °C		0.01	1	
EFF_{BCK}	Efficiency	V_{BUCKIN} = 5 V, Vout = 0.9 V, HP mode I_{OUT} = 10 mA I_{OUT} = 100 mA I_{OUT} = 400 mA I_{OUT} = 1000 mA I_{OUT} = 2000 mA		 78 80 81 80 73		%

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OUT-LO}	Load transient regulation(4)	HP mode, 3.0 V < VBUCKIN < 5.5 V, 5 mA < I_{OUT} < 2 A ΔI_{OUT} = 1300 mA, t_F = 500 ns			35	mV
		HP mode 3.0 V < VBUCKIN < 5.5 V, 5 mA < I_{OUT} < 2 A, ΔI_{OUT} = 1300 mA, t_R = 500 ns.	-34			
		LP mode, 0 < I_{OUT} < 50 mA, ΔI_{OUT} = 50 mA, tR = tF = 500 ns			30	
V_{OUT-LI}	Line transient regulation	ΔVBUCKIN = 600 mV, I_{OUT} = 500 mA, tR = tF = 10 µs, HP mode		2		
$V_{OUT-OVR}$	Power-up overshoot	2.8 V < VBUCKIN < 5.5 V, I_{OUT} = 1 mA, TA = 25 °C		5		
$t_{LP-HP-BCK}$	Recovery time from LP to HP mode	V_{OUT_LP} = V_{OUT_HP}			60 (4)	µs
t_{SU_BCK}	Startup delay (delay before voltage starts to rise)	Delay time from PWRCTRL signal (PWRCTRL_DLY = 0)		25 (3)	40 (4)	
t_{SS_BCK}	Soft-start duration	2.8 V < VBUCKIN < 5.5 V, 1 mA < I_{OUT} < 100 mA, V_{OUT}- = 1.5 V		235	400	
SR_{BCK}	Output voltage slew rate	Slew rate during startup	3.7	6.3		mV/µs
		DVS slew rate of a voltage programmed change low to high or high to low, from V_{OUT} = 0.5 V to 1.5 V	1	3.1		
t_{SD_BCK}	Shutdown duration	From V_{OUT} = 1.5 V to V_{OUT} < 0.2 V, 2.8 V < VBUCKIN < 5.5 V, I_{OUT}< 1 mA, slow PD			1.5	ms
		From V_{OUT}=1.5 V to V_{OUT} <0.2 V, 2.8 V < VBUCKIN < 5.5 V, I_{OUT} < 1 mA, fast PD			0.3	

1. *Guaranteed by design - not tested in production. Load transient performances are strongly impacted by the external passive component characteristics. The load transient is also influenced by the parasitic elements of the PCB layout. For more info see the forthcoming AN.*
2. *The output ripple voltage is the result of the inductor ripple current flowing through the output capacitor and depends on the capacitance value, ESR, and ESL. The actual output ripple voltage is also influenced by the parasitic elements of the PCB layout.*
3. *See 1: startup sequence.*
4. *Guaranteed by design - not tested in production.*

3.4.11 BUCK4, BUCK5

Table 16. Electrical and timing parameter specifications (BUCK4, BUCK5)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BUCK4, BUCK5						
V_{BUCKIN}	Main input voltage range		2.8		5.5	V
V_{OUT}	Output voltage	V_{BUCKIN} > Vout + 0.8 V, V_{BUCKIN} > 2.8 V Programmable value		1.5 to 4.2		
		Voltage programming step		100		mV
$V_{OUT-ACC}$	Output voltage open loop accuracy	HP mode 1.5 V < V_{OUT} < 3.3 V	-1.5		+1.5	%
		LP mode	-4		+4	
$V_{OUT-REG}$	Output load regulation (1)	HP mode, CCM mode 1 mA < I_{OUT} < 0.5 A	-1		+1	%
$V_{OUT-RIPP}$	Output voltage ripple (2)	HP mode, 3.0 V < V_{BUCKIN} < 5.5 V, 1.5 V < V_{OUT} < 3.3 V		10		mV_{PP}

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{OUT-RIPP}$	Output voltage ripple (2)	5 mA < I_{OUT} < 500 mA				mV_{PP}
		HP mode, I_{OUT} = 500 mA		3		
		Forced PWM mode ON, HP mode, I_{OUT} = 250 mA		1		
		LP mode, I_{OUT} = 50 mA		20		
$I_{OUT\_LP\_PEAK}$	Peak output current in LP mode	2.8 V < V_{BUCKIN} < 5.5 V, t_{PEAK} up to 1 ms	200			mA
I_{OUT}	Max output current (3)	Hp mode, 2.8 V < 5.5 V Programmable value in NVM_BUCKS_IOUT_SHR	250 500			mA
I_{BCKLIM}	Inductor peak current limit (with typical BoM list)	Programmable value in NVM_BUCKS_IOUT_SHR Ref. Section 1: Device configuration table NVM setting A and B version Max output current steps (0.25 A, 0.5 A) can be defined based on the selected inductor peak current limit level		1.1 1.5		A
f_{REFCLK}	Reference switching frequency	CCM mode		2		MHz
I_{Q_BCK}	Total quiescent current	I_{OUT} = 0 mA, HP mode		130	300	µA
		I_{OUT} = 0 mA, LP mode		40	80	
I_{BUCKIN_LKG}	Input leakage current	B_{UCK} output disabled, Tj = 25 °C		0.01	1.5	
EFF_{BCK}	Efficiency	V_{BUCKIN} = 5 V, V_{OUT} = 1.8 V HP mode, Tj = 50 °C, LP mode, I_{OUT} = 0.1 mA LP mode, I_{OUT} = 1 mA I_{OUT} = 10 mA I_{OUT} = 100 mA I_{OUT} = 500 mA		40 78 85 87 88		%
V_{OUT-LO}	Load transient regulation (1)	HP mode; 3.0 V < V_{BUCKIN} < 5.5 V, ΔV (in-out) > 1.5 V, 5 mA < I_{OUT} < 500 mA, ΔI_{OUT} = 100 mA, tR = tF = 1 µs, forced PWM mode ON			15	mV
		HP mode, 3.0 V < V_{BUCKIN} < 5.5 V ΔV (in-out) > 1.5 V, 5 mA < I_{OUT} < 500 mA, ΔI_{OUT} = 100 mA t_R = t_F = 1µs, forced PWM mode OFF			20	
		LP mode, 0 < I_{OUT} <5 0 mA, ΔI_{OUT} = 50 mA, t_R = t_F = 1 µs			30	
V_{OUT-LI}	Line transient regulation	ΔV_{BUCKIN} = 600 mV, ΔI_{OUT} = 0, t_R = t_F =10 µs ΔV (in-out) > 1.5 V, 1.8 V < V_{OUT} < 3.3 V, HP mode		1.5		
$V_{OUT-OVR}$	Power-up overshoot	2.8 V < V_{BUCKIN} < 5.5 V, I_{OUT} = 1 mA, T_A = 25 °C, 1.5 V < V_{OUT} < 4.2 V		5		
$t_{LP-HP-BCK}$	Recovery time from LP to HP mode	V_{OUT_LP} = V_{OUT_HP}			40(3)	µs
t_{SU_BCK}	Startup delay (delay before voltage starts to rise)	Delay time from PWRCTRL signal (PWRCTRL_DLY = 0)		25 (4)	40 (3)	µs
t_{SS_BCK}	Soft-start duration	2.8 V < V_{BUCKIN} < 5.5 V, 1 mA < I_{OUT} < 100 mA, V_{OUT} = 4.2 V		235	400	µs
SR_{BCK}	Output voltage slew rate	Slew rate during startup	10.3	17.5		mV/µs
		DVS slew rate of a voltage programmed change low to high or high to low, from V_{OUT} = 1.5 V to 4.2 V	2	3.1		

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{SD_BCK}	Shutdown duration	From V_{OUT} = 3.3 V to V_{OUT} < 0.2 V, 2.8 V < V_{BUCKIN} < 5.5 V, I_{OUT} < 1 mA, slow PD			1.5	ms
		From V_{OUT} = 3.3 V to V_{OUT} < 0.2 V, 2.8 V < V_{BUCKIN} < 5.5 V, I_{OUT} < 1 mA, fast PD			0.3	

1. *Guaranteed by design - not tested in production. Load transient performances are strongly impacted by the external passive components characteristics. The load transient is also influenced by the parasitic elements of the PCB layout. For more info see the forthcoming AN.*
2. *See 1: startup sequence.*
3. *Guaranteed by design - not tested in production.*
4. *See 1: startup sequence.*

3.4.12 BUCK7

Table 17. Electrical and timing parameter specifications (BUCK7)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BUCK7						
V_{BUCKIN}	Main input voltage range		2.8		5.5	V
V_{OUT}	Output voltage	V_{BUCKIN} > Vout 0.8 V, V_{BUCKIN} > 2.8 V programmable value		1.5 to 4.2		
		Voltage programming step		100		mV
$V_{OUT-ACC}$	Output voltage open loop accuracy	HP mode 1.5 V < V_{OUT} < 4.2 V	-1.5		+1.5	%
		LP mode, 0 < I_{OUT} < 50 mA	-4		+4	
$V_{OUT-REG}$	Output load regulation (1)	HP mode, CCM mode 1 mA < I_{OUT} < 2.5 A	-1		+1	
$V_{OUT-RIPP}$	Output voltage ripple (3)	HP mode, 2.8 V < V_{BUCKIN}< 5.5 V, 5 mA < I_{OUT} < 2500 mA		15 (2)		mV_{PP}
		LP mode, 3.0 V < V_{BUCKIN} < 5.5 V, 1.5 V < V_{OUT} < 4.2 V 1 mA < I_{OUT} < 50 mA		20 (2)		
$I_{OUT\_LP\_PEAK}$	Peak output current in LP mode	2.8 V < V_{BUCKIN} < 5.5 V, t_{PEAK} up to 1 ms	200			mA
I_{BKLIM}	Inductor peak current limit (with typical BoM list)	Programmable value in NVM_BUCKS_IOUT_SHR Ref. Section 1 NVM setting A and B version Max output current steps (1 A, 1.5 A, 2 A, 2.5 A) can be defined based on the selected inductor peak current limit level		2.1 2.6 3.1 3.6		A
I_{OUT}	Max output current (4)	Hp mode, 2.8 V < 5.5 V Programmable value in NVM_BUCKS_IOUT_SHR	1000 1500 2000 2500			mA
f_{REFCLK}	Reference switching frequency	CCM mode		2		MHz
I_{Q_BCK}	Total quiescent current	I_{OUT} = 0 mA, HP mode		115	300	µA
		I_{OUT} = 0 mA, LP mode		30	80	
I_{BUCKIN_LKG}	Input leakage current	BUCK output disabled, T_j = 25 °C		0.01	1	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
EFF_{BCK}	Efficiency	V_{BUCKIN} = 5 V, V_{OUT} = 3.3 V, HP mode, T_j = 50 °C I_{OUT} = 10 mA I_{OUT} = 100 mA I_{OUT} = 600 mA I_{OUT} = 2500 mA		 90 92 93 85		%
V_{OUT-LO}	Load transient regulation (1)	HP mode, 5 mA < I_{OUT} < 2500 mA, ΔI_{OUT} = 1000 mA, t_R = t_F = 1µs, 3.0 V < V_{BUCKIN} < 5.5 V, ΔV (in-out) > 1.5 V			35	mV
		LP mode, 0 < I_{OUT} < 50 mA, ΔI_{OUT} = 50 mA, t_R = t_F = 1 µs			30	
V_{OUT-LI}	Line transient regulation	ΔV_{BUCKIN} = 600 mV, ΔI_{OUT} = 0, t_R = t_F = 10 µs, ΔV (in-out) > 1.5 V 1.8 V < V_{OUT} < 3.3 V, HP mode		2		
$V_{OUT-OVR}$	Power-up overshoot	2.8 V < V_{BUCKIN} < 5.5 V, I_{OUT} = 1 mA, T_A = 25 °C 1.5 V < V_{OUT}< 4.2 V		5		
$t_{LP-HP-BCK}$	Recovery time from LP to HP mode	V_{OUT_LP} = V_{OUT_HP}			60 (4)	µs
t_{SU_BCK}	Startup delay (delay before voltage starts to rise)	Delay time from PWRCTRL signal (PWRCTRL_DLY =0)		25 (3)	40 (4)	µs
t_{SS_BCK}	Soft-start duration	2.8 V < V_{BUCKIN}<5.5 V 1 mA < I_{OUT} <100 mA V_{OUT}=4.2 V		235	400	µs
SR_{BCK}	Output voltage slew rate	Slew rate during startup	10.3	17.5		mV/µs
		DVS slew rate of a voltage programmed change low to high or high to low, from V_{OUT} = 1.5 V to 4.2 V	2	3.1		
t_{SD_BCK}	Shutdown duration	From V_{OUT} = 3.3 V to V_{OUT} < 0.2 V, 2.8 V < V_{BUCKIN} < 5.5 V, I_{OUT} < 1 mA slow PD			1.5	ms
		From V_{OUT} = 3.3 V to V_{OUT} < 0.2 V, 2.8 V < V_{BUCKIN} < 5.5 V, I_{OUT} < 1 mA fast PD			0.3	

1. *Guaranteed by design - not tested in production. Load transient performances are strongly impacted by the external passive components characteristics. The load transient is also influenced by the parasitic elements of the PCB layout. For more info see the forthcoming AN.*
2. *The output ripple voltage is the result of the inductor ripple current flowing through the output capacitor and depends on the capacitance value, ESR, and ESL. The actual output ripple voltage is also influenced by the parasitic elements of the PCB layout.*
3. *See 1: startup sequence.*
4. *Guaranteed by design - not tested in production.*

4 Power regulator descriptions

4.1 Overview

The STPMIC25 has a large input voltage range from 2.8 V to 5.5 V to supply applications typically from a 5 V DC wall-adaptor or from a 1-cell 3.6 V Li-Ion/Li-PO battery.

The STPMIC25 provides all the regulators needed to power supply a complete application:

- 8 LDOs + 1 reference voltage LDO for DDR memories
- 7 step-down (buck) converters

Table 18. General description

Regulator	Output voltage (V)	Programming step (mV)	Rated output current (mA)	Application use
LDO1	1.8	-	20	VDDA18AON
LDO2, LDO5, LDO6, LDO7	0.9 V to 4.0 V bypass mode	100	400/200/100/50	General purpose (eMMC, DDR4 VPP, SD card, LCD camera)
LDO8	0.9 V to 4.0 V bypass mode	100	150	General purpose (low voltage peripheral)
LDO3 normal mode	0.9 V to 4.0 V	100	120	General purpose/lpDDR VDD1
LDO3 sink-source mode	V_{REFDDR}	-	+/-120 (rms) +/-230 (peak)	DDR3L/DDR4 terminations (VTT)
LDO3 bypass mode	V_{INLDO3}	-	80	lpDDR VDD1
LDO4	3.3	-	40	VDD33USB VDD33UCPD
V_{REFDDR}	V_{OUT6} / 2	-	+/-5 (rms) +/-10 (peak)	Reference voltage for DDR memories
B_{UCK1}, B_{UCK6}	0.5 V to 1.5 V	10	2000, 1500, 1000, 500	Buck1 = VDDCPU Buck6 = VDDQ (DDR3L, DDR4, lpDDR3, lpDDR4)
B_{UCK2}, B_{UCK3}	0.5 V to 1.5 V	10	2000, 1500, 1000, 500	Buck2 = VDDCORE Buck3 = VDDGPU
BUCK4, BUCK5	1.5 V to 4.2 V	100	500, 250	Buck4 = VDD (VDDIO) Buck5 = VDDA18x
BUCK7	1.5 V to 4.2 V	100	2500, 2000, 1500, 1000	General purpose

Note: V_{IN} is the main STPMIC25 supply. All buck converters and linear regulators have dedicated or shared power supply pins. The dedicated V_{IO} supply is for all digital interface pins.

Except forV_{BUS}, no other supply voltages must be applied before V_{IN} or set higher than V_{IN}.

4.2 LDO regulators

LDO1 is a fixed 1.8 V low drop linear regulator designed to be typically used to supply the VDDA18AON MPU application domain that needs to be powered.

LDO2, LDO5, LDO6, LDO7, and LDO8 are general purpose LDOs suitable to supply MPU application peripherals. All these LDOs are provided with a bypass mode function.

LDO3 serves for DDR3, DDR3L, DDR4 memory termination (sink-source mode) or to support the general purpose mode or bypass mode, which is typically suitable for supplying lpDDR's 1.8 V power domain.

LDO4 is a fixed 3.3 V regulator designed to supply a 3V3 USB PHY circuit. It has two voltage sources (V_{IN} or V_{BUS}) which allows the LDO4 output voltage to stay at 3.3 V when V_{IN} is powered by a discharged battery < 3.3 V and V_{BUS} powered by 5 V.

V_{REFDDR} is a sink-source reference voltage dedicated for lpDDR/DDR.

4.2.1 Common features

Enable/disable - each LDO can be enabled or disabled independently:

- Automatically during the POWER_UP or POWER_DOWN sequence depending on the NVM settings.
- By software (I^2C access): setting the EN bit in the related LDO control register.
- By PWRCTRLx pins state change: the PWRCTRLx pins need to be programmed by I^2C to enable this feature.

V_{LDOOUT} voltage setting - LDO output voltage can be set:

- Automatically during the POWER_UP or POWER_DOWN sequence depending on the NVM settings.
- By software (I^2C access): setting the VOUT bit field in the related LDO control register.
- By PWRCTRLx pins state change: the PWRCTRLx pins need to be programmed by I^2C to select the output voltages needed to meet the MPU application requirements.

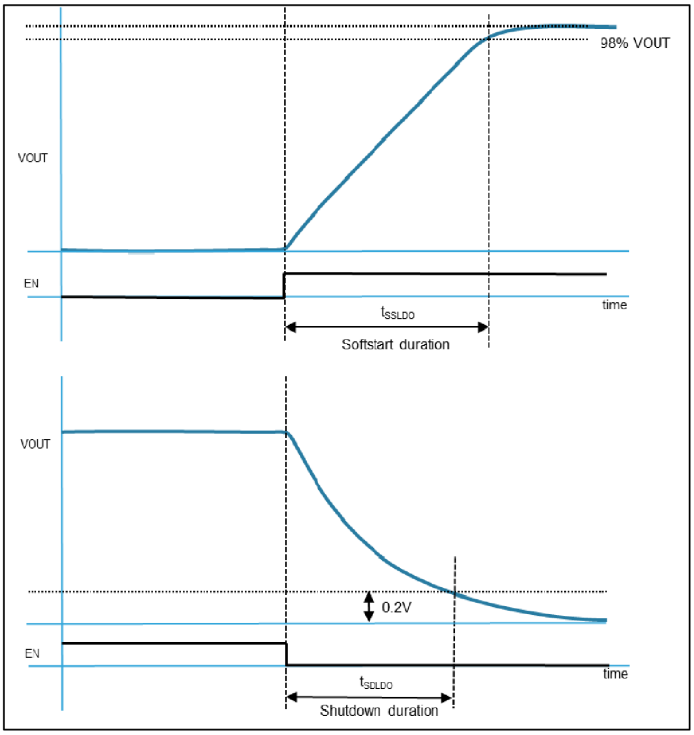
Bypass mode operation - this mode is set by the BYPASS bit in the related LDO control register:

When in bypass mode, the LDO operates as a power switch allowing voltage to bypass from the V_{LDOIN} to the V_{LDOOUT} of a corresponding LDO. The LDO can be enabled or disabled as in normal operation. See the “**Enable/disable**” description above.

Soft-start: this feature aims to limit input inrush current during the LDO startup phase. LDO soft-start duration is defined by the t_{SSLDO} parameter.

See Figure 3

Figure 3. **LDO startup/shutdown timings**



Output discharge: When LDO is disabled, a pull-down discharge is automatically enabled. It allows the LDO output voltage to discharge within a t_{SDLDO} time delay. The LDO output is low before disabling the next regulators in the next ranking slot. It is active by default. It can be disabled by software to put the LDO output in high impedance when LDO is disabled (LDOS_PD_CR1 and LDOS_PD_CR2 registers).

OCP and Hiccup management: Each LDO supports OCP and can operate in Hiccup mode. When the output load of the LDO exceeds the I_{LDOLIM} overcurrent limit threshold, the LDO starts decreasing the output voltage, limiting the output current to I_{LDOLIM}. If the overcurrent lasts more than t_{OCPDB_LDO}:

- An interrupt is generated (if the interrupt has been unmasked by software)
- Hiccup mode (default behavior): the LDO is turned OFF for the t_{HICCUP_DLY} duration and then turned ON again
- Fail safe mode (alternative behavior): the PMIC is turned OFF for the tHICCUP_DLY duration and then turned ON again (or goes into FAIL_SAFE_LOCK state)

See Section 5.4.9 for details on OCP & Hiccup management.

LDO2, LDO5, LDO6, and LDO7 have programmable I_{LDOLIM} overcurrent limit thresholds. I_{LDOLIM} thresholds are programmed in the NVM_LDOS_IOUT_SHR NVM register.

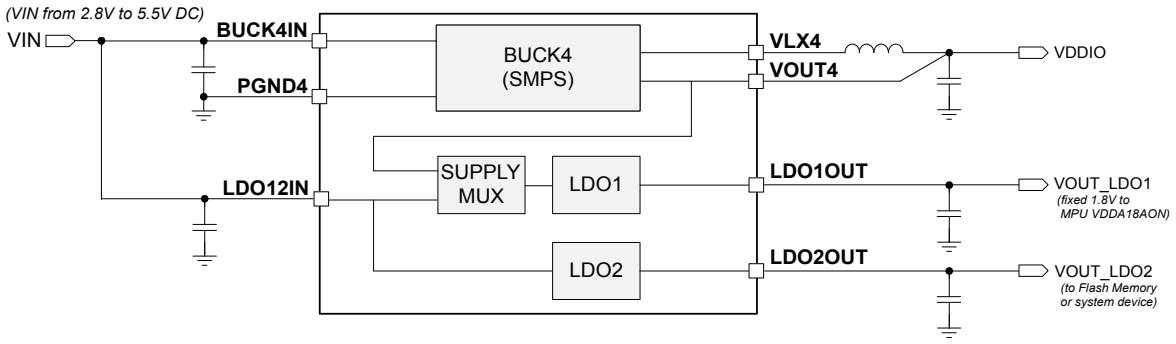
For LDO2, LDO5, LDO6, LDO7, and LDO8, the OCP is also supported when the LDO works in bypass mode operation.

4.2.2 LDO1's special features

LDO1 is usually dedicated to supply the MPU's VDDA18AON power, always ON domain having very low power consumption. The LDO1 and BUCK4 are the first rails enabled in the power ON sequence. Thus, the LDO1 can be powered from V_{IN} and cannot be pre-regulated from a buck converter, as all buck converters must be enabled after LDO1 (due to the VDDA18AON domain constraint). LDO1 has a very low quiescent current to reduce power consumption during STANDBY mode.

LDO1 has two power sources: L_{DO12IN} and V_{OUT4} (see Figure 4). By default, at reset, the LDO1 input is always L_{DO12IN}. When the application is powered ON, the software switches the LDO1 input from L_{DO12IN} to V_{OUT4} allowing LDO1's power efficiency to improve.

Figure 4. **LDO1 input supply mux**



4.2.3 LDO3's special features

The LDO3 is a multipurpose LDO with three operating modes:

- **Normal mode** – LDO3 works as general purpose LDO as well as LDO2, 5, 6, 7, and 8.
- **Bypass mode** – LDO3 operates as a power switch as well as LDO2, 5, 6, 7, and 8.
- **Sink-source mode** – LDO3 can regulate the output voltage working in sink source mode. This mode is dedicated to supply the termination of DDR3/DDR3L or DDR4 IC memories with fixed output voltage. If LDO3 is used in this mode, LDO3IN must be powered from the output of BUCK6 (See Figure 6). The output voltage is fixed and follows $V_{OUT6}/2$ even during the BUCK6 ramp-up and ramp-down phases. The overcurrent limitation works both during sink and source output current modes.

4.2.4 LDO4's special features

LDO4 has two power sources: V_{IN} and V_{BUS} (see Figure 1). The selection among these two power inputs is automatic. In other words, no user intervention is needed. The internal circuit continuously monitors voltage levels on these pins and selects the input source having the highest input voltage.

LDO4 can be dedicated to supply USB HS analog PHY power domain and USB Type-C power delivery PHY applications.

The LDO4 output voltage is fixed at 3.3 V.

4.2.5 REFDDR's special features

Like LDO3, the VREFDDR (DDR reference voltage) is a sink-source LDO. It is dedicated to supply the reference voltage (VREF) pin of lpDDR3, DDR3, DDR3L, lpDDR4 and DDR4 memories.

The VREFDDR output voltage is fixed at $V_{OUT6}/^2$. The input of VREFDDR is internally connected to V_{OUT6}.

In the case that BUCK6 is enabled/disabled when VREFDDR is enabled, the output of the VREFDDR follows the BUCK6 startup/shutdown output voltage behavior, while maintaining $V_{OUT6}/^2$.

4.2.6 LDO output voltage settings

Table 19. **LDO output voltage settings**

	V_{OUT}[4:0] (decimal)	V_{OUT}[V] LDO2/LDO3/LDO5/LDO6/LDO7/LDO8
Step 100 mV	0	0.9
	1	1.0
	2	1.1
	3	1.2
	4	1.3
	5	1.4
	6	1.5
	7	1.6
	8	1.7
	9	1.8
	10	1.9
	11	2.0
	12	2.1
	13	2.2
	14	2.3
	15	2.4
	16	2.5
	17	2.6
	18	2.7
	19	2.8
	20	2.9
	21	3.0
	22	3.1
	23	3.2
	24	3.3
	25	3.4
	26	3.5
	27	3.6
	28	3.7
	29	3.8
	30	3.9
	31	4.0

4.2.7 Examples of DDR memory power supply topology using LDOs

Figure 5. **LDO3 uses in sink/source mode with DDR4**

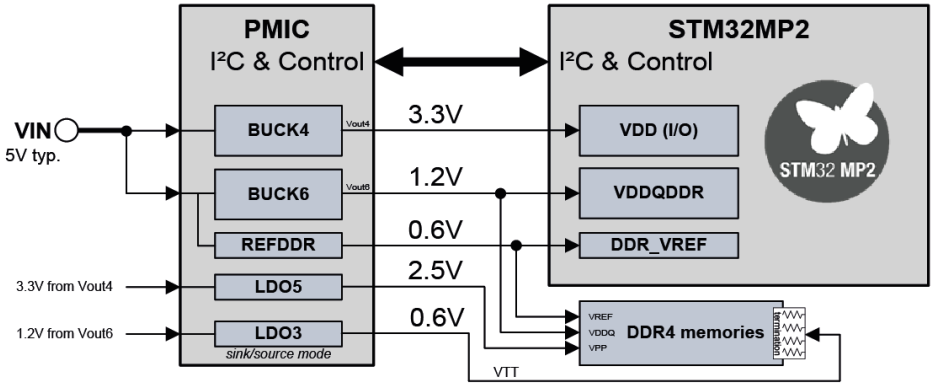


Figure 6. **LDO3 uses in sink/source mode with DDR3L**

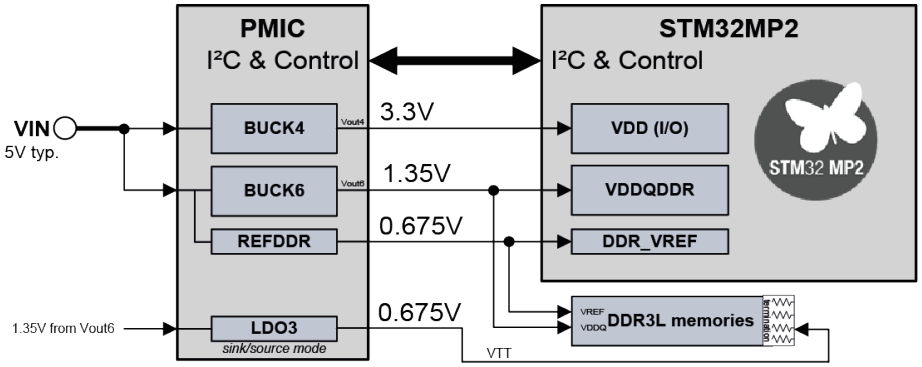
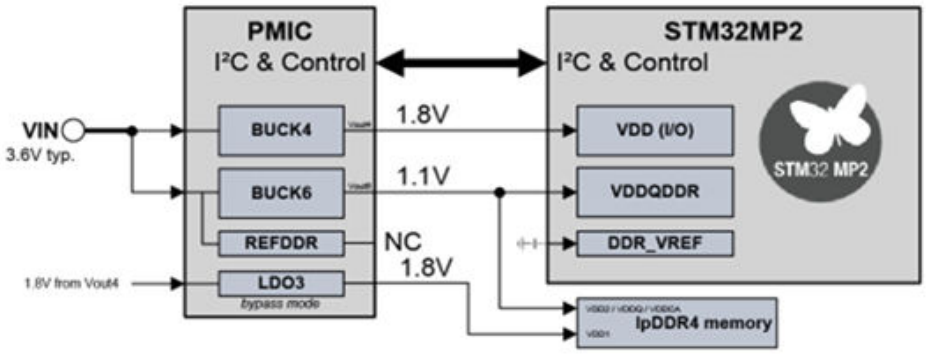


Figure 7. **LDO3 uses in bypass mode with lpDDR4**



4.3 Buck converters

General description

The STPMIC25 includes 7 buck converters that are optimized to supply circuits with high current consumption and meet fast transient response requirements.

All converters are based on an adaptive constant-on-time controller (COT) that guarantees an excellent transient response and high efficiency across a wide range of operating conditions.

Each converter can work in two power modes: HP mode and LP mode. These modes differ both in performance and quiescent current consumption. The highest performance can be reached in HP mode.

While in LP mode, the STPMIC25 has a much lower consumption and reduced general buck converter performance.

The switching frequency of the converter is typically 2 MHz in a steady-state CCM condition.

In a typical MPU application:

- BUCK1 is primarily dedicated to supply power to the VDDCPU domain.
- BUCK2 is primarily dedicated to supply power to the VDDCORE domain.
- BUCK3 is primarily dedicated to supply power to the VDDGPU domain.
- BUCK4 is primarily dedicated to supply power to the VDD (VIO) domain.
- BUCK5 is primarily dedicated to supply power to the VDDA18 domain.
- BUCK6 is primarily dedicated to supply power to the DDR memory and VDDQDDR domains.
- BUCK7's general purpose is to supply power to application peripherals.

BUCK1, BUCK2, BUCK3, BUCK6, and BUCK7 have excellent load transient responses across operating conditions.

BUCK4 and BUCK5 supply sensitive power domains and they have a low output voltage ripple across operating conditions.

4.3.1 Buck converters' common features

Enable/Disable: each buck can be enabled or disabled independently (same behavior as LDO: see Section 4.2.1)

V_{OUT} voltage setting: output voltage can be set:

- Automatically during a POWER_UP or POWER_DOWN sequence depending on the NVM settings.
- By software (I²C access): setting the V_{OUT} bit field in the related buck control register.
- By PWRCTRLx pins state change: the BUCKx converter behaves according to BUCKx_MAIN_CR and BUCKx_ALT_CR content setting. BUCKx_MAIN_CR or BUCKx_ALT_CR is selected by the PWRCTRL pin allocated to BUCKx (see section Section 5.4.6 (PWRCTRLx)).

Forced PWM mode (CCM mode**):** each buck can be forced to work in PWM mode to keep a constant frequency and low ripple.

HP/LP mode: each buck supports High Power (HP) mode and Low Power (LP) mode:

High Power mode (HP): buck converters work with maximum performance response.

Low Power mode (LP): the target of the LP mode is to decrease quiescent current. Buck converters work with limited performance.

In LP mode, buck converters support max $I_{OUT\_LP\_PEAK}$ peak currents.

HP/LP and forced PWM modes are activated by two bits PREG_MODE [1:0] register as follows:

00: HP (or auto mode)

01: LP

10: Forced PWM (CCM)

11: reserved

Clock synchronization and clock phase shifting: in HP mode, when all buck converters work in a steady state in CCM mode, they are synchronized with a clock and are shifted by 45° in the following order:

- BUCK1
- 45°: BUCK4
- 90°: BUCK2
- 135°: BUCK5
- 180°: BUCK3
- 225°: BUCK6
- 270°: BUCK7

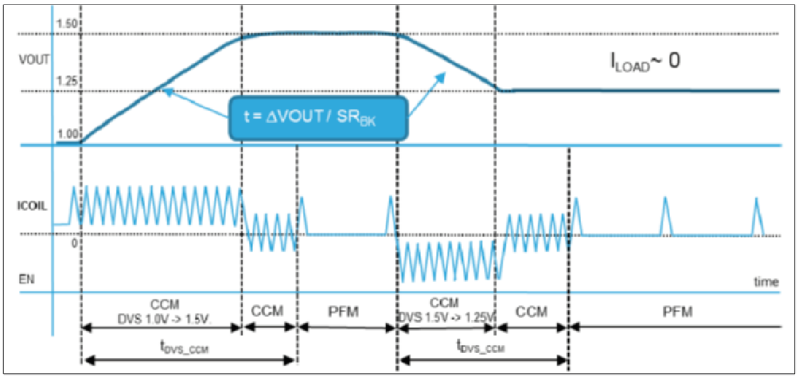
Note: It is possible to force all buck converters' synchronization by 45° phase shifting by setting all buck converters in forced CCM mode. This improves EMI and avoids peak current on the main power supply input source.

Frequency spreading: switching frequency spreading is supported to help manage EMC.

Dynamic voltage scaling (DVS): when the buck output voltage is increased/decreased dynamically by the software, the buck output voltage (V_{OUT}) is stepped up/down following the S_{RBK} slew rate.

When a lower V_{OUT} is set, part of the buck converter output energy is discharged from the output capacitor following the S_{RBK} slew rate, providing current back to the input supply capacitor. This operation improves the total power efficiency.

Figure 8. Buck dynamic voltage scaling (DVS)



OCP and Hiccup management: Each buck converter supports OCP and can operate in Hiccup mode. When the output load of the buck exceeds the I_{OUT} max output current (related to inductor peak current limit threshold I_{BKLIM}), the PWM pulse is immediately stopped, and the buck starts to decrease output voltage, limiting the output current. If the overcurrent lasts more than t_{OCPDB_BUCK}:

- An interrupt is generated (if the interrupt has been unmasked by software).
- Default behavior: the buck is turned OFF for t_{HICCUP_DLY} duration and then turned ON again.
- Alternative behavior: the PMIC is turned OFF for t_{HICCUP_DLY} duration and then turned ON again (or goes to FAIL_SAFE_LOCK state).

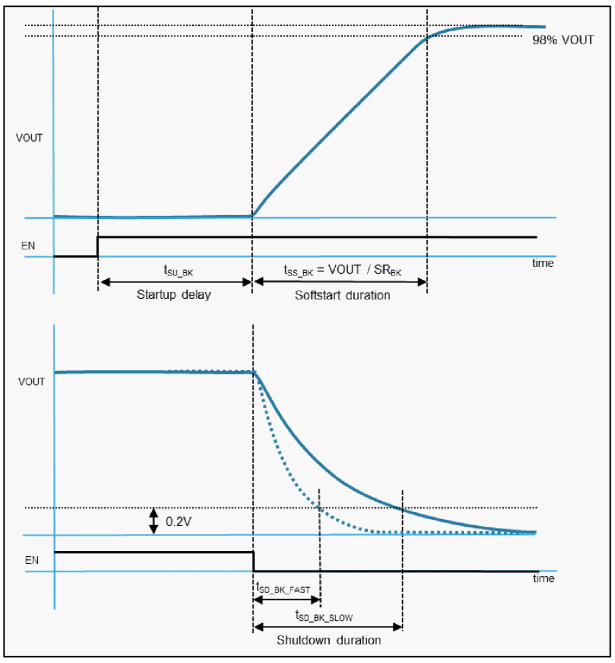
See Section 5.4.9 for details on OCP & hiccup management.

All buck converters have a programmable I_{OUT} max current threshold. I_{OUT} thresholds are programmed in the NVM_BUCKS_IOUT_SHR NVM register.

Output discharge: when the buck is disabled, a configurable pull-down (PD) discharge is automatically enabled. The buck output voltage discharges in tSD_BKtime duration (with typical recommended BOM) so that the buck converter output voltage is low before disabling the next regulators in the next ranking slot. Four values are configurable by software at runtime: no pull-down, slow-PD, fast-PD and forced slow-PD by setting BUCKS_PD_CR1/2. Fast discharge output can be modified by software in fast-PD when the buck is disabled, or it can be disabled by software to make the buck converter output in high impedance when it is disabled. See Figure 9 which shows fast-PD and slow-PD behavior.

Startup sequence: when a buck is enabled, a startup delay (tSU_BCK) occurs before the output voltage starts to rise, and is followed by a soft-start voltage ramp (tSS_BCK). See Figure 9

Figure 9. Buck startup/shutdown timings



4.3.2 Buck output voltage settings

Table 20. **Buck output voltage settings**

	V_{OUT}[6:0] (decimal)	V_{OUT}[V] BUCK1/2/3/6	V_{OUT}[V] BUCK4/5/7
Step 10 mV	0	0.50	1.5
	1	0.51	1.5
	2	0.52	1.5
	3	0.53	1.5
	4	0.54	1.5
	5	0.55	1.5
	6 to 94	...	1.5
	95	1.45	1.5
	96	1.46	1.5
	97	1.47	1.5
	98	1.48	1.5
	99	1.49	1.5
	100	1.50	1.5
Step 100 mV	101	1.50	1.6
	102	1.50	1.7
	103	1.50	1.8
	104	1.50	1.9
	105	1.50	2.0
	106 to 122	1.50	...
	123	1.50	3.8
	124	1.50	3.9
	125	1.50	4.0
	126	1.50	4.1
	127	1.50	4.2

5 Feature descriptions

5.1 Functional state machine

Overview

STPMIC25 integrates advanced low power features controlled by the application processor through I²C, six digital control pins (PONKEYn, WAKEUPn, PWRCTRL1/2/3, and RSTn) and one interrupt output line (INTn).

The main parameter settings can be programmed in a non-volatile memory (NVM) as default values at the startup time. See Section 5.5.2

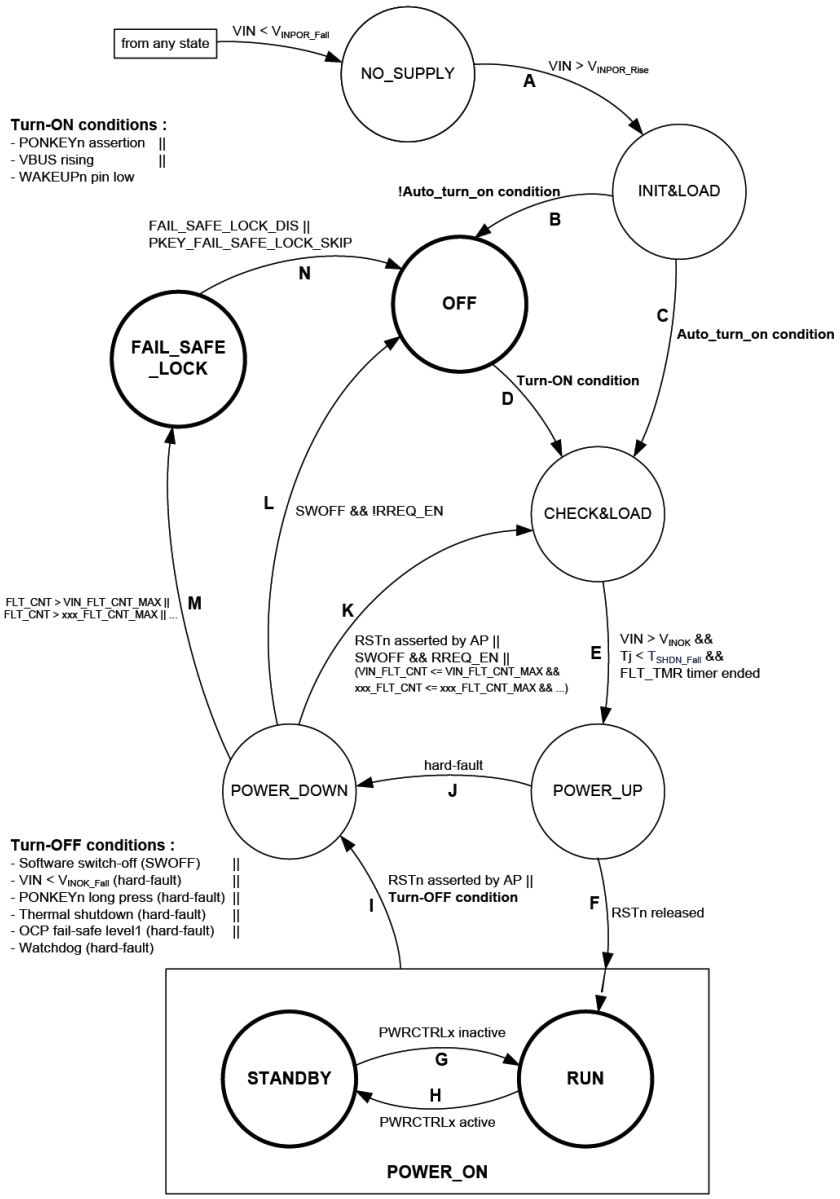
All regulators can be independently controlled from the PWRCTRLx pins. This allows flexible configuration and a fast transition between different power strategies at the application level.

Other features are provided to fulfill high-end application processors and advanced operating system needs:

- Multiple turn-on/turn-off conditions
- Mask_reset and restart_request options
- Overcurrent and overvoltage protection
- Thermal protection
- Watchdog
- Interrupt controller
- Safety management
- STANDBY ⇔ RUN states

PMIC state machine - STPMIC25 state machine is described in Figure 10

Figure 10. **PMIC state machine**



5.1.1 Transition conditions

Table 21. PMIC state machine transition conditions

Transition symbol	State transition	Transition condition
A	NO_SUPPLY to INIT&LOAD	V_{IN} > V_{INPOR_Rise}
B	INIT&LOAD to OFF	**! Auto_turn_on condition:** Init_OK && loadNVM_OK && !(AUTO_TURN_ON || PONKEYn_low || VBUS_high)
C	INIT&LOAD to CHECK&LOAD	**Auto_turn_on condition:** Init_OK && loadNVM_OK && (AUTO_TURN_ON || PONKEYn_low || VBUS_high)
D	OFF to CHECK&LOAD	**Turn-on condition:** PONKEYn falling edge || VBUS rising edge || WAKEUPn pin low
E	CHECK&LOAD to POWER_UP	**CHECK&LOAD is a transitory state going to POWER_UP:** V_{IN} > V_{INOK} && Tj < T_{SHDN_Fall} && FLT_TMR timer ended (see Table 24)
F	POWER_UP to RUN	When a power-up sequence ends without hard-fault, the PMIC releases RSTn, transition F occurs when the RSTn signal goes higher than V_{IH}. (see Section 5.4.7)
G	STANDBY to RUN	PWRCTRLx inactive (see Section 5.4.6)
H	RUN to STANDBY	PWRCTRLx active and all buck converters in LP mode or turned off (see Section 5.4.6)
I	POWER_ON to POWER_DOWN	**RSTn signal asserted by AP** **Turn-off condition:** Software switch-off (SWOFF) || V_{IN} < VINOK_Fall (hard-fault) || PONKEYn long press (hard-fault) || Thermal shutdown (hard-fault) || OCP fail-safe level1 (hard-fault) || Watchdog (hard-fault) See Section 5.4.4
J	POWER_UP to POWER_DOWN	**Turn-off condition (hard-fault):** V_{IN} < VINOK_Fall (hard-fault) || PONKEYn long press (hard-fault) || Thermal shutdown (hard-fault) || OCP fail-safe level1 (hard-fault) || Watchdog (hard-fault)
K	POWER_DOWN to CHECK&LOAD	RSTn asserted by AP || (SWOFF && RREQ_EN) || (VIN_FLT_CNT <= VIN_FLT_CNT_MAX && PKEY_FLT_CNT <= PKEY_FLT_CNT_MAX && TSHDN_FLT_CNT <= TSHDN_FLT_CNT_MAX && OCP_FLT_CNT <= OCP_FLT_CNT_MAX && WDG_FLT_CNT <= WDG_FLT_CNT_MAX)
L	POWER_DOWN to OFF	SWOFF && !RREQ_EN

Transition symbol	State transition	Transition condition
M	POWER_DOWN to FAIL_SAFE_LOCK	VIN_FLT_CNT > VIN_FLT_CNT_MAX || PKEY_FLT_CNT > PKEY_FLT_CNT_MAX || TSHDN_FLT_CNT > TSHDN_FLT_CNT_MAX || OCP_FLT_CNT > OCP_FLT_CNT_MAX || WDG_FLT_CNT > WDG_FLT_CNT_MAX
N	FAIL_SAFE_LOCK to OFF	**Transition to force leaving the fail-safe locked state:** FAIL_SAFE_LOCK_DIS (NVM bit) || PKEY_LKP_FSLS (PONKEY Long Key Press Fail-Safe-Lock-Skip bit)

5.1.2 State explanations

5.1.2.1 *NO_SUPPLY*

V_{IN} is below V_{INPOR_Fall} - see Section 5.4.1. No output state can be guaranteed in this state.

5.1.2.2 *INIT&LOAD*

The INIT&LOAD state is immediately reached when V_{IN} is higher than V_{INPOR_Rise}.

STPMIC25 releases internal POR circuitry, it initializes, all registers are reset, the NVM load is performed (see Section 5.5.2), and RSTn is asserted.

If the Auto_turn_on condition is true, PMIC makes a transition to the CHECK&LOAD state. Prior to leaving the INIT&LOAD state, the TURN_ON_SR is reset, and then the TURN_ON_SR[AUTO] bit is set.

If the Auto_turn_on condition is false, STPMIC25 evaluates the PONKEYn and VBUS status. If the turn on condition is not recognized, STPMIC25 makes the transition to the OFF state, otherwise it sets the proper bit in TURN_ON_SR and makes the transition to the CHECK&LOAD state (see Table 21.).

5.1.2.3 *OFF*

The OFF state is entered from the INIT&LOAD state, the POWER_DOWN state, or the FAIL_SAFE_LOCK state.

In the OFF state, the PMIC is in the lowest power consumption state, and all regulators are turned OFF. The voltage references are OFF and RSTn is asserted by PMIC.

All fail-safe counters are reset (xxx_FLT_CNT). Fail-safe timers (FLT_TMR), reset-fault-counter-timers (RST_FLT_CNT_TMR), and watchdog timers are stopped.

The transition to the CHECK&LOAD state (see Table 21) is triggered by a turn-on condition (see Section 5.4.3)

Prior to leaving the OFF state, the TURN_ON_SR is reset, then the related turn-on condition bit is set in the TURN_ON_SR register.

5.1.2.4 *CHECK&LOAD*

CHECK&LOAD is a transitional state from a user point of view. It prepares the PMIC to power-up.

The PMIC enables internal reference voltages, thermal monitoring, and V_{IN} monitoring.

The NVM is reloaded into shadow registers. Some registers are initialized with default values from the NVM content.

RSTn is asserted by the PMIC.

After the CHECK&LOAD state, the PMIC always transitions to the POWER-UP state if power-up conditions are fulfilled (see Table 21) and the fault timer (FLT_TMR) ends. The fault timer waits before restarting the PMIC after a hard-fault (see Section 5.4.5)

5.1.2.5 *POWER_UP*

The PMIC starts sequential regulators following a sequence that is predefined in the NVM and a default voltage that is predefined in the NVM (see Section 5.2).

During the power-up sequence, RSTn is asserted by the PMIC. When the power-up sequence ends without a hard-fault, the PMIC releases an RSTn signal.

5.1.2.6 *POWER_ON*

When the PMIC transitions from POWER_UP to POWER_ON, it always goes into the RUN state first.

In the **RUN** state, the PMIC can be set to deliver power at full performance and features. Each regulator can switch power states (MAIN_CR or ALT_CR) depending on the PWRCTRLx pin settings (see Section 5.4.6).

In the **STANDBY** application conditions state, the PMIC can reach the minimum of quiescent current by disabling internal IPs and by reducing their performances, such as reference accuracy. The PMIC can be set in the STANDBY state only if all buck converters are set in LP mode or turned OFF. See Table 6. Consumption in typical application scenarios.

Note: The PMIC exits from the STANDBY state in the case that any buck converter is set in HP mode.

When a turn-off condition or RSTn assertion from MPU occurs, the PMIC moves to the POWER_DOWN state.

In case of a hard-fault turn-off condition, before the PMIC leaves the POWER_ON state:

- The corresponding hard-fault counter is incremented (see Table 24): xxx_FLT_CNT ++
- The FLT_TMR is loaded with the corresponding hard-fault duration and started (see Table 24)

5.1.2.7 *POWER_DOWN*

The PMIC asserts RSTn, then sequentially turns-off the regulators starting with the regulators not enabled in the power-up sequence (= rank0: enabled by software at runtime), then in reverse sequence order in the POWER_UP state (see Section 5.2).

When the POWER_DOWN sequence ends, before the transition to the next state, the watchdog is disabled (WDG_EN = 0) and status registers are updated according to the turn-off condition source:

- TURN_ON_SR and TURN_OFF_SR and RESTART_SR and OCP_SR1 and OCP_SR2 are reset (cleared)
- If RSTn is asserted by AP (PMIC transition to K in Table 26):
  - RESTART_SR[R_RST] bit is set
- Else If SWOFF && RREQ_EN (PMIC transition to K in Table 26):
  - RESTART_SR[R_SWOFF] bit is set
- Else If SWOFF && !RREQ_EN (PMIC transition to L in Table 26):
  - TURN_OFF_SR[SWOFF] is set
- Else (it is a hard-fault turn-off condition, then depending on the hard-fault source):
  - If hard-fault is OCP:
    - OCP_SR1 or OCP_SR2 is updated with the OCP fault source
  - If PMIC transitions to M:
    - TURN_OFF_SR is updated with fault source
  - If PMIC transitions to K:
    - RESTART_SR is updated with fault source

Note: If another turn-off condition is triggered during the POWER DOWN sequence, it is ignored. So, only the original power-down trigger source is registered.

5.1.2.8 *FAIL_SAFE_LOCK*

The FAIL_SAFE_LOCK state is entered from the POWER_DOWN state with M transition (a hard-fault counter *xxx_FLT_CNT* that exceeds the max number of PMIC restart occurrences *xxx_FLT_CNT_MAX*).

In the FAIL_SAFE_LOCK state, the PMIC is in the lowest power consumption state: all regulators are turned OFF, voltage references are OFF, and RSTn is asserted by the PMIC.

The PMIC is locked in that state until it POR: a turn-on condition does not power-up the PMIC.

Nevertheless, the PMIC is allowed to skip the FAIL_SAFE_LOCK state in specific conditions of N transition (see Section 5.4.5.2).

5.2 POWER_UP / POWER_DOWN sequence

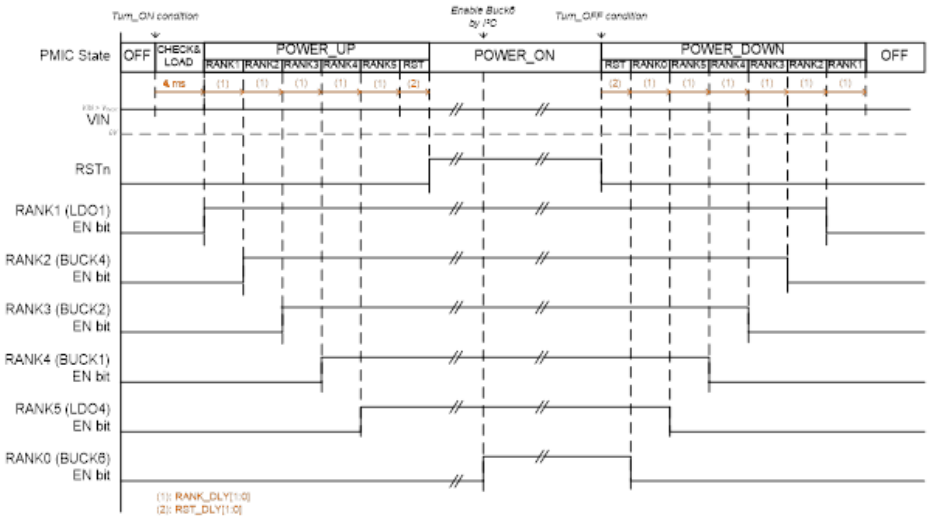
The PMIC starts and stops regulators following sequential rank procedures called POWER_UP and POWER_DOWN, respectively.

During POWER_UP each regulator is started at one of the 6-rank phases programmed in the NVM. Each rank phase is separated by a delay (1.5 ms, 3 ms, 4.5 ms, and 6 ms) programmed in the NVM.

An additional delay can be programmed in the NVM to release the RSTn signal later than last rank phase. This delay is also applied after the Turn_OFF condition, in between RSTn signal assertion and when the first regulator is powered off (RANK0).

The default rank sequence for each regulator, default output voltage of each regulator, default rank duration, and additional RSTn default delays are predefined in the NVM. Those values can be adapted by reprogramming the PMIC NVM with expected values.

Figure 11. PMIC POWER_UP and POWER_DOWN sequence example



For RANK_DLY and RST_DLY, see Table 91

Note: RANK0 means that the regulator is not turned ON.

5.2.1 OFF and CHECK&LOAD:

The PMIC is initially in the OFF state. The RSTn pin is asserted by the PMIC. Once a Turn_ON condition occurs, the PMIC goes into the CHECK&LOAD state. As the turn-ON condition is valid (for example: $V_{IN} > V_{INOK}$) the PMIC goes into the POWER_UP state.

5.2.2 POWER_UP:

In the POWER_UP state, RSTn is kept asserted by the PMIC.

The PMIC enables regulators sequentially by 1.5 ms slots (according to the default rank sequence and default output voltage defined in the NVM).

For example (see Figure 11:

RANK1 (LDO1) then RANK2 (BUCK4) then RANK3 (BUCK2) then RANK4 (BUCK1) then RANK5 (LDO4).

Once the RANK5 ends, the PMIC releases RSTn and then it goes into the POWER_ON state.

Note: Regulator RANK0 (BUCK6 in this example) is not turned ON automatically.

5.2.3 POWER_ON:

In the POWER_ON state, all regulators are managed by the application processor's software (I²C control) or by the PWRCTRL pin (see Section 5.3.5). In the example of Figure 11 BUCK6 is enabled by the AP's software at runtime.

5.2.4 POWER_DOWN:

Once a turn-OFF condition occurs, the PMIC asserts RSTn then the PMIC shuts down RANK0 regulators that have been started by software (BUCK6 in the Figure 11 example).

Then the PMIC disables the regulators sequentially in reverse rank order from the POWER_UP sequence, by 1.5 ms slots.

For example (see Figure 11):

RANK5 (LDO4) then RANK4 (BUCK1) then RANK3 (BUCK2) then RANK2 (BUCK4) then RANK1 (LDO1).

When the RANK1 ends, the PMIC goes into the OFF state (RSTn is kept asserted).

The analog behavior of regulators is detailed in Section 4

5.3 Digital pin description

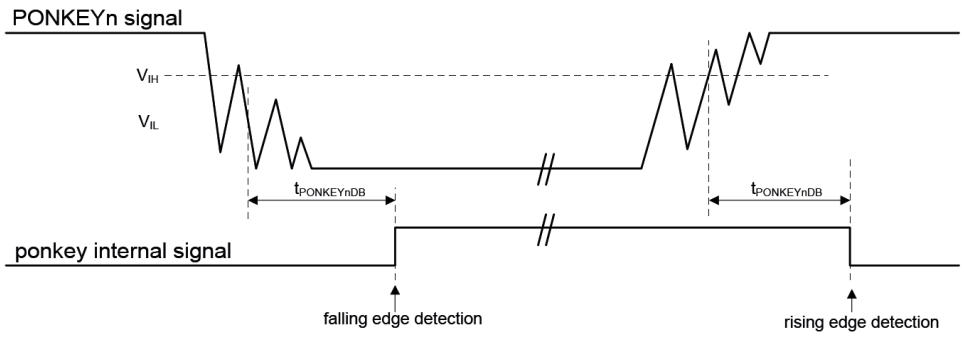
5.3.1 PONKEYn

The PONKEYn signal is intended to be connected to a push-button at the application level. If the push-button is pressed by a user, the PONKEYn signal is grounded. If the push-button is released by the user, the PONKEYn signal is floating, but the internal PMIC R_{PU} ties PONKEYn to V_{IN}.

Main characteristics:

- Digital input
- Active low
- Programmable pull-up (R_{PU}) internally connected to V_{IN}; R_{PU} active by default
- Debounce filter on rising and falling edges (see Figure 12)
- Turn-ON condition on falling edge (after debounce) when PMIC is in the OFF state
- Turn-ON condition on low level from a PMIC POR (see Section 5.4.3)
- Interrupt on falling and rising edges (after debounce)
- Turn-OFF condition on PONKEYn long press (duration programmable)

Figure 12. PONKEYn debounce filter behavior



PONKEYn falling edge: the debounce filter timer is enabled once the PONKEYn voltage is lower than V_{IL}. If a bounce voltage higher than V_{IH} occurs, the debounce filter timer is canceled and so on.

PONKEYn rising edge: the debounce filter timer is enabled once the PONKEYn voltage is higher than V_{IH}. If a bounce voltage lower than V_{IL} occurs, the debounce filter timer is canceled and so on.

5.3.2 WAKEUPn

Main characteristics:

- Digital input
- Active low
- Programmable pull-up (R_{PU}) internally connected to V_{INTLDO}; R_{PU} active by default
- Turn-ON condition on low level (1)
- Interrupt on falling and rising edges (1)

1. *WAKEUPn has no debounce filter. The PMIC detects a pulse smaller than the $t_{WAKEUPnAS}$ duration. The PMIC must detect a pulse equal to or longer than the $t_{WAKEUPnAS}$ duration.*

5.3.3 RSTn

The RSTn is a bidirectional reset pin both for the PMIC and the application processor:

- Digital input: active low input reset (when not asserted by the PMIC): the application processor can assert RSTn low to force the PMIC to power cycle.
- Open drain output: the PMIC can assert RSTn low to reset the application processor, typically during a power-ON or a power-OFF sequence and a power cycling reset sequence. Pull-up (R_{PU}) is internally connected to V_{IO}.

5.3.4 INTn

The PMIC asserts INTn low when a PMIC interrupt is pending (and not masked):

- Digital output (open drain)
- Active low
- Pull-up (R_{PU}) internally connected to V_{IO}

5.3.5 PWRCTRL1, PWRCTRL2, PWRCTRL3

Power control signals aim to control the regulator's behavior. Typically, power control signals are driven to ‘1’ or ‘0’ by the application processor to manage different power modes at application level.

PWRCTRLx pin characteristics:

- Digital input
- Level sensitive
- Programmable polarity
- Rising and falling delay cells
- Inactive by default
- Programmable pull-up (R_{PU}) internally connected to V_{IO} or pull-down (R_{PD}), and R_{PU} is active by default.
- No debounce

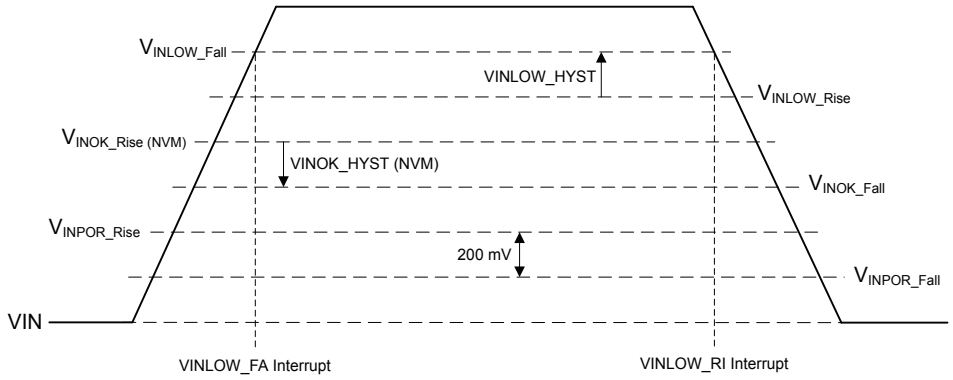
See Section 5.4.6 for behavior description.

5.4 Feature descriptions

5.4.1 V_{IN} monitoring

The main input supply pin V_{IN} is monitored permanently by the PMIC state machine. There are different threshold triggers on V_{IN}. The lowest to the highest thresholds are: V_{INPOR}, V_{INOK}, and V_{INLOW} as presented in the Figure 13.

Figure 13. V_{IN} monitoring thresholds



5.4.1.1 *V_{INPOR}*

V_{INPOR} is the minimum voltage required to supply the PMIC internal circuitry. It is specified by two hardcoded thresholds with 200 mV hysteresis:

Below V_{INPOR_Fall}, the PMIC is considered as not supplied.

Above V_{INPOR_Rise}, the PMIC internal circuitry is functional.

Note: Once V_{IN} rises above V_{INPOR_Rise}, PMIC internal circuitry remains functional until V_{IN} falls below V_{INPOR_Fall}.

Refer to Section 3.4.1 for threshold values.

5.4.1.2 *V_{INOK}*

V_{INOK} is the minimal voltage required to allow the PMIC to work in the POWER_ON state.

It is specified by V_{INOK_Rise} threshold and V_{INOK_HYST} hysteresis values that can be adjusted in the NVM, respectively by the V_{INOK_RISE}[1:0] and V_{INOK_HYST}[1:0] bits field.

If V_{IN} falls below V_{INOK_Fall} (V_{INOK_Fall} = V_{INOK_Rise} – V_{INOK_HYST}), then it is considered as a hard-fault turn-OFF condition and the PMIC immediately starts the POWER_DOWN sequence (see Section 5.4.4.). Following this condition, the PMIC waits for the t_{VINOK_Fall} delay before it can restart, even if V_{IN} goes back higher than V_{INOK_Rise} before the t_{VINOK_Fall} delay ends.

Definition: The V_{IN} > V_{INOK} condition means that if V_{IN} rises above V_{INOK_Rise} then V_{IN} remains higher than V_{INOK_Fall}. Reciprocally, V_{IN} < V_{INOK} means that V_{IN} < V_{INOK_Fall} or V_{IN} is less than the V_{INOK_Rise} threshold (this definition is just to simplify the state machine description).

5.4.1.3 *V_{INLOW}*

V_{INLOW} operates as a flag: V_{INLOW_Fall} and V_{INLOW_Rise} are configurable software thresholds that notify the AP (via an interrupt line) when the V_{IN} voltage crosses one of those two thresholds.

V_{INLOW} can be enabled and configured by programming the register V_{INLOW_CR}.

V_{INLOW_Rise} and V_{INLOW_Fall} thresholds generate respectively V_{INLOW_RI} and V_{INLOW_FA} interrupts, allowing the application processor to take relevant actions. They can be unmasked independently.

The V_{INLOW_RI} interrupt is asserted once V_{IN} goes below the V_{INLOW_Rise} threshold.

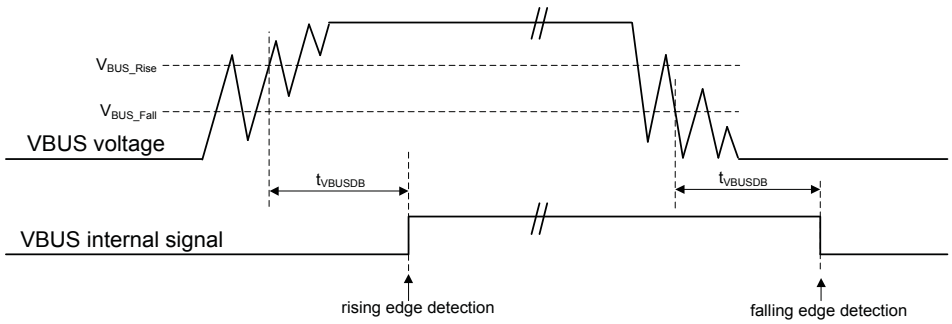
The V_{INLOW_FA} interrupt is asserted once V_{IN} goes higher than the V_{INLOW_Fall} threshold.

Refer to Section 6.6

5.4.2 V_{BUS} monitoring

V_{BUS} is monitored permanently by the PMIC state machine. V_{BUS} monitoring is filtered by the t_{VBUSDB} debounce timer for both rising and falling voltages as shown in Figure 14

Figure 14. V_{BUS} debounce filter behavior



5.4.3 Turn-on conditions

A turn-on condition is required to power-up the PMIC and to reach the POWER_ON state. A turn-on condition is only valid from the OFF state, or alternatively from the NO_SUPPLY state (the PMIC has no VIN initially).

The PMIC manages several turn-on conditions:

- PONKEYn pin assertion
- VBUS voltage presence
- WAKEUPn pin assertion
- AUTO turn-on (AUTO_TURN_ON bit set in the NVM)
- Fail-safe restart condition

Note: A fail-safe restart condition is not a real turn-on condition, but rather an allowed restart condition following a failure event triggering a turn-off event. See Section 5.4.5.

5.4.3.1 *PONKEYn / VBUS / WAKEUPn turn-on detection conditions*

A turn-on condition can be triggered by 3 external signal sources:

PONKEYn is tied low initially. The PMIC is in a NO_SUPPLY state. When the VIN voltage rises and crosses the V_{INPOR_Rise} threshold, the PMIC goes into the INIT&LOAD state (transition A), and then it goes into the CHECK&LOAD state (transition C).

PONKEYn is initially released. The PMIC is in the OFF state. When the PONKEYn is asserted, a turn-on condition occurs.

WAKEUPn asserted low is always a turn-on condition.

VBUS is tied high initially (VBUS > V_{BUS_Rise}). The PMIC is in the NO_SUPPLY state. When the VIN voltage rises and crosses the V_{INPOR_Rise} threshold, the PMIC goes into the INIT&LOAD state (transition A), and then it goes into the CHECK&LOAD state (transition C).

VBUS is initially < V_{BUS_Fall}. The PMIC is in the OFF state. When the VBUS voltage rises and crosses V_{BUS_Rise}, a turn-on condition occurs.

Table 22. Turn-on conditions from external trigger source summary

Source	Turn-on condition	Debounce
PONKEYn pin	PONKEYn signal low from the PMIC in a NO_SUPPLY state when VIN rises and crosses V_{INPOR_Rise}	N/A

Source	Turn-on condition	Debounce
PONKEYn pin	PONKEYn signal falling edge when the PMIC is in the OFF state	$t_{PONKEYnDB}$
WAKEUPn pin	WAKEUPn signal low	No debounce
VBUS pin	VBUS signal high from the PMIC in the NO_SUPPLY state when VIN rises and crosses V_{INPOR_Rise}	N/A
VBUS pin	VBUS signal rising edge when the PMIC is in the OFF state	t_{VBUSDB}

5.4.3.2 *AUTO turn-ON*

AUTO turn-ON allows the PMIC to be turned ON automatically when V_{IN} rises from $V_{IN} < V_{INPOR\_Fall}$. An AUTO turn-ON event is triggered only from a NO_SUPPLY state transition:

1. V_{IN} rises from V_{INPOR_Fall} to V_{INPOR_Rise}
2. PMIC goes into INIT&LOAD state then the AUTO_TURN_ON bit is enabled in the NVM
3. PMIC goes into the CHECK&LOAD state, waiting for $V_{IN} > V_{INOK}$
4. PMIC POWER_UP

The AUTO turn-ON is enabled in the NVM by default in NVM content.

5.4.4 Turn-off conditions

Turn-off conditions are triggered by events or stimulus leading the PMIC to perform a POWER_DOWN sequence.

Following the POWER_DOWN sequence, the PMIC can switch to the OFF state or to the FAIL_SAFE_LOCK state or restart automatically (power cycle), depending on the source that has triggered the turn-off condition.

There are six sources triggering a turn-off condition detailed in Table 23

Table 23. Turn-off condition trigger sources

Source	Type	Turn-off condition	Power cycle condition
Software switch-OFF	switch-off	Writing 1 to SWOFF bit.	RREQ_EN = 1
V_{INOK_Fall}	hard-fault	V_{IN} falls below the V_{INOK_Fall} threshold (with V_{IN} keeps it higher than $V_{IN\_POR\_Fall}$). See Section 5.4.1.	VIN_FLT_CNT <= VIN_FLT_CNT_MAX
PONKEYn long key press	hard-fault	PKEY_LKP_OFF bit set or NVM_PKEY_LKP_OFF bit set (NVM). Long key press duration can be set in PKEY_LKP_TMR[3:0] bitfield or in NVM_PKEY_LKP_TMR[1:0] bit field (NVM). PONKEYn signal is asserted low for a duration > PKEY_LKP_TMR[3:0].	PKEY_FLT_CNT <= PKEY_FLT_CNT_MAX
Thermal shutdown	hard-fault	PMIC junction temperature exceeds the T_{SHDN_Rise} threshold. See Section 5.4.8.	TSHDN_FLT_CNT <= TSHDN_FLT_CNT_MAX
Overcurrent protection	hard-fault	Overcurrent detected on a regulator (related regulator NVM_FS_OCP_xxx. (1) bit set in NVM or FS_OCP_xxx (1) bit set by software). See Section 5.4.9.	OCP_FLT_CNT <= OCP_FLT_CNT_MAX
Watchdog	hard-fault	Watchdog feature active and timer expired. See Section 5.4.10.	WDG_FLT_CNT <= WDG_FLT_CNT_MAX

1. *xxx: instance name of the regulator, eg: LDO1, LDO2, BUCK1,*

5.4.4.1 *Turn-OFF condition triggered by software switch-off*

When the software sets the SWOFF bit, the PMIC starts a POWER_DOWN sequence immediately, then the PMIC goes into the OFF state. The TURN_OFF_SR is set accordingly.

If the software has set both the RREQ_EN and SWOFF bits, the PMIC restarts automatically after the POWER_DOWN sequence (transition K) and goes into the POWER_ON state. The RESTART_SR register is set accordingly.

5.4.4.2 *Turn-OFF condition triggered by a hard fault*

Each hard-fault source has a hard-fault counter: see Table 24

Each time a hard-fault event occurs, a turn-off condition is triggered and it is managed by fail-safe management. See Section 5.4.5

5.4.5 Fail-safe management

Each hard-fault source has an independent fail-safe counter that is incremented each time a hard-fault turn-off condition occurs (see Table 24). If the counter value is below (or equal to) the max limit, then the PMIC restarts (= power cycling on fault condition). Alternatively, if the counter is higher than the max limit, then the PMIC goes into the FAIL_SAFE_LOCK state to avoid cyclic hard failures.

Sequence details:

When a turn-off condition is triggered by a hard-fault source (see Table 23):

- The corresponding hard-fault counter is incremented (see Table 24): xxx_FLT_CNT ++
- The FLT_TMR is loaded with the corresponding hard-fault duration and starts (see Table 24)
- The PMIC switches to the POWER_DOWN sequence
- Once the POWER_DOWN sequence ends:
  - If all counters xxx_FLT_CNT <= xxx_FLT_CNT_MAX then the PMIC goes into the CHECK&LOAD state, then PMIC waits for a FLT_TMR timer expiration before restarting (see Table 29), then it goes into POWER_UP, and then it goes in POWER_ON state. The corresponding bit in the RESTART_SR status register is set.
  - Else if one of the counters xxx_FLT_CNT > xxx_FLT_CNT_MAX then PMIC goes into the FAIL_SAFE_LOCK state. The corresponding bit in the TURN_OFF_SR status register is set. Even when the FAIL_SAFE_LOCK is skipped, the PMIC waits for FLT_TMR expiration before restarting.

Table 24. Hard-fault fail-safe counters and waits before restarting timer

Source	Fail-safe counters	Max fault iteration (NVM shadow register)	Wait before restart timer duration FLT_TMR[x]
V_{INOK_Fall}	VIN_FLT_CNT[3:0]	VIN_FLT_CNT_MAX[3:0]	t_{VINOK_Fall}
PONKEYn long press	PKEY_FLT_CNT[3:0]	PKEY_FLT_CNT_MAX[3:0]	0
Thermal shutdown	TSHDN_FLT_CNT[3:0]	TSHDN_FLT_CNT_MAX[3:0]	t_{TSHDN_DLY}
Overcurrent protection (OCP)	OCP_FLT_CNT[3:0]	OCP_FLT_CNT_MAX[3:0]	t_{HICCUP_DLY}
Watchdog	WDG_FLT_CNT[3:0]	WDG_FLT_CNT_MAX[3:0]	0

Notes:

1- When a counter (xxx_FLT_CNT[3:0]) reaches 0xF, all the next counter increments keep the counter value at 0xF (and not restart to 0). This allows for infinite PMIC restart iterations to be set when xxx_FLT_CNT_MAX[3:0] is set to 0xF.

2- Setting 0 in xxx_FLT_CNT_MAX makes the PMIC go into the FAIL_SAFE_LOCK state after the first corresponding turn-off hard-fault condition (PMIC restarts 0 time).

3- Setting 0xF in xxx_FLT_CNT_MAX makes the PMIC always restart after any corresponding urn-off fault condition as highlighted above in *Note 1* (PMIC restarts indefinitely).

4- Programming the NVM with tHICCUP_DLY ='0' means no wait before restart.

5.4.5.1 *Hard-fault counters reset and auto-reset*

To avoid reaching the FAIL_SAFE_LOCK state due to isolated turn-off hard-fault conditions, all counters can be reset automatically when no turn-off hard-fault condition occurs in RST_FTL_CNT_TMR timer duration. (See Table 25 for timer duration NVM settings):

From the NO_SUPPLY state and until a first turn-off condition occurs, the RST_FTL_CNT_TMR timer is disabled.

Once and each time a turn-off hard-fault condition occurs, the RST_FTL_CNT_TMR timer is reset to the RST_FLT_CNT_TMR[1:0] value and restarted.

When the RST_FTL_CNT_TMR timer elapses:

- All counters (*_FLT_CNT) are reset
- The RST_FTL_CNT_TMR timer is stopped until a new turn-off hard-fault condition occurs

If PMIC reaches the FAIL_SAFE_LOCK state before the RST_FTL_CNT_TMR timer elapses, then RST_FTL_CNT_TMR timer is reset and stopped.

A RSTn condition has no effect on the RST_FTL_CNT_TMR timer.

In the OFF state, the RST_FTL_CNT_TMR timer is reset and stopped, and all counters (*_FLT_CNT) are reset.

Table 25. Reset fault counter timer settings

RST_FLT_CNT_TMR[1:0] (NVM shadow register)	Timer duration
00	disabled
01	1 min
10	6 min
11	60 min

5.4.5.2 *FAIL_SAFE_LOCK state skipping*

When the PMIC enters into the FAIL_SAFE_LOCK state, it remains in this state until PMIC POR (VIN < V_{INPOR_Fall}).

Alternatively, there are two programmable options to force the PMIC to switch from the FAIL_SAFE_LOCK state to the OFF state:

- A PONKEYn long key press if the software sets the PKEY_LKP_FSLS bit prior to entering the FAIL_SAFE_LOCK state or if the NVM_PKEY_LKP_FSLS bit is set in the NVM.
- Set the bit FAIL_SAFE_LOCK_DIS in the NVM. It disables the FAIL_SAFE_LOCK feature (when the PMIC enters into the FAIL_SAFE_LOCK state, it immediately transitions to the OFF state).

Note: When the PMIC performs the transition from the FAIL_SAFE_LOCK state to the OFF state, a turn-ON condition should occur to power-up the PMIC (the AUTO_TURN_ON bit has no effect on the FAIL_SAFE_LOCK state to the OFF state transition).

5.4.6 Power control management (PWRCTRLx)

PWRCTRL1, PWRCTRL2, and PWRCTRL3 are digital inputs controlled from an application processor (see Section 5.3.5). They are dedicated to managing different application power modes or special regulator reset features.

PWRCTRL1, PWRCTRL2, PWRCTRL3 can be independently muxed onto each regulator instance (BUCKx or LDOx).

For example, BUCK1 may be controlled by PWRCTRL2, and BUCK2, BUCK7, and LDO8 can be controlled by PWRCTRL1, and so on.

A regulator instance can be controlled from a single PWRCTRL signal.

For each regulator instance, a PWRCTRL input can be used either to:

- Switch between the xxx_MAIN_CR register or the xxx_ALT_CR register of a regulator (where xxx is the regulator instance)
  - The regulator behaves according to the selected xxx_MAIN_CR or xxx_ALT_CR register
- Reset a regulator instance to its default value (from the NVM)

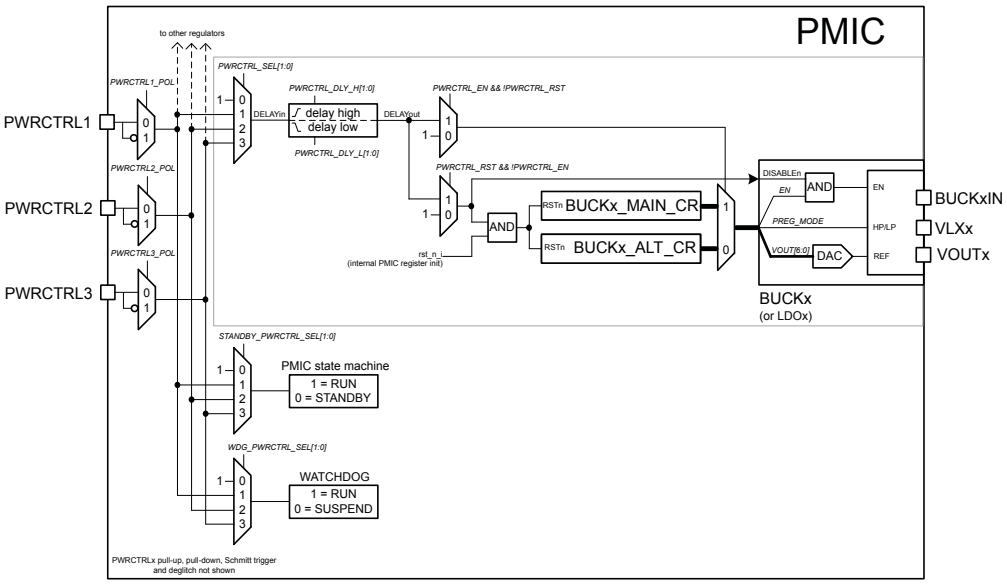
PWRCTRL1, PWRCTRL2, or PWRCTRL3 can be used to switch the PMIC state machine RUN to STANDBY (see Table 21).

PWRCTRL1, PWRCTRL2, or PWRCTRL3 can be used to suspend the watchdog, typically when the AP is in low-power mode.

The Figure 15 provides the logic circuitry principle showing:

- How a buck converter is controlled from a PWRCTRLx
- How the PMIC state machine is driven to switch between RUN <=> STANDBY states

Figure 15. PWRCTRLx logic circuitry principle (TO BE CONTROLLE BY DESIGN)



PWRCTRL1_POL, PWRCTRL2_POL, and PWRCTRL3_POL bits set the polarity of PWRCTRL1, PWRCTRL2, and PWRCTRL3, respectively. Those settings are applicable for all regulators (not linked to a single regulator).

PWRCTRLx_POL: polarity of PWRCTRLx signal (with x= 1,2,3): 0: active low; 1: active high.

See Table 26.

Table 26. PWRCTRLx polarity truth table

PWRCTRLx input level	PWRCTRLx_POL	PWRCTRLx logic level
0	0	Active
1	0	Inactive
0	1	Inactive
1	1	Active

Note: x is the instance number of the PWRCTRL pin.

STANDBY_PWRCTRL_SEL[1:0]: State machine control source selection for state transition RUN <=> STANDBY when the PMIC is in the POWER_ON state (see Section 5.1).

WDG_PWRCTRL_SEL[1:0]: Watchdog control source selection. When PWRCTRLx is active, the watchdog timer is suspended. When PWRCTRLx is inactive, the watchdog timer is running (if watchdog is enabled) (see Section 5.4.10).

Note: There is one instance of the following registers per regulator instance:

PWRCTRL_SEL[1:0]: BUCKx control/reset source selection.

PWRCTRL_DLY_H[1:0]: BUCKx control/reset source shift delay from low to **H**igh level (typically to perform the power ON sequence between different regulators; driven by a PWRCTRL signal). 0 = no delay; 1 = 1.5 ms delay; 2 = 3 ms delay; and 3 = 6 ms delay.

PWRCTRL_DLY_L[1:0]: BUCKx control/reset source shift delay from high to **L**ow level (typically to emulate the power OFF sequence between different regulators; driven by a PWRCTRL signal). 0 = no delay; 1 = 1.5 ms delay; 2 = 3 ms delay; and 3 = 6 ms delay.

PWRCTRL_EN: BUCKx control source enable. 0: disable, 1: enable. When enabled, BUCKx is controlled from a PWRCTRL signal:

- If PWRCTRL is inactive, the BUCKx_MAIN_CR register is used to control BUCKx
- If PWRCTRL is active, the BUCKx_ALT_CR register is used to control BUCKx

PWRCTRL_RST: BUCKx independent reset source enable. 0: disable, 1: enable. When enabled, BUCKx is reset from a PWRCTRL signal. See Section 5.4.6.2 for details:

1. If PWRCTRL is active
2. BUCKx is disabled (forced by the DISABLEn signal in Figure 15)
3. The BUCKx_MAIN_CR and BUCKx_ALT_CR registers are reset to default value (the NVM default value is reloaded in both registers).
4. If PWRCTRL is inactive, the BUCKx_MAIN_CR register is used to control BUCKx.

Notes:

1 - If both *PWRCTRL_EN and PWRCTRL_RST* are set by mistake, both the control source and independent reset features are disabled (no effect).

2 - The above bit field descriptions are also applicable for LDOs by replacing BUCKx with LDOx.

Table 27. Regulator control truth table

PWRCTRLx logic level	PWRCTRL_RST	PWRCTRL_EN	Regulator control register
active or inactive	0	0	xxx_MAIN_CR
active	0	1	xxx_ALT_CR
inactive	0	1	xxx_MAIN_CR
active	1	0	xxx regulator disabled (OFF) xxx_MAIN_CR & xxx_ALT_CR registers are reset to default value
inactive	1	0	xxx_MAIN_CR
active or inactive	1	1	xxx_MAIN_CR

Note: : x is the instance number of the PWRCTRL pin; xxx is the instance name of a regulator.

5.4.6.1 *PWRCTRL delay high and delay low behaviors*

PWRCTRL delay blocks are independent for each regulator. A delay block allows a PWRCTRLx signal to shift by preprogrammed delays. Each delay block is composed of two parts (a delay high and a delay low). The first operates at a high input level, and the second operates at a low input level.

Delay blocks are typically used to emulate power sequences between regulators when entering or leaving a low power mode.

High level delay behavior:

When the input signal goes from low to high level, the “high level delay timer” (PWRCTRL_DLY_H[1:0]) is started. Once the timer expires, the output goes high.

If the input signal changes from high to low before the “high level delay timer” expires, the “high level delay timer” is stopped and reset, and the output keeps the previous value.

Low level delay behavior:

Same behavior as for the high level delay but on low level input.

When the input signal goes from high to low level, the “low level delay timer” (PWRCTRL_DLY_L[1:0]) is started. Once the timer expires, the output goes low.

If the input signal changes from low to high before the “low level delay timer” expires, the “low level delay timer” is stopped and reset, and the output keeps the previous value.

Note: The "high level delay timer" and "low level delay timer" are both driven from a level (and not from an edge) to ensure that the output is always copying the input after any delay expires.

Figure 16 illustrates this example, using the PWRCTRL2 to control the BUCK1 and the BUCK2:

Settings for the Figure 16 example:

PWRCTRL2_POL = 0; // PWRCTRL2 active low = bypass

// BUCK1 settings

BUCK1_PWRCTRL_CR[PWRCTRL_SEL[1:0]] = 2; // PWRCTRL2 as BUCK1 control source

BUCK1_PWRCTRL_CR[PWRCTRL_DLY_H[1:0]] = 0; // no delay on PWRCTRL2 going from low to high for BUCK1

BUCK1_PWRCTRL_CR[PWRCTRL_DLY_L[1:0]] = 2; // 3 ms delay on PWRCTRL2 going from high to low for BUCK1

BUCK1_PWRCTRL_CR[PWRCTRL_EN] = 1; // enable the PWRCTRL input feature for BUCK1

// BUCK2 settings

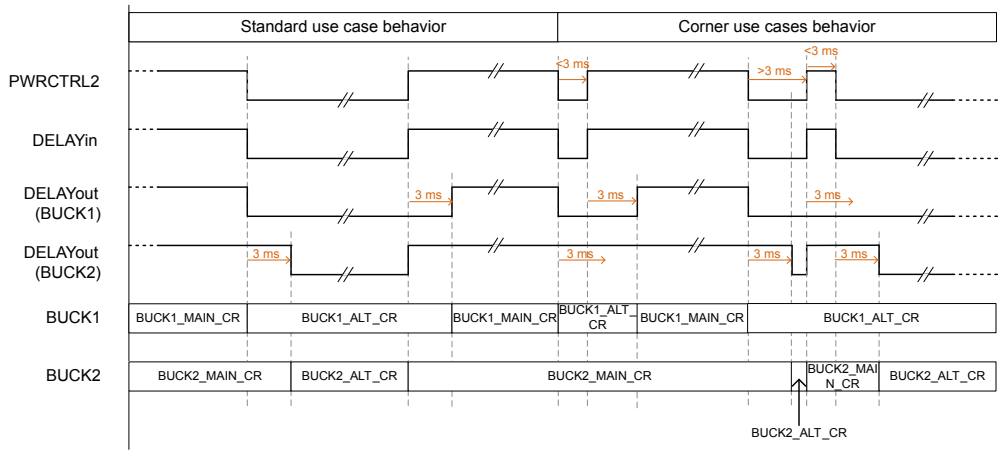
BUCK2_PWRCTRL_CR[PWRCTRL_SEL[1:0]] = 2; // PWRCTRL2 as BUCK2 control source

BUCK2_PWRCTRL_CR[PWRCTRL_DLY_H[1:0]] = 2; // 3 ms delay on PWRCTRL2 going from low to high for BUCK2

BUCK2_PWRCTRL_CR[PWRCTRL_DLY_L[1:0]] = 0; // no delay on PWRCTRL2 going from high to low for BUCK2

BUCK2_PWRCTRL_CR[PWRCTRL_EN] = 1; // enable the PWRCTRL input feature for BUCK2

Figure 16. Delay rising and delay falling behaviors example



5.4.6.2 *Regulator independent reset detailed behaviors (PWRCTRL_RST)*

The independent reset feature is controlled from a PWRCTRLx input pin (*PWRCTRL_SRC[1:0]*) and it is enabled by setting the *PWRCTRL_RST* bit. This feature allows a regulator to reset to its default NVM value from an AP hardware signal “on the fly” (which cannot be done by I^2C access).

When the PWRCTRLx input pin is active, regulator xxx is forced into OFF mode. xxx_MAIN_CR and xxx_ALT_CR registers are both reset to default value (NVM default value is reloaded in both registers from the related NVM shadow register).

When the PWRCTRLx input pin is inactive, regulator xxx is controlled from xxx_MAIN_CR register content.

Figure 16 provides an example to illustrate Section *5.4.6.2* using the PWRCTRL3 to control the LDO2 independent reset.

Assumptions and settings for the Figure 17 example:

LDO2 reset value (from the NVM):

- LDO2_MAIN_CR[VOUT] = 2.9 V
- LDO2_MAIN_CR[EN] = 1

Software settings:

PWRCTRL3_POL = 0; // PWRCTRL3 active low = bypass

// LDO2 settings

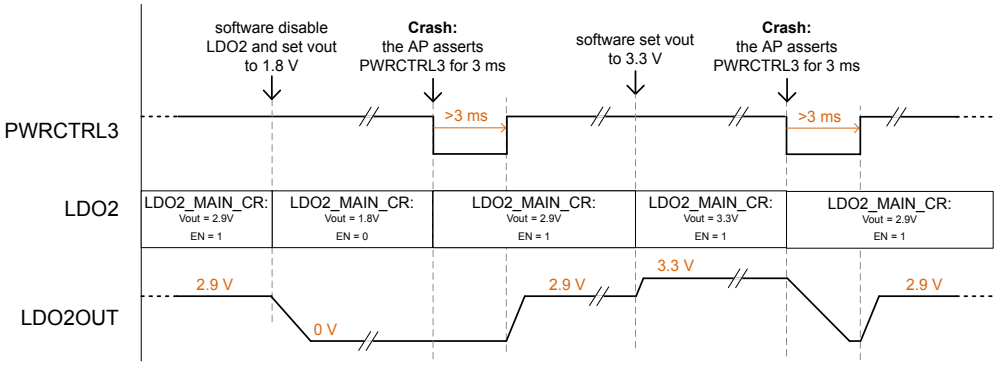
LDO2_PWRCTRL_CR[PWRCTRL_SEL[1:0]] = 3; // PWRCTRL3 as LDO2 control source

LDO2_PWRCTRL_CR[PWRCTRL_DLY_H[1:0]] = 0; // no delay on PWRCTRL3 going high for LDO2

LDO2_PWRCTRL_CR[PWRCTRL_DLY_L[1:0]] = 0; // no delay on PWRCTRL3 going low for LDO2

LDO2_PWRCTRL_CR[PWRCTRL_RST] = 1; // enable the PWRCTRL3 input to control LDO2 independent reset

Figure 17. Regulator independent reset behaviors example



5.4.7 Reset management (RSTn) and mask_reset software option

RSTn is a bidirectional reset pin both for the PMIC and the application processor. It has a digital input/open drain output topology with an internal pull-up resistor (R_{PU}).

- When the PMIC asserts RSTn, it drives the RSTn signal low (open drain internal transistor). The application processor is forced into a reset state.
- When the PMIC does not assert RSTn, the RSTn pin is in high impedance and the RSTn signal goes high (due to the pull-up resistor) if the RSTn signal is not asserted low externally (for example: by a reset push-button or from an application processor asserting the reset signal low). In that case, the PMIC RSTn pin becomes a digital input and it monitors the RSTn signal.

In the POWER_ON state, the RSTn pin can be driven by the application processor or a reset push-button.

When the application processor asserts RSTn low more than the t_{RSTnAS} duration, it immediately triggers a reset sequence of the PMIC by performing a noninterruptible power cycle:

1. The PMIC asserts RSTn low (forcing the AP to keep it in reset, and in the case that the AP releases the reset before the end of the sequence)
2. POWER_DOWN sequence
3. CHECK &LOAD
4. POWER_UP sequence
5. PMIC deasserts RSTn and monitors RSTn
6. PMIC waits for the RSTn signal to go high before entering POWER_ON (to prevent an infinite loop of reset sequence)

The PMIC can detect a negative pulse on RSTn shorter than the tRSTnAS duration. The PMIC must detect a negative pulse longer or equal to the tRSTnAS duration.

5.4.7.1 mask_reset software option

From step 2 to step 4 (in the above sequence), LDOs and buck regulators follow a POWER_DOWN sequence followed by a POWER_UP sequence as defined in Section 5.2; except for regulators having the **mask_reset** option bit set.

The **mask_reset** option can be defined for each regulator by setting the corresponding MRST bit in corresponding BUCKS_MRST_CR or LDOS_MRST_CR registers.

For example, for BUCK4: set the BUCK4_MRST bit in BUCKS_MRST_CR.

When the **mask_reset** option is set to a regulator, the MAIN and ALTERNATE related registers are not reset and content is maintained during and after the reset power cycle. Nevertheless, the PWRCTRLx settings are reset for all regulators, including those having the **mask_reset** option set:

- POWER_DOWN is not performed
- MAIN and ALTERNATE register values are not reset and their contents are maintained with the current value
- PWRCTRLx register settings are reset (xxx_PWRCTRL_CR)

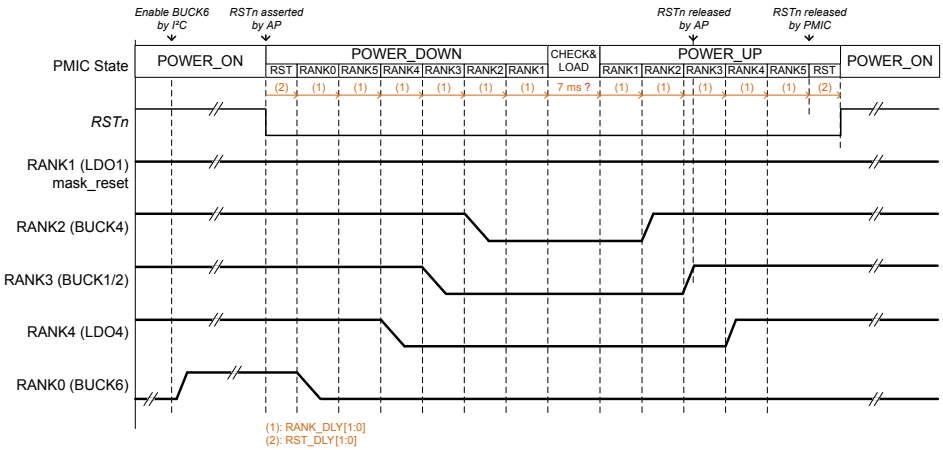
The PMIC always ends the power cycle in the POWER_ON state, regardless of the PWRCTRLx value, as all PWRCTRLx settings have been reset during the power cycle.

If RSTn is asserted in MAIN mode, regulators having the **mask_reset** option set are not impacted at all by the reset sequence, keeping V_{OUT}, EN, and PREG_MODE unchanged.

In case RSTn is asserted in the ALTERNATE mode, VOUT, EN, and PREG_MODE switch to the content of the [regulator]_MAIN_CR register values when the POWER_DOWN sequence ends before the POWER_UP sequence starts.

The Figure 18 illustrates a reset power cycle of the PMIC.

Figure 18. Reset power-cycle sequence example



For RANK_DLY and RST_DLY see Table 91

Settings related to the example in Figure 18:

LDO1 with **mask_reset** option set (LDOS_MRST_CR[LDO1_MRST] = 1), is not impacted by the reset power-cycle.

BUCK1, BUCK2, BUCK4, and LDO4 are powered down and up at their respective ranks defined in the NVM.

BUCK6 is enabled by I^2C. So, it is powered down first and not restarted (as not defined in the NVM to start).

mask_reset is valid once. It is cleared in the CHECK&LOAD state. So, it is cleared following a turn-OFF condition, a V_{INPOR}, and a RSTn assertion.

When RSTn is released by the application processor, the PMIC keeps RSTn asserted (the RSTn signal keeps low) meaning that the application processor is kept in reset until the PMIC releases the RSTn signal.

5.4.8 Thermal protection

The PMIC implements a thermal protection to prevent overheating damage. PMIC junction temperature is permanently monitored by an embedded thermal sensor.

The first level of thermal protection consists of an alarm sent by an interrupt to the application processor:

- When Tj rises above the T_{WRN_Rise} threshold, the PMIC generates an THW_RI interrupt
- When Tj falls below the T_{WRN_Fall} threshold, the PMIC generates an THW_FA interrupt

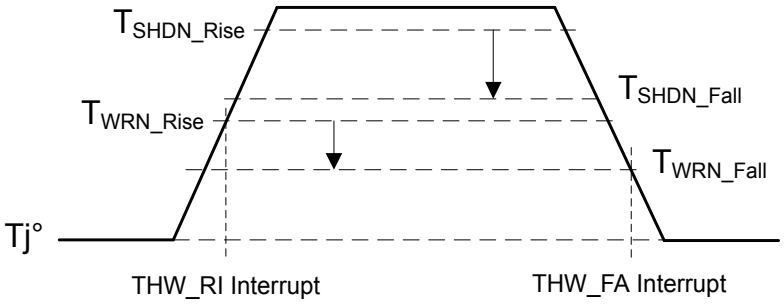
The application processor can manage to decrease the application activity load to decrease the application power consumption. Alternatively, a second level of thermal protection may occur.

The second level of thermal protection consists of triggering a turn-OFF hard-fault condition:

- When Tj rises above the T_{SHDN_Rise} threshold, the PMIC generates a turn-OFF hard-fault condition, and the thermal fail-safe counter is incremented (TSHDN_FLT_CNT ++):
  - If the thermal fail-safe counter reaches the maximum number of power cycles defined in the NVM (TSHDN_FLT_CNT > TSHDN_FLT_CNT_MAX) then the PMIC goes into the FAIL_SAFE_LOCK state.
  - Alternatively, when Tj falls below the T_{SHDN_Fall} threshold and a t_{TSHDN_DLY} delay ends, the PMIC restarts.

See Section 5.4.5 for details about fail-safe counter management.

Figure 19. **Thermal protection thresholds**



5.4.9 Overcurrent (OCP) and Hiccup mode

All regulators implement protection against overcurrent (OC) on their output.

Note: Short-circuits (SC) are managed by the overcurrent protection.

For each regulator, the PMIC embeds 2 levels of protection against overcurrent and short-circuits:

- Level 0 (default): independent regulator OCP Hiccup mode management
- Level 1: PMIC OCP fail-safe management (see Section 5.4.5)
- The default level of protection is defined in the NVM (NVM_FS_OCP_SHR1/2) for each regulator, and can be changed at runtime by software (FS_OCP_CR1/2)

5.4.9.1 Level 0: independent regulator OCP Hiccup mode management

Each PMIC regulator operates independently in Hiccup mode:

- When a short-circuit or an overcurrent occurs, the output current is limited to I_{LDOLIM} (for LDO) and I_{BKLIM} (for buck).
- If the SC or OC lasts more than t_{OCPDB_LDO} or t_{OCPDB_BUCK} (respectively for LDO or buck):
  - The regulator turns OFF for the t_{HICCUP_DLY} duration
  - An interrupt is generated (if the interrupt is unmasked by software)
- Once the t_{HICCUP_DLY} timer elapses, the regulator turns ON
  - If the SC or OC is removed, the LDO operates normally
  - If the SC or OC stays present, the regulator goes into step 1, repeating the cycle until the overload disappears (hiccup)

Notes:

- 1) When the t_{HICCUP_DLY} timer duration is set to 0, the regulator is turned-OFF (interrupt-generated) and it does not restart (step 3 is skipped).
- 2) The t_{HICCUP_DLY} timer duration can be adjusted in the NVM by setting the HICCUP_DLY[1:0] bit field in the NVM_BUCKS_IOUT_SHR2 shadow register then programming the NVM.
- 3) The t_{HICCUP_DLY} timer is reset if a POWER_DOWN occurs at the same time. In this way, the IP can restart with its assigned RANK at the next POWER_UP. This happens even if the mask reset is set and/or t_{HICCUP_DLY} is set to ‘0’.

5.4.9.2 *Level 1: PMIC OCP fail-safe management*

Each PMIC regulator can be set independently to trigger a hard-fault condition when an overcurrent or a short circuit occurs:

- When a short-circuit or an overcurrent occurs, the output current is limited to I_{LDOLIM} (for LDO) and I_{BKLIM} (for buck).
- If the SC or OC lasts more than t_{OCPDB_LDO} or t_{OCPDB_BUCK} (respectively for LDO or buck), the PMIC generates a turn-OFF hard-fault condition. OCP_SR1 or OCP_SR2 is updated with the OCP fault source, and the OCP fail-safe counter (1) is incremented (OCP_FLT_CNT ++):
  - If the OCP fail-safe counter reaches the maximum number of power cycles defined in the NVM (OCP_FLT_CNT > OCP_FLT_CNT_MAX), the PMIC goes in FAIL_SAFE_LOCK state.
  - Alternatively, when the t_{HICCUP_DLY} delay ends, the PMIC restarts.

1. *There is a single OCP fail-safe counter (OCP_FLT_CNT) for all regulators. It is incremented each time a regulator triggers a hard-fault regardless of the regulator instance.*

5.4.10 Watchdog management

The PMIC has an internal watchdog timer. A watchdog timer expiration generates a turn-OFF hard-fault condition (see Section 5.4.4.2) followed either by a PMIC restart (power cycling) or by the PMIC going into the FAIL_SAFE_LOCK state.

The watchdog can be enabled/disabled by software or at power-up (NVM settings), respectively:

- Software: set/reset WDG_EN bit at runtime
- NVM: set/reset NVM_WDG_EN bit then program the NVM

The watchdog timer duration can be set in a range from 1 s to 256 s by 1 s step by setting the WDG_TMR_SET[7:0] bit field. The default watchdog timer duration can be set in the NVM by setting NVM_WDG_TMR_SET[1:0] then programming the NVM.

Note: Each time the NVM is reloaded (typically in the CHECK&LOAD state), the NVM_WDG_EN bit is copied into the WDG_EN bit and the NVM_WDG_TMR_SET[1:0] bit field related duration is set into the WDG_TMR_SET[7:0] bit field. In the POWER_ON state, the software can override the default watchdog values (NVM) by setting the WDG_EN bit and/or the WDG_TMR_SET[7:0] bit field.

As soon as the watchdog is enabled, the software should periodically set the WDG_RST bit (self-cleared) to reload the timer downcounter WDG_TMR_CNT[7:0] with the value defined in the WDG_TMR_SET[7:0] bit field.

The software can read the watchdog timer downcounter (WDG_TMR_CNT[7:0]) to check the remaining duration before expiration.

A turn-OFF hard-fault condition occurs if the watchdog timer expires. The turn-off condition is followed by a POWER_DOWN sequence either by a PMIC restart (POWER_UP then POWER_ON) or by the PMIC going into the FAIL_SAFE_LOCK state. (See Section 5.4.5 for details about the behavior following a turn-off hard-fault event).

Enabling the watchdog (from WDG_EN = 0 to 1) to reload the timer downcounter (WDG_TMR_CNT[7:0]) with the value defined in the WDG_TMR_SET[7:0] bit field.

When enabled, the watchdog timer remains active in the POWER_ON state (in the RUN or in the STANDBY state). In all other states, the watchdog timer is frozen.

The watchdog timer can be disabled at runtime by setting WDG_EN = 0. Alternatively, the watchdog timer is automatically disabled when PMIC goes into the OFF state or the FAIL_SAFE_LOCK state (regardless of turn-OFF condition source).

When enabled (WDG_EN = 1), the watchdog timer can be suspended automatically from one PWRCTRLx signal. The WDG_PWRCTRL_SEL[1:0] bit field allows for the selection of the PWRCTRLx source to suspend the watchdog. It is suitable to automatically suspend/freeze the watchdog when the application is in low power mode:

- When PWRCTRLx is inactive (the application is running), the watchdog timer downcounter is running. The software should set the WDG_RST bit periodically to reload the timer downcounter.
- When PWRCTRLx is active (the application is in low-power mode), the watchdog timer downcounter is suspended (frozen). When PWRCTRLx becomes inactive (the application leaves the low-power mode), the watchdog downcounter restarts from the current WDG_TMR_CNT[7:0] value (counter WDG_TMR_CNT[7:0] is not reloaded from WDG_TMR_SET[7:0] value).

5.4.10.1 *Frequency spreading for buck converters*

Electromagnetic interference (EMI) is an issue prevalent to DC-DC converters, as these signals can cause disturbances to the system at large.

There are many proposed solutions to mitigate EMI, but STPMIC25 is focused on spread spectrum frequency modulation (**SSFM**). SSFM is a way to utilize PWM technology by randomly varying the switching frequency within a set range of 10 to 20% centered at the desired average 2 MHz switching frequency. This works to eliminate harsh and potentially disastrous peaks at the switching frequency.

5.5 Programming

5.5.1 I²C interface

The I²C interface works in slave mode. It supports both standard and fast modes with a data rate up to 400 Kb/s. It also supports fast mode plus (Fm+) with a data rate up to 1 Mb/s that is a suitable frequency for DVS operations.

5.5.1.1 *Device ID*

There is a device ID system to address the STPMIC25.

The address is stored in the NVM_I²C_ADDR_SHR[6:0] shadow register bit field. The hard coded I²C default address defined in the NVM is 0x33.

Table 28. Device ID format

b7	b6	b5	b4	b3	b2	b1	b0
AddID6	AddID5	AddID4	AddID3	AddID2	AddID1	AddID0	R/W

5.5.1.2 *Read/write operation*

Each transaction is composed of a start condition followed by a packet number (8-bit long) representing either a device ID plus R/W command, register address, or register data coming to/from the slave.

Table 28 An acknowledgment is needed after each packet. This acknowledgment is given by the receiver of the packet. Transaction examples are given in Table 29 and Table 30. Multi-read and multi-write operations are supported.

Table 29. Register address format

b7	b6	b5	b4	b3	b2	b1	b0
RegAdd7	RegAdd6	RegAdd5	RegAdd4	RegAdd3	RegAdd2	RegAdd1	RegAdd0

Table 30. Register data format

b7	b6	b5	b4	b3	b2	b1	b0
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Figure 20. I²C read operation

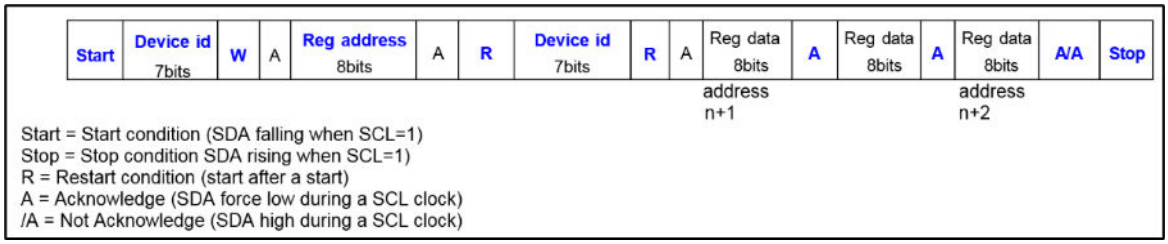
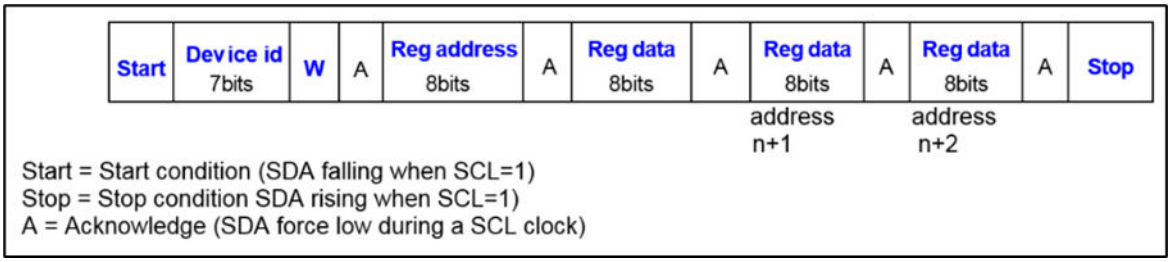


Figure 21. **I²C write operation**



5.5.2 Non-volatile memory (NVM)

The PMIC's built-in non-volatile memory provides a high flexibility to support a wide range of applications.

Its write management through I²C allows for the customization of the PMIC directly in final applications during product development and mass production.

The NVM read operation is performed automatically in the INIT&LOAD state and in the CHECK&LOAD state to set control registers with default values and configure the POWER_UP and POWER_DOWN sequence.

The NVM write operation can be performed several times (NVM_{END} cycles max) during application development debugging procedures. Once the final settings have been defined, these can be written in the NVM content of each part mounted on the customer application that is written in the production line under a controlled environment.

In addition, the PMIC supports the NVM CRC check (or checksum) to guarantee its content integrity. The CRC is computed by the PMIC during an NVM write operation. After the NVM write, the user reads back the NVM content to check that the content is OK (and implicitly that the computed CRC is valid). Then, each time the PMIC reads the NVM (in the INIT&LOAD and in the CHECK&LOAD states) if the CRC is not OK, the PMIC does not start up.

5.5.2.1 NVM read operation

The NVM read operation is fully managed by the PMIC.

For each read operation, the PMIC automatically loads the NVM content into NVM shadow registers. It means that shadow register content is a copy of NVM content.

When the PMIC power supply is connected (VIN > V_{INPOR_Rise}), the PMIC state machine goes into the INIT&LOAD state (see Section 5.1). In this state, an NVM read operation is performed to check if the PMIC can start up automatically, depending on the AUTO_TURN_ON NVM bit value.

If the AUTO_TURN_ON bit is not set, the PMIC goes into the OFF state; or, the PMIC goes into the CHECK&LOAD state and continues to POWER_UP automatically.

Before each POWER_UP sequence, the NVM read operation is performed in the CHECK&LOAD state. NVM content is loaded into shadow registers and NVM content integrity is checked with CRC. Additionally, the PMIC initializes BUCK and LDO control registers with values predefined in the NVM and it configures the POWER_UP and POWER_DOWN sequence of regulators.

5.5.2.2 *NVM write operation (PMIC customization)*

The NVM write operation can be performed by the I²C interface for customization purposes (see max cycles in NVM_{END}).

The writing procedure can be performed in two ways:

- Customizing a pre-programmed device directly from the application host processor via the I²C interface
- **NVM write operation generic sequence:**
  1. Apply VIN to the application: the PMIC goes into the POWER_ON state (1)
  2. Write NVM shadow registers with expected customization values
  3. Initiate a “NVM program operation” command - write NVM_CMD[1:0] = ‘01’
  4. Wait for the NVM write operation to be completed: wait for NVM_BUSY to become 0
  5. Check for the NVM write operation to succeed: NVM_WRITE_FAIL = 0 in NVM_SR
  6. Check new NVM content by initiating an NVM read operation: write NVM_CMD[1:0] = ‘10’ and wait for NVM_BUSY to become 0
  7. A power OFF/ON cycle is needed to load the new NVM content

  The following conditions should be fulfilled to allow an NVM write operation:
- V_{IN} must be minimum V_{NVM_PROG}

  The NVM write operation works at least in the POWER_ON state to allow the application to reprogram the NVM at runtime (via I²C). Writing into NVM shadow registers does not affect NVM content until the NVM write operation is executed.

  WARNING: If V_{IN} goes below V_{NVM_PROG} during the write operation, the NVM content integrity may be corrupted and the PMIC may not start up anymore.

1. *The PMIC has the AUTO_TURN_ON bit set by default to power up automatically. This is to allow the NVM write operation without generating turn-on conditions. (TBC)*

5.5.2.3 *I²C address:*

Special attention must be given when a new I²C address needs to be programmed.

When a different I²C address is written in NVM_I²C_ADDR_SHR, this new address becomes effective only after a “NVM write operation” after reloading the NVM (INIT&LOAD or CHECK&LOAD state).

If a “NVM write operation” is not performed following the I²C address change in the shadow register, the previously programmed I²C address is loaded from the NVM during the next POWER_UP sequence.

5.5.2.4 *LOCK_NVM write operation*

When the PMIC is customized with the LOCK_NVM bit set into the NVM_I²C_ADD_SHR followed by a programing command (NVM_CMD[1:0] = 0b01), then the NVM write operation becomes disabled immediately. Any new programing command execution is ignored and set NVM_WRITE_FAIL bit in NVM_SR.

6 Register descriptions

6.1 Register map

All NVM_xxx bits of shadow registers have related xxx mirror bits in the control registers section allowing the software to override the NVM's predefined values at runtime. Each time the NVM is reloaded, related xxx mirror bits are also reloaded with the NVM's predefined values.

All bits "reserved" in registers with R/W must not be modified.

So, before writing on a register having a "reserved" bit, the user should read the content of the register and should only modify bits that are not "reserved," then write to the register.

Hex	Register Name	R/W	BITS[7:0]							
			7	6	5	4	3	2	1	0
Status registers										
0x00	PRODUCT_ID	R	PMIC_REF_ID[3:0]				PMIC_NVM_ID[3:0]			
0x01	VERSION_SR	R	MAJOR_VERSION[3:0]				MINOR_VERSION[3:0]			
0x02	TURN_ON_SR	R	-	-	-	-	AUTO	VBUS	WKUP	PKEY
0x03	TURN_OFF_SR	R	-	-	WDG_FLT	THSDN_FLT	OCP_FLT	VIN_FLT	PKEY_FLT	SWOFF
0x04	RESTART_SR	R	-	R_RST	R_WDG_FLT	R_THSDN_FLT	R_OCP_FLT	R_VIN_FLT	R_PKEY_FLT	R_SWOFF
0x05	OCP_SR1	R	OCP_REFDDR	OCP_BUCK7	OCP_BUCK6	OCP_BUCK5	OCP_BUCK4	OCP_BUCK3	OCP_BUCK2	OCP_BUCK1
0x06	OCP_SR2	R	OCP_LDO8	OCP_LDO7	OCP_LDO6	OCP_LDO5	OCP_LDO4	OCP_LDO3	OCP_LDO2	OCP_LDO1
0x07	EN_SR1	R	EN_REFDDR	EN_BUCK7	EN_BUCK6	EN_BUCK5	EN_BUCK4	EN_BUCK3	EN_BUCK2	EN_BUCK1
0x08	EN_SR2	R	EN_LDO8	EN_LDO7	EN_LDO6	EN_LDO5	EN_LDO4	EN_LDO3	EN_LDO2	EN_LDO1
0x09	FS_CNT_SR1	R	VIN_FLT_CNT[3:0]				PKEY_FLT_CNT[3:0]			
0x0A	FS_CNT_SR2	R	THSDN_FLT_CNT[3:0]				OCP_FLT_CNT[3:0]			
0x0B	FS_CNT_SR3	R	-	-	-	-	WDG_FLT_CNT[3:0]			
0x0C	MODE_SR	R	-	-	-	OP_MODE	LDO4_VIN_SRC	PWRCTRL3	PWRCTRL2	PWRCTRL1
Control registers										
0x10	MAIN_CR	R/W	-	STANDBY_PWRCTRL[1:0]		PWRCTRL_POL[2:0]			RREQ_EN	SWOFF
0x11	VINLOW_CR	R/W	-		VINLOW_HYST[1:0]		VINLOW_RISE[2:0]			VINLOW_EN
0x12	PKEY_LKP_CR	R/W	PKEY_LKP_CONFIG[1:0]		-	-	PKEY_LKP_TMR[3:0]			
0x13	WDG_CR	R/W	-	-	-	-	WDG_PWRCTRL[1:0]		WDG_RST	WDG_EN
0x14	WDG_TMR_CR	R/W	WDG_TMR_SET[7:0]							
0x15	WDG_TMR_SR	R	WDG_TMR_CNT[7:0]							
0x16	FS_OCP_CR1	R/W	FS_OCP_REFDDR	FS_OCP_BUCK7	FS_OCP_BUCK 6	FS_OCP_BUCK5	FS_OCP_BUCK4	FS_OCP_BUCK3	FS_OCP_BUCK2	FS_OCP_BUCK1
0x17	FS_OCP_CR2	R/W	FS_OCP_LDO8	FS_OCP_LDO7	FS_OCP_LDO6	FS_OCP_LDO5	FS_OCP_LDO4	FS_OCP_LDO3	FS_OCP_LDO2	FS_OCP_LDO1
0x18	PADS_PULL_CR	R/W	PWRCTRL3_PULL[1:0]		PWRCTRL2_PULL[1:0]		PWRCTRL1_PULL[1:0]		WKUP_PU	PKEY_PU
0x19	BUCKS_PD_CR1	R/W	BUCK4_PD[1:0]		BUCK3_PD[1:0]		BUCK2_PD[1:0]		BUCK1_PD[1:0]	

Hex	Register Name	R/W	BITS[7:0]							
			7	6	5	4	3	2	1	0
Status registers										
0x1A	BUCKS_PD_CR2	R/W	-	-	BUCK7_PD[1:0]		BUCK6_PD[1:0]		BUCK5_PD[1:0]	
0x1B	LDOS_PD_CR1	R/W	LDO8_PD	LDO7_PD	LDO6_PD	LDO5_PD	LDO4_PD	LDO3_PD	LDO2_PD	LDO1_PD
0x1C	LDOS_PD_CR2	R/W	-	-	-	-	-	-	-	REFDDR_PD
0x1D	BUCKS_MRST_CR	R/W	REFDDR_MRST	BUCK7_MRST	BUCK6_MRST	BUCK5_MRST	BUCK4_MRST	BUCK3_MRST	BUCK2_MRST	BUCK1_MRST
0x1E	LDOS_MRST_CR	R/W	LDO8_MRST	LDO7_MRST	LDO6_MRST	LDO5_MRST	LDO4_MRST	LDO3_MRST	LDO2_MRST	LDO1_MRST
Spread spectrum frequency modulation										
0x1F	SSFM_CR	R/W	SSFM_EN	SSFM_CF	SSFM_DEEP[1:0]		SSFM_STEP[3:0]			
BUCKs control registers										
0x20	BUCK1_MAIN_CR1	R/W	-	VOUT[6:0]						
0x21	BUCK1_MAIN_CR2	R/W	-	-	-	-	-	PREG_MODE[1:0]		EN
0x22	BUCK1_ALT_CR1	R/W	-	VOUT[6:0]						
0x23	BUCK1_ALT_CR2	R/W	-	-	-	-	-	PREG_MODE[1:0]		EN
0x24	BUCK1_PWRCTRL_CR	R/W	PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL[1:0]		PWRCTRL_CMD[1:0]	
0x25	BUCK2_MAIN_CR1	R/W	-	VOUT[6:0]						
0x26	BUCK2_MAIN_CR2	R/W	-	-	-	-	-	PREG_MODE[1:0]		EN
0x27	BUCK2_ALT_CR1	R/W	-	VOUT[6:0]						
0x28	BUCK2_ALT_CR2	R/W	-	-	-	-	-	PREG_MODE[1:0]		EN
0x29	BUCK2_PWRCTRL_CR	R/W	PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL[1:0]		PWRCTRL_CMD[1:0]	
0x2A	BUCK3_MAIN_CR1	R/W	-	VOUT[6:0]						
0x2B	BUCK3_MAIN_CR2	R/W	-	-	-	-	-	PREG_MODE[1:0]		EN
0x2C	BUCK3_ALT_CR1	R/W	-	VOUT[6:0]						
0x2D	BUCK3_ALT_CR2	R/W	-	-	-	-	-	PREG_MODE[1:0]		EN
0x2E	BUCK3_PWRCTRL_CR	R/W	PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL[1:0]		PWRCTRL_CMD[1:0]	
0x2F	BUCK4_MAIN_CR1	R/W	-	VOUT[6:0]						
0x30	BUCK4_MAIN_CR2	R/W	-	-	-	-	-	PREG_MODE[1:0]		EN
0x31	BUCK4_ALT_CR1	R/W	-	VOUT[6:0]						
0x32	BUCK4_ALT_CR2	R/W	-	-	-	-	-	PREG_MODE[1:0]		EN
0x33	BUCK4_PWRCTRL_CR	R/W	PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL[1:0]		PWRCTRL_CMD[1:0]	
0x34	BUCK5_MAIN_CR1	R/W	-	VOUT[6:0]						
0x35	BUCK5_MAIN_CR2	R/W	-	-	-	-	-	PREG_MODE[1:0]		EN
0x36	BUCK5_ALT_CR1	R/W	-	VOUT[6:0]						
0x37	BUCK5_ALT_CR2	R/W	-	-	-	-	-	PREG_MODE[1:0]		EN
0x38	BUCK5_PWRCTRL_CR	R/W	PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL[1:0]		PWRCTRL_CMD[1:0]	
0x39	BUCK6_MAIN_CR1	R/W	-	VOUT[6:0]						

Hex	Register Name	R/W	BITS[7:0]							
			7	6	5	4	3	2	1	0
Status registers										
0x3A	BUCK6_MAIN_CR2	R/W	-	-	-	-	-	PREG_MODE[1:0]		EN
0x3B	BUCK6_ALT_CR1	R/W	-	VOUT[6:0]						
0x3C	BUCK6_ALT_CR2	R/W	-	-	-	-	-	PREG_MODE[1:0]		EN
0x3D	BUCK6_PWRCTRL_CR	R/W	PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL[1:0]		PWRCTRL_CMD[1:0]	
0x3E	BUCK7_MAIN_CR1	R/W	-	VOUT[6:0]						
0x3F	BUCK7_MAIN_CR2	R/W	-	-	-	-	-	PREG_MODE[1:0]		EN
0x40	BUCK7_ALT_CR1	R/W	-	VOUT[6:0]						
0x41	BUCK7_ALT_CR2	R/W	-	-	-	-	-	PREG_MODE[1:0]		EN
0x42	BUCK7_PWRCTRL_CR	R/W	PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL[1:0]		PWRCTRL_CMD[1:0]	
LDO control registers										
0x4C	LDO1_MAIN_CR	R/W	INPUT_SRC	-	-	-	-	-	-	EN
0x4D	LDO1_ALT_CR	R/W	INPUT_SRC	-	-	-	-	-	-	EN
0x4E	LDO1_PWRCTRL_CR	R/W	PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL[1:0]		PWRCTRL_CMD[1:0]	
0x4F	LDO2_MAIN_CR	R/W	-	BYPASS	VOUT[4:0]					EN
0x50	LDO2_ALT_CR	R/W	-	BYPASS	VOUT[4:0]					EN
0x51	LDO2_PWRCTRL_CR	R/W	PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL[1:0]		PWRCTRL_CMD[1:0]	
0x52	LDO3_MAIN_CR	R/W	SNK_SRC	BYPASS	VOUT[4:0]					EN
0x53	LDO3_ALT_CR	R/W	SNK_SRC	BYPASS	VOUT[4:0]					EN
0x54	LDO3_PWRCTRL_CR	R/W	PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL[1:0]		PWRCTRL_CMD[1:0]	
0x55	LDO4_MAIN_CR	R/W	INPUT_SRC[1:0]		-	-	-	-	-	EN
0x56	LDO4_ALT_CR	R/W	INPUT_SRC[1:0]		-	-	-	-	-	EN
0x57	LDO4_PWRCTRL_CR	R/W	PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL[1:0]		PWRCTRL_CMD[1:0]	
0x58	LDO5_MAIN_CR	R/W	-	BYPASS	VOUT[4:0]					EN
0x59	LDO5_ALT_CR	R/W	-	BYPASS	VOUT[4:0]					EN
0x5A	LDO5_PWRCTRL_CR	R/W	PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL[1:0]		PWRCTRL_CMD[1:0]	
0x5B	LDO6_MAIN_CR	R/W	-	BYPASS	VOUT[4:0]					EN
0x5C	LDO6_ALT_CR	R/W	-	BYPASS	VOUT[4:0]					EN
0x5D	LDO6_PWRCTRL_CR	R/W	PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL[1:0]		PWRCTRL_CMD[1:0]	
0x5E	LDO7_MAIN_CR	R/W	-	BYPASS	VOUT[4:0]					EN
0x5F	LDO7_ALT_CR	R/W	-	BYPASS	VOUT[4:0]					EN
0x60	LDO7_PWRCTRL_CR	R/W	PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL[1:0]		PWRCTRL_CMD[1:0]	
0x61	LDO8_MAIN_CR	R/W	-	BYPASS	VOUT[4:0]					EN

Hex	Register Name	R/W	BITS[7:0]							
			7	6	5	4	3	2	1	0
Status registers										
0x62	LDO8_ALT_CR	R/W	-	BYPASS	VOUT[4:0]					EN
0x63	LDO8_PWRCTRL_CR	R/W	PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL[1:0]		PWRCTRL_CMD[1:0]	
0x64	REFDDR_MAIN_CR	R/W	-	-	-	-	-	-	-	EN
0x65	REFDDR_ALT_CR	R/W	-	-	-	-	-	-	-	EN
0x66	REFDDR_PWRCTRL_CR	R/W	PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL[1:0]		PWRCTRL_CMD[1:0]	
Interrupt control registers										
0x70	INT_PENDING_R1	R	VBUS_RI	VBUS_FA	VINLOW_RI	VINLOW_FA	WKP_RI	WKP_FA	PKEY_RI	PKEY_FA
0x71	INT_PENDING_R2	R	-	-	-	-			THW_RI	THW_FA
0x72	INT_PENDING_R3	R	REFDDR_OC P	BUCK7_OCP	BUCK6_OCP	BUCK5_OCP	BUCK4_OCP	BUCK3_OCP	BUCK2_OCP	BUCK1_OCP
0x73	INT_PENDING_R4	R	LDO8_OCP	LDO7_OCP	LDO6_OCP	LDO5_OCP	LDO4_OCP	LDO3_OCP	LDO2_OCP	LDO1_OCP
0x74	INT_CLEAR_R1	W/R0	VBUS_ CLR[1:0]		VINLOW_ CLR[1:0]		WKP_ CLR[1:0]		PKEY_ CLR[1:0]	
0x75	INT_CLEAR_R2	W/R0	-	-	-	-	-	-	THW _CLR	
0x76	INT_CLEAR_R3	W/R0	REFDDR_OCP_CLR	BUCK7_OCP_CLR	BUCK6_OCP_CLR	BUCK5_OCP_CLR	BUCK4_OCP_CLR	BUCK3_OCP_CLR	BUCK2_OCP_CLR	BUCK1_OCP_CLR
0x77	INT_CLEAR_R4	W/R0	LDO8_OCP_CLR	LDO7_OCP_CLR	LDO6_OCP_CLR	LDO5_OCP_CLR	LDO4_OCP_CLR	LDO3_OCP_CLR	LDO2_OCP_CLR	LDO1_OCP_CLR
0x78	INT_MASK_R1	R/W	VBUS_ MASK[1:0]		VINLOW_ MASK[1:0]		WKP_MASK[1:0]		PKEY_ MASK[1:0]	
0x79	INT_MASK_R2	R/W	-	-	-	-	-	-	THW_MASK[1:0]	
0x7A	INT_MASK_R3	R/W	REFDDR_OCP_MASK	BUCK7_OCP_MASK	BUCK6_OCP_MASK	BUCK5_OCP_MASK	BUCK4_OCP_MASK	BUCK3_OCP_MASK	BUCK2_OCP_MASK	BUCK1_OCP_MASK
0x7B	INT_MASK_R4	R/W	LDO8_OCP_MASK	LDO7_OCP_MASK	LDO6_OCP_MASK	LDO5_OCP_MASK	LDO4_OCP_MASK	LDO3_OCP_MASK	LDO2_OCP_MASK	LDO1_OCP_MASK
0x7C	INT_SRC_R1	R	VBUS	!VBUS	VINLOW	!VINLOW	WKP	!WKP	PKEY	!PKEY
0x7D	INT_SRC_R2	R	-	-	-	-	-	-	THW	!THW
0x7E	INT_SRC_R3	R	REFDDR_OCP_SRC	BUCK7_OCP_SRC	BUCK6_OCP_SRC	BUCK5_OCP_SRC	BUCK4_OCP_SRC	BUCK3_OCP_SRC	BUCK2_OCP_SRC	BUCK1_OCP_SRC
0x7F	INT_SRC_R4	R	LDO1_OCP_SRC	LDO1_OCP_SRC	LDO1_OCP_SRC	LDO1_OCP_SRC	LDO1_OCP_SRC	LDO1_OCP_SRC	LDO1_OCP_SRC	LDO1_OCP_SRC
0x80	INT_DBG_LATCH_R1	W/R0	VBUS_FRC[1:0]		VINLOW_FRC[1:0]		WKP_FRC[1:0]		PKEY_FRC[1:0]	
0x81	INT_DBG_LATCH_R2	W/R0	-	-	-	-	-	-	THW_FRC[1:0]	
0x82	INT_DBG_LATCH_R3	W/R0	REFDDR_OCP_FRC	BUCK1_OCP_FRC	BUCK1_OCP_FRC	BUCK1_OCP_FRC	BUCK1_OCP_FRC	BUCK1_OCP_FRC	BUCK1_OCP_FRC	BUCK1_OCP_FRC
0x83	INT_DBG_LATCH_R4	W/R0	LDO1_OCP_FRC	LDO1_OCP_FRC	LDO1_OCP_FRC	LDO1_OCP_FRC	LDO1_OCP_FRC	LDO1_OCP_FRC	LDO1_OCP_FRC	LDO1_OCP_FRC
NVM user control registers										
0x8E	NVM_SR	R	-	-	-	-	-	-	WRITE_FAIL	BUSY

Hex	Register Name	R/W	BITS[7:0]							
			7	6	5	4	3	2	1	0
Status registers										
0x8F	NVM_CR	R/W	-	-	-	-	-	-	CMD[1:0]	
NVM user shadow registers										
0x90	NVM_MAIN_CTRL_SHR1	R/W	VINOK_HYST[1:0]		VINOK_RISE[1:0]		NVM_WDG_TMR_SET[1:0]		NVM_WDG_EN	AUTO_TURNON
0x91	NVM_MAIN_CTRL_SHR2	R/W	RANK_DLY[1:0]		RST_DLY[1:0]		NVM_PKEY_LKP_CONFIG[1:0]		NVM_PKEY_LKP_TMR[1:0]	
0x92	NVM_RANK_SHR1	R/W	-	-	BUCK2_RANK[2:0]			BUCK1_RANK[2:0]		
0x93	NVM_RANK_SHR2	R/W	-	-	BUCK4_RANK[2:0]			BUCK3_RANK[2:0]		
0x94	NVM_RANK_SHR3	R/W	-	-	BUCK6_RANK[2:0]			BUCK5_RANK[2:0]		
0x95	NVM_RANK_SHR4	R/W	-	-	REF_DDR_RANK[2:0]			BUCK7_RANK[2:0]		
0x96	NVM_RANK_SHR5	R/W	-	-	LDO2_RANK[2:0]			LDO1_RANK[2:0]		
0x97	NVM_RANK_SHR6	R/W	-	-	LDO4_RANK[2:0]			LDO3_RANK[2:0]		
0x98	NVM_RANK_SHR7	R/W	-	-	LDO6_RANK[2:0]			LDO5_RANK[2:0]		
0x99	NVM_RANK_SHR8	R/W	-	-	LDO8_RANK[2:0]			LDO7_RANK[2:0]		
0x9A	NVM_BUCK_MODE_SHR1	R/W	BUCK4_PREG_MODE[1:0]		BUCK3_PREG_MODE[1:0]		BUCK2_PREG_MODE[1:0]		BUCK1_PREG_MODE[1:0]	
0x9B	NVM_BUCK_MODE_SHR2	R/W	-	-	BUCK7_PREG_MODE[1:0]		BUCK6_PREG_MODE[1:0]		BUCK5_PREG_MODE[1:0]	
0x9C	NVM_BUCK1_VOUT_SHR	R/W	-	NVM_VOUT[6:0]						
0x9D	NVM_BUCK2_VOUT_SHR	R/W	-	NVM_VOUT[6:0]						
0x9E	NVM_BUCK3_VOUT_SHR	R/W	-	NVM_VOUT[6:0]						
0x9F	NVM_BUCK4_VOUT_SHR	R/W	-	NVM_VOUT[6:0]						
0xA0	NVM_BUCK5_VOUT_SHR	R/W	-	NVM_VOUT[6:0]						
0xA1	NVM_BUCK6_VOUT_SHR	R/W	-	NVM_VOUT[6:0]						
0xA2	NVM_BUCK7_VOUT_SHR	R/W	-	NVM_VOUT[6:0]						
0xA3	NVM_LDO2_SHR	R/W	-	NVM_BYPASS	NVM_VOUT[4:0]					-
0xA4	NVM_LDO3_SHR	R/W	SNK_RSC	NVM_BYPASS	NVM_VOUT[4:0]					-
0xA5	NVM_LDO5_SHR	R/W	-	NVM_BYPASS	NVM_VOUT[4:0]					-
0xA6	NVM_LDO6_SHR	R/W	-	NVM_BYPASS	NVM_VOUT[4:0]					-
0xA7	NVM_LDO7_SHR	R/W	-	NVM_BYPASS	NVM_VOUT[4:0]					-
0xA8	NVM_LDO8_SHR	R/W	-	NVM_BYPASS	NVM_VOUT[4:0]					-
0xA9	NVM_PD_SHR1	R/W	NVM_BUCK4_PD[1:0]		NVM_BUCK3_PD[1:0]		NVM_BUCK2_PD[1:0]		NVM_BUCK1_PD[1:0]	

Hex	Register Name	R/W	BITS[7:0]							
			7	6	5	4	3	2	1	0
Status registers										
0xAA	NVM_PD_SHR2	R/W	NVM_RDDR_PD	-	NVM_BUCK7_PD[1:0]		NVM_BUCK6_PD[1:0]		NVM_BUCK5_PD[1:0]	
0xAB	NVM_PD_SHR3	R/W	NVM_LDO8_PD	NVM_LDO7_PD	NVM_LDO6_PD	NVM_LDO5_PD	NVM_LDO4_PD	NVM_LDO3_PD	NVM_LDO2_PD	NVM_LDO1_PD
0xAC	NVM_BUCKS_IOUT_SHR1	R/W	BUCK4_ILIM[1:0]		BUCK3_ILIM[1:0]		BUCK2_ILIM[1:0]		BUCK1_ILIM[1:0]	
0xAD	NVM_BUCKS_IOUT_SHR2	R/W	HICCUP_DLY[1:0]		BUCK7_ILIM[1:0]		BUCK6_ILIM[1:0]		BUCK5_ILIM[1:0]	
0xAE	NVM_LDOS_IOUT_SHR	R/W	LDO7_ILIM[1:0]		LDO6_ILIM[1:0]		LDO5_ILIM[1:0]		LDO2_ILIM[1:0]	
0xAF	NVM_FS_OCP_SHR1	R/W	NVM_FS_OCP_REFDDR	NVM_FS_OCP_BUCK7	NVM_FS_OCP_BUCK6	NVM_FS_OCP_BUCK5	NVM_FS_OCP_BUCK4	NVM_FS_OCP_BUCK3	NVM_FS_OCP_BUCK2	NVM_FS_OCP_BUCK1
0xB0	NVM_FS_OCP_SHR2	R/W	NVM_FS_OCP_LDO8	NVM_FS_OCP_LDO7	NVM_FS_OCP_LDO6	NVM_FS_OCP_LDO5	NVM_FS_OCP_LDO4	NVM_FS_OCP_LDO3	NVM_FS_OCP_LDO2	NVM_FS_OCP_LDO1
0xB1	NVM_FS_SHR1	R/W	VIN_FLT_CNT_MAX[3:0]				PKEY_FLT_CNT_MAX[3:0]			
0xB2	NVM_FS_SHR2	R/W	TSHDN_FLT_CNT_MAX[3:0]				OCP_FLT_CNT_MAX[3:0]			
0xB3	NVM_FS_SHR3	R/W	-	FS_LOCK_DIS	RST_FLT_CNT_TMR[1:0]		WDG_FLT_CNT_MAX[3:0]			
0xB5	NVM_I²C_ADDR_SHR	R/W	LOCK_NVM	I2C_ADDR[6:0]						
0xB6	NVM_USER_SHR1	R/W	NVM_USER1[7:0]							
0xB7	NVM_USER_SHR2	R/W	NVM_USER2[7:0]							

6.2 Status registers

6.2.1 Product ID status register (PRODUCT_ID_SR)

Table 31. PRODUCT_ID_SR

7	6	5	4	3	2	1	0
PMIC_REF_ID[3:0]				PMIC_NVM_ID[3:0]			
R	R	R	R	R	R	R	R

- Address: 0x00
- Default: 0x2X (X depends on PMIC variant)
- Description: PMIC product ID status register.

[7:4]	**PMIC_REF_ID[3:0]**: PMIC family of devices 0010: STPMIC25 product family (fixed value)
[3:0]	Version A and B only 0000: Customized 0001: A 0010: B 0100: D

6.2.2 Version status register (VERSION_SR)

Table 32. **VERSION_SR**

7	6	5	4	3	2	1	0
MAJOR_VERSION[3:0]				MINOR_VERSION[3:0]			
R	R	R	R	R	R	R	R

- Address: 0x01
- Default: 0x11
- Description: PMIC version status register.

[7:4]	MAJOR_VERSION[3:0]
[3:0]	MINOR_VERSION[3:0]

6.2.3 Turn-on status register (TURN_ON_SR)

Table 33. **TURN_ON_SR**

7	6	5	4	3	2	1	0
FORCED	Reserved	Reserved	Reserved	AUTO	VBUS	WKUP	PKEY
R	R	R	R	R	R	R	R

- Address: 0x02
- Default: 0b1000xxxx where x depends on the turn-on condition
- Description: Stores last condition, which has turned-on the PMIC.

From the NO_SUPPLY state, if the AUTO_TURN_ON bit is set in the NVM, the TURN_ON_SR [AUTO] is set.

In the OFF state, the TURN_ON_SR is cleared. When a turn-on condition occurs, the related turn-on bit is set in TURN_ON_SR before leaving the OFF state. The TURN_ON_SR is cleared in the POWER_DOWN state.

[7]	**FORCED**: The PMIC turn-on condition is triggered by the DFT option 0: False 1: True
[6:4]	reserved
[3]	**AUTO**: The PMIC turn-on condition is triggered by the AUTO_TURN_ON bit in the NVM. See section Section 5.4.3.1 AUTO turn-ON. 0: False 1: True
[2]	**VBUS**: The PMIC turn-on condition is triggered by the VBUS signal. See Section 5.4.3.1 0: False 1: True
[1]	**WKUP**: The PMIC turn-on condition is triggered by the WAKEUPn signal. See Section 5.4.3.1 0: False 1: True
[0]	**PKEY**: The PMIC turn-on condition is triggered by the PONKEYn signal. See Section 5.4.3.1 0: False 1: True

6.2.4 Turn-off status register

7	6	5	4	3	2	1	0
Reserved	Reserved	WDG_FLT	TSHDN_FLT	OCP_FLT	VIN_FLT	PKEY_FLT	SWOFF
R	R	R	R	R	R	R	R

- Address: 0x03
- Default: 0b00xxxxxx where x depends on the turn-off condition
- Description: Stores last condition, which turns OFF the PMIC.

The TURN_OFF_SR register is reset in the POWER_DOWN state. Then TURN_OFF_SR is set either when going into the OFF state or when going into the FAIL_SAFE_LOCK state (see Section 5.4.4 and Section 5.1.2).

[7:6]	reserved
[5]	**WDG_FLT**: Last turn-off is due to watchdog hard-fault source while WDG_FLT_CNT > WDG_FLT_CNT_MAX. 0: False 1: True
[4]	**THSDN_FLT**: Last turn-off is due to thermal shutdown hard-fault source while TSHDN_FLT_CNT > TSHDN_FLT_CNT_MAX. 0: False 1: True
[3]	**OCP_FLT**: Last turn-off is due to regulator overcurrent hard-fault source while OCP_FLT_CNT > OCP_FLT_CNT_MAX. 0: False 1: True
[2]	**VIN_FLT**: Last turn-off is due to VIN falling below VINOK_Fall hard-fault source while VIN_FLT_CNT > VIN_FLT_CNT_MAX. (This is valid only if VIN is kept higher than VINPOR_Fall; or the PMIC fully resets) 0: False 1: True
[1]	**PKEY_FLT**: Last turn-off is due to PONKEYn long key press hard-fault source while PKEY_FLT_CNT > PKEY_FLT_CNT_MAX. 0: False 1: True
[0]	**SWOFF**: Last turn-off is due to software switch OFF (SWOFF bit set and RREQ_EN bit clear in the MAIN_CR register). 0: False 1: True

6.2.5 Restart status register (RESTART_SR)

Table 34. **RESTART_SR**

7	6	5	4	3	2	1	0
Reserved	R_RST	R_WDG_FLT	R_TSHDN_FLT	R_OCP_FLT	R_VIN_FLT	R_PKEY_FLT	R_SWOFF
R	R	R	R	R	R	R	R

- Address: 0x04
- Default: 0b0xxxxxxx where x depends on a power-OFF condition which restarts the PMIC
- Description: Stores last condition, which restarts the PMIC (power cycle).

The RESTART_SR register is reset in the POWER_DOWN state. Then RESTART_SR is set when going into the CHECK&LOAD state (see Section 5.4.4: Turn-off conditions and Section 5.1.2: State explanations).

[7]	reserved
[6]	**R_RST**: Last restart is due to RSTn pin asserted low by the application processor (or by a user reset button) 0: False 1: True
[5]	**R_WDG_FLT**: Last restart is due to watchdog hard-fault source while WDG_FLT_CNT <= WDG_FLT_CNT_MAX. 0: False 1: True
[4]	**R_TSHDN_FLT**: Last restart is due to thermal shutdown hard-fault source while TSHDN_FLT_CNT <= TSHDN_FLT_CNT_MAX. 0: False 1: True
[3]	**R_OCP_FLT**: Last restart is due to regulator overcurrent hard-fault source while OCP_FLT_CNT <= OCP_FLT_CNT_MAX. (overcurrent source is saved in OCP_SR1 or in OCP_SR2) 0: False 1: True
[2]	**R_VIN_FLT**: Last restart is due to VIN falling below V_{INOK_Fall} hard-fault source while VIN_FLT_CNT <= VIN_FLT_CNT_MAX. (This is valid only if VIN is kept higher than V_{INPOR_Fall}; or PMIC fully resets) 0: False 1: True
[1]	**R_PKEY_FLT**: Last restart is due to PONKEYn long key press hard-fault source while PKEY_FLT_CNT <= PKEY_FLT_CNT_MAX. 0: False 1: True
[0]	**R_SWOFF**: Last restart is due to a restart request from AP (setting both SWOFF bit and RREQ_EN bit in MAIN_CR register). 0: False 1: True

6.2.6 Overcurrent protection status register 1 (OCP_SR1)

Table 35. Overcurrent protection status register 1 (OCP_SR1)

7	6	5	4	3	2	1	0
OCP_REFDDR	OCP_BUCK7	OCP_BUCK6	OCP_BUCK5	OCP_BUCK4	OCP_BUCK3	OCP_BUCK2	OCP_BUCK1
R	R	R	R	R	R	R	R

- Address: 0x05
- Default: 0bxxxxxxxx where x depends on regulator that has triggered the OCP.
- Description: If the PMIC turned OFF or restarted due to an OCP from regulator, OCP_SR1 or OCP_SR2 store the regulator instance that triggered the OCP.

The OCP_SR1 register is reset in the POWER_DOWN state. If an OCP hard-fault condition occurred, then the OCP_SR1 register is set before leaving the POWER_DOWN state (see Section 5.4.9 and Section 5.4.4 and Section 5.1.2).

[7]	**OCP_REFDDR**: Last turn-off or restart is due to overcurrent protection on REFDDR. 0: False 1: True
[6]	**OCP_BUCK7**: Last turn-off or restart is due to overcurrent protection on BUCK7. 0: False 1: True
[5]	**OCP_BUCK6**: Last turn-off or restart is due to overcurrent protection on BUCK6. 0: False 1: True
[4]	**OCP_BUCK5**: Last turn-off or restart is due to overcurrent protection on BUCK5. 0: False 1: True
[3]	**OCP_BUCK4**: Last turn-off or restart is due to overcurrent protection on BUCK4. 0: False 1: True
[2]	**OCP_BUCK3**: Last turn-off or restart is due to overcurrent protection on BUCK3. 0: False 1: True
[1]	**OCP_BUCK2**: Last turn-off or restart is due to overcurrent protection on BUCK2. 0: False 1: True
[0]	**OCP_BUCK1**: Last turn-off or restart is due to overcurrent protection on BUCK1. 0: False 1: True

6.2.7 Overcurrent protection status register 2 (OCP_SR2)

7	6	5	4	3	2	1	0
OCP_LDO8	OCP_LDO7	OCP_LDO6	OCP_LDO5	OCP_LDO4	OCP_LDO3	OCP_LDO2	OCP_LDO1
R	R	R	R	R	R	R	R

- Address: 0x06
- Default: 0bxxxxxxxx where x depends on regulator that has triggered the OCP.
- Description: If the PMIC is turned OFF or is restarted due to an OCP from a regulator, OCP_SR1 or OCP_SR2 store the regulator instance that triggered the OCP.

The OCP_SR2 register is reset in the POWER_DOWN state. If an OCP hard-fault condition occurred, then the OCP_SR2 register is set before leaving the POWER_DOWN state (see Section 5.4.9 and Section 5.4.4 and Section 5.1.2).

[7]	**OCP_LDO8**: Last turn-off or restart is due to overcurrent protection on LDO8. 0: False 1: True
[6]	**OCP_LDO7**: Last turn-off or restart is due to overcurrent protection on LDO7. 0: False 1: True
[5]	**OCP_LDO6**: Last turn-off or restart is due to overcurrent protection on LDO6. 0: False 1: True
[4]	**OCP_LDO5**: Last turn-off or restart is due to overcurrent protection on LDO5. 0: False 1: True
[3]	**OCP_LDO4**: Last turn-off or restart is due to overcurrent protection on LDO4. 0: False 1: True
[2]	**OCP_LDO3**: Last turn-off or restart is due to overcurrent protection on LDO3. 0: False 1: True
[1]	**OCP_LDO2**: Last turn-off or restart is due to overcurrent protection on LDO2. 0: False 1: True
[0]	**OCP_LDO1**: Last turn-off or restart is due to overcurrent protection on LDO1. 0: False 1: True

6.2.8 Enable status register 1 (EN_SR1)

Table 36. **EN_SR1**

7	6	5	4	3	2	1	0
EN_REFDDR	EN_BUCK7	EN_BUCK6	EN_BUCK5	EN_BUCK4	EN_BUCK3	EN_BUCK2	EN_BUCK1
R	R	R	R	R	R	R	R

- Address: 0x07
- Default: 0bxxxxxxxx where x depends on regulator status (0 = disabled, 1 = enabled)
- Description: This register reflects the IP current enable status despite the setting in MAIN or ALT configurations.

[7]	**EN_REFDDR**: Current internal enable status of REFDDR. 0: Disabled 1: Enabled
[6]	**EN_BUCK7**: Current internal enable status of BUCK7. 0: Disabled 1: Enabled
[5]	**EN_BUCK6**: Current internal enable status of BUCK6. 0: Disabled 1: Enabled
[4]	**EN_BUCK5**: Current internal enable status of BUCK5. 0: Disabled 1: Enabled
[3]	**EN_BUCK4**: Current internal enable status of BUCK4. 0: Disabled 1: Enabled
[2]	**EN_BUCK3**: Current internal enable status of BUCK3. 0: Disabled 1: Enabled
[1]	**EN_BUCK2**: Current internal enable status of BUCK2. 0: Disabled 1: Enabled
[0]	**EN_BUCK1**: Current internal enable status of BUCK1. 0: Disabled 1: Enabled

6.2.9 Enable status register 2 (EN_SR2)

Table 37. **EN_SR2**

7	6	5	4	3	2	1	0
EN_LDO8	EN_LDO7	EN_LDO6	EN_LDO5	EN_LDO4	EN_LDO3	EN_LDO2	EN_LDO1
R	R	R	R	R	R	R	R

- Address: 0x08
- Default: 0bxxxxxxxx where x depends on regulator status (0 = disabled, 1 = enabled)
- Description: This register reflects the IP current enable status despite the setting in MAIN or ALT configurations.

[7]	**EN_LDO8**: Current internal enable status of LDO8. 0: Disabled 1: Enabled
[6]	**EN_LDO7**: Current internal enable status of LDO7. 0: Disabled 1: Enabled
[5]	**EN_LDO6**: Current internal enable status of LDO6. 0: Disabled 1: Enabled
[4]	**EN_LDO5**: Current internal enable status of LDO5. 0: Disabled 1: Enabled
[3]	**EN_LDO4**: Current internal enable status of LDO4. 0: Disabled 1: Enabled
[2]	**EN_LDO3**: Current internal enable status of LDO3. 0: Disabled 1: Enabled
[1]	**EN_LDO2**: Current internal enable status of LDO2. 0: Disabled 1: Enabled
[0]	**EN_LDO1**: Current internal enable status of LDO1. 0: Disabled 1: Enabled

6.2.10 Fail-safe counter status register 1 (FS_CNT_SR1)

Table 38. FS_CNT_SR1

7	6	5	4	3	2	1	0
VIN_FLT_CNT[3:0]				PKEY_FLT_CNT[3:0]			
R	R	R	R	R	R	R	R

- Address: 0x09
- Default: 0x00
- Description: Fail-safe counters store the number of hard-fault occurrences. There is one fail-safe counter by hard fault source (see Section 5.4.5). FS_CNT_SR1 is reset in the OFF state.

[7:4]	**VIN_FLT_CNT[3:0]**: number of occurrences triggered by a VIN falling below V_{INOK_Fall} hard-fault source. (This is valid only if VIN is kept higher than V_{INPOR_Fall}; or PMIC fully resets)
[3:0]	**PKEY_FLT_CNT[3:0]**: number of occurrences triggered by a PONKEYn long key press hard-fault source.

Note: When a counter (xxx_FLT_CNT[3:0]) reaches 0xF, all next counter increments keep the counter value at 0xF (and not restart to 0).

6.2.11 Fail-safe counter status register 2 (FS_CNT_SR2)

Table 39. FS_CNT_SR2

7	6	5	4	3	2	1	0
TSHDN_FLT_CNT[3:0]				OCP_FLT_CNT[3:0]			
R	R	R	R	R	R	R	R

- Address: 0x0A
- Default: 0x00
- Description: Fail-safe counters store the number of hard-fault occurrences. There is one fail-safe counter by hard fault source (see Section 5.4.5). FS_CNT_SR2 is reset in the OFF state.

[7:4]	**TSHDN_FLT_CNT[3:0]**: number of occurrences triggered by a thermal shutdown hard-fault source.
[3:0]	**OCP_FLT_CNT[3:0]**: number of occurrences triggered by regulator overcurrent hard-fault source.

Note: When a counter (xxx_FLT_CNT[3:0]) reaches 0xF, all next counter increments keep the counter value at 0xF (and not restart to 0).

6.2.12 Fail-safe counter status register 3 (FS_CNT_SR3)

Table 40. FS_CNT_SR3

7	6	5	4	3	2	1	0
reserved	reserved	reserved	reserved	WDG_FLT_CNT[3:0]			
R	R	R	R	R	R	R	R

- Address: 0x0B
- Default: 0x00
- Description: Fail-safe counters store the number of hard-fault occurrences. There is one fail-safe counter by hard fault source (see Section 5.4.5). FS_CNT_SR3 is reset in OFF state.

[7:4]	reserved
[3:0]	**WDG_FLT_CNT[3:0]**: number of occurrences triggered by watchdog hard-fault source.

Note: When a counter (xxx_FLT_CNT[3:0]) reaches 0xF, all next counter increments keep the counter value at 0xF (and not restart to 0).

6.2.13 Mode status register (MODE_SR)

Table 41. MODE_SR

7	6	5	4	3	2	1	0
Reserved[3:1]			OP_MODE	LDO4_VIN_SRC	PWRCTRL3	PWRCTRL2	PWRCTRL1
R	R	R	R	R	R	R	R

- Address: 0x0C
- Default: 0bxxxxxxxx where x depends on source state
- Description: Contains the current state of the related source.

[7:5]	Reserved
[4]	**OP_MODE**: PMIC operating state 0: PMIC operates in the RUN state 1: PMIC operates in the STANDBY state
[3]	**LDO4_VIN_SRC**: LDO4 input source. Provides status of LDO4 input switch selection (value only valid when LDO4 is enabled) 0: VIN supply selected 1: VBUS supply selected
[2]	**PWRCTRL3**: logic state of the PWRCTRL3 input (see Table 26) 0: PWRCTRL3 is active 1: PWRCTRL3 is inactive
[1]	**PWRCTRL2**: logic state of the PWRCTRL2 input (see Table 26) 0: PWRCTRL2 is active 1: PWRCTRL2 is inactive
[0]	**PWRCTRL1**: logic state of the PWRCTRL1 input(see Table 26) 0: PWRCTRL1 is active 1: PWRCTRL1 is inactive

6.3 Control registers

6.3.1 Main control register (MAIN_CR)

Table 42. **MAIN_CR**

7	6	5	4	3	2	1	0
1	STANDBY_PWRCTRL_SEL[1:0]		PWRCTRL3_POL	PWRCTRL2_POL	PWRCTRL1_POL	RREQ_EN	SWOFF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x10
- Default: 0b10000000
- Description: main control register (see Table 26). This register is initialized to the default value in the CHECK&LOAD state.

[7]	reserved: should be written to '1'
[6:5]	**STANDBY_PWRCTRL_SEL[1:0]**: Source selection to switch to the PMIC state machine in the RUN state or the STANDBY state. (only valid in the POWER_ON state) 00: No source (the PMIC operates in the RUN state) 01: PWRCTRL1 control source 10: PWRCTRL2 control source 11: PWRCTRL3 control source (PWRCTRLx inactive: RUN state; PWRCTRLx active: STANDBY state)
[4]	**PWRCTRL3_POL**: specifies PWRCTRL3 pin polarity. 0: PWRCTRL3 active low 1: PWRCTRL3 active high (see Table 26)
[3]	**PWRCTRL2_POL**: specifies PWRCTRL2 pin polarity. 0: PWRCTRL2 active low 1: PWRCTRL2 active high (see Table 26)
[2]	**PWRCTRL1_POL**: specifies PWRCTRL1 pin polarity. 0: PWRCTRL1 active low 1: PWRCTRL1 active high (see Table 26)
[1]	**RREQ_EN**: Allows the PMIC power cycle when the software switch OFF bit is (SWOFF) set. 0: PMIC goes in OFF state when SWOFF bit is set 1: PMIC performs a power cycle when the SWOFF bit is set
[0]	**SWOFF**: Software switch OFF bit. 0: no effect 1: switch-OFF requested (turn-off condition). The PMIC goes into the POWER_DOWN state immediately.

6.3.2 VINLOW monitoring control register (VINLOW_CR)

Table 43. **VINLOW_CR**

7	6	5	4	3	2	1	0
reserved	reserved	VINLOW_HYST[1:0]		VINLOW_RISE[2:0]			VINLOW_EN
R	R	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x11
- Default: 0x00
- Description: VINLOW monitoring control register (see Section 5.4.1). This register is initialized to the default value in the CHECK&LOAD state.

[7:6]	reserved
[5:4]	**VINLOW_HYST[1:0]**: VINLOW threshold hysteresis 00: 100 mV 01: 200 mV 10: 300 mV 11: 400 mV
[3:1]	**VINLOW_RISE[2:0]**: VINLOW_Rise threshold = 000: VINOK_Fall + 50 mV 001: VINOK_Fall + 100 mV 010: VINOK_Fall + 150 mV 011: VINOK_Fall + 200 mV 100: VINOK_Fall + 250 mV 101: VINOK_Fall + 300 mV 110: VINOK_Fall + 350 mV 111: VINOK_Fall + 400 mV
[0]	**VINLOW_EN**: VINLOW monitoring enable bit 0: VINLOW monitoring is disabled 1: VINLOW monitoring is enabled

6.3.3 PONKEYn long key press control register (PKEY_LKP_CR)

Table 44. **PKEY_LKP_CR**

7	6	5	4	3	2	1	0
PKEY_LKP_OFF	PKEY_LKP_FSLS	reserved	reserved	PKEY_LKP_TMR[3:0]			
R/W	R/W			R/W	R/W	R/W	R/W

- Address: 0x12
- Default: 0bXX00XXXX where X depends on the value programmed in the NVM
- Description: PONKEYn long key press control register. This register is initialized to the default value in the CHECK&LOAD state.

[7]]	**PKEY_LKP_OFF**: (see Section 5.4.4) 0: no effect 1: A PONKEYn long key press triggers a turn-off condition Default value is defined by NVM_PKEY_LKP_OFF NVM bit
[6]	**PKEY_LKP_FSLS**: (see Section 5.4.5.2) 0: no effect 1: A PONKEYn long key press allows the PMIC to go from the FAIL_SAFE_LOCK state to the OFF state Default value is defined by the NVM_PKEY_LKP_FSLS NVM bit
[5:4]	reserved
[3:0]	**PKEY_LKP_TMR[3:0]**: PONKEYn long key press timer duration 0000: 1 s 0001: 2 s 0010: 3 s 0011: 4 s 0100: 5 s 0101: 6 s 0110: 7 s 0111: 8 s 1000: 9 s 1001: 10 s 1010: 11 s 1011: 12 s 1100: 13 s 1101: 14 s 1110: 15 s 1111: 16 s Default value is defined by the NVM_PKEY_LKP_TMR[1:0] NVM bit field

6.3.4 Watchdog control register (WDG_CR)

Table 45. **WDG_CR**

7	6	5	4	3	2	1	0
reserved	reserved	reserved	reserved	WDG_PWRCTRL_SEL[1:0]		WDG_RST	WDG_EN
R	R	R	R	R/W	R/W	W/R0/SC	R/W

- Address: 0x13
- Default: 0b0000000X where X depends on the value programmed in the NVM
- Description: Watchdog control register (see Section 5.4.10). This register is initialized to the default value in the CHECK&LOAD state.

[7:4]	Reserved
[3:2]	**WDG_PWRCTRL_SEL[1:0]**: Watchdog suspends source selection. 00: No source (if WDG_EN = 1, watchdog timer always runs) 01: PWRCTRL1 WDG suspends control source 10: PWRCTRL2 WDG suspends control source 11: PWRCTRL3 WDG suspends control source When the watchdog is enabled (WDG_EN = 1): if the PWRCTRLx control source is inactive, the watchdog timer runs; if the PWRCTRLx control source is active, the watchdog timer is suspended
[1]	**WDG_RST**: watchdog timer reset 0: NA 1: Watchdog downcounter WDG_TMR_CNT[7:0] is reloaded with the value in WDG_TMR_SET[7:0] (self-cleared bit)
[0]	**WDG_EN**: watchdog enable bit 0: watchdog is disabled 1: watchdog is enabled Default value is defined by the NVM_WDG_EN NVM bit

6.3.5 Watchdog timer control register (WDG_TMR_CR)

Table 46. WDG_TMR_CR

7	6	5	4	3	2	1	0
WDG_TMR_SET[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	W/R0	R/W

- Address: 0x14
- Default: 0xXX where X depends on the value programmed in NVM
- Description: Watchdog timer control register (see Section 5.4.10). This register is initialized to the default value in the CHECK&LOAD state.

[7:0]	WDG_TMR_SET[7:0]: Watchdog timer duration settings 0x00 = 1 s 0x00 = 2 s … 0xFF= 256 s Default value is defined by the NVM_WDG_TMR_SET[1:0] NVM bit

6.3.6 Watchdog timer status register (WDG_TMR_SR)

Table 47. WDG_TMR_SR

7	6	5	4	3	2	1	0
WDG_TMR_CNT[7:0]							
R	R	R	R	R	R	R	R

- Address: 0x15
- Default: 0x00
- Description: Watchdog timer status register. Watchdog downcounter providing remaining duration (in second) before watchdog expiration.

This register is initialized to the default value in the CHECK&LOAD state.

[7:0]	**WDG_TMR_CNT[7:0]:** Watchdog timer downcounter 0xFF = 256 s … 0x01 = 2 s 0x00 = 1 s

6.3.7 Fail-safe overcurrent protection control register 1 (FS_OCP_CR1)

Table 48. **FS_OCP_CR1**

7	6	5	4	3	2	1	0
FS_OCP_REFDDR	FS_OCP_BUCK7	FS_OCP_BUCK6	FS_OCP_BUCK5	FS_OCP_BUCK4	FS_OCP_BUCK3	FS_OCP_BUCK2	FS_OCP_BUCK1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x16
- Default: 0xXX where X depends on the value programmed in the NVM
- Description: Fail-safe overcurrent protection control register 1 (see Section 5.4.9). This register is initialized to the default value in the CHECK&LOAD state.

[7]	**FS_OCP_REFDDR**: REFDDR OCP management mode selection. 0: OCP hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[6]	**FS_OCP_BUCK7**: BUCK7 OCP management mode selection. 0: OCP hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[5]	**FS_OCP_BUCK6**: BUCK6 OCP management mode selection. 0: OCP hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[4]	**FS_OCP_BUCK5**: BUCK5 OCP management mode selection. 0: OCP hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[3]	**FS_OCP_BUCK4**: BUCK4 OCP management mode selection. 0: OCP hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[2]	**FS_OCP_BUCK3**: BUCK3 OCP management mode selection. 0: OCP hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[1]	**FS_OCP_BUCK2**: BUCK2 OCP management mode selection. 0: OCP hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[0]	**FS_OCP_BUCK1**: BUCK1 OCP management mode selection. 0: OCP hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)

6.3.8 Fail-safe overcurrent protection control register 2 (FS_OCP_CR2)

Table 49. **FS_OCP_CR2**

7	6	5	4	3	2	1	0
FS_OCP_LDO8	FS_OCP_LDO7	FS_OCP_LDO6	FS_OCP_LDO5	FS_OCP_LDO4	FS_OCP_LDO3	FS_OCP_LDO2	FS_OCP_LDO1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x17
- Default: 0xXX where X depends on the value programmed in NVM
- Description: Fail-safe overcurrent protection control register 2 (see Section 5.4.9). This register is initialized to the default value in the CHECK&LOAD state.

[7]	**FS_OCP_LDO8**: LDO8 OCP management mode selection. 0: OCP hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[6]	**FS_OCP_LDO7**: LDO7 OCP management mode selection. 0: OCP hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[5]	**FS_OCP_LDO6**: LDO6 OCP management mode selection. 0: OCP hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[4]	**FS_OCP_LDO5**: LDO5 OCP management mode selection. 0: OCP hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[3]	**FS_OCP_LDO4**: LDO4 OCP management mode selection. 0: OCP hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[2]	**FS_OCP_LDO3**: LDO3 OCP management mode selection. 0: OCP hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[1]	**FS_OCP_LDO2**: LDO2 OCP management mode selection. 0: OCP hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[0]	**FS_OCP_LDO1**: LDO1 OCP management mode selection. 0: OCP hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)

6.3.9 Pads pull control register (PADS_PULL_CR)

Table 50. **PADS_PULL_CR**

7	6	5	4	3	2	1	0
PWRCTRL3_PULL[1:0]		PWRCTRL2_PULL[1:0]		PWRCTRL1_PULL[1:0]		WKUP_PU	PKEY_PU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x18
- Default: 0b01010111
- Description: Pads pull control register. This register is initialized to the default value in the CHECK&LOAD state.

[7:6]	**PWRCTRL3_PULL[1:0]**: PWRCTRL3 pad pull resistor selection. 00: no pull 01: pull-up active (R_{PU}) 10: pull-down active (R_{PD}) 11: no pull
[5:4]	**PWRCTRL2_PULL[1:0]**: PWRCTRL2 pad pull resistor selection. 00: no pull 01: pull-up active (R_{PU}) 10: pull-down active (R_{PD}) 11: no pull
[3:2]	**PWRCTRL1_PULL[1:0]**: PWRCTRL1 pad pull resistor selection. 00: no pull 01: pull-up active (R_{PU}) 10: pull-down active (R_{PD}) 11: no pull
[1]	**WKUP_PU**: WAKEUPn pull-up control. 0: no pull 1: pull-up active (R_{PU})
[0]	**PKEY_PU**: PONKEYn pull-up control. 0: no pull 1: pull-up active (R_{PU})

6.3.10 Buck pull-down control register 1 (BUCKS_PD_CR1)

Table 51. **BUCKS_PD_CR1**

7	6	5	4	3	2	1	0
BUCK4_PD[1:0]		BUCK3_PD[1:0]		BUCK2_PD[1:0]		BUCK1_PD[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x19
- Default: 0bXXXXXXXX where X depends on the value programmed in the NVM
- Description: Bucks pull-down control register 1.
  - This register is initialized to the default value in the INIT&LOAD and in the CHECK&LOAD states.

[7:6]	**BUCK4_PD[1:0]**: BUCK4 pull-down selection. 00: no pull-down 01: slow pull-down active when BUCK4 is disabled (EN = 0) 10: fast pull-down active when BUCK4 is disabled (EN = 0) 11: slow pull-down forced active
[5:4]	**BUCK3_PD[1:0]**: BUCK3 pull-down selection. 00: no pull-down 01: slow pull-down active when BUCK3 is disabled (EN = 0) 10: fast pull-down active when BUCK3 is disabled (EN = 0) 11: slow pull-down forced active
[3:2]	**BUCK2_PD[1:0]**: BUCK2 pull-down selection. 00: no pull-down 01: slow pull-down active when BUCK2 is disabled (EN = 0) 10: fast pull-down active when BUCK2 is disabled (EN = 0) 11: slow pull-down forced active
[1:0]	**BUCK1_PD[1:0]**: BUCK1 pull-down selection. 00: no pull-down 01: slow pull-down active when BUCK1 is disabled (EN = 0) 10: fast pull-down active when BUCK1 is disabled (EN = 0) 11: slow pull-down forced active

6.3.11 Buck pull-down control register 2 (BUCKS_PD_CR2)

Table 52. **BUCKS_PD_CR2**

7	6	5	4	3	2	1	0
reserved	reserved	BUCK7_PD[1:0]		BUCK6_PD[1:0]		BUCK5_PD[1:0]	
R	R	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x1A
- Default: 0bXXXXXXXX where X depends on the value programmed in the NVM
- Description: Bucks pull-down control register 2.
  - This register is initialized to the default value in the INIT&LOAD and in the CHECK&LOAD states.

[7:6]	reserved
[5:4]	**BUCK7_PD[1:0]**: BUCK7 pull-down selection. 00: no pull-down 01: slow pull-down active when BUCK7 is disabled (EN = 0) 10: fast pull-down active when BUCK7 is disabled (EN = 0) 11: slow pull-down forced active
[3:2]	**BUCK6_PD[1:0]**: BUCK6 pull-down selection. 00: no pull-down 01: slow pull-down active when BUCK6 is disabled (EN = 0) 10: fast pull-down active when BUCK6 is disabled (EN = 0) 11: slow pull-down forced active
[1:0]	**BUCK5_PD[1:0]**: BUCK5 pull-down selection. 00: no pull-down 01: slow pull-down active when BUCK5 is disabled (EN = 0) 10: fast pull-down active when BUCK5 is disabled (EN = 0) 11: slow pull-down forced active

6.3.12 LDO pull-down control register 1 (LDOS_PD_CR1)

Table 53. **LDOS_PD_CR1**

7	6	5	4	3	2	1	0
LDO8_PD	LDO7_PD	LDO6_PD	LDO5_PD	LDO4_PD	LDO3_PD	LDO2_PD	LDO1_PD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x1B
- Default: 0bXXXXXXXX where X depends on the value programmed in NVM
- Description: LDOs pull-down control register 1.
  - This register is initialized to the default value in the INIT&LOAD and in the CHECK&LOAD states.

[7]	**LDO8_PD**: 0: no pull-down 1: pull-down active when LDO8 is disabled (EN = 0)
[6]	**LDO7_PD**: 0: no pull-down 1: pull-down active when LDO7 is disabled (EN = 0)
[5]	**LDO6_PD**: 0: no pull-down 1: pull-down active when LDO6 is disabled (EN = 0)
[4]	**LDO5_PD**: 0: no pull-down 1: pull-down active when LDO5 is disabled (EN = 0)
[3]	**LDO4_PD**: 0: no pull-down 1: pull-down active when LDO4 is disabled (EN = 0)
[2]	**LDO3_PD**: 0: no pull-down 1: pull-down active when LDO3 is disabled (EN = 0)
[1]	**LDO2_PD**: 0: no pull-down 1: pull-down active when LDO2 is disabled (EN = 0)
[0]	**LDO1_PD**: 0: no pull-down 1: pull-down active when LDO1 is disabled (EN = 0)

6.3.13 LDO pull-down control register 2 (LDOS_PD_CR2)

7	6	5	4	3	2	1	0
reserved	reserved	reserved	reserved	reserved	reserved	reserved	REFDDR_PD
R	R	R	R	R	R	R	R/W

- Address: 0x1C
- Default: 0b0000000X where X depends on the value programmed in NVM
- Description: LDOs pull-down control register 2.

This register is initialized to the default value in the INIT&LOAD and in the CHECK&LOAD states.

[7:1]	reserved
[0]	**REFDDR_PD**: 0: no pull-down 1: pull-down active when REFDDR is disabled (EN = 0)

6.3.14 Mask reset buck control register (BUCKS_MRST_CR)

7	6	5	4	3	2	1	0
REFDDR_MRST	BUCK7_MRST	BUCK6_MRST	BUCK5_MRST	BUCK4_MRST	BUCK3_MRST	BUCK2_MRST	BUCK1_MRST
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x1D
- Default: 0x00
- Description: mask reset buck control register.

See Section 5.4.7.1. This register is initialized to the default value in the CHECK&LOAD state.

[7]	**REFDDR_MRST**: mask reset setting 0: inactive 1: active
[6]	**BUCK7_MRST**: mask reset setting 0: inactive 1: active
[5]	**BUCK6_MRST**: mask reset setting 0: inactive 1: active
[4]	**BUCK5_MRST**: mask reset setting 0: inactive 1: active
[3]	**BUCK4_MRST**: mask reset setting 0: inactive 1: active
[2]	**BUCK3_MRST**: mask reset setting 0: inactive 1: active
[1]	**BUCK2_MRST**: mask reset setting 0: inactive 1: active
[0]	**BUCK1_MRST**: mask reset setting 0: inactive 1: active

6.3.15 Mask reset buck control register (BUCKS_MRST_CR)

Table 54. **LDOS_MRST_CR**

7	6	5	4	3	2	1	0
LDO8_MRST	LDO7_MRST	LDO6_MRST	LDO5_MRST	LDO4_MRST	LDO3_MRST	LDO2_MRST	LDO1_MRST
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x1E
- Default: 0x00
- Description: mask reset LDO control register.

See Section 5.4.7.1. This register is initialized to the default value in the CHECK&LOAD state.

[7]	**LDO8_MRST**: mask reset setting 0: inactive 1: active
[6]	**LDO7_MRST**: mask reset setting 0: inactive 1: active
[5]	**LDO6_MRST**: mask reset setting 0: inactive 1: active
[4]	**LDO5_MRST**: mask reset setting 0: inactive 1: active
[3]	**LDO4_MRST**: mask reset setting 0: inactive 1: active
[2]	**LDO3_MRST**: mask reset setting 0: inactive 1: active
[1]	**LDO2_MRST**: mask reset setting 0: inactive 1: active
[0]	**LDO1_MRST**: mask reset setting 0: inactive 1: active

6.4 Spread spectrum control register (SSMOD_CR)

7	6	5	4	3	2	1	0
SSFM_EN	SSFM_CFG	SSFM_DEEP[1:0]		SSFM_STEP[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- ADDRESS: 0x1F
- DEFAULT: 0x00
- DESCRIPTION: spread spectrum frequency modulation control register.
- This register is initialized to the default value in the CHECK&LOAD state; writable in the POWER_ON state only.

[7]	**SSFM_EN**: Spread-spectrum frequency modulation enabled. 0: inactive 1: active
[6]	**SSFM_CFG**: Spread-spectrum frequency modulation waveform shape. 0: triangular 1: sawtooth
[5:4]	**SSFM_DEEP**: Spread-spectrum frequency modulation analog parameter configuration.
[3:0]	**SSFM_STEP[3:0]**: Spread-spectrum frequency modulation period. Triangular modulation: (SSMOD_STEP+1)*30 µs Sawtooth modulation: (SSMOD_STEP+1)*16 µs

6.5 Power supply control registers

6.5.1 BUCKx MAIN mode control register 1 (BUCKx_MAIN_CR1) (x = 1 to 7)

7	6	5	4	3	2	1	0
reserved	VOUT[6:0]						
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x20/0x25/0x2A/0x2F/0x34/0x39/0x3E
- Default: 0b0XXXXXXX where X depends on the value programmed in the NVM
- Description: BUCK1 to BUCK7 MAIN mode control register 1.

This register is initialized to the default value in the CHECK&LOAD state. The user can write to these registers to set the voltage of BUCKx, which is applied to the MAIN mode (see Section 5.4.6 and 0 BUCKconverter).

[7]	reserved
[6:0]	VOUT[6:0]: Buck output voltage settings. See Table 25. BUCK output voltage settings. The default value is defined in the BUCKx_VOUT[2:0] bit field of NVM_BUCKs_VOUT_SHRx NVM shadow registers.

6.5.2 BUCKx MAIN mode control register 2 (BUCKx_MAIN_CR2) (x = 1 to 7)

Table 55. BUCKx_MAIN_CR2

7	6	5	4	3	2	1	0
reserved	reserved	reserved	reserved	reserved	PREG_MODE[1:0]		EN
R	R	R	R	R	R/W	R/W	R/W

- Address: 0x21/0x26/0x2B/0x30/0x35/0x3A/0x3F
- Default: 0b00000XXX where X depends on the value programmed in NVM
- Description: BUCK1 to BUCK7 MAIN mode control register 2.

This register is initialized to the default value in the CHECK&LOAD state. The user can write to these registers to control the enable and regulation modes of BUCKx, which are applied to the MAIN mode (see Section 5.4.6 and 0 BUCKconverter).

[7:3]	reserved
[2:1	**PREG_MODE**: select regulation mode 00: BUCKx operates in high power mode (HP) 01: BUCKx operates in low power mode (LP) 10: BUCKx operates in forced PWM mode (CCM) 11: reserved
[0]	**EN**: 0: BUCKx is disabled 1: BUCKx is enabled The default value is defined in the BUCKx_RANK[2:0] bit field of NVM_BUCKs_RANK_SHR NVM shadow registers. If BUCKx_RANK[2:0] = 0, BUCKx is disabled at power up; if BUCKx_RANK[2:0] = y (with 6 > y > 0) BUCKx is enabled at power up at rank y (see Section 5.2)

6.5.3 BUCKx ALTERNATE mode control register 1 (BUCKx_ALT_CR1) (x = 1 to 7)

Table 56. BUCKx_ALT_CR1

7	6	5	4	3	2	1	0
reserved	VOUT[6:0]						
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x22/0x27/0x2C/0x31/0x36/0x3B/0x40
- Default: 0b0XXXXXXX where X depends on the value programmed in NVM
- Description: BUCK1 to BUCK7 ALT mode control register 1.

This register is initialized to the default value in the CHECK&LOAD state. The user can write to these registers to set the voltage of BUCKx, which is applied to the ALTERNALTE mode (see Section 5.4.6 and 0 BUCKconverter).

[7]	reserved
[6:0]	**VOUT[6:0]**: Buck output voltage settings. See Table 20 The default value is the same as BUCKx_MAIN_CR1

6.5.4 BUCKx ALTERNATE mode control register 2 (BUCKx_ALT_CR2) (x = 1 to 7)

Table 57. BUCKx_ALT_CR2

7	6	5	4	3	2	1	0
reserved	reserved	reserved	reserved	reserved	PREG_MODE[1:0]		EN
R	R	R	R	R	R/W	R/W	R/W

- Address: 0x23/0x28/0x2D/0x32/0x37/0x3C/0x41
- Default: 0b00000XXX where X depends on the value programmed in NVM
- Description: BUCK1 to BUCK7 ALTERNATE mode control register 2.

This register is initialized to the default value in the CHECK&LOAD state. The user can write to these registers to control the enable and regulation modes of BUCKx, which are applied to the ALTERNATE mode (see Section 5.4.6 and 0 BUCK converter).

[7:3]	reserved
[2:1]	**PREG_MODE[1:0]**: select regulation mode 00: BUCKx operates in high power mode (HP) 01: BUCKx operates in low power mode (LP) 10: BUCKx operates in forced PWM mode (CCM) 11: Reserved
[0]	**EN**: 0: BUCKx is disabled 1: BUCKx is enabled The default value is the same as BUCKx_MAIN_CR2

6.5.5 BUCKx PWRCTRL control register (BUCKx_PWRCTRL_CR) (x = 1 to 7)

Table 58. BUCKx_PWRCTRL_CR

7	6	5	4	3	2	1	0
PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL[1:0]		PWRCTRL_RST	PWRCTRL_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x24/0x29/0x2E/0x33/0x38/0x3D/0x42
- Default: 0x00
- Description: BUCK1 to BUCK7 PWRCTRL control register.

This register is initialized to the default value in the CHECK&LOAD state. The user can write to these registers to allocate a PWRCTRL signal for controlling the BUCKx (see Section 5.4.6).

[7:6]	**PWRCTRL_DLY_H[1:0]**: BUCKx control/reset source shift delay from low to **H**igh level 00: no delay 01: 1.5 ms delay 10: 3 ms delay 11: 6 ms delay
[5:4]	**PWRCTRL_DLY_L[1:0]**: BUCKx control/reset source shift delay from high to **L**ow level 00: no delay 01: 1.5 ms delay 10: 3 ms delay 11: 6 ms delay
[3:2]	**PWRCTRL_SEL[1:0]**: BUCKx control/reset PWRCTRL source selection 00: No control source 01: PWRCTRL1 control source 10: PWRCTRL2 control source 11: PWRCTRL3 control source
[1]	**PWRCTRL_RST**: BUCKx independent reset source enable 0: no effect 1: reset enable (when the selected PWRCTRL source is active, BUCKx is disabled and the BUCKx control registers are reset to the default value. When the selected PWRCTRL source is inactive, BUCKx operates according to BUCKx_MAIN_CR1 / 2. See Table 27).
[0]	**PWRCTRL_EN**: BUCKx control source enable 0: disable (BUCKx operates according to BUCKx_MAIN_CR1 / 2) 1: enable (BUCKx operates according to BUCKx_MAIN_CR1 / 2 or BUCKx_ALT_CR1 / 2 depending on the PWRCTRL selected source. See Table 27).

6.5.6 LDOx MAIN mode control register (LDOx_MAIN_CR) (x = 2/5/6/7/8)

Table 59. LDOx_MAIN_CR

7	6	5	4	3	2	1	0
reserved	BYPASS	VOUT[4:0]					EN
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x4F/0x58/0x5B/0x5E/0x61
- Default: 0b0XXXXXXX where X depends on the value programmed in NVM
- Description: LDO2/LDO5/LDO6/LDO7/LDO8 MAIN mode control register.

This register is initialized to the default value in the CHECK&LOAD state. The user can write to these registers to control enable, bypass mode, and set the voltage of the related LDO instance which is applied to the MAIN mode (see Section 5.4.6

[7]	reserved
[6]	**BYPASS**: select bypass mode operation 0: LDOx operates in normal mode 1: LDOx operates in bypass mode The default value is defined by the BYPASS bit of the NVM_LDOx_SHR NVM shadow register
[5:1]	**VOUT[4:0]**: LDOx output voltage settings. See Section 4.2.6 The default value is defined in the VOUT[4:0] bit field of NVM_LDOx_SHR NVM shadow registers
[0]	**EN**: 0: LDOx is disabled 1: LDOx is enabled The default value is defined in the LDOx_RANK[2:0] bit field of the NVM_LDOs_RANK_SHR NVM shadow registers. If LDOx_RANK[2:0] = 0, LDOx is disabled at power up; if LDOx_RANK[2:0] = y (with 6 > y > 0) LDOx is enabled at power up at rank y (see Section 5.2)

6.5.7 LDOx ALTERNATE mode control register (LDOx_ALT_CR) (x = 2/5/6/7/8)

Table 60. LDOx_ALT_CR

7	6	5	4	3	2	1	0
reserved	BYPASS	VOUT[4:0]					EN
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x50/0x59/0x5C/0x5F/0x62
- Default: 0b0XXXXXXX where X depends on the value programmed in the NVM
- Description: LDO2/LDO5/LDO6/LDO7/LDO8 ALTERNATE mode control register.

This register is initialized to the default value in the CHECK&LOAD state. The user can write to these registers to control enable, bypass mode, and set the voltage of the related LDO instance, which is applied to the ALTERNATE mode (see Section 5.4.6.

[7]	reserved
[6]	**BYPASS**: select bypass mode operation 0: LDOx operates in normal mode 1: LDOx operates in bypass mode The default value is the same as LDOx_MAIN_CR
[5:1]	**VOUT[4:0]**: LDOx output voltage settings. See Section 4.2.6 The default value is the same as LDOx_MAIN_CR
[0]	**EN**: 0: LDOx is disabled 1: LDOx is enabled The default value is the same as LDOx_MAIN_CR

6.5.8 LDOx PWRCTRL control register (LDOx_PWRCTRL_CR) (x = 1 to 8)

Table 61. LDOx_PWRCTRL_CR

7	6	5	4	3	2	1	0
PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL[1:0]		PWRCTRL_RST	PWRCTRL_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x4E/0x51/0x54/0x57/0x5A/0x5D/0x60/0x63
- Default: 0x00
- Description: LDO1 to LDO8 PWRCTRL control register.

This register is initialized to the default value in the CHECK&LOAD state. The user can write to these registers to allocate a PWRCTRL signal for controlling the LDOx (see Section 5.4.6).

[7:6]	**PWRCTRL_DLY_H[1:0]**: LDOx control/reset source shift delay from low to **H**igh level 00: no delay 01: 1.5 ms delay 10: 3 ms delay 11: 6 ms delay
[5:4]	**PWRCTRL_DLY_L[1:0]**: LDOx control/reset source shift delay from high to **L**ow level 00: no delay 01: 1.5 ms delay 10: 3 ms delay 11: 6 ms delay
[3:2]	**PWRCTRL_SEL[1:0]**: LDOx control/reset PWRCTRL source selection. 00: No control source 01: PWRCTRL1 control source 10: PWRCTRL2 control source 11: PWRCTRL3 control source
[1]	**PWRCTRL_RST**: LDOx independent reset source enable 0: no effect 1: reset enable (when the selected PWRCTRL source is active, LDOx is disabled and LDOx control registers are reset to the default value. When the selected PWRCTRL source is inactive, LDOx operates according to LDOx_MAIN_CR. See Table 27).
[0]	**PWRCTRL_EN**: LDOx control source enable 0: disable (LDOx operates according to LDOx_MAIN_CR) 1: enable (LDOx operates according to LDOx_MAIN_CR or LDOx_ALT_CR depending on the PWRCTRL selected source. See Table 27).

6.5.9 LDO1 MAIN mode control register (LDO1_MAIN_CR)

Table 62. LDO1_MAIN_CR

7	6	5	4	3	2	1	0
INPUT_SRC	reserved	reserved	reserved	reserved	reserved	reserved	EN
R/W	R	R	R	R	R	R	R/W

- Address: 0x4C
- Default: 0b0000000X where X depends on the value programmed in the NVM
- Description: LDO1 MAIN mode control register.

This register is initialized to the default value in the CHECK&LOAD state. The user can write to these registers to control enable LDO1, which is applied to the MAIN mode (see Section 5.4.6.

[7]	**INPUT_SRC**: 0: LDO12IN as source 1: VOUT4 as source
[6:1]	reserved
[0]	**EN**: 0: LDO1 is disabled 1: LDO1 is enabled The default value is defined in the LDO1_RANK[2:0] bit field of the NVM_LDOs_RANK_SHR1 NVM shadow registers. If LDO1_RANK[2:0] = 0, LDO1 is disabled at power up; if LDO1_RANK[2:0] = y (with 6 > y > 0) LDO1 is enabled at power up at rank y (see Section 5.2)

6.5.10 LDO1 ALTERNATE mode control register (LDO1_ALT_CR)

Table 63. LDO1_ALT_CR

7	6	5	4	3	2	1	0
INPUT_SRC	reserved	reserved	reserved	reserved	reserved	reserved	EN
R/W	R	R	R	R	R	R	R/W

- Address: 0x4D
- Default: 0b0000000X where X depends on the value programmed in the NVM
- Description: LDO1 ALTERNATE mode control register.

This register is initialized to the default value in the CHECK&LOAD state. The user can write to these registers to control enable LDO1, which is applied to the ALTERNATE mode (see Section 5.4.6.

[7]	**INPUT_SRC**: 0: LDO12IN as source 1: VOUT4 as source
[6:1]	reserved
[0]	**EN**: 0: LDO1 is disabled 1: LDO1 is enabled The default value is the same as LDO1_MAIN_CR

6.5.11 LDO3 MAIN mode control register (LDO3_MAIN_CR)

Table 64. LDO3_MAIN_CR

7	6	5	4	3	2	1	0
SNK_SRC	BYPASS	VOUT[4:0]					EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x52
- Default: 0bXXXXXXXX where X depends on the value programmed in the NVM
- Description: LDO3 MAIN mode control register.

This register is initialized to the default value in the CHECK&LOAD state. The user can write to these registers to control enable, bypass mode or SNK_SRC mode, and set the voltage of LDO3, which is applied to the MAIN mode (see Section 5.4.6.

[7]	**SNK_SRC**: select sink/source mode operation (see Section 4.2.3) 0: LDO3 operates in normal or bypass mode 1: LDO3 operates in sink/source mode The default value is defined by the SNK_SRC bit of the NVM_LDO3_SHR NVM shadow register Note: the SNK_SRC bit has higher priority than the BYPASS mode operation (in the case that both bits are set at the same time)
[6]	**BYPASS**: select bypass mode operation 0: LDO3 operates in normal mode 1: LDO3 operates in bypass mode The default value is defined by the BYPASS bit of the NVM_LDO3_SHR NVM shadow register
[5:1]	**VOUT[4:0]**: LDO3 output voltage settings. See Section 4.2.6 The default value is defined in the VOUT[4:0] bit field of the NVM_LDO3_SHR NVM shadow registers
[0]	**EN**: 0: LDO3 is disabled 1: LDO3 is enabled The default value is defined in the LDO3_RANK[2:0] bit field of the NVM_LDOs_RANK_SHR2 NVM shadow registers. If LDO3_RANK[2:0] = 0, LDO3 is disabled at power up; if LDO3_RANK[2:0] = y (with 6 > y > 0) LDO3 is enabled at power up at rank y (see Section 5.2)

6.5.12 LDO3 ALTERNATE mode control register (LDO3_ALT_CR)

Table 65. LDO3_ALT_CR

7	6	5	4	3	2	1	0
SNK_SRC	BYPASS	VOUT[4:0]					EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x53
- Default: 0bXXXXXXXX where X depends on the value programmed in the NVM
- Description: LDO3 ALTERNATE mode control register.

This register is initialized to the default value in the CHECK&LOAD state. The user can write to these registers to control enable, bypass mode or SNK_SRC mode, and set the voltage of LDO3, which is applied to the ALTERNATE mode (see Section 5.4.6).

[7]	**SNK_SRC**: select sink/source mode operation (see Section 4.2.3) 0: LDO3 operates in sink/source mode 1: LDO3 operates in sink/source mode The default value is the same as LDO3_MAIN_CR Note: SNK_SRC bit has a higher priority than the BYPASS mode operation (in case both bits are set at the same time)
[6]	**BYPASS**: select bypass mode operation 0: LDO3 operates in normal mode 1: LDO3 operates in bypass mode The default value is the same as LDO3_MAIN_CR
[5:1]	**VOUT[4:0]**: LDO3 output voltage settings. See Section 4.2.6 The default value is the same as LDO3_MAIN_CR
[0]	**EN**: 0: LDO3 is disabled 1: LDO3 is enabled The default value is the same as LDO3_MAIN_CR

6.5.13 LDO4 MAIN mode control register (LDO4_MAIN_CR)

Table 66. LDO4_MAIN_CR

7	6	5	4	3	2	1	0
INPUT_SRC[1:0]		reserved	reserved	reserved	reserved	reserved	EN
R/W	R/W	R	R	R	R	R	R/W

- Address: 0x55
- Default: 0b0000000X where X depends on the value programmed in the NVM
- Description: LDO4 MAIN mode control register.

This register is initialized to the default value in the CHECK&LOAD state. The user can write to these registers to control enable or to force the power input source of LDO4, which is applied to the MAIN mode (see Section 5.4.6).

[7:6]	**INPUT_SRC[1:0]**: force power input source 00: automatic input source selection (the higher voltage is automatically selected) 01: supply input source is VIN 10: supply input source is VBUS 11: automatic input source selection (the higher voltage is automatically selected)
[5:1]	reserved
[0]	**EN**: 0: LDO4 is disabled 1: LDO4 is enabled The default value is defined in the LDO4_RANK[2:0] bit field of the NVM_LDOs_RANK_SHR2 NVM shadow registers. If LDO4_RANK[2:0] = 0, LDO4 is disabled at power-up. If LDO4_RANK[2:0] = y (with 6 > y > 0), LDO4 is enabled at power-up at rank y (see Section 5.2)

6.5.14 LDO4 ALTERNATE mode control register (LDO4_ALT_CR)

Table 67. **LDO4_ALT_CR**

7	6	5	4	3	2	1	0
INPUT_SRC[1:0]		reserved	reserved	reserved	reserved	reserved	EN
R/W	R/W	R	R	R	R	R	R/W

- Address: 0x56
- Default: 0b0000000X where X depends on the value programmed in the NVM
- Description: LDO4 ALTERNATE mode control register.

This register is initialized to the default value in the CHECK&LOAD state. The user can write to these registers to control enable or to force the power input source of LDO4, which is applied to the ALTERNATE mode (see Section 5.4.6).

[7:6]	**INPUT_SRC[1:0]**: force power input source 00: automatic input source selection (the higher voltage is automatically selected) 01: supply input source is VIN 10: supply input source is VBUS 11: automatic input source selection (the higher voltage is automatically selected)
[5:1]	reserved
[0]	**EN**: 0: LDO4 is disabled 1: LDO4 is enabled The default value is the same as LDO4_MAIN_CR

6.5.15 REFDDR MAIN mode control register (REFDDR_MAIN_CR)

Table 68. REFDDR_MAIN_CR

7	6	5	4	3	2	1	0
reserved	reserved	reserved	reserved	reserved	reserved	reserved	EN
R	R	R	R	R	R	R	R/W

- Address: 0x64
- Default: 0b0000000X where X depends on the value programmed in the NVM
- Description: REFDDR MAIN mode control register.

This register is initialized to the default value in the CHECK&LOAD state. The user can write to these registers to control enable REFDDR, which is applied to the MAIN mode (see Section 5.4.6).

[7:1]	reserved
[0]	**EN**: 0: REFDDR is disabled 1: REFDDR is enabled The default value is defined in the REFDDR_RANK[2:0] bit field of the NVM_LDOs_RANK_SHR5 NVM shadow registers. If REFDDR_RANK[2:0] = 0, REFDDR is disabled at power-up. If REFDDR_RANK[2:0] = y (with 6 > y > 0), REFDDR is enabled at power-up at rank y (see Section 5.2)

6.5.16 REFDDR ALTERNATE mode control register (REFDDR_ALT_CR)

Table 69. REFDDR_ALT_CR

7	6	5	4	3	2	1	0
reserved	reserved	reserved	reserved	reserved	reserved	reserved	EN
R	R	R	R	R	R	R	R/W

- Address: 0x65
- Default: 0b0000000X where X depends on the value programmed in the NVM
- Description: REFDDR ALTERNATE mode control register.

This register is initialized to the default value in the CHECK&LOAD state. The user can write to these registers to control enable REFDDR, which is applied to the ALTERNATE mode (see Section 5.4.6).

[7:1]	reserved
[0]	**EN**: 0: REFDDR is disabled 1: REFDDR is enabled The default value is the same as REFDDR_MAIN_CR

6.5.17 REFDDR PWRCTRL control register (REFDDR_PWRCTRL_CR)

Table 70. **REFDDR_PWRCTRL_CR**

7	6	5	4	3	2	1	0
PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL[1:0]		PWRCTRL_RST	PWRCTRL_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x66
- Default: 0x00
- Description: REFDDR PWRCTRL control register.

This register is initialized to the default value in the CHECK&LOAD state. The user can write to these registers to allocate a PWRCTRL signal for controlling the REFDDR (see Section 5.4.6).

[7:6]	**PWRCTRL_DLY_H[1:0]**: REFDDR control/reset source shift delay from low to **H**igh level 00: no delay 01: 1.5 ms delay 10: 3 ms delay 11: 6 ms delay
[5:4]	**PWRCTRL_DLY_L[1:0]**: REFDDR control/reset source shift delay from high to **L**ow level 00: no delay 01: 1.5 ms delay 10: 3 ms delay 11: 6 ms delay
[3:2]	**PWRCTRL_SEL[1:0]**: REFDDR control/reset PWRCTRL source selection 00: No control source 01: PWRCTRL1 control source 10: PWRCTRL2 control source 11: PWRCTRL3 control source
[1]	**PWRCTRL_RST**: REFDDR independent reset source enable 0: no effect 1: reset enable (when the selected PWRCTRL source is active, REFDDR is disabled, and REFDDR control registers are reset to the default value. When the selected PWRCTRL source is inactive, REFDDR operates according to REFDDR_MAIN_CR. See Table 27)
[0]	**PWRCTRL_EN**: REFDDR control source enable 0: disable (REFDDR operates according to REFDDR_MAIN_CR) 1: enable (REFDDR operates according to REFDDR_MAIN_CR or REFDDR_ALT_CR depending on the PWRCTRL selected source. See Table 27)

6.6 Interrupt registers

6.6.1 Interrupt management overview

Interrupts are probed in the POWER_ON state only. All interrupts are masked by default. All interrupt registers are reset to the default value as long as RSTn is asserted.

- **INT_PENDING_Rx**
  - Stores events of interrupt sources, regardless if the interrupts are masked or not masked.
  - Corresponding bits are kept set until they are cleared (using INT_CLEAR_Rx registers).
- **INT_CLEAR_Rx**
  - Setting a bit in these registers clears the corresponding pending bit in the INT_PENDING_Rx registers. A bit in the INT_PENDING_Rx registers can be cleared only if the corresponding interrupt source disappears. Alternatively, the bit stays set after being cleared. In the case of the INT_PENDING_Rx bit generated by edge triggering, they can be directly deleted without checking the INT_SOURCE_RX.
- **INT_MASK_Rx**
  - Clearing a bit in these registers unmasks the corresponding interrupt.
  - The INTn pin is forced low as long as the corresponding interrupt bit is set in INT_PENDING_Rx.
- **INT_SOURCE_Rx**
  - These registers provide the actual state of interrupt sources.
  - If an interrupt source is present, the corresponding bit is set. If the interrupt source disappears, the corresponding bit is cleared.
- **INT_DBG_LATCH_Rx**
  - Setting a bit in these registers emulates the corresponding interrupt event. These registers aim to test and to debug the application processor software interrupt handler.

6.6.2 Interrupt pending register 1 (INT_PENDING_R1)

Table 71. INT_PENDING_R1

7	6	5	4	3	2	1	0
VBUS_RI	VBUS_FA	VINLOW_RI	VINLOW_FA	WKP_RI	WKP_FA	PKEY_RI	PKEY_FA
R	R	R	R	R	R	R	R

- Address: 0x70
- Default: 0x00
- Description: Interrupt pending register 1 (see Section 6.6.1).

This register is reset to the default value as long as RSTn is asserted.

For all bits:

0: interrupt not pending

1: interrupt pending

[7]	**VBUS_RI**: Voltage on the VBUS pin rises above the V_{BUS_Rise} threshold
[6]	**VBUS_FA**: Voltage on the VBUS pin falls below the V_{BUS_Fall} threshold
[5]	**VINLOW_RI**: Voltage on the VIN pin falls below the V_{INLOW_Rise} threshold
[4]	**VINLOW_FA**: Voltage on the VIN pin rises above the V_{INLOW_Fall} threshold
[3]	**WKP_RI**: WAKEUP rising edge
[2]	**WKP_FA**: WAKEUP falling edge
[1]	**PKEY_RI**: PONKEYn rising edge
[0]	**PKEY_FA**: PONKEYn falling edge

6.6.3 Interrupt pending register 2 (INT_PENDING_R2)

Table 72. INT_PENDING_R2

7	6	5	4	3	2	1	0
reserved	reserved	reserved	reserved	reserved	reserved	THW_RI	THW_FA
R	R	R	R	R	R	R	R

- Address: 0x78
- Default: 0x00
- Description: Interrupt pending register 2 (see Section 6.6.1).

This register is reset to the default value as long as RSTn is asserted.
For all bits:
0: interrupt not pending
1: interrupt pending

[7:2]	reserved
[1]	**THW_RI**: Temperature rises above the T_{WRN_Rise} threshold
[0]	**THW_FA**: Temperature fall below the T_{WRN_Fall} threshold

6.6.4 Interrupt pending register 3 (INT_PENDING_R3)

Table 73. INT_PENDING_R3

7	6	5	4	3	2	1	0
REFDDR_OCP	BUCK7_OCP	BUCK6_OCP	BUCK5_OCP	BUCK4_OCP	BUCK3_OCP	BUCK2_OCP	BUCK1_OCP
R	R	R	R	R	R	R	R

- Address: 0x72
- Default: 0x00
- Description: Interrupt pending register 3 (see Section 6.6.1).

This register is reset to the default value as long as RSTn is asserted.
For all bits:
0: interrupt not pending
1: interrupt pending

[7]	**REFDDR_OCP**: Overcurrent detected on REFDDR
[6]	**BUCK7_OCP**: Overcurrent detected on BUCK7
[5]	**BUCK6_OCP**: Overcurrent detected on BUCK6
[4]	**BUCK5_OCP**: Overcurrent detected on BUCK5
[3]	**BUCK4_OCP**: Overcurrent detected on BUCK4
[2]	**BUCK3_OCP**: Overcurrent detected on BUCK3
[1]	**BUCK2_OCP**: Overcurrent detected on BUCK2
[0]	**BUCK1_OCP**: Overcurrent detected on BUCK1

6.6.5 Interrupt pending register 4 (INT_PENDING_R4)

Table 74. INT_PENDING_R4

7	6	5	4	3	2	1	0
LDO8_OCP	LDO7_OCP	LDO6_OCP	LDO5_OCP	LDO4_OCP	LDO3_OCP	LDO2_OCP	LDO1_OCP
R	R	R	R	R	R	R	R

- Address: 0x73
- Default: 0x00
- Description: Interrupt mask register 1 to 4 (see Section 6.6.1).

This register is reset to the default value as long as RSTn is asserted.
For all bits:
0: interrupt not pending
1: interrupt pending

[7]	**LDO8_OCP**: Overcurrent detected on LDO8
[6]	**LDO7_OCP**: Overcurrent detected on LDO7
[5]	**LDO6_OCP**: Overcurrent detected on LDO6
[4]	**LDO5_OCP**: Overcurrent detected on LDO5
[3]	**LDO4_OCP**: Overcurrent detected on LDO4
[2]	**LDO3_OCP**: Overcurrent detected on LDO3
[1]	**LDO2_OCP**: Overcurrent detected on LDO2
[0]	**LDO1_OCP**: Overcurrent detected on LDO1

6.6.6 Interrupt clear registers (INT_CLEAR_Rx) (x = 1 to 4)

Table 75. INT_CLEAR_Rx

7	6	5	4	3	2	1	0
Same as INT_PENDING_Rx							
W/R0	W/R0	W/R0	W/R0	W/R0	W/R0	W/R0	W/R0

- Address: 0x74/0x75/0x76/0x77
- Default: 0x00
- Description: Interrupt clear registers 1 to 4 (see Section 6.6.1).

Writing 1 clears the corresponding interrupt bit in INT_PENDING_Rx. The bit is self-cleared, and always reads 0.

6.6.7 Interrupt mask registers (INT_MASK_Rx) (x = 1 to 4)

Table 76. INT_MASK_Rx

7	6	5	4	3	2	1	0
Same as INT_PENDING_Rx							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x78/0x79/0x7A/0x7B
- Default: 0xFF
- Description: Interrupt clear registers 1 to 4 (see Section 6.6.1).

Writing 0 unmasks the corresponding interrupt bit in INT_PENDING_Rx. These registers are reset to the default value as long as RSTn is asserted.

For all bits:

0: interrupt is unmasked

1: interrupt is masked

6.6.8 Interrupt source registers (INT_SRC_Rx) (x = 1 to 4)

Table 77. INT_SRC_Rx

7	6	5	4	3	2	1	0
Same as INT_PENDING_Rx							
R	R	R	R	R	R	R	R

- Address: 0x7C/0x7D/0x7E/0x7F
- Default: 0xXX (where X depends on the actual state of interrupt sources)
- Description: Interrupt source registers 1 to 4 (see Section 6.6.1).

For all bits:

0: interrupt source is not present

1: interrupt source is present

6.6.9 Interrupt debug latch registers (INT_DBG_LATCH_Rx) (x = 1 to 4)

Table 78. INT_DBG_LATCH_Rx

7	6	5	4	3	2	1	0
Same as INT_PENDING_Rx							
W/R0	W/R0	W/R0	W/R0	W/R0	W/R0	W/R0	W/R0

- Address: 0x80/0x81/0x82/0x83
- Default: 0x00
- Description: Interrupt debug latch registers 1 to 4 (see Section 6.6.1).

Setting a bit emulates the corresponding interrupt event. The bit is self-cleared, and always reads 0.

6.7 NVM registers

6.7.1 NVM status register (NVM_SR)

Table 79. NVM_SR

7	6	5	4	3	2	1	0
reserved	reserved	reserved	reserved	reserved	reserved	NVM_WRITE_FAIL	NVM_BUSY
R	R	R	R	R	R	R	R

- Address: 0x8E
- Default: 0x00
- Description: NVM status register.

[7:2	reserved
[1]	**NVM_WRITE_FAIL**: Error in writing to the NVM. The LOCK_NVM bit is set. 0: Write is successful or no write operation done 1: Write to the NVM failed
[0]	**NVM_BUSY**: NVM controller status 0: NVM controller is in an idle state 0: NVM controller is in an idle state 1: NVM controller is in a busy state Self-cleared when the operation is completed

6.7.2 NVM control register (NVM_CR)

Table 80. **NVM_CR**

7	6	5	4	3	2	1	0
reserved	reserved	reserved	reserved	reserved	reserved	NVM_CMD[1:0]	
R	R	R	R	R	R	R/W	R/W

- Address: 0x8F
- Default: 0x00
- Description: NVM control register.

[7:2]	reserved
[1:0]	**NVM_CMD[1:0]**: NVM controller command bits to control the NVM operation on the NVM shadow register bits. 00: No operation 01: Program (write shadow register to the NVM) 10: Read (load NVM content into shadow register) 11: No operation

6.8 NVM shadow registers

All NVM shadow registers are reloaded from the NVM content in the INIT&LOAD state and in the CHECK&LOAD state. Then mirror registers or mirror bit fields (in Section 6.3 and Section 6.5) are set to the default value.

6.8.1 NVM main control shadow register 1 (NVM_MAIN_CTRL_SHR1)

Table 81. NVM_MAIN_CTRL_SHR1

7	6	5	4	3	2	1	0
VINOK_HYST[1:0]		VINOK_RISE[1:0]		NVM_WDG_TMR_SET[1:0]		NVM_WDG_EN	AUTO_TURN_ON
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x90
- Default: Depends on the PMIC part number
- Description: NVM main control shadow register 1.

[7:6]	**VINOK_HYST[1:0]**: V_{INOK_HYST} threshold voltage 00: 200 mV 01: 300 mV 10: 400 mV 11: 500 mV
[5:4]	**VINOK_RISE[1:0]**: V_{INOK_Rise} threshold voltage 00: 3.1 V 01: 3.3 V 10: 3.5 V 11: 4.0 V
[3:2]	**NVM_WDG_TMR_SET [1:0]**: watchdog timer duration default value 00: 10 s 01: 20 s 10: 50 s 11: 100 s
[1]	**NVM_WDG_EN**: watchdog default value 0: Watchdog is disabled 1: Watchdog is enabled
[0]	**AUTO_TURN_ON**: 0: PMIC does not start automatically on VIN rising 1: PMIC starts automatically on VIN rising

6.8.2 NVM main control shadow register 2 (NVM_MAIN_CTRL_SHR2)

Table 82. NVM_MAIN_CTRL_SHR2

7	6	5	4	3	2	1	0
RANK_DLY[1:0]		RST_DLY[1:0]		NVM_PKEY_LKP_OFF	NVM_PKEY_LKP_FSLS	NVM_PKEY_LKP_TMR[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0x91
Default: Depends on the PMIC part number
Description: NVM main control shadow register 2.

[7:6]	**RANK_DLY[1:0]**: power-up/power-down step (RANK) duration: 00: 1.5 ms 01: 3 ms 10: 4.5 ms 11: 6 ms (see Section 5.2)
[5:4]	**RST_DLY[1:0]**: RST release delay after POWER_UP sequence: 00: no delay 01: 1.5 ms 10: 3 ms 11: 6 ms (see Section 5.2)
[3]	**NVM_PKEY_LKP_OFF**: PONKEYn long key press turn-off condition default value (see Section 5.4.4) 0: no effect 1: A PONKEYn long key press triggers a turn-off condition
[2]	**NVM_PKEY_LKP_FSLS**: PONKEYn long key press fail-safe lock state skipping default value (see Section 5.4.5.2) 0: no effect 1: A PONKEYn long key press allows the PMIC to go from the FAIL_SAFE_LOCK state to the OFF state
[1:0]	**NVM_PKEY_LKP_TMR[1:0]**: PONKEYn long key press timer duration default value 00: 2 s 01: 5 s 10: 10 s 11: 15 s

6.8.3 NVM rank shadow register 1 (NVM_RANK_SHR1)

Table 83. NVM_RANK_SHR1

7	6	5	4	3	2	1	0
reserved	reserved	BUCK2_RANK[2:0]			BUCK1_RANK[2:0]		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x92
- Default: Depends on the PMIC part number
- Description: NVM rank shadow register 1 (see section Section 5.2).

[7:6]	reserved
[5:3]	**BUCK2_RANK[2:0]**: 000: rank0 001: rank1 010: rank2 011: rank3 100: rank4 101: rank5 110: rank0 111: rank0
[2:0]	**BUCK1_RANK[2:0]**: 000: rank0 001: rank1 010: rank2 011: rank3 100: rank4 101: rank5 110: rank0 111: rank0

6.8.4 NVM rank shadow register 2 (NVM_RANK_SHR2)

Table 84. NVM_RANK_SHR2

7	6	5	4	3	2	1	0
reserved	reserved	BUCK4_RANK[2:0]			BUCK3_RANK[2:0]		
R	R	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x93
- Default: Depends on the PMIC part number
- Description: NVM rank shadow register 2.

Same bit field as section *6.7.3 NVM rank shadow register 1 (NVM_RANK_SHR1).*

6.8.5 NVM rank shadow register 3 (NVM_RANK_SHR3)

Table 85. NVM_RANK_SHR3

7	6	5	4	3	2	1	0
reserved	reserved	BUCK6_RANK[2:0]			BUCK5_RANK[2:0]		
R	R	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x94
- Default: Depends on the PMIC part number
- Description: NVM rank shadow register 3.

Same bit field as Section 6.8.3

6.8.6 NVM rank shadow register 4 (NVM_RANK_SHR4)

Table 86. NVM_RANK_SHR4

7	6	5	4	3	2	1	0
reserved	reserved	reserved	REFDDR_RANK[2:0]		BUCK7_RANK[2:0]		
R	R	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x95
- Default: Depends on the PMIC part number
- Description: NVM rank shadow register 4 (see Section 5.2).

[7:6]	reserved
[5:3]	**REFDDR_RANK[2:0]**: 000: rank0 001: rank1 010: rank2 011: rank3 100: rank4 101: rank5 110: rank0 111: rank0
[2:0]	**BUCK7_RANK[2:0]**: 000: rank0 001: rank1 010: rank2 011: rank3 100: rank4 101: rank5 110: rank0 111: rank0

6.8.7 NVM rank shadow register 5 (NVM_RANK_SHR5)

Table 87. **NVM_RANK_SHR5**

7	6	5	4	3	2	1	0
reserved	reserved	LDO2_RANK[2:0]			LDO1_RANK[2:0]		
R	R	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0x96
Default: Depends on the PMIC part number
Description: NVM rank shadow register 5 (see Section 5.2).

[7:6]	reserved
[5:3]	**LDO2_RANK[2:0]**: 000: rank0 001: rank1 010: rank2 011: rank3 100: rank4 101: rank5 110: rank0 111: rank0
[2:0]	**LDO1_RANK[2:0]**: 000: rank0 001: rank1 010: rank2 011: rank3 100: rank4 101: rank5 110: rank0 111: rank0

6.8.8 NVM rank shadow register 6 (NVM_RANK_SHR6)

Table 88. NVM_ RANK_SHR6

7	6	5	4	3	2	1	0
reserved	reserved	LDO4_RANK[2:0]			LDO3_RANK[2:0]		
R	R	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x97
- Default: Depends on the PMIC part number
- Description: NVM rank shadow register 6.

Same bit field as Section 6.8.7.

6.8.9 NVM rank shadow register 7 (NVM_RANK_SHR7)

Table 89. NVM_RANK_SHR7

7	6	5	4	3	2	1	0
reserved	reserved	LDO6_RANK[2:0]			LDO5_RANK[2:0]		
R	R	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0x98
Default: Depends on the PMIC part number
Description: NVM rank shadow register 7.
Same bit field as Section 6.8.7

6.8.10 NVM rank shadow register 8 (NVM_RANK_SHR8)

Table 90. NVM_RANK_SHR8

7	6	5	4	3	2	1	0
reserved	reserved	LDO8_RANK[2:0]			LDO7_RANK[2:0]		
R	R	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0x99
Default: Depends on the PMIC part number
Description: NVM rank shadow register 8.
Same bit field as section Section 6.8.7.

6.8.11 NVM BUCK mode shadow register 1 (NVM_BUCK_MODE_SHR1)

Table 91. NVM_BUCK_MODE_SHR1

7	6	5	4	3	2	1	0
BUCK4_PREG_MODE[1:0		BUCK3_PREG_MODE[1:0		BUCK2_PREG_MODE[1:0		BUCK1_PREG_MODE[1:0	
R/W		R/W		R/W		R/W	

- Address: 0x9A
- Default: Depends on the PMIC part number
- Description: NVM BUCK mode shadow register 1 (see Section 5.2).

[7:6]	**BUCK4_PREG_MODE[1:0]:** 00: BUCK4 operates in high power mode (HP) 01: BUCK4 operates in low power mode (LP) 10: BUCK4 operates in forced PWM mode (CCM) 11: reserved
[5:4]	**BUCK3_PREG_MODE[1:0]:** 00: BUCK3 operates in high power mode (HP) 01: BUCK3 operates in low power mode (LP) 10: BUCK3 operates in forced PWM mode (CCM) 11: reserved
[3:2]	**BUCK2_PREG_MODE[1:0]:** 00: BUCK2 operates in high power mode (HP) 01: BUCK2 operates in low power mode (LP) 10: BUCK2 operates in forced PWM mode (CCM) 11: reserved
[1:0]	**BUCK1_PREG_MODE[1:0]:** 00: BUCK1 operates in high power mode (HP) 01: BUCK1 operates in low power mode (LP) 10: BUCK1 operates in forced PWM mode (CCM) 11: reserved

6.8.12 NVM BUCK mode shadow register 2 (NVM_BUCK_MODE_SHR2)

Table 92. NVM_BUCK_MODE_SHR2

7	6	5	4	3	2	1	0
reserved	reserved	BUCK7_PREG_MODE[1:0		BUCK6_PREG_MODE[1:0		BUCK5_PREG_MODE[1:0	
R/W	R/W	R/W		R/W		R/W	

- Address: 0x9B
- Default: Depends on the PMIC part number
- Description: NVM BUCK mode shadow register 2 (see Section 5.2).

[7:6]	reserved
[5:4]	**BUCK7_PREG_MODE[1:0]:** 00: BUCK7 operates in high power mode (HP) 01: BUCK7 operates in low power mode (LP) 10: BUCK7 operates in forced PWM mode (CCM) 11: reserved
[3:2]	**BUCK6_PREG_MODE[1:0]:** 00: BUCK6 operates in high power mode (HP) 01: BUCK6 operates in low power mode (LP) 10: BUCK6 operates in forced PWM mode (CCM) 11: reserved
[1:0]	**BUCK5_PREG_MODE[1:0]:** 00: BUCK5 operates in high power mode (HP) 01: BUCK5 operates in low power mode (LP) 10: BUCK5 operates in forced PWM mode (CCM) 11: reserved

6.8.13 NVM BUCKx output voltage shadow register (NVM_BUCKx_VOUT_SHR) (x = 1 to 7)

Table 93. NVM_BUCKx_VOUT_SHR

7	6	5	4	3	2	1	0
reserved	VOUT[6:0]						
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x9C to 0xA2
- Default: Depends on the PMIC part number
- Description: NVM BUCK1 to BUCK7 output voltage shadow registers.

The contents of these registers are copied into BUCKx_MAIN_CR1 and BUCKx_ALT_CR1 in the CHECK&LOAD state (see Section 4.3.2).

[7]	reserved
[6:0]	**VOUT[6:0]:** BUCKx default output voltage settings. See Table 20.

6.8.14 NVM LDOx shadow register (NVM_LDOx_SHR) (x = 2/5/6/7/8)

Table 94. NVM_LDOx_SHR

7	6	5	4	3	2	1	0
reserved	BYPASS	VOUT[4:0]					reserved
R	R/W	R/W	R/W	R/W	R/W	R/W	R

- Address: 0xA3/A5 to 0xA8
- Default: Depends on the PMIC part number
- Description: NVM LDO2/LDO5/LDO6/LDO7/LDO8 control shadow registers.

The contents of these registers are copied into LDOx_MAIN_CR and LDOx_ALT_CR in the CHECK&LOAD state (see Section 4.2.6).

[7]	reserved
[6]	**BYPASS:** select default bypass mode operation: 0: LDOx operates in normal mode by default 1: LDOx operates in bypass mode by default
[5:1]	**VOUT[4:0]**: LDOx default output voltage settings. See Section 4.2.6.
[0]	reserved

6.8.15 NVM LDO3 control shadow register (NVM_LDO3_SHR)

Table 95. NVM_LDO3_SHR

7	6	5	4	3	2	1	0
reserved	BYPASS	VOUT[4:0]					reserved
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0xA4
- Default: Depends on the PMIC part number
- Description: NVM LDO3 control shadow register.

The content of this register is copied into LDO3_MAIN_CR and LDO3_ALT_CR in the CHECK&LOAD state (see Section 4.2.6).

[7]	**reserved**
[6]	**BYPASS:** select default bypass mode operation: 0: LDOx operates in normal mode by default 1: LDOx operates in bypass mode by default
[5:1]	**VOUT[4:0]**: LDOx default output voltage settings. See Table 19.
[0]	**reserved**

6.8.16 NVM pull-down control shadow register 1 (NVM_PD_SHR1)

Table 96. **NVM_PD_SHR1**

7	6	5	4	3	2	1	0
BUCK4_PD[1:0]		BUCK3_PD[1:0]		BUCK2_PD[1:0]		BUCK1_PD[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0xA9
- Default: Depends on the PMIC part number
- Description: NVM pull-down control shadow register 1.

The content of this register is copied into BUCKS_PD_CR1 in the INIT&LOAD and the CHECK&LOAD states.

[7:6]	**BUCK4_PD[1:0]**: BUCK4 pull-down selection. 00: no pull-down 01: slow pull-down active when BUCK4 is disabled (EN = 0) 10: fast pull-down active when BUCK4 is disabled (EN = 0) 11: slow pull-down forced active
[5:4]	**BUCK3_PD[1:0]**: BUCK3 pull-down selection. 00: no pull-down 01: slow pull-down active when BUCK3 is disabled (EN = 0) 10: fast pull-down active when BUCK3 is disabled (EN = 0) 11: slow pull-down forced active
[3:2]	**BUCK2_PD[1:0]**: BUCK2 pull-down selection. 00: no pull-down 01: slow pull-down active when BUCK2 is disabled (EN = 0) 10: fast pull-down active when BUCK2 is disabled (EN = 0) 11: slow pull-down forced active
[1:0]	**BUCK1_PD[1:0]**: BUCK1 pull-down selection. 00: no pull-down 01: slow pull-down active when BUCK1 is disabled (EN = 0) 10: fast pull-down active when BUCK1 is disabled (EN = 0) 11: slow pull-down forced active

6.8.17 NVM pull-down control shadow register 2 (NVM_PD_SHR2)

Table 97. NVM_PD_SHR2

7	6	5	4	3	2	1	0
REFDDR_PD	reserved	BUCK7_PD[1:0]		BUCK6_PD[1:0]		BUCK5_PD[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0xAA
- Default: Depends on the PMIC part number
- Description: NVM pull-down control shadow register 2.

The content of this register is copied into BUCKS_PD_CR2 in the INIT&LOAD and the CHECK&LOAD states.

[7]	**REFDDR_PD**: 0: no pull-down 1: pull-down active when REFDDR is disabled (EN = 0)
[6]	reserved
[5:4]	**BUCK7_PD[1:0]**: BUCK7 pull-down selection. 00: no pull-down 01: slow pull-down active when BUCK7 is disabled (EN = 0) 10: fast pull-down active when BUCK7 is disabled (EN = 0) 11: slow pull-down forced active
[3:2]	**BUCK6_PD[1:0]**: BUCK6 pull-down selection. 00: no pull-down 01: slow pull-down active when BUCK6 is disabled (EN = 0) 10: fast pull-down active when BUCK6 is disabled (EN = 0) 11: slow pull-down forced active
[1:0]	**BUCK5_PD[1:0]**: BUCK5 pull-down selection. 00: no pull-down 01: slow pull-down active when BUCK5 is disabled (EN = 0) 10: fast pull-down active when BUCK5 is disabled (EN = 0) 11: slow pull-down forced active

6.8.18 NVM pull-down control shadow register 3 (NVM_PD_SHR3)

Table 98. NVM_PD_SHR3

7	6	5	4	3	2	1	0
LDO8_PD	LDO7_PD	LDO6_PD	LDO5_PD	LDO4_PD	LDO3_PD	LDO2_PD	LDO1_PD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0xAB
- Default: Depends on the PMIC part number
- Description: NVM pull-down control shadow register 3.

The content of this register is copied into LDOS_PD_CR1 in the INIT&LOAD and the CHECK&LOAD states.

[7]	**LDO8_PD**: 0: no pull-down 1: pull-down active when LDO8 is disabled (EN = 0)
[6]	**LDO7_PD**: 0: no pull-down 1: pull-down active when LDO7 is disabled (EN = 0)
[5]	**LDO6_PD**: 0: no pull-down 1: pull-down active when LDO6 is disabled (EN = 0)
[4]	**LDO5_PD**: 0: no pull-down 1: pull-down active when LDO5 is disabled (EN = 0)
[3]	**LDO4_PD**: 0: no pull-down 1: pull-down active when LDO4 is disabled (EN = 0)
[2]	**LDO3_PD**: 0: no pull-down 1: pull-down active when LDO3 is disabled (EN = 0)
[1]	**LDO2_PD**: 0: no pull-down 1: pull-down active when LDO2 is disabled (EN = 0)
[0]	**LDO1_PD**: 0: no pull-down 1: pull-down active when LDO1 is disabled (EN = 0)

6.8.19 NVM BUCKs output current limitation shadow register 1 (NVM_BUCKS_IOUT_SHR1)

Table 99. **NVM_BUCKS_IOUT_SHR1**

7	6	5	4	3	2	1	0
BUCK4_ILIM[1:0]		BUCK3_ILIM[1:0]		BUCK2_ILIM[1:0]		BUCK1_ILIM[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0xAC
- Default: Depends on the PMIC part number
- Description: NVM BUCKs output current limitation shadow register 1.

[7:6]	**BUCK4_ILIM[1:0]**: output current limitation 00: 250 mA 01: 500 mA 10: 500 mA 11: 500 mA
[5:4]	**BUCK3_ILIM[1:0]**: output current limitation 00: 500 mA 01: 1000 mA 10: 1500 mA 11: 2000 mA
[3:2]	**BUCK2_ILIM[1:0]**: output current limitation 00: 500 mA 01: 1000 mA 10: 1500 mA 11: 2000 mA
[1:0]	**BUCK1_ILIM[1:0]**: output current limitation 00: 500 mA 01: 1000 mA 10: 1500 mA 11: 2000 mA

6.8.20 NVM BUCKs output current limitation shadow register 2 (NVM_BUCKS_IOUT_SHR2)

Table 100. NVM_BUCKS_IOUT_SHR2

7	6	5	4	3	2	1	0
HICCUP_DLY[1:0]		BUCK7_ILIM[1:0]		BUCK6_ILIM[1:0]		BUCK5_ILIM[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0xAD
- Default: Depends on the PMIC part number
- Description: NVM BUCKs output current limitation shadow register 2.

[7:6]	**HICCUP_DLY[1:0]**: output current limitation 00: 0 ms 01: 100 ms 10: 500 ms 11: 1000 ms
[5:4]	**BUCK7_ILIM[1:0]**: output current limitation 00: 1000 mA 01: 1500 mA 10: 2000 mA 11: 2500 mA
[3:2]	**BUCK6_ILIM[1:0]**: output current limitation 00: 500 mA 01: 1000 mA 10: 1500 mA 11: 2000 mA
[1:0]	**BUCK5_ILIM[1:0]**: output current limitation 00: 250 mA 01: 500 mA 10: 500 mA 11: 500 mA

6.8.21 NVM LDOs output current limitation shadow register (NVM_LDOS_IOUT_SHR)

Table 101. **NVM_LDOS_IOUT_SHR**

7	6	5	4	3	2	1	0
LDO7_ILIM[1:0]		LDO6_ILIM[1:0]		LDO5_ILIM[1:0]		LDO2_ILIM[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0xAE
- Default: Depends on the PMIC part number
- Description: NVM LDOs output current limitation shadow register.

[7:6]	**LDO7_ILIM[1:0]**: output current limitation 00: 50 mA 01: 100 mA 10: 200 mA 11: 400 mA
[5:4]	**LDO6_ILIM[1:0]**: output current limitation 00: 50 mA 01: 100 mA 10: 200 mA 11: 400 mA
[3:2]	**LDO5_ILIM[1:0]**: output current limitation 00: 50 mA 01: 100 mA 10: 200 mA 11: 400 mA
[1:0]	**LDO2_ILIM[1:0]**: output current limitation 00: 50 mA 01: 100 mA 10: 200 mA 11: 400 mA

6.8.22 NVM fail-safe overcurrent protection shadow register 1 (NVM_FS_OCP_SHR1)

Table 102. NVM_FS_OCP_SHR1

7	6	5	4	3	2	1	0
NVM_FS_OCP_REFDDR	NVM_FS_OCP_BUCK7	NVM_FS_OCP_BUCK6	NVM_FS_OCP_BUCK5	NVM_FS_OCP_BUCK4	NVM_FS_OCP_BUCK3	NVM_FS_OCP_BUCK2	NVM_FS_OCP_BUCK1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0xAF
- Default: Depends on the PMIC part number
- Description: NVM fail-safe overcurrent protection shadow register 1 (see Section 5.4.9).

[7]	**NVM_FS_OCP_REFDDR**: REFDDR OCP management mode selection. 0: OCP Hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[6]	**NVM_FS_OCP_BUCK7**: BUCK7 OCP management mode selection. 0: OCP Hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[5]	**NVM_FS_OCP_BUCK6**: BUCK6 OCP management mode selection. 0: OCP Hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[4]	**NVM_FS_OCP_BUCK5**: BUCK5 OCP management mode selection. 0: OCP Hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[3]	**NVM_FS_OCP_BUCK4**: BUCK4 OCP management mode selection. 0: OCP Hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[2]	**NVM_FS_OCP_BUCK3**: BUCK3 OCP management mode selection. 0: OCP Hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[1]	**NVM_FS_OCP_BUCK2**: BUCK2 OCP management mode selection. 0: OCP Hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[0]	**NVM_FS_OCP_BUCK1**: BUCK1 OCP management mode selection. 0: OCP Hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)

6.8.23 NVM fail-safe overcurrent protection shadow register 2 (NVM_FS_OCP_SHR2)

Table 103. **NVM_FS_OCP_SHR2**

7	6	5	4	3	2	1	0
NVM_FS_OCP_L_DO8	NVM_FS_OCP_L_DO7	NVM_FS_OCP_L_DO6	NVM_FS_OCP_L_DO5	NVM_FS_OCP_L_DO4	NVM_FS_OCP_L_DO3	NVM_FS_OCP_L_DO2	NVM_FS_OCP_L_DO1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0xB0
- Default: Depends on the PMIC part number
- Description: NVM fail-safe overcurrent protection shadow register 2 (see Section 5.4.9).

[7]	**NVM_FS_OCP_LDO8**: LDO8 OCP management mode selection. 0: OCP Hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[6]	**NVM_FS_OCP_LDO7**: LDO7 OCP management mode selection. 0: OCP Hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[5]	**NVM_FS_OCP_LDO6**: LDO6 OCP management mode selection. 0: OCP Hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[4]	**NVM_FS_OCP_LDO5**: LDO5 OCP management mode selection. 0: OCP Hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[3]	**NVM_FS_OCP_LDO4**: LDO4 OCP management mode selection. 0: OCP Hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[2]	**NVM_FS_OCP_LDO3**: LDO3 OCP management mode selection. 0: OCP Hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[1]	**NVM_FS_OCP_LDO2**: LDO2 OCP management mode selection. 0: OCP Hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[0]	**NVM_FS_OCP_LDO1**: LDO1 OCP management mode selection. 0: OCP Hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)

6.8.24 NVM fail-safe shadow register 1 (NVM_FS_SHR1)

Table 104. NVM_FS_SHR1

7	6	5	4	3	2	1	0
VIN_FLT_CNT_MAX[3:0]				PKEY_FLT_CNT_MAX[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0xB1
- Default: Depends on the PMIC part number
- Description: NVM fail-safe shadow register 1 (see Section 5.4.5).

[7:4]	**VIN_FLT_CNT_MAX[3:0]**: setting of the maximum number of occurrences triggered by a VIN falling below V_{INOK_Fall} hard-fault source. 0000: 0 hard-faults allowed (PMIC goes in FAIL_SAFE_LOCK_STATE when the 1st hard-fault condition occurs) 0001: 1 hard-fault allowed (the PMIC goes in FAIL_SAFE_LOCK_STATE when the 2nd hard-fault condition occurs) … 1110: 14 hard-faults allowed (the PMIC goes in FAIL_SAFE_LOCK_STATE when the 15th hard-fault condition occurs) 1111: ∞ hard-faults allowed (fail-safe disabled: the PMIC always restarts when the hard-fault condition occurs)
[3:0]	**PKEY_FLT_CNT_MAX[3:0]**: setting of the maximum number of occurrences triggered by a PONKEYn long key press hard-fault source. 0000: 0 hard-faults allowed (the PMIC goes in FAIL_SAFE_LOCK_STATE when the 1st hard-fault condition occurs) 0001: 1 hard-fault allowed (the PMIC goes in FAIL_SAFE_LOCK_STATE when the 2nd hard-fault condition occurs) … 1110: 14 hard-faults allowed (the PMIC goes in FAIL_SAFE_LOCK_STATE when the 15th hard-fault condition occurs) 1111: ∞ hard-faults allowed (fail-safe disabled: the PMIC always restarts when a hard-fault condition occurs)

6.8.25 NVM fail-safe shadow register 2 (NVM_FS_SHR2)

Table 105. **NVM_FS_SHR2**

7	6	5	4	3	2	1	0
TSHDN_FLT_CNT_MAX[3:0]				OCP_FLT_CNT_MAX[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0xB2
- Default: Depends on the PMIC part number
- Description: NVM fail-safe shadow register 2 (see Section 5.4.5).

[7:4]	**TSHDN_FLT_CNT_MAX[3:0]**: setting of the maximum number of occurrences triggered by a thermal shutdown hard-fault source. 0000: 0 hard-faults allowed (the PMIC goes in FAIL_SAFE_LOCK_STATE when the 1st hard-fault condition occurs) 0001: 1 hard-fault allowed (the PMIC goes in FAIL_SAFE_LOCK_STATE when the 2nd hard-fault condition occurs) … 1110: 14 hard-faults allowed (the PMIC goes in FAIL_SAFE_LOCK_STATE when the 15th hard-fault condition occurs) 1111: ∞ hard-faults allowed (fail-safe disabled: the PMIC always restarts when a hard-fault condition occurs)
[3:0]	**OCP_FLT_CNT_MAX[3:0]**: setting of the maximum number of occurrences triggered by regulator overcurrent hard-fault source. 0000: 0 hard-faults allowed (the PMIC goes in FAIL_SAFE_LOCK_STATE when the 1st hard-fault condition occurs) 0001: 1 hard-fault allowed (the PMIC goes in FAIL_SAFE_LOCK_STATE when the 2nd hard-fault condition occurs) … 1110: 14 hard-faults allowed (the PMIC goes in FAIL_SAFE_LOCK_STATE when the 15th hard-fault condition occurs) 1111: ∞ hard-faults allowed (fail-safe disabled: the PMIC always restarts when a hard-fault condition occurs)

6.8.26 NVM fail-safe shadow register 3 (NVM_FS_SHR3)

Table 106. **NVM_FS_SHR3**

7	6	5	4	3	2	1	0
reserved	FAIL_SAFE_LOCK_DIS	RST_FLT_CNT_TMR[1:0]		WDG_FLT_CNT_MAX[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0xB3
- Default: Depends on the PMIC part number
- Description: NVM fail-safe shadow register 3 (see Section 5.4.5).

[7]	reserved
[6]	**FAIL_SAFE_LOCK_DIS**: disable fail-safe lock state (pass through) 0: FAIL_SAFE_LOCK feature enabled (the PMIC stays in the FAIL_SAFE_LOCK state) 1: FAIL_SAFE_LOCK feature disabled (the PMIC passes through the FAIL_SAFE_LOCK state to go into the OFF state)
[5:4]	**RST_FLT_CNT_TMR[1:0]**: reset fault counter timer settings. When the timer elapses, it automatically clears all fault counters (*_FLT_CNT) 00: disabled 01: 1 minute 10: 6 minutes 11: 60 minutes
[3:0]	**WDG_FLT_CNT_MAX[3:0]**: setting of the maximum number of occurrences triggered by a watchdog hard-fault source. 0000: 0 hard-faults allowed (the PMIC goes into the FAIL_SAFE_LOCK_STATE when the 1st hard-fault condition occurs) 0001: 1 hard-fault allowed (PMIC goes into the FAIL_SAFE_LOCK_STATE when the 2nd hard-fault condition occurs) … 1110: 14 hard-faults allowed (the PMIC goes into the FAIL_SAFE_LOCK_STATE when the 15th hard-fault condition occurs) 1111: ∞ hard-faults allowed (fail-safe disabled: the PMIC always restarts when a hard-fault condition occurs)

6.8.27 NVM I²C device address shadow register (NVM_I2C_ADDR_SHR)

Table 107. NVM_I2C_ADD_SHR

7	6	5	4	3	2	1	0
LOCK_NVM	I²C_ADDR[6:0]						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0xB5
- Default: Depends on the PMIC part number
- Description: NVM I²C device address shadow register.

The content of this register take effect after the NVM programming command, then the NVM reloads (INIT&LOAD state or CHECK&LOAD state or NVM read command).

The LOCK_NVM bit takes effect on both shadow registers write and NVM programming command. A successful program operation is enough to have the lock active (without any reload).

[7]	**LOCK_NVM**: NVM write access lock: 0: NVM write allowed 1: NVM write disabled
[6:0]	**I²C_ADDR[6:0]**: I²C device address.

6.8.28 NVM user free shadow register (NVM_USER_SHRx) (x = 1 to 2)

Table 108. NVM_USER_SHRx

7	6	5	4	3	2	1	0
NVM_USERx[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0xB6, 0xB7
- Default: 0x00 (genuine PMIC) or user defined value
- Description: User free shadow register 1 and 2.

Free usage scratch registers save end-product application data in the NVM.

It requires an NVM programing command to save content in the NVM.

[7:0]	**NVM_USERx[7:0]**: user defined value.

7 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 WFQFN 56L (6.5X6.5X0.9) package information

Figure 22. WFQFN 56L (6.5X6.5X0.9) package outline

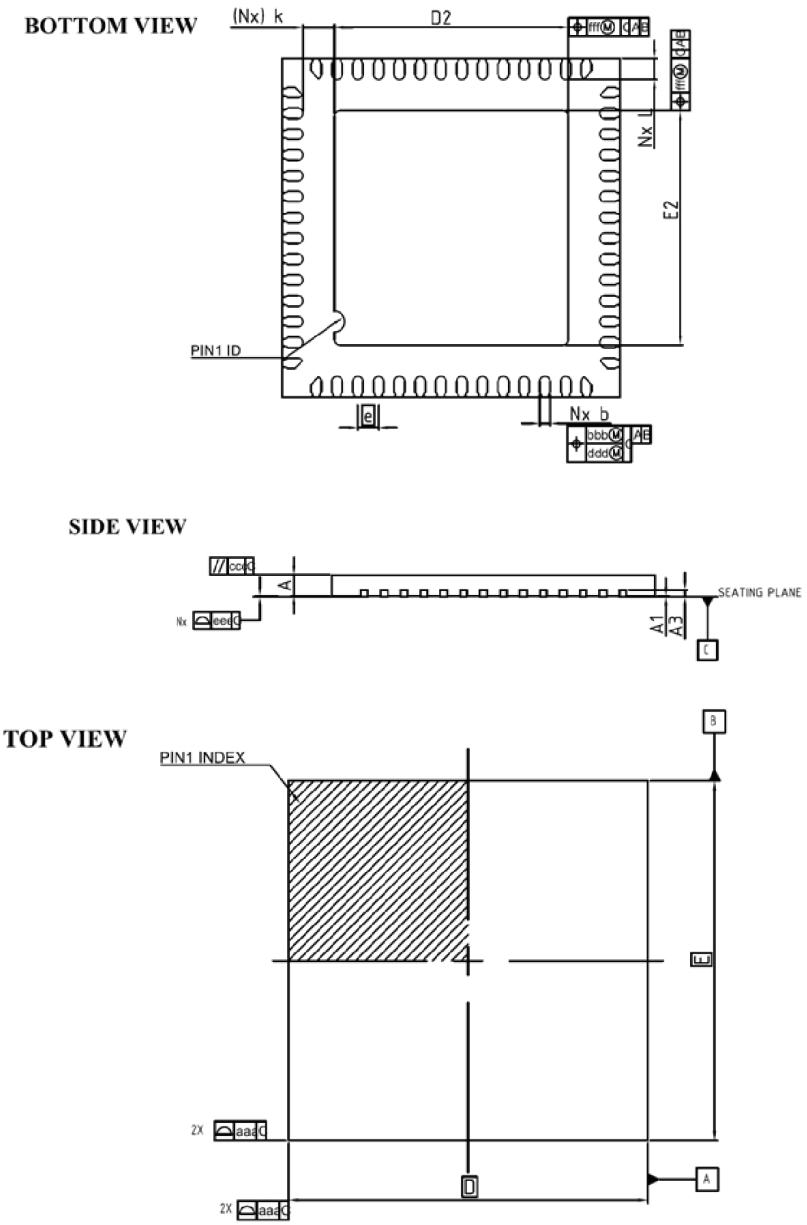


Table 109. **WFQFN 56L (6.5X6.5X0.9) mechanical data**

Symbol	mm		
	Min.	Typ.	Max.
A	0.80	0.85	0.90
A1	0.00	-	0.05
A3		0.20 REF.	
b	0.17	0.20	0.23
D		6.5 BSC	
D2	4.45	4.50	4.55
e		0.4 BSC	
E		6.5 BSC	
E2	4.45	4.50	4.55
L	0.35	0.40	0.45
k	0.20		
N		56	

8 Ordering information

Table 110. **Ordering information**

Order code	Part number	Marking	VIO (BUCK4) programming option	Packing
STPMIC25APQR	STPMIC25A	STPMIC25A	3.3 V	WFQFN 56L (6.5x6.5x0.9)
STPMIC25BPQR	STPMIC25B	STPMIC25B	1.8 V	
STPMIC25DPQR	STPMIC25D	STPMIC25D	3.3 V	

Revision history

Table 111. **Document revision history**

Date	Version	Changes
27-Mar-2024	1	First release.
10-Apr-2024	2	Minor text changes.
12-Apr-2024	3	Updated footnote in Table 14, Table 15, Table 16, Table 17 and max value in V_{OUT-LO} in Table 15.
30-Sep-2024	4	Updated Section 1: Device configuration table and Table 7.

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