# TCAL9538 8-Bit I²C-Bus, SMBus I/O Expander With Interrupt Output, Reset, and Agile I/O Configuration Registers

## 1 Features

- Operating power-supply voltage range of 1.08 V to 3.6 V
- Low standby current consumption of 1 µA typical at 1.8 V
- 1-MHz fast mode plus I²C bus
- Hardware address pin allows two devices on the same I²C, SMBus bus
- Active-low reset input ($\overline{\text{RESET}}$ )
- Open-drain active-low interrupt output ($\overline{\text{INT}}$ )
- Input or output configuration register
- Polarity inversion register
- Configurable I/O drive strength register
- Pull-up and pull-down resistor configuration register
- Internal power-on reset
- Noise filter on SCL or SDA inputs
- Latched outputs with high-current drive maximum capability for directly driving LEDs
- Latch-up performance exceeds 100 mA per JESD 78, class II
- ESD protection exceeds JESD 22
  - 4000-V Human-body model (A114-A)
  - 1000-V Charged-device model (C101)

## 2 Applications

- Servers
- Routers (telecom switching equipment)
- Personal computers
- Personal electronics
- Industrial automation
- Gaming consoles
- Products with GPIO-limited processors

## 3 Description

The TCAL9538 device provides general purpose parallel input/output (I/O) expansion for the two-line bidirectional I2C bus (or SMBus) protocol and is designed for 1.08-V to 3.6-V $V_{CC}$ operation.

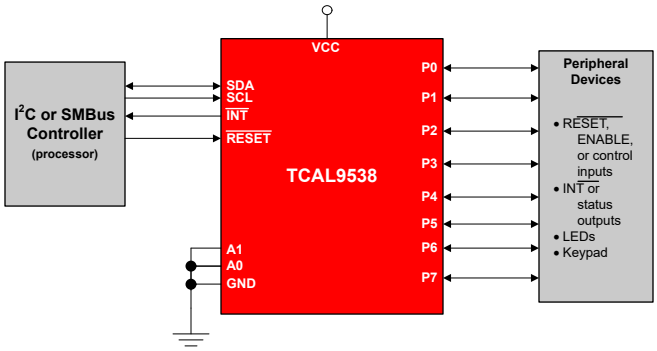
The device supports 100-kHz (Standard-mode), 400-kHz (Fast-mode), and 1-MHz (fast-mode-plus) I²C clock frequencies. I/O expanders such as the TCAL9538 provide a simple solution when additional I/Os are needed for switches, sensors, push-buttons, LEDs, fans, and so on.

The TCAL9538 has Agile I/O ports which include additional features designed to enhance the I/O performance in terms of speed, power consumption and EMI. The additional features are: programmable output drive strength, programmable pull-up and pull-down resistors, latchable inputs, maskable interrupt, interrupt status register, and programmable open-drain or push-pull outputs.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) |
|---|---|---|
| TCAL9538 | TSSOP (16) | 6.4 mm × 6.4 mm |
| | UQFN (16) | 2.6 mm × 1.8 mm |
| | X2QFN (16) | 1.6 mm x 1.6 mm |

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**Simplified Schematic**

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# 4 Pin Configuration and Functions

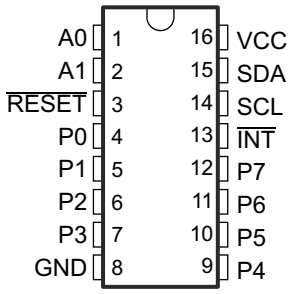


**Figure 4-1. PW (TSSOP) Package, 16-Pin (Top View)**

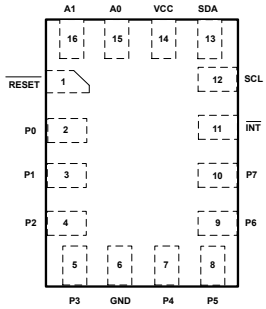


**Figure 4-2. RSV (UQFN) Package, 16-Pin (Top View)**

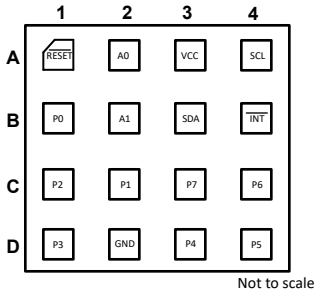


**Figure 4-3. DTU (X2QFN) Package, 16-Pin (Top View)**

**Table 4-1. Pin Functions**

| PIN | | | | TYPE[1] | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | TSSOP (PW) | QFN (RSV) | X2QFN (DTU) | | |
| A0 | 1 | 15 | A2 | I | Address input. Connect directly to $V_{CC}$ or ground |
| A1 | 2 | 16 | B2 | I | Address input. Connect directly to $V_{CC}$ or ground |
| GND | 8 | 6 | D2 | – | Ground |
| $\overline{INT}$ | 13 | 11 | B4 | O | Interrupt output. Connect to $V_{CC}$ through a pull-up resistor |
| P0 | 4 | 2 | B1 | I/O | P-port input/output (push-pull design structure). At power on, P0 is configured as an input |
| P1 | 5 | 3 | C2 | I/O | P-port input/output (push-pull design structure). At power on, P1 is configured as an input |
| P2 | 6 | 4 | C1 | I/O | P-port input/output (push-pull design structure). At power on, P2 is configured as an input |
| P3 | 7 | 5 | D1 | I/O | P-port input/output (push-pull design structure). At power on, P3 is configured as an input |
| P4 | 9 | 7 | D3 | I/O | P-port input/output (push-pull design structure). At power on, P4 is configured as an input |
| P5 | 10 | 8 | D4 | I/O | P-port input/output (push-pull design structure). At power on, P5 is configured as an input |
| P6 | 11 | 9 | C4 | I/O | P-port input/output (push-pull design structure). At power on, P6 is configured as an input |
| P7 | 12 | 10 | C3 | I/O | P-port input/output (push-pull design structure). At power on, P7 is configured as an input |
| $\overline{RESET}$ | 3 | 1 | A1 | I | Active-low reset input. Connect to $V_{CC}$ through a pull-up resistor, if no active connection is used |
| SCL | 14 | 12 | A4 | I | Serial clock bus. Connect to $V_{CC}$ through a pull-up resistor |
| SDA | 15 | 13 | B3 | I/O | Serial data bus. Connect to $V_{CC}$ through a pull-up resistor |
| $V_{CC}$ | 16 | 14 | A3 | – | Supply voltage |

(1) I = Input, O = Output, I/O = Input or Output.

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# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 | 4 | V |
| $V_I$ | Input voltage(2) | | –0.5 | 4 | V |
| $V_O$ | Output voltage(2) | | –0.5 | 4 | V |
| $I_{IK}$ | Input clamp current | $V_I < 0$ | | –20 | mA |
| $I_{OK}$ | Output clamp current | $V_O < 0$ | | –20 | mA |
| $I_{IOK}$ | Input-output clamp current | $V_O < 0$ or $V_O > V_{CC}$ | | ±20 | mA |
| $I_{OL}$ | Continuous output low current | $V_O$ = 0 to $V_{CC}$ | | 50 | mA |
| $I_{OH}$ | Continuous output high current | $V_O$ = 0 to $V_{CC}$ | | –50 | mA |
| $I_{CC}$ | Continuous current through GND | | | –200 | mA |
| $I_{CC}$ | Continuous current through $V_{CC}$ | | | 160 | mA |
| $T_J$ | Junction temperature | | | 130 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) *Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.*
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±4000 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC specification JS-002, all pins(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.


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## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 1.08 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | All Pins | 0.7 * $V_{CC}$ | 3.6 | V |
| $V_{IL}$ | Low-level input voltage | All Pins | -0.5 | 0.3 * $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | P0-P7 | | –10 | mA |
| $I_{OH}$ (Total of all ports) | High-level output current | P0-P7 | | –160 | mA |
| $I_{OL}$ | Low-level output current ($V_{OL}$ ≤ 0.3 V) | P0-P7 | | 25 | mA |
| $I_{OL}$ (Total of all ports) | Low-level output current ($V_{OL}$ ≤ 0.3 V) | P0-P7 | | 160 | mA |
| $T_A$ | Ambient temperature | | –40 | 125 | °C |
| $T_J$ | Junction temperature | | | 125 | °C |

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## 5.4 Thermal Information

| THERMAL METRIC[1] | | Package | | | UNIT |
|---|---|---|---|---|---|
| | | PW (TSSOP) | RSV (UQFN) | DTU (X2QFN) | |
| | | PINS | PINS | PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 115.7 | 123.1 | 143.4 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 46.1 | 65.0 | 55.6 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 62.0 | 54.6 | 81.9 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 6.0 | 2.9 | 1.3 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 61.4 | 52.9 | 81.8 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.


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## 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Input diode clamp voltage | | $I_I$ = –18 mA | 1.08 V to 3.6 V | –1.2 | | | V |
| $V_{PORR}$ | Power-on reset voltage, $V_{CC}$ rising | | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | | | 0.85 | 1.0 | V |
| $V_{PORF}$ | Power-on reset voltage, $V_{CC}$ falling | | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | | 0.6 | 0.75 | | V |
| $V_{OH}$ | P-port high-level output voltage[1] | | $I_{OH}$ = –8 mA; CC-XX = 11b | 1.08 V | 0.8 | | | V |
| | | | | 1.65 V | 1.4 | | | |
| | | | | 2.3 V | 2.1 | | | |
| | | | | 3 V | 2.8 | | | |
| | | | $I_{OH}$ = –2.5 mA & CC-XX = 00b; $I_{OH}$ = –5 mA & CC-XX = 01b; $I_{OH}$ = –7.5 mA & CC-XX = 10b; $I_{OH}$ = –10 mA & CC-XX = 11b; | 1.08 V | 0.75 | | | |
| | | | | 1.65 V | 1.4 | | | |
| | | | | 2.3 V | 2.1 | | | |
| | | | | 3 V | 2.8 | | | |
| $V_{OL}$ | Low-level output voltage | P ports | $I_{OL}$ = 8 mA; CC-XX = 11b | 1.08 V | | | 0.2 | V |
| | | | | 1.65 V | | | 0.15 | |
| | | | | 2.3 V | | | 0.1 | |
| | | | | 3.0 V | | | 0.1 | |
| | | P ports | $I_{OL}$ = 2.5 mA and CC-XX = 00b; $I_{OL}$ = 5 mA and CC-XX = 01b; $I_{OL}$ = 7.5 mA and CC-XX = 10b; $I_{OL}$ = 10 mA and CC-XX = 11b; | 1.08 V | | | 0.25 | V |
| | | | | 1.65 V | | | 0.15 | |
| | | | | 2.3 V | | | 0.1 | |
| | | | | 3.0 V | | | 0.1 | |
| $I_{OL}$ | Low-level output current | SDA | $V_{OL}$ = 0.4 V | 1.08 V to 3.6 V | 20 | | | mA |
| | | $\overline{INT}$ | $V_{OL}$ = 0.4 V | | 4 | | | |
| $I_I$ | Input leakage current | P ports | $V_I$ = $V_{CC}$ or GND | 1.08 V to 3.6 V | | | ±1 | µA |
| | | | $V_I$ = 3.6 V | 0 V | | | ±1 | |
| $I_I$ | Input leakage current | SCL, SDA, $\overline{RESET}$ | $V_I$ = $V_{CC}$ or GND | 1.08 V to 3.6 V | | | ±1 | |
| $I_I$ | Input leakage current | | $V_I$ = $V_{CC}$ or GND | 1.08 V to 3.6 V | | | ±1 | µA |

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## 5.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Quiescent current | Operating mode (400 kHz) | SDA, $\overline{RESET}$ =$V_{CC}$, P ports, ADDR = $V_{CC}$ or GND, I/O = inputs, $f_{SCL}$ = 400 kHz, –40°C < $T_A$ ≤ 85°C | 3.6 V | | 11 | 15 | µA |
| | | | | 2.7 V | | 8 | 11 | |
| | | | | 1.95 V | | 5 | 8 | |
| | | | | 1.32 V | | 2 | 6 | |
| | | | SDA, $\overline{RESET}$ =$V_{CC}$, P ports, ADDR = $V_{CC}$ or GND, I/O = inputs, $f_{SCL}$ = 400 kHz, 85°C < $T_A$ ≤ 125°C | 3.6 V | | 7 | 24 | µA |
| | | | | 2.7 V | | 5 | 18 | |
| | | | | 1.95 V | | 4 | 14 | |
| | | | | 1.32 V | | 2 | 11 | |
| | | Operating mode (1 MHz) | SDA, $\overline{RESET}$ = $V_{CC}$, P ports, ADDR = $V_{CC}$ or GND, I/O = inputs, $f_{SCL}$ = 1 MHz, –40°C < $T_A$ ≤ 85°C | 3.6 V | | | 34 | µA |
| | | | | 2.7 V | | | 24 | |
| | | | | 1.95 V | | | 18 | |
| | | | | 1.32 V | | | 12 | |
| | | | SDA, $\overline{RESET}$ = $V_{CC}$, P ports, ADDR = $V_{CC}$ or GND, I/O = inputs, $f_{SCL}$ = 1 MHz, 85°C < $T_A$ ≤ 125°C | 3.6 V | | | 42 | µA |
| | | | | 2.7 V | | | 30 | |
| | | | | 1.95 V | | | 22 | |
| | | | | 1.32 V | | | 16 | |
| | | Standby mode | SCL, SDA, $\overline{RESET}$ = $V_{CC}$, P port, ADDR = $V_{CC}$ or GND, I/O = inputs, $I_O$ = 0, $f_{SCL}$ = 0 kHz, -40 °C < $T_A$ ≤ 85 °C | 3.6 V | | 1 | 3 | µA |
| | | | | 2.7 V | | 0.8 | 2.0 | |
| | | | | 1.95 V | | 0.6 | 1.6 | |
| | | | | 1.32 V | | 0.6 | 1.4 | |
| | | | SCL, SDA, $\overline{RESET}$ = $V_{CC}$. P port, ADDR = $V_{CC}$ or GND, I/O = inputs, $I_O$ = 0, $f_{SCL}$ = 0 kHz, 85 °C < $T_A$ ≤ 125 °C | 3.6 V | | | 14 | µA |
| | | | | 2.7 V | | | 10 | |
| | | | | 1.95 V | | | 8 | |
| | | | | 1.32 V | | | 6 | |
| $R_{pu(int)}$ | internal pull-up resistance | P port | | | 70 | 100 | 140 | kΩ |
| $R_{pd(int)}$ | internal pull-down resistance | | | | | | | |
| $C_I$ | Input pin capacitance | SCL | $V_I$ = $V_{CC}$ or GND | 1.08 V to 3.6 V | | 2.5 | 5 | pF |
| $C_{IO}$ | Input-output pin capacitance | SDA | $V_{IO}$ = $V_{CC}$ or GND | 1.08 V to 3.6 V | | 6 | 8 | pF |
| | | P port | $V_{IO}$ = $V_{CC}$ or GND | 1.08 V to 3.6 V | | 6 | 8.5 | |

(1) Each I/O must be externally limited to a maximum of 25 mA, CC-XX refers to output drive strength register setting.

## 5.6 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| **$\overline{RESET}$** | | | | |
| $t_w$ | Reset pulse duration | 80 | | ns |
| $t_{REC}$ | Reset recovery time | 0 | | ns |
| $t_{RESET}$ | Time to reset | 400 | | ns |
| **P-Ports** | | | | |
| $t_{PH}$ | Minimum pulse width on P-Port that causes an interrupt | 30 | | ns |


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## 5.7 I²C Bus Timing Requirements

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| **I²C Bus - Standard Mode** | | | | | |
| $f_{scl}$ | I²C clock frequency | | 0 | 100 | kHz |
| $t_{sch}$ | I²C clock high time | | 4 | | µs |
| $t_{scl}$ | I²C clock low time | | 4.7 | | µs |
| $t_{sp}$ | I²C spike time | | | 50 | ns |
| $t_{sds}$ | I²C serial-data setup time | | 250 | | ns |
| $t_{sdh}$ | I²C serial-data hold time | | 0 | | ns |
| $t_{icr}$ | I²C input rise time | | | 1000 | ns |
| $t_{icf}$ | I²C input fall time | | | 300 | ns |
| $t_{ocf}$ | I²C output fall time | 10-pF to 400-pF bus | | 300 | ns |
| $t_{buf}$ | I²C bus free time between stop and start | | 4.7 | | µs |
| $t_{sts}$ | I²C start or repeated start condition setup | | 4.7 | | µs |
| $t_{sth}$ | I²C start or repeated start condition hold | | 4 | | µs |
| $t_{sps}$ | I²C stop condition setup | | 4 | | µs |
| $t_{vd(data)}$ | Valid data time | SCL low to SDA output valid | | 3.45 | µs |
| $t_{vd(ack)}$ | Valid data time of ACK condition | ACK signal from SCL low to SDA (out) low | | 3.45 | µs |
| $C_b$ | I²C bus capacitive load | | | 400 | pF |
| **I²C Bus - Fast Mode** | | | | | |
| $f_{scl}$ | I²C clock frequency | | 0 | 400 | kHz |
| $t_{sch}$ | I²C clock high time | | 0.6 | | µs |
| $t_{scl}$ | I²C clock low time | | 1.3 | | µs |
| $t_{sp}$ | I²C spike time | | | 50 | ns |
| $t_{sds}$ | I²C serial-data setup time | | 100 | | ns |
| $t_{sdh}$ | I²C serial-data hold time | | 0 | | ns |
| $t_{icr}$ | I²C input rise time | | 20 | 300 | ns |
| $t_{icf}$ | I²C input fall time | | 20 × ($V_{CC}$ / 5.5 V) | 300 | ns |
| $t_{ocf}$ | I²C output fall time | 10-pF to 400-pF bus | 20 × ($V_{CC}$ / 5.5 V) | 300 | ns |
| $t_{buf}$ | I²C bus free time between stop and start | | 1.3 | | µs |
| $t_{sts}$ | I²C start or repeated start condition setup | | 0.6 | | µs |
| $t_{sth}$ | I²C start or repeated start condition hold | | 0.6 | | µs |
| $t_{sps}$ | I²C stop condition setup | | 0.6 | | µs |
| $t_{vd(data)}$ | Valid data time | SCL low to SDA output valid | | 0.9 | µs |
| $t_{vd(ack)}$ | Valid data time of ACK condition | ACK signal from SCL low to SDA (out) low | | 0.9 | µs |
| $C_b$ | I²C bus capacitive load | | | 400 | pF |
| **I²C Bus - Fast Mode Plus** | | | | | |
| $f_{scl}$ | I²C clock frequency | | 0 | 1000 | kHz |
| $t_{sch}$ | I²C clock high time | | 0.26 | | µs |
| $t_{scl}$ | I²C clock low time | | 0.5 | | µs |
| $t_{sp}$ | I²C spike time | | | 50 | ns |
| $t_{sds}$ | I²C serial-data setup time | | 50 | | ns |
| $t_{sdh}$ | I²C serial-data hold time | | 0 | | ns |

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## 5.7 I²C Bus Timing Requirements (continued)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{icr}$ | I²C input rise time | | | 120 | ns |
| $t_{icf}$ | I²C input fall time | | 20 × ($V_{CC}$ / 5.5 V) | 120 | ns |
| $t_{ocf}$ | I²C output fall time | 10-pF to 550-pF bus | 20 × ($V_{CC}$ / 5.5 V) | 120 | ns |
| $t_{buf}$ | I²C bus free time between stop and start | | 0.5 | | µs |
| $t_{sts}$ | I²C start or repeated start condition setup | | 0.26 | | µs |
| $t_{sth}$ | I²C start or repeated start condition hold | | 0.26 | | µs |
| $t_{sps}$ | I²C stop condition setup | | 0.26 | | µs |
| $t_{vd(data)}$ | Valid data time | SCL low to SDA output valid | | 0.45 | µs |
| $t_{vd(ack)}$ | Valid data time of ACK condition | ACK signal from SCL low to SDA (out) low | | 0.45 | µs |
| $C_b$ | I²C bus capacitive load | | | 550 | pF |

## 5.8 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{iv}$ | Interrupt valid time | P port | $\overline{INT}$ | | | 1 | µs |
| $t_{ir}$ | Interrupt reset delay time | SCL | $\overline{INT}$ | | | 1 | µs |
| $t_{pv}$ | Output data valid time | SCL | P port | | | 400 | ns |
| $t_{ps}$ | Input data setup time | P port | SCL | 0 | | | ns |
| $t_{ph}$ | Input data hold time | P port | SCL | 300 | | | ns |


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## 5.9 Typical Characteristics

$T_A$ = 25°C (unless otherwise noted)

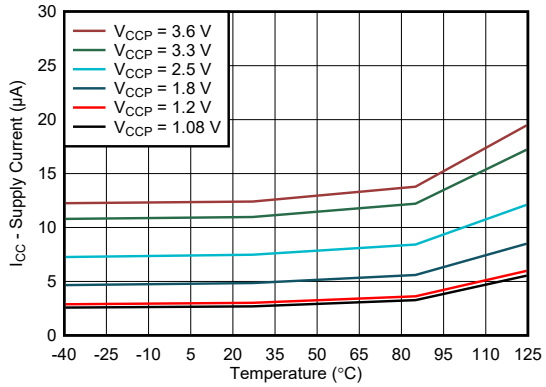


**Figure 5-1. Supply Current vs Temperature - FM mode**

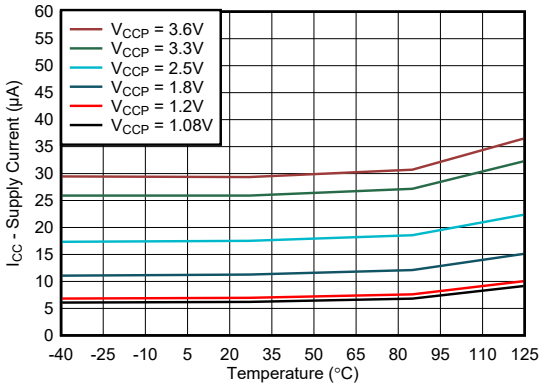


**Figure 5-2. Supply Current vs Temperature - FM+ mode**

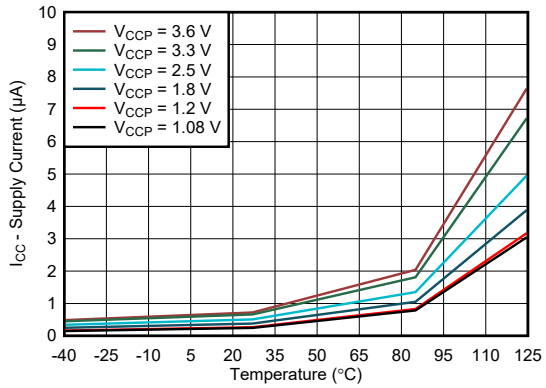


**Figure 5-3. Standby Supply Current vs Temperature**

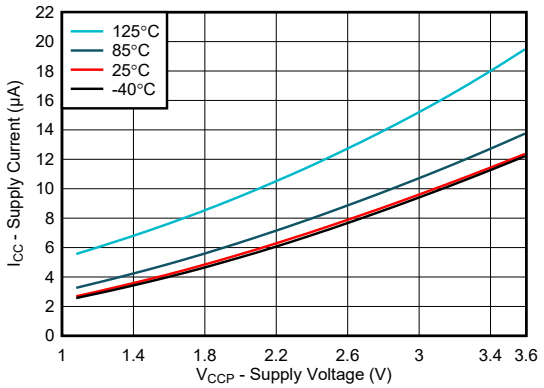


**Figure 5-4. Supply Current vs Supply Voltage - FM mode**

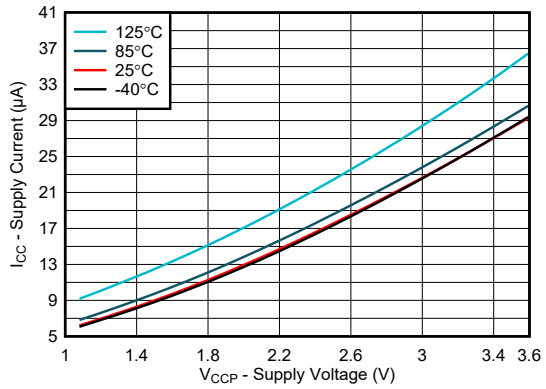


**Figure 5-5. Supply Current vs Supply Voltage - FM+ mode**

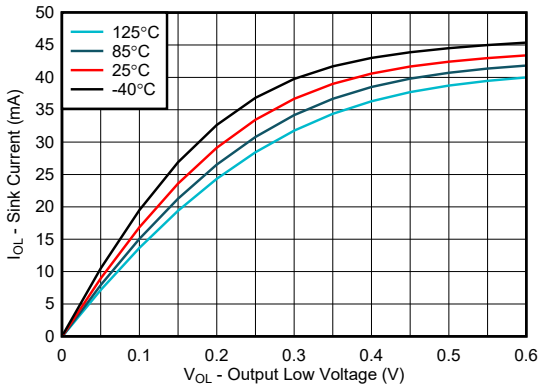


**Figure 5-6. I/O Sink Current vs Output Low Voltage, $V_{CC}$ = 1.08 V**

## 5.9 Typical Characteristics (continued)

$T_A$ = 25°C (unless otherwise noted)

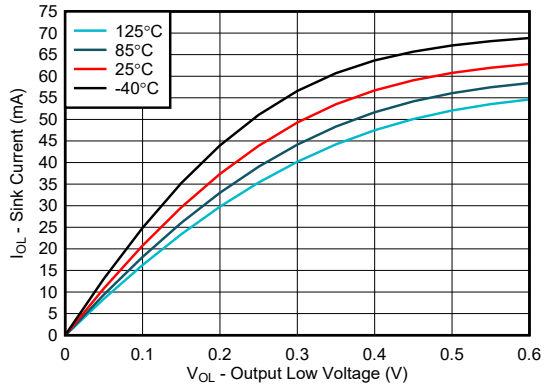


**Figure 5-7. I/O Sink Current vs Output Low Voltage, $V_{CC}$ = 1.2 V**

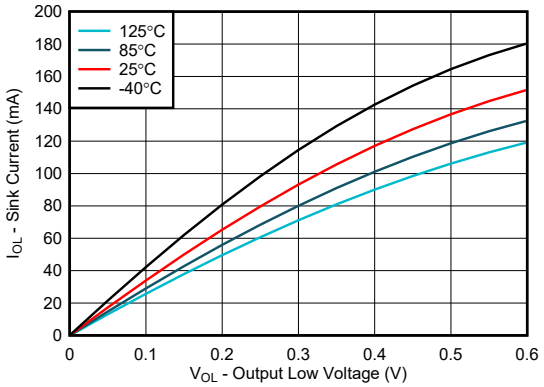


**Figure 5-8. I/O Sink Current vs Output Low Voltage, $V_{CC}$ = 1.8 V**

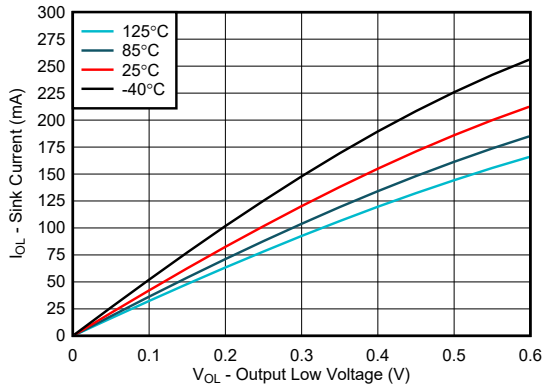


**Figure 5-9. I/O Sink Current vs Output Low Voltage, $V_{CC}$ = 2.5 V**

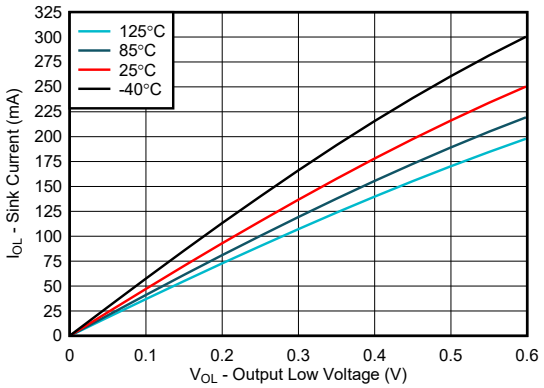


**Figure 5-10. I/O Sink Current vs Output Low Voltage, $V_{CC}$ = 3.3 V**

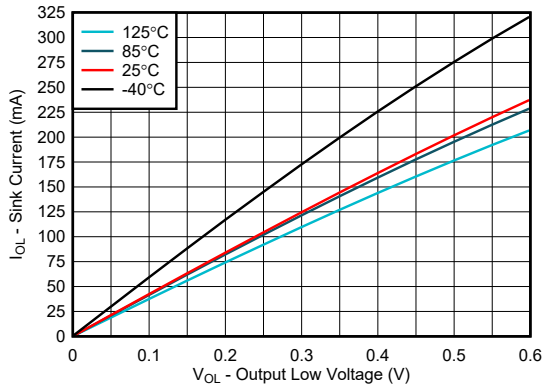


**Figure 5-11. I/O Sink Current vs Output Low Voltage, $V_{CC}$ = 3.6 V**

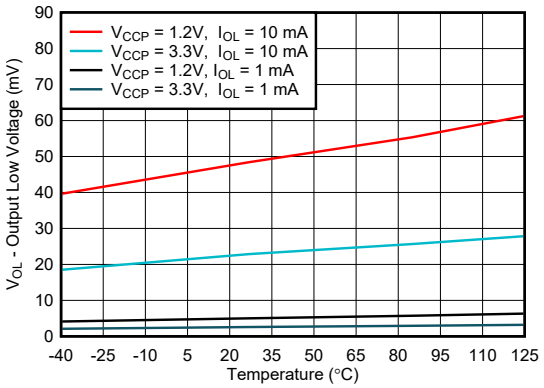


**Figure 5-12. I/O Low Voltage vs Temperature**


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## 5.9 Typical Characteristics (continued)

$T_A$ = 25°C (unless otherwise noted)

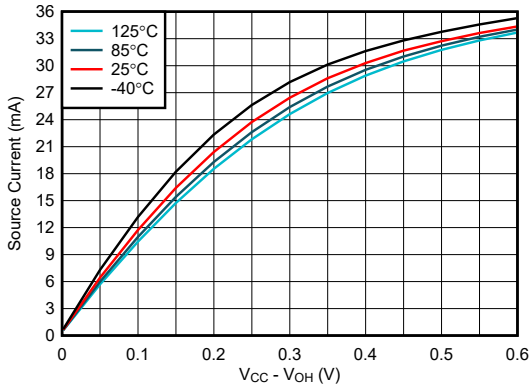


**Figure 5-13. I/O Source Current vs Output High Voltage , $V_{CC}$ = 1.08 V**

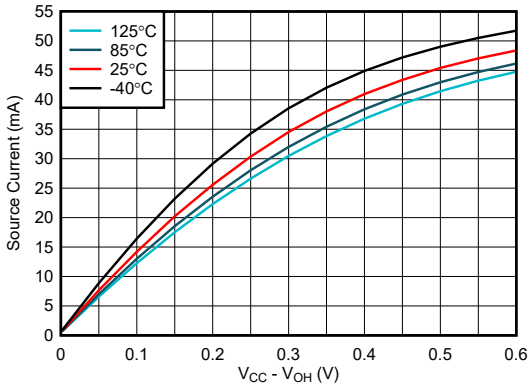


**Figure 5-14. I/O Source Current vs Output High Voltage, $V_{CC}$ = 1.2 V**

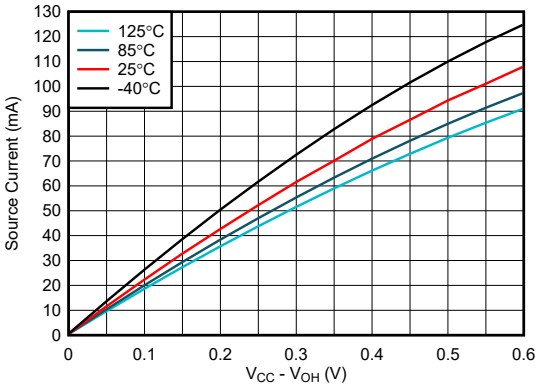


**Figure 5-15. I/O Source Current vs Output High Voltage, $V_{CC}$ = 1.8 V**

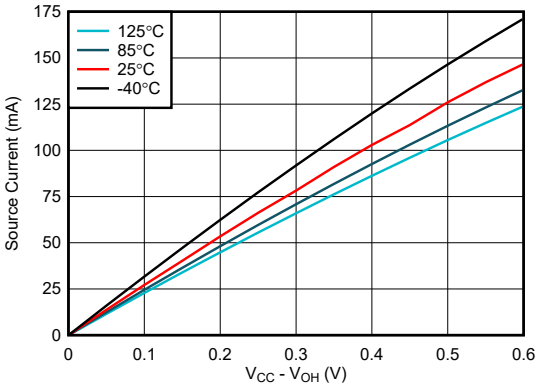


**Figure 5-16. I/O Source Current vs Output High Voltage, $V_{CC}$ = 2.5 V**

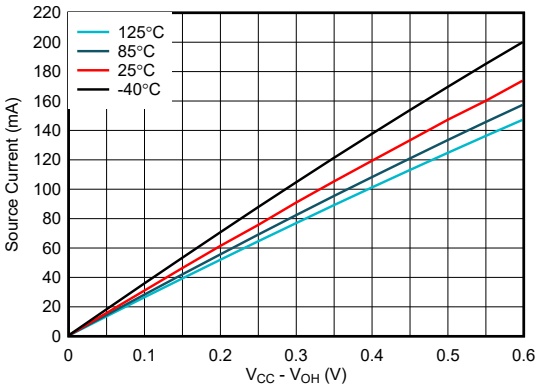


**Figure 5-17. I/O Source Current vs Output High Voltage, $V_{CC}$ = 3.3 V**

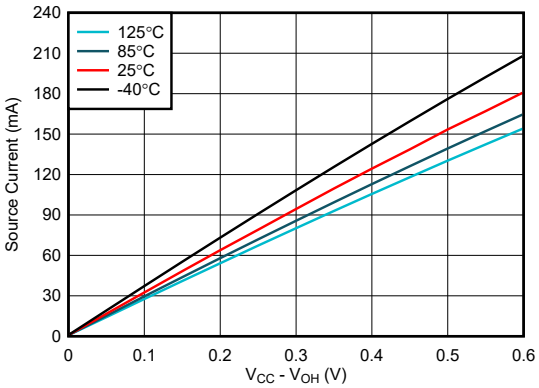


**Figure 5-18. I/O Source Current vs Output High Voltage, $V_{CC}$ = 3.6 V**

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## 5.9 Typical Characteristics (continued)

$T_A$ = 25°C (unless otherwise noted)

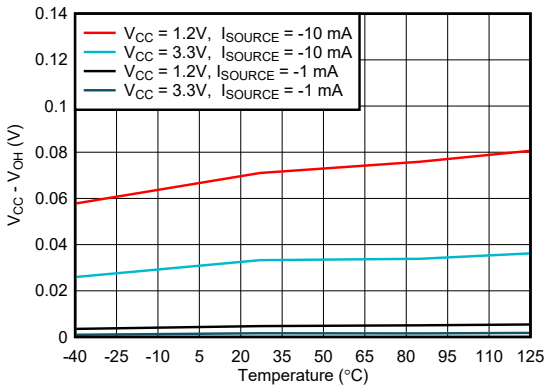


**Figure 5-19. I/O High Voltage vs Temperature**


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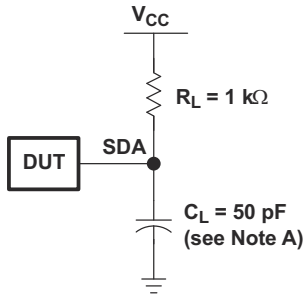
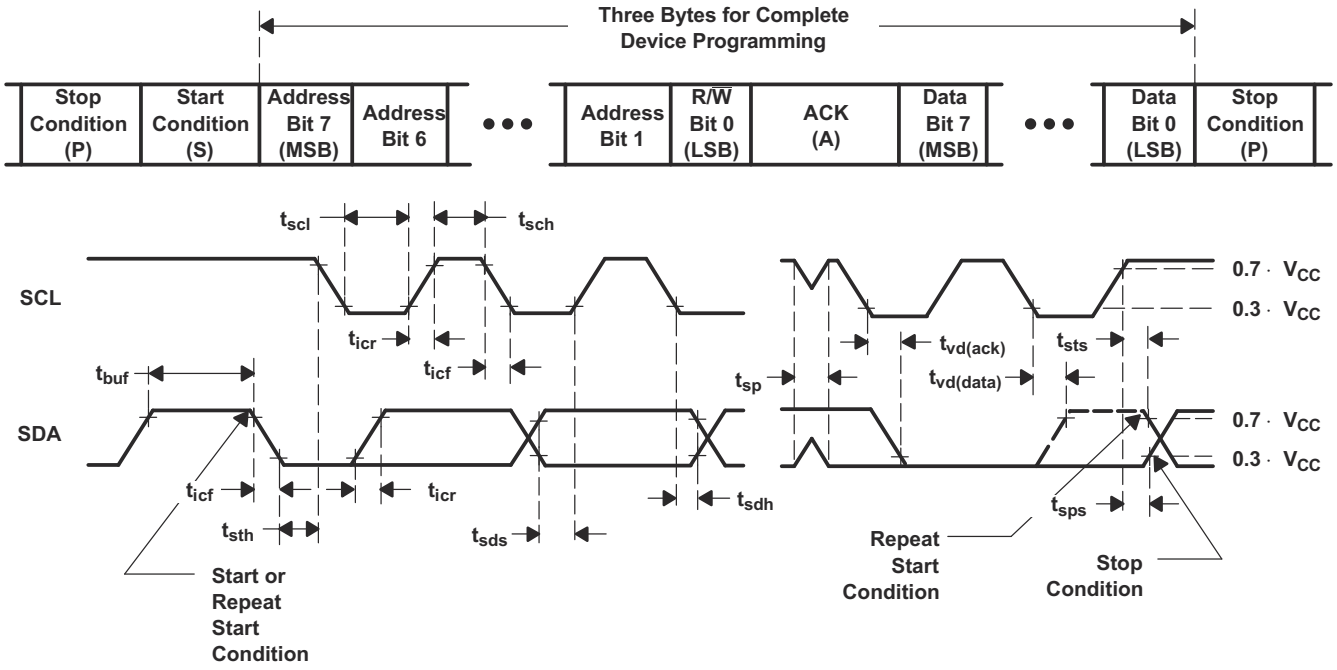
# 6 Parameter Measurement Information




SDA LOAD CONFIGURATION




VOLTAGE WAVEFORMS

| BYTE | DESCRIPTION |
|---|---|
| 1 | $I^2C$ address |
| 2, 3 | P-port data |

A. $C_L$ includes probe and jig capacitance. tocf is measured with $C_L$ of 10 pF or 400 pF.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r/t_f$ ≤ 30 ns.
C. All parameters and waveforms are not applicable to all devices.

**Figure 6-1. $I^2C$ Interface Load Circuit and Voltage Waveforms**

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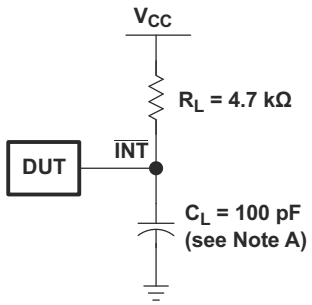
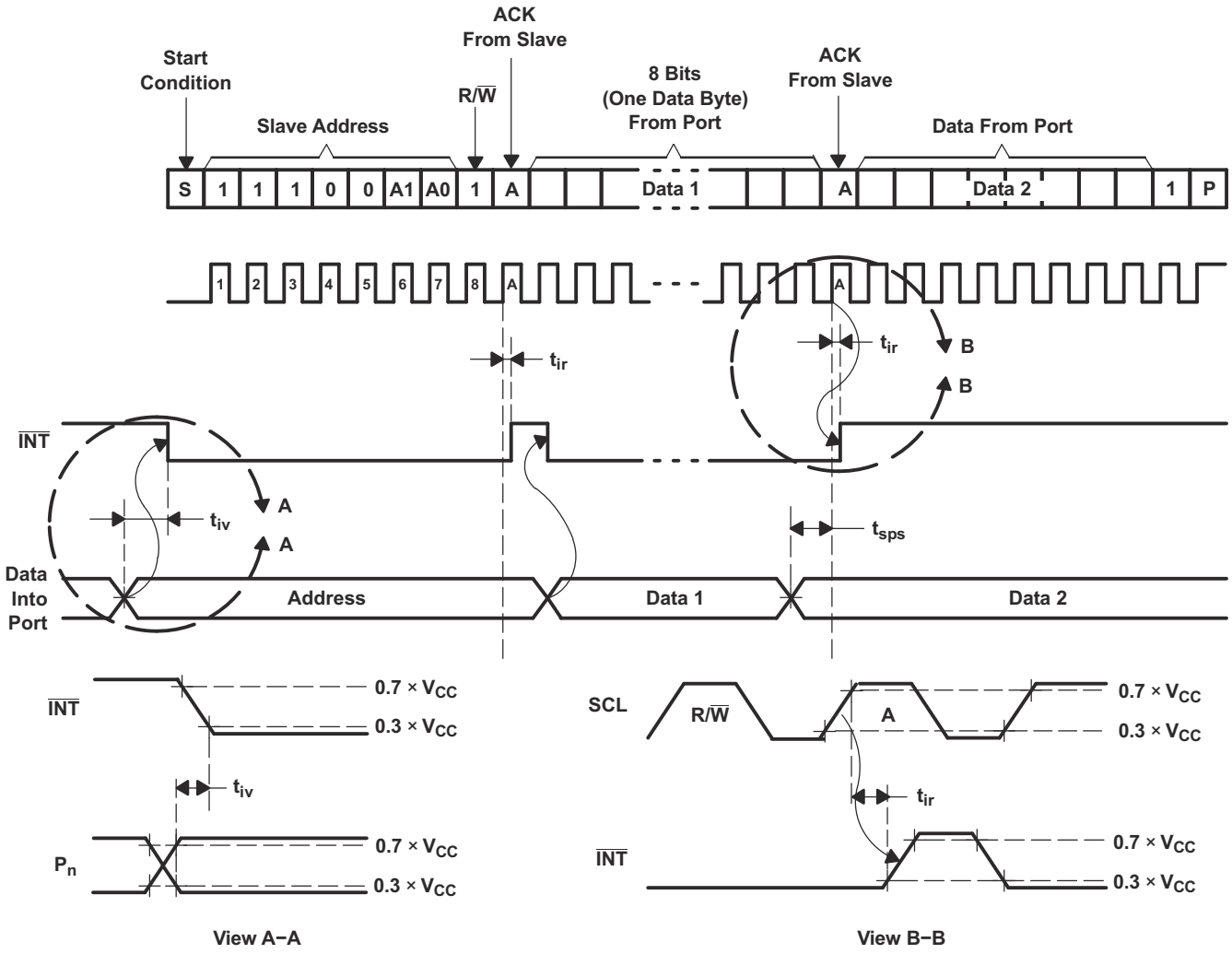



INTERRUPT LOAD CONFIGURATION




View A–A

View B–B

A. $C_L$ includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r/t_f$ ≤ 30 ns.

C. All parameters and waveforms are not applicable to all devices.

**Figure 6-2. Interrupt Load Circuit and Voltage Waveforms**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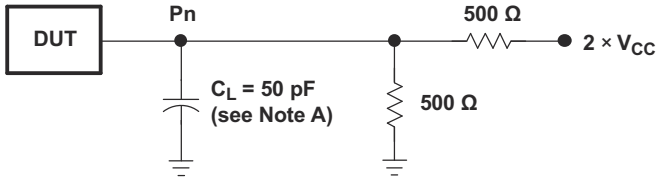
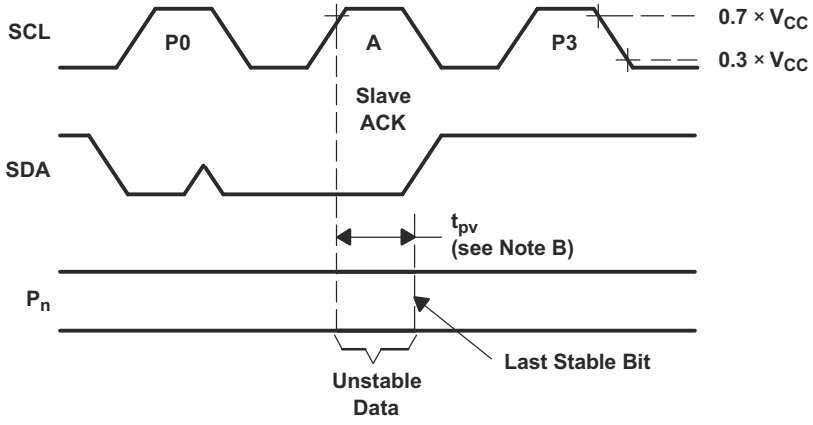
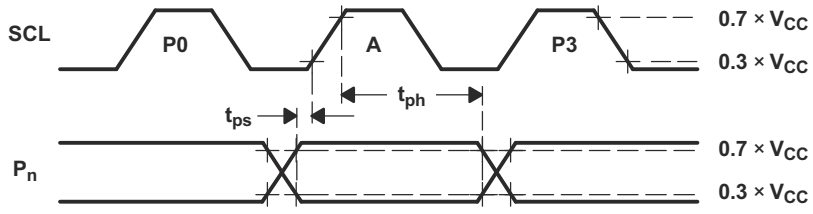



P-PORT LOAD CONFIGURATION




WRITE MODE (R/$\overline{W}$ = 0)




READ MODE (R/$\overline{W}$ = 1)

A. $C_L$ includes probe and jig capacitance.
B. $t_{pv}$ is measured from 0.7 × $V_{CC}$ on SCL to 50% I/O (Pn) output.
C. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r/t_f$ ≤ 30 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

**Figure 6-3. P-Port Load Circuit and Timing Waveforms**

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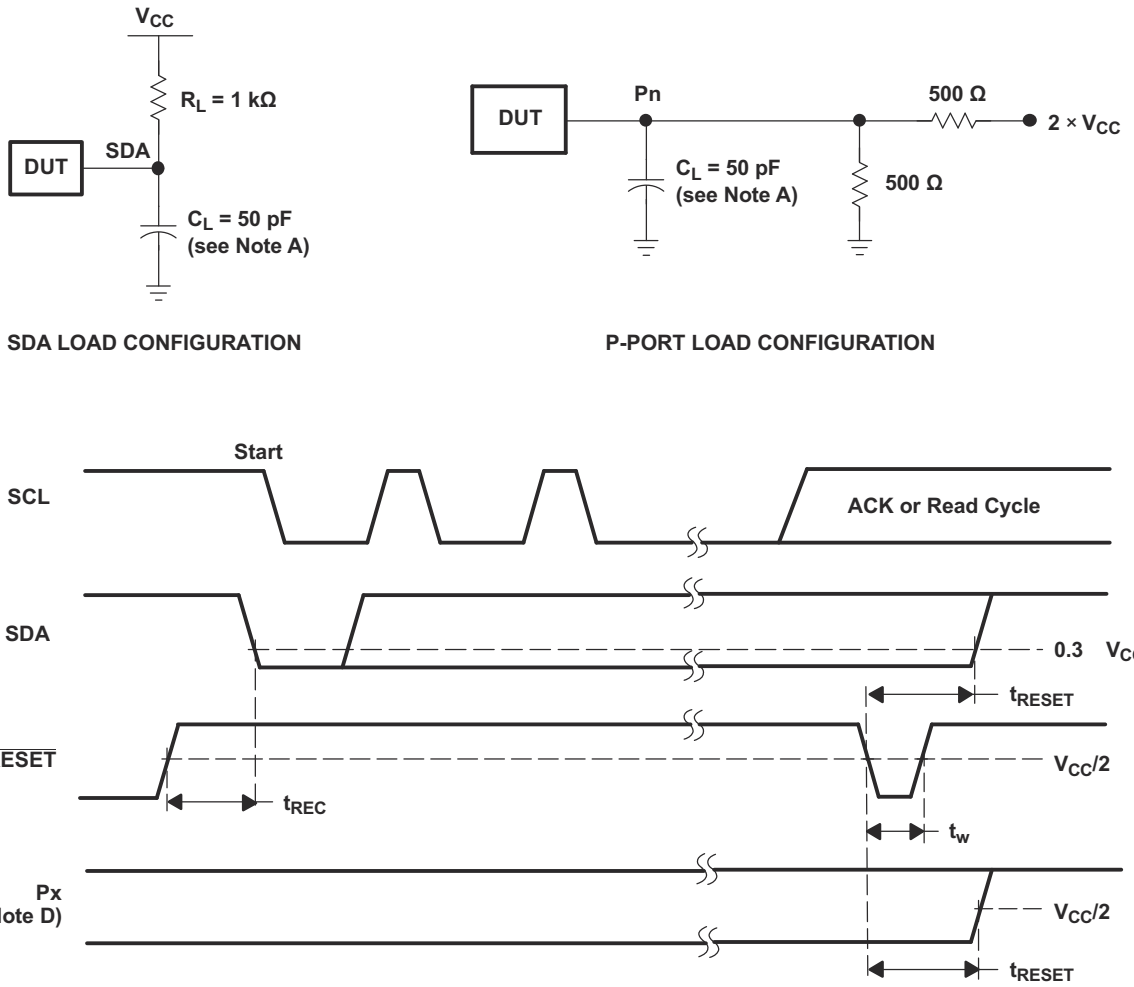


A. $C_L$ includes probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r/t_f$ ≤ 30 ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. I/Os are configured as inputs.
E. All parameters and waveforms are not applicable to all devices.

**Figure 6-4. Reset Load Circuits and Voltage Waveforms**


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# 7 Detailed Description

## 7.1 Overview

The TCAL9538 is a general purpose I/O expander for the two-line bidirectional bus ($I^2C$) is designed for 1.08-V to 3.6-V operation. It provides general-purpose remote I/O expansion for processors through $I^2C$ communication, an interface consisting of serial clock (SCL), and serial data (SDA) signals.

The TCAL9538 digital core consists of 8-bit data registers which allow the user to configure the I/O port characteristics. At power-up or after a software reset call, the I/Os are configured as inputs. However, the system controller can configure the I/Os as either inputs or outputs by writing to the Configuration registers. The data for each input or output is kept in the corresponding Input Port or Output Port register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system controller. Additionally, the TCAL9538 has Agile I/O functionality which is specifically targeted to enhance the I/O ports. The Agile I/O features and registers include programmable output drive strength, programmable pull-up and pull-down resistors, latchable inputs, maskable interrupts, interrupt status register, and programmable open-drain or push-pull outputs. These configuration registers improve the I/O by increasing flexibility and allowing the user to optimize their design for power consumption, speed, and EMI.

Other features of the device include an interrupt that is generated on the $\overline{INT}$ pin whenever an input port changes state. The device can be reset to its default state by issuing a software reset command or by cycling power to the device and causing a power-on reset. The hardware selectable address pins allow multiple TCAL9538 devices to be connected to the same $I^2C$ bus.

The TCAL9538 open-drain interrupt ($\overline{INT}$) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system controller that an input state has changed. The $\overline{INT}$ pin can be connected to the interrupt input of a processor. By sending an interrupt signal on this line, the device can inform the processor if there is incoming data on the remote I/O ports without having to communicate via the $I^2C$ bus. Thus, the device can remain a simple target device.

The system controller can re-initialize $I^2C$/SMBus state machine in the event of a timeout or other improper operation by asserting a low on the $\overline{RESET}$ input pin without resetting the sticky registers to default values.

Two hardware pins (A0 and A1) can be used to program and vary the fixed $I^2C$ address, and allow multiple devices to share the same $I^2C$ bus or SMBus.

## 7.2 Functional Block Diagrams

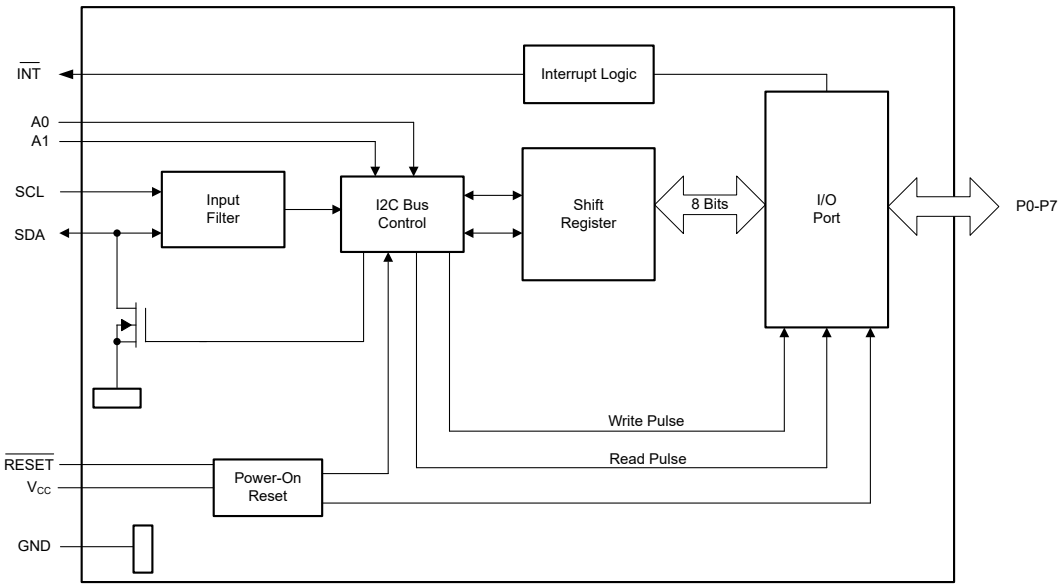
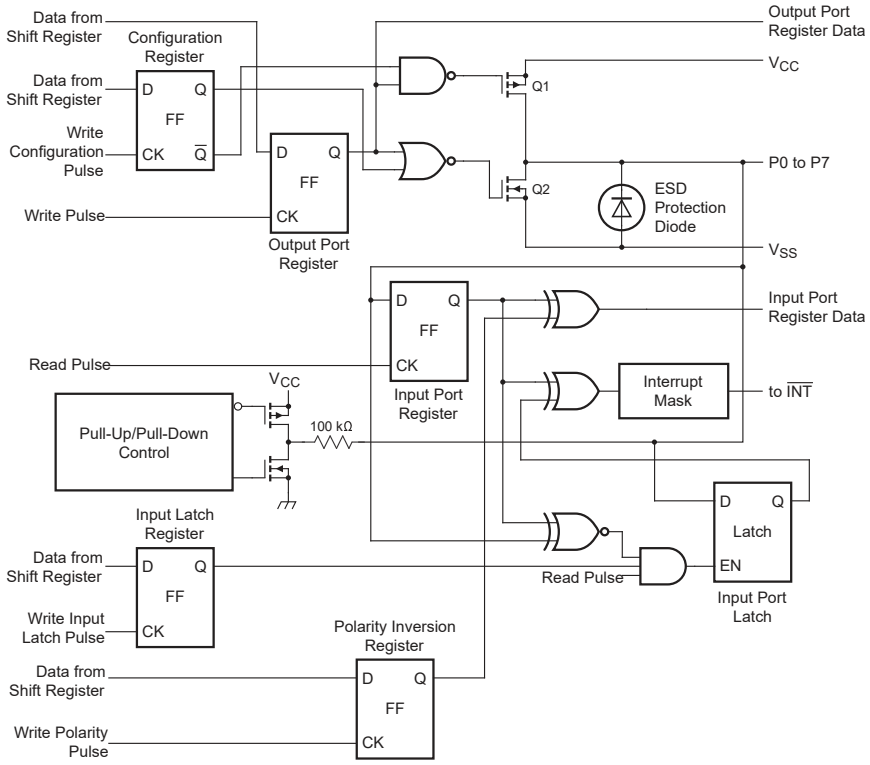



**Figure 7-1. Logic Diagram (Positive Logic)**




A. On power up or reset, all registers return to default values.

**Figure 7-2. Simplified Schematic of P0 to P7**

## 7.3 Feature Description

### 7.3.1 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 are off (see Section 7.2), which creates a high-impedance input. The input voltage may be raised above the supply voltage to a maximum of 3.6V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the output port register. In this case, there are low-impedance paths between the I/O pin and either supply or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

### 7.3.2 Adjustable Output Drive Strength

The output drive strength registers allow the user to control the drive level of the GPIO. Each GPIO can be configured independently to one of the four possible current levels. By programming these bits the user is changing the number of transistor pairs or 'fingers' that drive the I/O pad. Figure 7-3 shows a simplified output stage. The behavior of the pad is affected by the Configuration register, the output port data, and the output drive strength register. When the output drive strength register bits are programmed to 01b, then only two of the fingers are active, reducing the current drive capability by 50%.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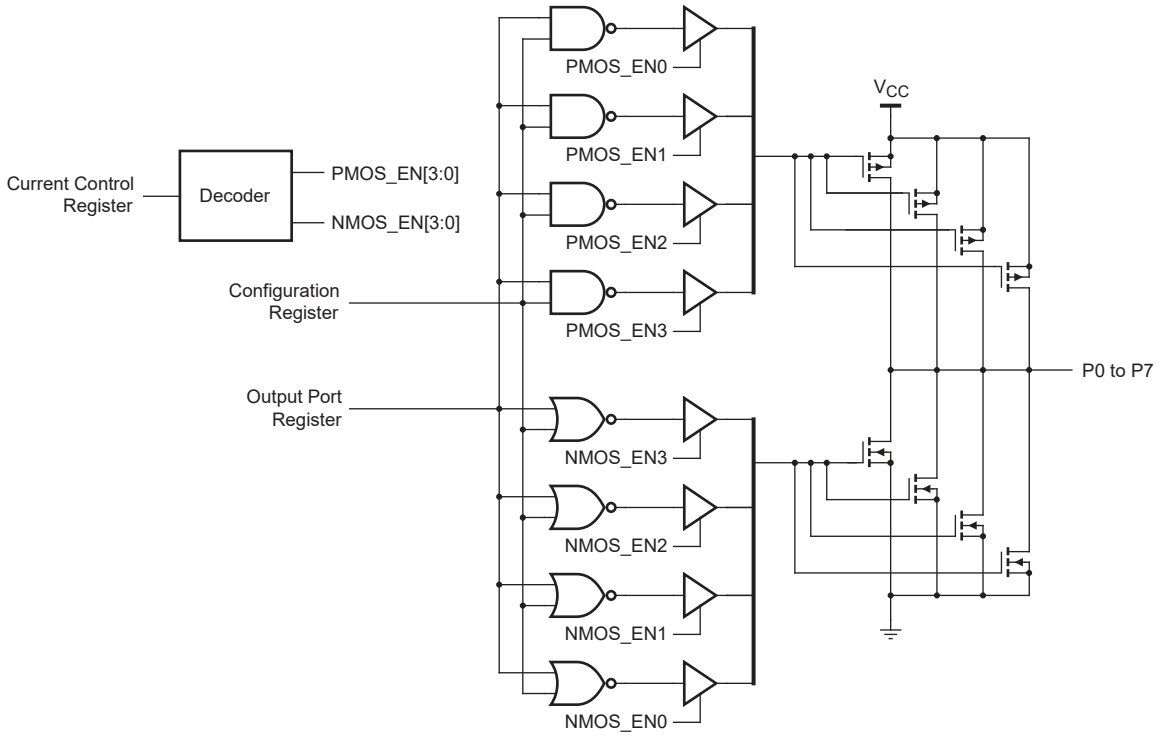


**Figure 7-3. Simplified output stage**

Reducing the current drive capability may be desirable to reduce system noise. When the output switches there is a peak current that is a function of the output drive selection. This peak current runs through the supply and GND package inductance's and creates a noise (some radiated, but more critically Simultaneous Switching Noise (SSN)). In other words, switching many outputs at the same time will create ground and supply noise. The output drive strength control through the Output Drive Strength registers allows the user to mitigate SSN issues without the need of additional external components.

### 7.3.3 Interrupt Output ($\overline{INT}$)

An interrupt is generated by any rising or falling edge of the port inputs in the input mode provided the interrupt feature is unmasked. After time $t_{iv}$, the $\overline{INT}$ signal is valid. Resetting the interrupt circuit is achieved when data on the port is changed back to the original setting or when data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$.

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the input port register.

The $\overline{INT}$ output has an open-drain structure and requires an external pull-up resistor to $V_{CC}$ if the interrupt feature is required; otherwise, it may be left floating.

### 7.3.4 Reset Input ($\overline{RESET}$)

The $\overline{RESET}$ input can be asserted to initialize the system while keeping the $V_{CC}$ supply at its operating level. A reset can be accomplished by holding the $\overline{RESET}$ pin low for a minimum of $t_W$. The TCAL9538 registers and $I^2C$/SMBus state machine are changed to their default state once $\overline{RESET}$ is low (0). When $\overline{RESET}$ is high (1), the I/O levels at the P port can be changed externally or through the controller. This input requires a pull-up resistor to $V_{CC}$, if no active connection is used. When $\overline{RESET}$ is toggled the input port register is updated to reflect the state of the GPIO pins.

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### 7.3.5 Software Reset Call

The software reset call is a command sent from the controller on the $I^2C$ bus that instructs all devices that support the command to be reset to the power-up default state. To function as expected, the $I^2C$ bus must be functional, and no devices can be hanging the bus.

The software reset call is defined as the following steps:

1. A start condition is sent by the $I^2C$ bus controller.
2. The address used is the reserved general call $I^2C$ bus address '0000 0000' with the R/W bit set to 0. The byte sent is 0x00.
3. Any devices supporting the general call functionality will ACK. If the R/W bit is set to 1 (read), the device will NACK.
4. Once the general call address is acknowledged, the controller sends only 1 byte of data equal to 0x06. If the data byte is any other value, the device does not acknowledge or reset. If more than 1 byte is sent, no more bytes is acknowledged, and the device ignores the $I^2C$ message considering as invalid.
5. After the 1 byte of data (0x06) is sent, the controller sends a STOP condition to end the Software Reset sequence. A repeated START condition is ignored by the device and no reset is performed.

Once the above steps are completed successfully, the device performs a reset. This clears all register values back to power-on defaults.

## 7.4 Device Functional Modes

### 7.4.1 Power-On Reset

When power (from 0 V) is applied to $V_{CC}$, an internal power-on reset holds the TCAL9538 in a reset condition until the supply has reached $V_{POR}$. At that time, the reset condition is released, and the TCAL9538 registers and $I^2C$/SMBus state machine initializes to their default states. After that, $V_{CC}$ must be lowered to below $V_{PORF}$ and back up to the operating voltage for a power-reset cycle.

## 7.5 Programming

### 7.5.1 $I^2C$ Interface

The bidirectional $I^2C$ bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

$I^2C$ communication with this device is initiated by a controller sending a Start condition, a high-to-low transition on the SDA input/output, while the SCL input is high (see Figure 7-4). After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/ $\overline{W}$).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. The address input of the target device must not be changed between the Start and the Stop conditions.

On the $I^2C$ bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see Figure 7-5).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the controller (see Figure 7-4).

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 7-6). When a target receiver is addressed, it must generate an ACK after each byte is received. Similarly, the controller must generate an ACK after each byte that it receives from the target transmitter. Setup and hold times must be met for proper operation.


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A controller receiver signals an end of data to the target transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the target. This is done by the controller receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the controller to generate a Stop condition.

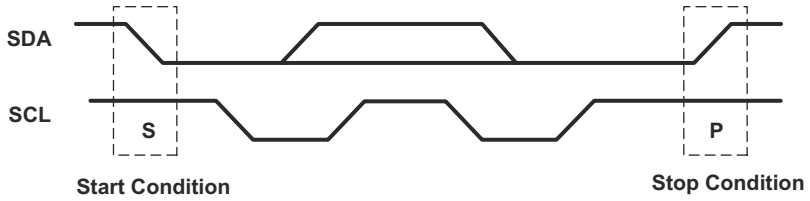


**Figure 7-4. Definition of Start and Stop Conditions**

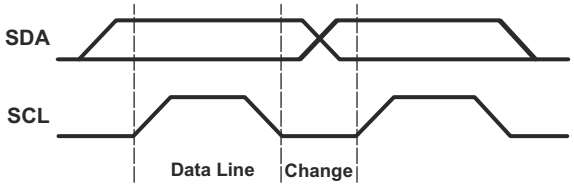


**Figure 7-5. Bit Transfer**

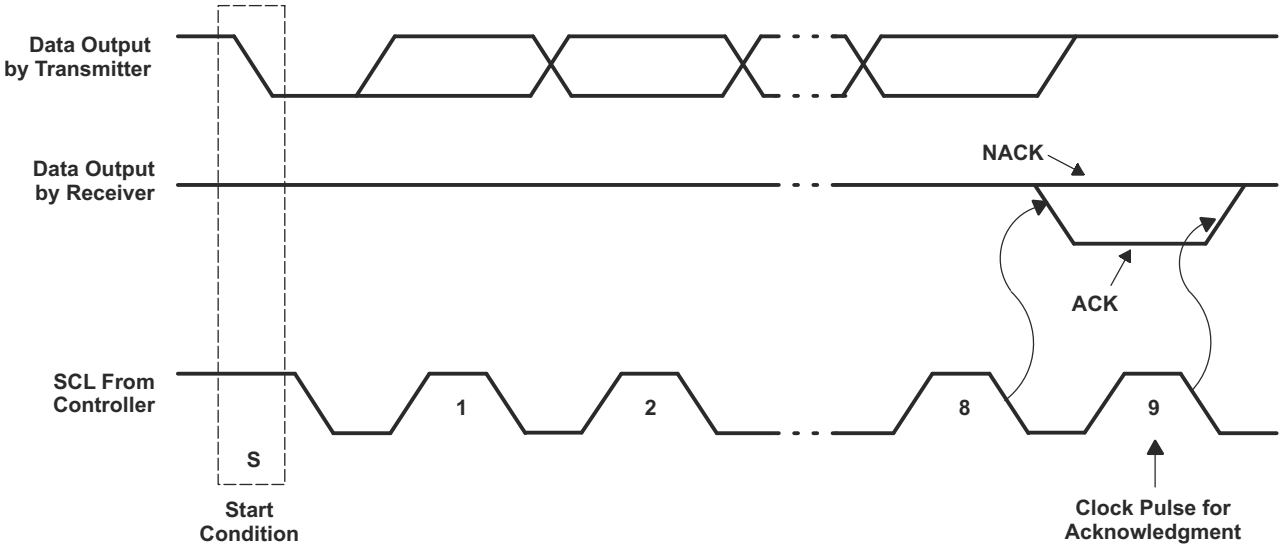


**Figure 7-6. Acknowledgment on the $I^2C$ Bus**

**Table 7-1. Interface Definition**

| BYTE | BIT | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 (MSB) | 6 | 5 | 4 | 3 | 2 | 1 | 0 (LSB) |
| Device $I^2C$ address | H | H | H | L | L | A1 | A0 | R/ $\overline{W}$ |
| I/O data bus | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |

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## 7.6 Register Maps

### 7.6.1 Device Address

The address of the TCAL9538 is shown in Figure 7-7.

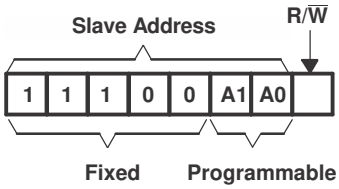


**Figure 7-7. TCAL9538 Address**

**Table 7-2. Address Reference**

| Inputs | | $I^2C$ BUS TARGET ADDRESS |
|---|---|---|
| A1 | A0 | |
| L | L | 112 (decimal), 70 (hexadecimal) |
| L | H | 113 (decimal), 71 (hexadecimal) |
| H | L | 114 (decimal), 72 (hexadecimal) |
| H | H | 115 (decimal), 73 (hexadecimal) |

The last bit of the target address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.


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### 7.6.2 Control Register and Command Byte

Following the successful acknowledgment of the address byte, the bus controller sends a command byte, which is stored in the control register in the TCAL9538. The lower two bits of this data byte reflect the internal registers (input, output, polarity inversion, or configuration) that are affected. Bit 6 in conjunction with the lower four bits of the Command byte are used to point to the extended features of the device (Agile IO). The command byte is sent only during a write transmission.

Once a new command has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent. Upon power-up, hardware reset, or software reset, the control register defaults to 00h.

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|

**Figure 7-8. Control Register Bits**

**Table 7-3. Command Byte**

| CONTROL REGISTER BITS | | | | | | | | COMMAND BYTE (HEX) | REGISTER | PROTOCOL | POWER-UP DEFAULT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 | Input Port | Read byte | xxxx xxxx |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01 | Output Port | Read/write byte | 1111 1111 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 02 | Polarity Inversion | Read/write byte | 0000 0000 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 03 | Configuration | Read/write byte | 1111 1111 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 40 | Output Drive Strength 0 | Read/write byte | 1111 1111 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 41 | Output Drive Strength 1 | Read/write byte | 1111 1111 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 42 | Input latch register | Read/write byte | 0000 0000 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 43 | Pull-up/pull-down enable register | Read/write byte | 0000 0000 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 44 | pull-up/pull-down selection register | Read/write byte | 1111 1111 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 45 | Interrupt mask register | Read/write byte | 1111 1111 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 46 | Interrupt status register | Read byte | 0000 0000 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 4F | Output port configuration register | Read/write byte | 0000 0000 |

### 7.6.3 Register Descriptions

The Input Port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. The input port register is read only. Writes to this register have no effect. The default value (X) is determined by the externally applied logic level. Before a read operation, a write transmission is sent with the command byte to indicate to the $I^2C$ device that the Input Port register will be accessed next.

**Table 7-4. Register 0 (Input Port Register)**

| BIT | I-7 | I-6 | I-5 | I-4 | I-3 | I-2 | I-1 | I-0 |
|---|---|---|---|---|---|---|---|---|
| DEFAULT | X | X | X | X | X | X | X | X |

The Output Port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

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**Table 7-5. Register 1 (Output Port Register)**

| BIT | O-7 | O-6 | O-5 | O-4 | O-3 | O-2 | O-1 | O-0 |
|---|---|---|---|---|---|---|---|---|
| DEFAULT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

The Polarity Inversion register (register 2) allows polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written to '1'), the corresponding port pin polarity is inverted. If a bit in this register is cleared (written to a '0'), the corresponding port pin's original polarity is retained.

**Table 7-6. Register 2 (Polarity Inversion Register)**

| BIT | P-7 | P-6 | P-5 | P-4 | P-3 | P-2 | P-1 | P-0 |
|---|---|---|---|---|---|---|---|---|
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The Configuration register (register 3) configures the direction of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

**Table 7-7. Register 3 (Configuration Register)**

| BIT | C-7 | C-6 | C-5 | C-4 | C-3 | C-2 | C-1 | C-0 |
|---|---|---|---|---|---|---|---|---|
| DEFAULT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

The output drive strength registers control the output drive level of the P port GPIO buffers. Each GPIO can be configured independently to the desired output current level by two register control bits. For example, Port P7 is controlled by register 41 (bits 7 and 6), port P6 is controlled by register 41 (bits 5 and 4), and so on. The output drive level of the GPIO is programmed 00b = 0.25x drive strength, 01b = 0.5x drive strength, 10b = 0.75x drive strength, or 11b = 1x for full drive strength capability.

**Table 7-8. Registers 40, and 41 (Output Drive Strength Registers)**

| BIT | CC-3 | CC-3 | CC-2 | CC-2 | CC-1 | CC-1 | CC-0 | CC-0 |
|---|---|---|---|---|---|---|---|---|
| DEFAULT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| BIT | CC-7 | CC-7 | CC-6 | CC-6 | CC-5 | CC-5 | CC-4 | CC-4 |
| DEFAULT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

The Input latch register enables and disables the input latch feature of the P port GPIO pins. This register is effective only when the pin is configured as an input port. When an input latch register bit is 0, the corresponding input pin state is not latched. A state change in the corresponding input pin generates an interrupt. A read of the input register clears the interrupt. If the input goes back to its initial logic state before the input port register is read, then the interrupt is cleared.

When an input latch register bit is set to 1, the corresponding input pin state is latched. A change of state of the input generates an interrupt and the input logic value is loaded into the corresponding bit of the input port register (registers 0 and 1). A read of the input port register clears the interrupt. However, if the input pin returns to its initial logic state before the input port register is read, then the interrupt is not cleared and the corresponding bit of the input port register keeps the logic value that initiated the interrupt.

For example, if the P4 input was at a logic 0 state and then transitions to a logic 1 state followed by going back to the logic 0 state, the input port register will capture this change and an interrupt will be generated (if unmasked). When the read is performed on the input port 0 register, the interrupt is cleared, assuming there were no additional inputs that have changed, and bit 4 of the input port register will read '1'. The next read of the input port register bit 4 should now read '0'.

An interrupt remains active when a non-latched input simultaneously switches state with a latched input and then returns to its original state. A read of the input register reflects only the change of state of the latched input and also clears the interrupt. If the input latch register changes from a latched to a non-latched configuration, the interrupt will be cleared if the input logic value returns to its original state.


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If the input pin is changed from a latched to a non-latched input, a read from the input port register reflects the current port logic level. If the input pin is changed from a non-latched to a latched input, the read from the input register reflects the latched logic level.

**Table 7-9. Register 42 (Input Latch Register)**

| BIT | L-7 | L-6 | L-5 | L-4 | L-3 | L-2 | L-1 | L-0 |
|---|---|---|---|---|---|---|---|---|
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The pull-up/pull-down enable register allows the user to enable or disable pull-up/pull-down resistors on the GPIO pins. Setting the bit to logic 1 enables the selection of pull-up/pull-down resistors. Setting the bit to logic 0 disconnects the pull-up/pull-down resistors from the GPIO pins. The resistors are disabled when the GPIOs are configured as outputs Use the pull-up/pull-down selection register to select either a pull-up or pull-down resistor.

**Table 7-10. Register 43 (Pull-Up/Pull-Down Enable Register)**

| BIT | PE-7 | PE-6 | PE-5 | PE-4 | PE-3 | PE-2 | PE-1 | PE-0 |
|---|---|---|---|---|---|---|---|---|
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The pull-up/pull-down selection register allows the user to configure each GPIO to have a pull-up or pull-down resistor by programming the respective register bit. Setting a bit to a logic 1 selects a 100 kΩ pull-up resistor for that GPIO pin. Setting a bit to logic 0 selects a 100 kΩ pull-down resistor for that GPIO pin. If the pull-up/pull-down feature is disabled via register 43, writing to this register has no effect on the GPIO pin.

**Table 7-11. Register 44 (Pull-Up/Pull-Down Selection Register)**

| BIT | PUD-7 | PUD-6 | PUD-5 | PUD-4 | PUD-3 | PUD-2 | PUD-1 | PUD-0 |
|---|---|---|---|---|---|---|---|---|
| DEFAULT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

The Interrupt mask register is defaulted to logic 1 upon power-on, disabling interrupts during system start-up. Interrupts may be enabled by setting corresponding mask bits to logic 0.

If an input changes state and the corresponding bit in the interrupt mask register is to 1, the interrupt is masked and the interrupt pin is not asserted. If the corresponding bit in the interrupt mask register is set to 0, the interrupt pin is asserted.

When an input changes state and the resulting interrupt is masked, setting the interrupt mask register bit to 0 will cause the interrupt pin to be asserted. If the interrupt mask bit of an input that is already currently the source of an interrupt is set to 1, the interrupt pin is de-asserted.

**Table 7-12. Register 45 (Interrupt Mask Register)**

| BIT | M-7 | M-6 | M-5 | M-4 | M-3 | M-2 | M-1 | M-0 |
|---|---|---|---|---|---|---|---|---|
| DEFAULT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

The Interrupt status register is a read only register used to identify the source of an interrupt. When read, a logic 1 indicates that the corresponding input pin was the source of the interrupt. A logic 0 indicates that the input pin is not the source of an interrupt. When a corresponding bit in the interrupt mask register is set to 1 (masked), the interrupt status bit will return to logic 0.

**Table 7-13. Register 46 (Interrupt Status Register)**

| BIT | S-7 | S-6 | S-5 | S-4 | S-3 | S-2 | S-1 | S-0 |
|---|---|---|---|---|---|---|---|---|
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The output port configuration register selects port-wise push-pull or open-drain I/O stage. A logic 0 configures the I/O as push-pull ( Q1 and Q2 are active, see Figure 7-2). A logic 1 configures the I/O as open-drain ( Q1

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is disabled, Q2 is active) and the recommended command sequence is to program this register (4F) before the Configuration register (03) sets the port pins as outputs.

**Table 7-14. Register 4F (Output Port Configuration Register)**

| BIT | Reserved | | | | | | | ODEN-0 |
|---|---|---|---|---|---|---|---|---|
| DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 7.6.4 Bus Transactions

Data is exchanged between the controller and TCAL9538 through write and read commands.

#### *7.6.4.1 Writes*

Data is transmitted to the TCAL9538 by sending the device address and setting the least-significant bit (LSB) to a logic 0 (see Figure 7-7 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte. There is no limitation on the number of data bytes sent in one write transmission.

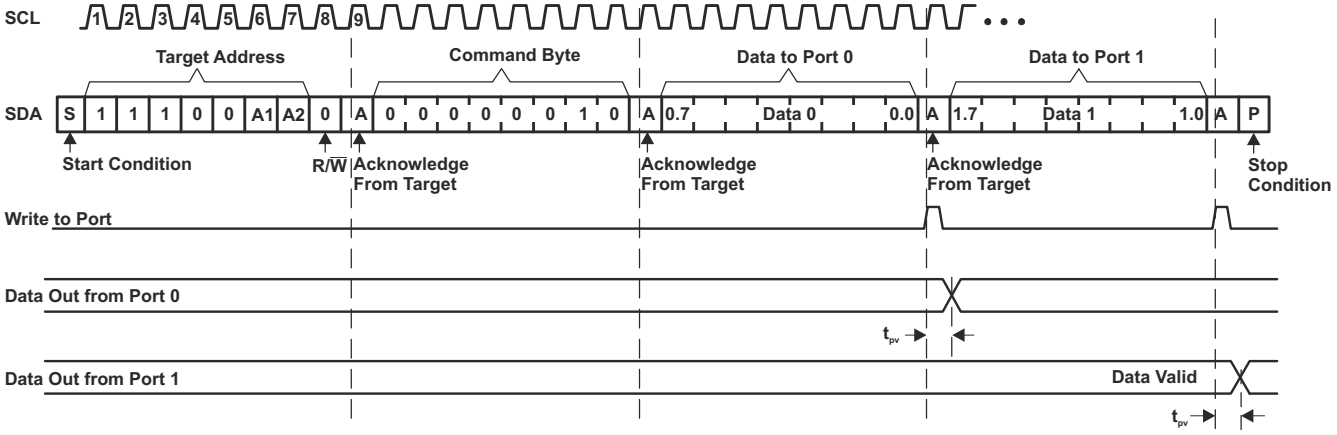


**Figure 7-9. Write to Output Port Registers**

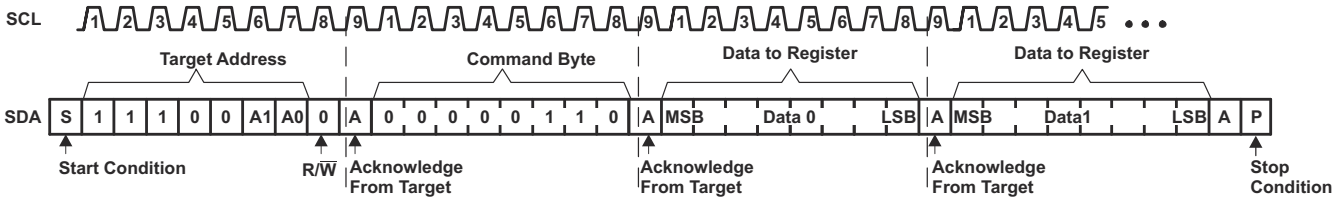


**Figure 7-10. Write to Configuration Registers**

#### *7.6.4.2 Reads*

The bus controller first must send the TCAL9538 address with the LSB set to a logic 0 (see Figure 7-7 for device address). The command byte is sent after the address and determines which register is accessed.

Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus controller must not acknowledge the data.


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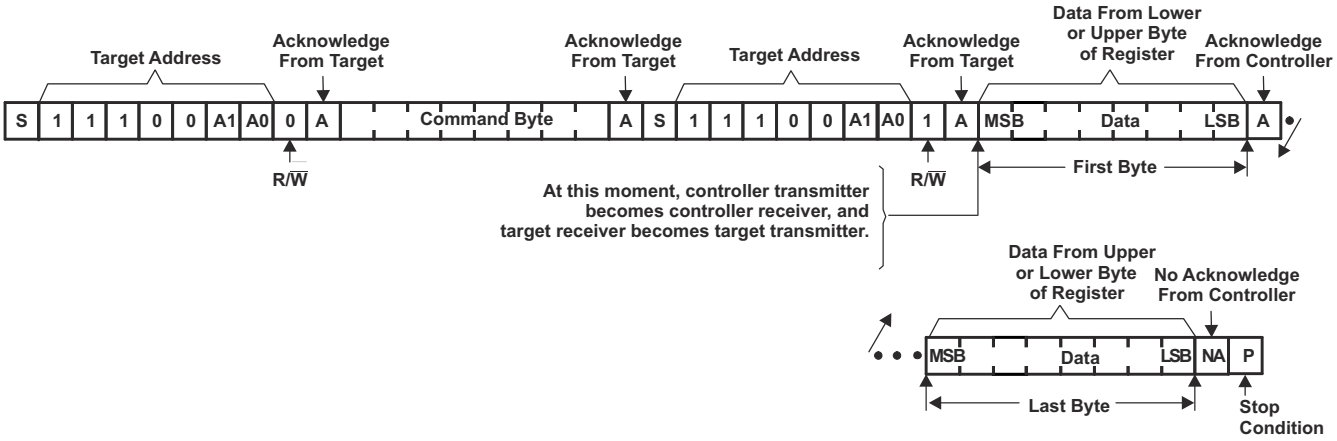
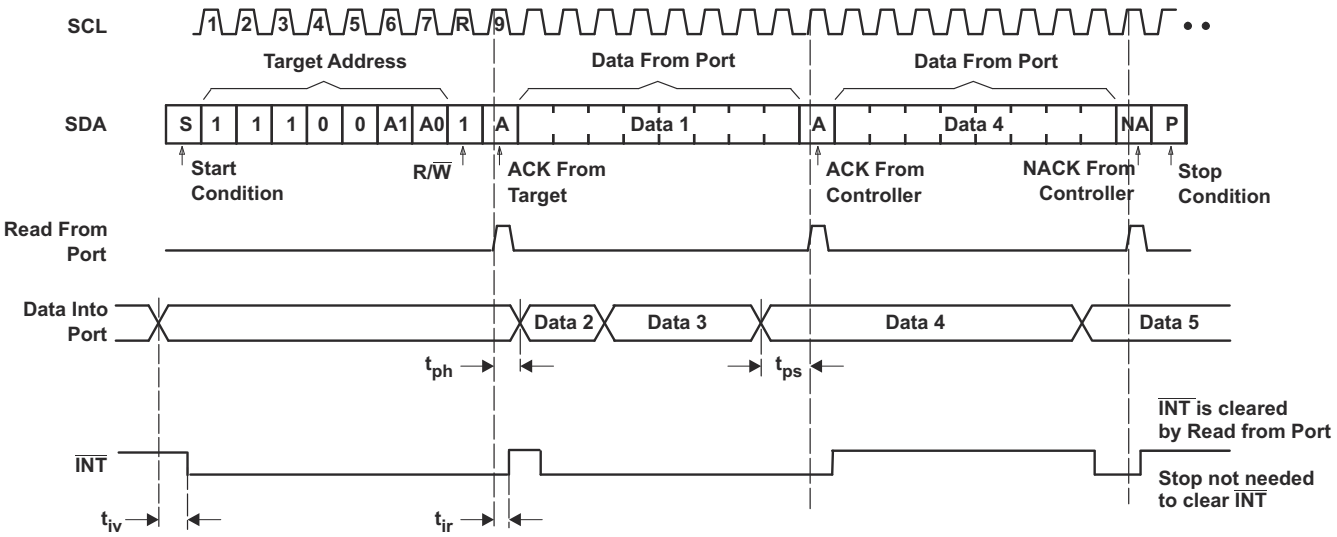



**Figure 7-11. Read From Register**




A. Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (read Input Port register).

B. This figure eliminates the command byte transfer, a restart, and target address call between the initial target address call and actual data transfer from P port (see Figure 7-11).

**Figure 7-12. Read Input Port Register**

# 8 Application and Implementation

**Note**

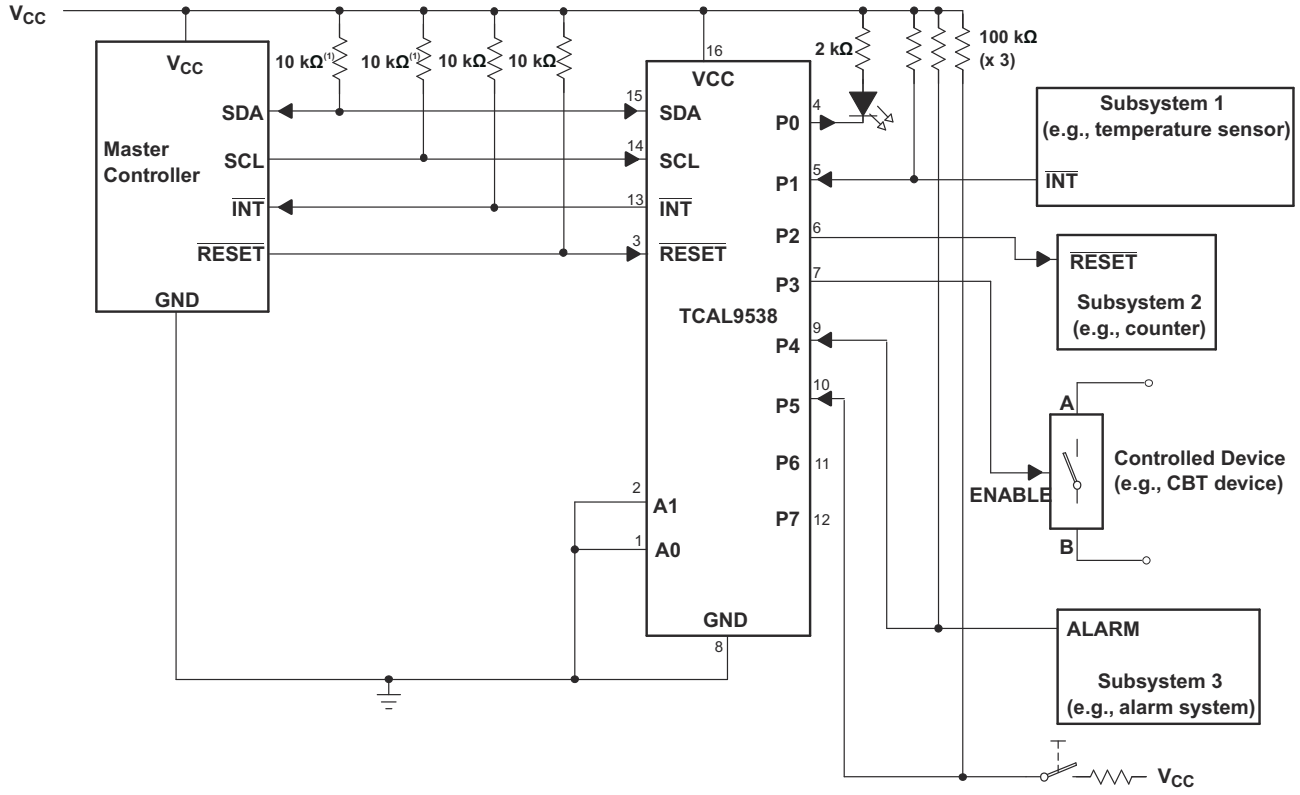
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

Applications of the TCAL9538 use this device connected as a target to an $I^2C$ controller (processor), and the $I^2C$ bus may contain any number of other target devices. The TCAL9538 is in a remote location from the controller, placed close to the GPIOs to which the controller needs to monitor or control.

## 8.2 Typical Application

Figure 8-1 shows an application in which the TCAL9538 can be used.




A. Device address configured as 1110000 for this example.
B. P0, P2 and P3 are configured as outputs.
C. P1, P4, and P5 are configured as inputs.
D. Resistors are required for inputs (on P port) that may float. If a driver to an input will never let the input float, a resistor is not needed. Outputs (in the P port) do not need pullup resistors.

**Figure 8-1. Typical Application Schematic**

### 8.2.1 Design Requirements

**Table 8-1. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Supply Voltage ($V_{CC}$) | 1.8 V |


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**Table 8-1. Design Parameters (continued)**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Output current rating, P-port sinking ($I_{OL}$) | 25 mA |
| Output current rating, P-port sourcing ($I_{OH}$) | 10 mA |
| $I^2C$ bus clock (SCL) speed | 1 MHz |

### 8.2.2 Detailed Design Procedure

The pull-up resistors, $R_P$, for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all targets on the $I^2C$ bus. The minimum pull-up resistance is a function of $V_{CC}$, $V_{OL,(max)}$, and $I_{OL}$:

$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}} \quad (1)$$

The maximum pull-up resistance is a function of the maximum rise time, $t_r$ (120 ns for fast-mode-plus operation, $f_{SCL}$ = 1 MHz) and bus capacitance, $C_b$:

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$

The maximum bus capacitance for an $I^2C$ bus must not exceed 400 pF for standard-mode or fast-mode operation, or 550 pF for fast-mode-plus. The bus capacitance can be approximated by adding the capacitance of the TCAL9538, $C_i$ for SCL, or $C_{io}$ for SDA. Plus the capacitance of wires, connections, traces, and the capacitance of additional targets on the bus.

#### *8.2.2.1 Minimizing $I_{CC}$ When I/Os Control LEDs*

When the I/Os are used to control LEDs, normally they are connected to $V_{CC}$ through a resistor as shown in Figure 8-2. For a P-port configured as an input, current consumption increases as $V_I$ becomes lower than $V_{CC}$. The LED is a diode, with threshold voltage $V_T$, and when a P-port is configured as an input the LED are off, but $V_I$ is a $V_T$ drop below $V_{CC}$.

For battery-powered applications, it is essential that the voltage of P-ports controlling LEDs is greater than or equal to $V_{CC}$ when the P-ports are configured as input to minimize current consumption. Figure 8-2 shows a high-value resistor in parallel with the LED. Figure 8-3 shows $V_{CC}$ less than the LED supply voltage by at least $V_T$. Both of these methods maintain the I/O $V_I$ at or above $V_{CC}$ and prevent additional supply current consumption when the P-port is configured as an input and the LED is off.

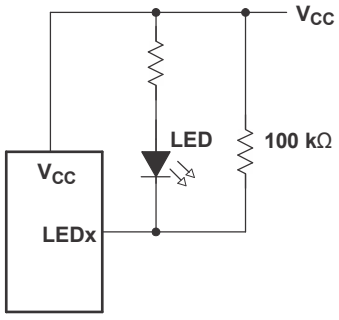


**Figure 8-2. High-Value Resistor in Parallel with LED**

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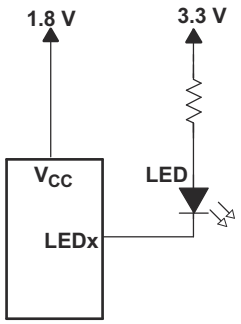
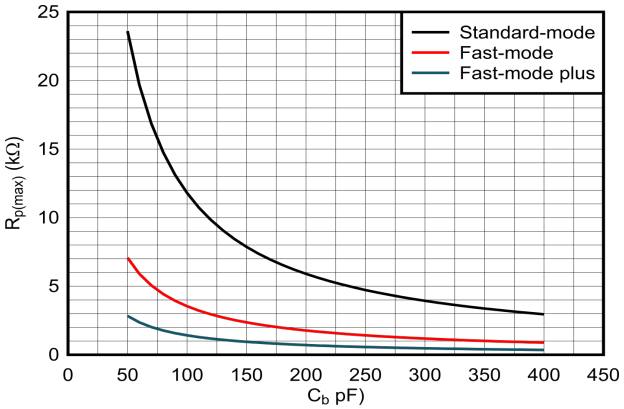



**Figure 8-3. Device Supplied by a Lower Voltage**

### 8.2.3 Application Curves




| | | |
|---|---|---|
| Standard-mode: | $f_{SCL}$ = 100 kHz | $t_r$ = 1 µs |
| Fast-mode: | $f_{SCL}$ = 400 kHz | $t_r$ = 300 ns |
| Fast-mode plus: | $f_{SCL}$ = 1 MHz | $t_r$ = 120 ns |

**Figure 8-4. Maximum Pullup Resistance ($R_{p(max)}$) vs Bus Capacitance ($C_b$)**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## 8.3 Power Supply Recommendations

### 8.3.1 Power-On Reset Requirements

In the event of a glitch or data corruption, TCAL9538 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in Figure 8-5 and Figure 8-6.

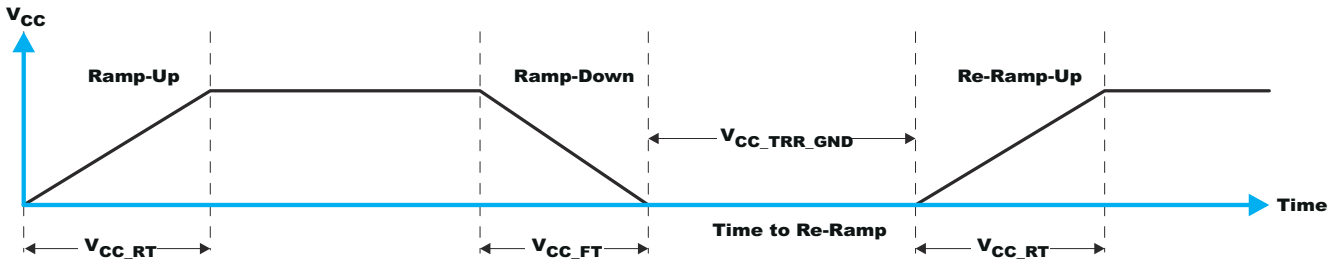


**Figure 8-5. V is lowered below 0.2 V or 0 V and then ramped up**

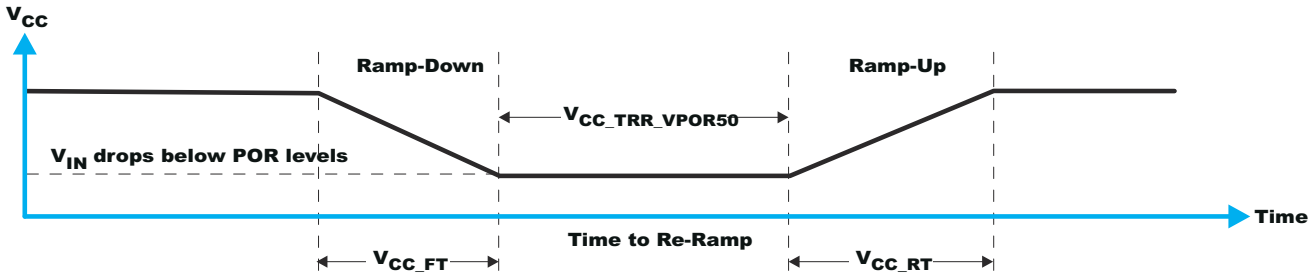


**Figure 8-6. V is lowered below the POR threshold, then ramped back up**

Table 8-2 specifies the performance of the power-on reset feature for TCAL9538 for both types of power-on reset.

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**Table 8-2. Recommended Supply Sequencing and Ramp Rates**

| PARAMETER(1) (2) | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{FT}$ | Fall rate | See Figure 8-5 | 0.1 | | 2000 | ms |
| $t_{RT}$ | Rise rate | See Figure 8-5 | 0.1 | | 2000 | ms |
| $t_{TRR\_GND}$ | Time to re-ramp (when $V_{CC}$ drops to GND) | See Figure 8-5 | 1 | | | µs |
| $t_{TRR\_POR50}$ | Time to re-ramp (when $V_{CC}$ drops to $V_{POR\_MIN}$ – 50 mV) | See Figure 8-6 | 1 | | | µs |
| $V_{CC\_GH}$ | Level that V can glitch down to, but not cause a functional disruption when V = 1 µs | See Figure 8-7 | | | 1.0 | V |
| $t_{GW}$ | Glitch width that will not cause a functional disruption when V = 0.5 × $V_{CCx}$ | See Figure 8-7 | | | 10 | µs |
| $V_{PORF}$ | Voltage trip point of POR on falling $V_{CC}$ | | 0.6 | | | V |
| $V_{PORR}$ | Voltage trip point of POR on rising $V_{CC}$ | | | | 1.0 | V |

(1) $T_A$ = 25°C (unless otherwise noted).
(2) Not tested. Specified by design.

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ($V_{CC\_GW}$) and height ($V_{CC\_GH}$) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 8-7 and Table 8-2 provide more information on how to measure these specifications.

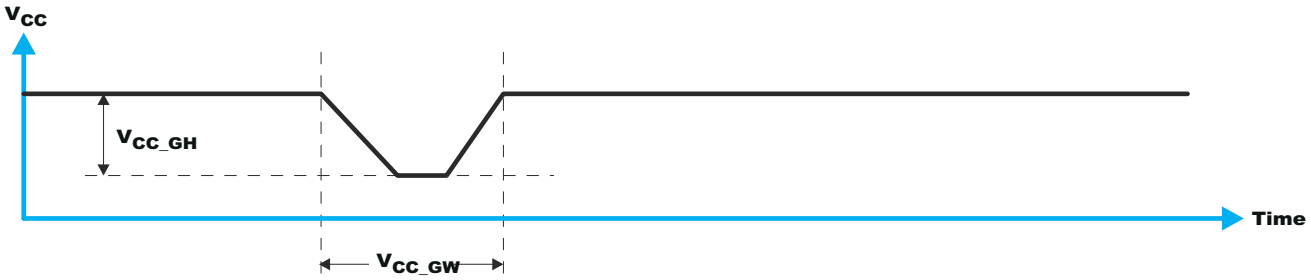


**Figure 8-7. Glitch Width and Glitch Height**

$V_{POR}$ is critical to the power-on reset. $V_{POR}$ is the voltage level at which the reset condition is released and all the registers and the $I^2C$/SMBus state machine are initialized to their default states. The value of $V_{POR}$ differs based on the V being lowered to or from 0. Figure 8-8 and Table 8-2 provide more details on this specification.


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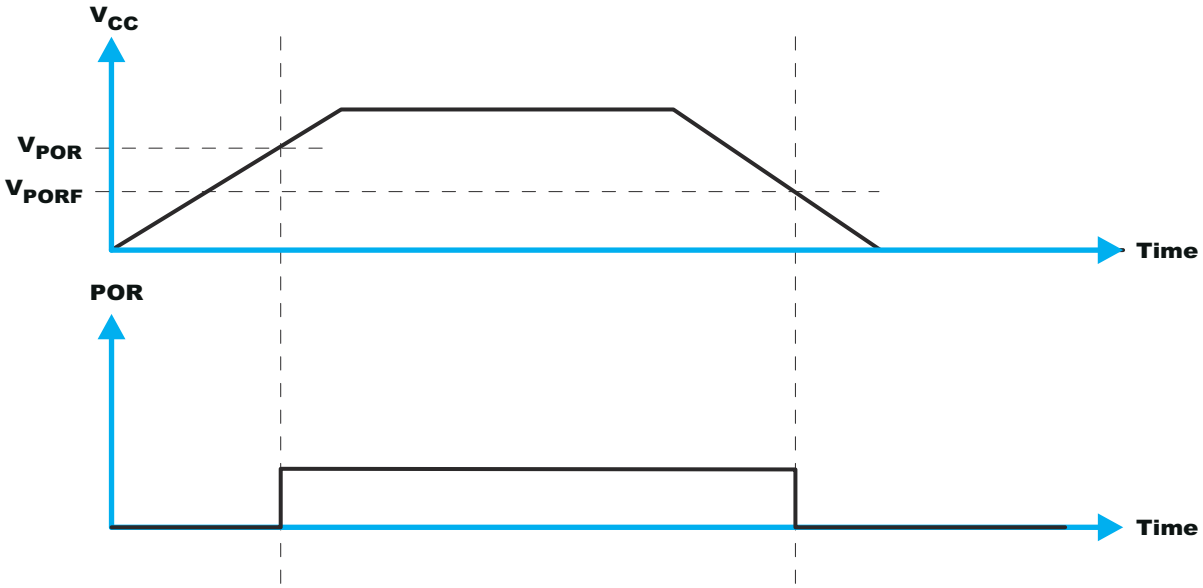


**Figure 8-8. $V_{POR}$**

## 8.4 Layout

### 8.4.1 Layout Guidelines

For printed circuit board (PCB) layout of the TCAL9538, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedance and differential pairs are not a concern for $I^2C$ signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and decoupling capacitors are commonly used to control the voltage on the supply pins, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple. These capacitors should be placed as close to the TCAL9538 as possible. These best practices are shown in Figure 8-9.

For the layout example provided in Figure 8-9, it is possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power and ground (GND). However, a 4 layer board is preferable for boards with higher density signal routing. On a 4 layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to power or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated in Figure 8-9.


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### 8.4.2 Layout Example

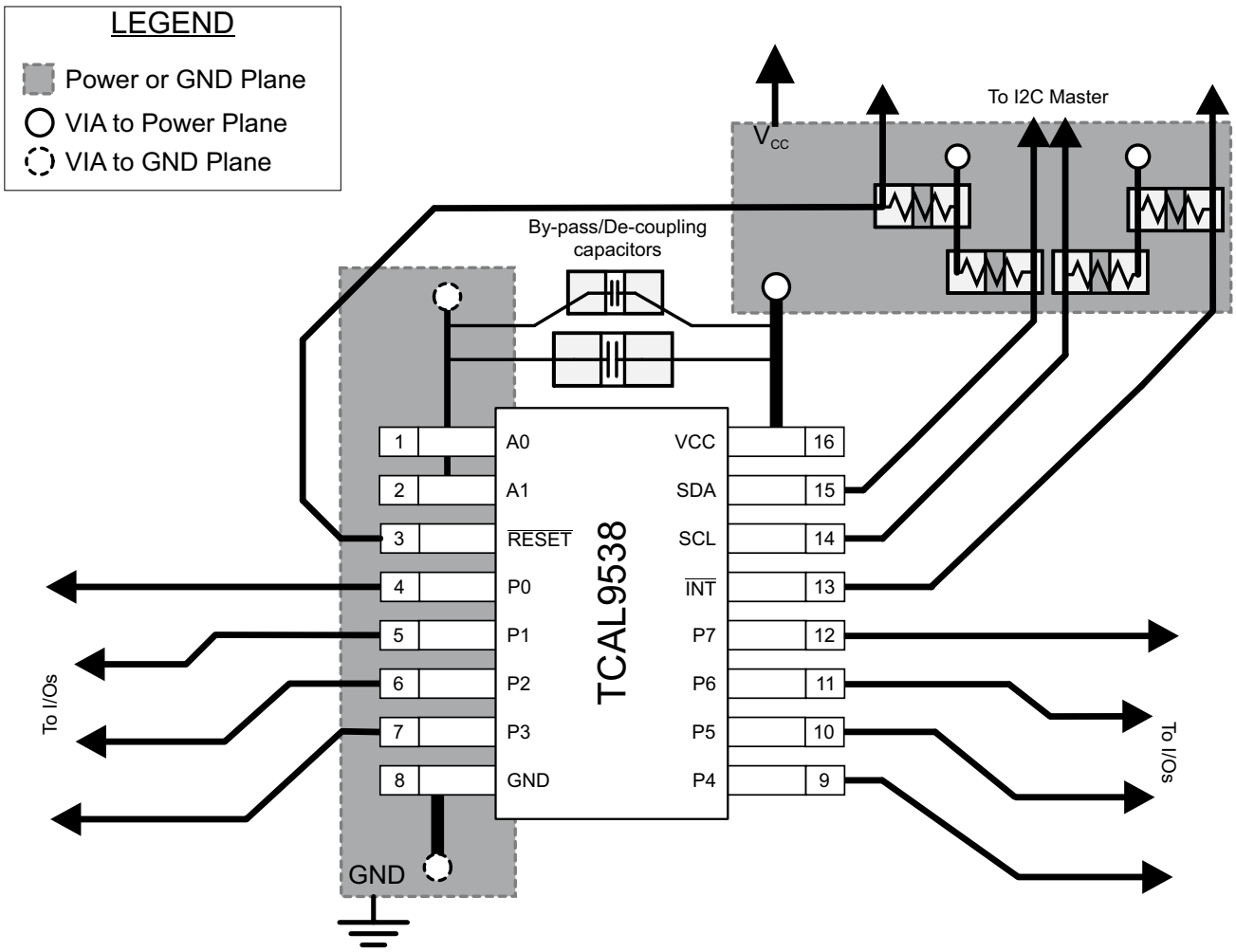


**Figure 8-9. TCAL9538 Layout**

# 9 Device and Documentation Support

## 9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.5 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision * (November 2022) to Revision A (November 2023) | Page |
|---|---|
| • Changed the document status from *Advanced Information* to *Production* data | 1 |

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TCAL9538DTUR | ACTIVE | X2QFN | DTU | 16 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | NJ | Samples |
| TCAL9538PWR | ACTIVE | TSSOP | PW | 16 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TL9538 | Samples |
| TCAL9538RSVR | ACTIVE | UQFN | RSV | 16 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 9538 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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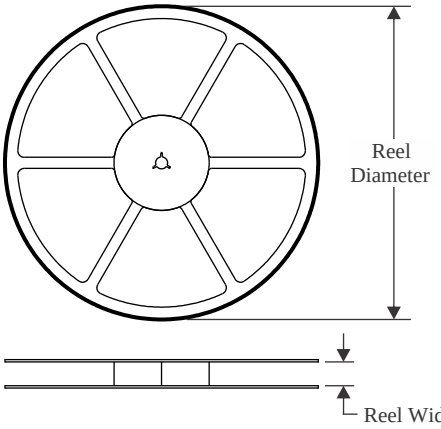
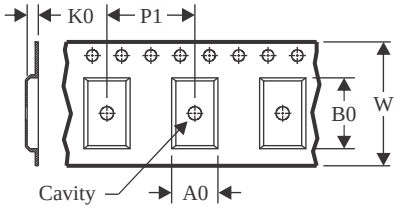
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

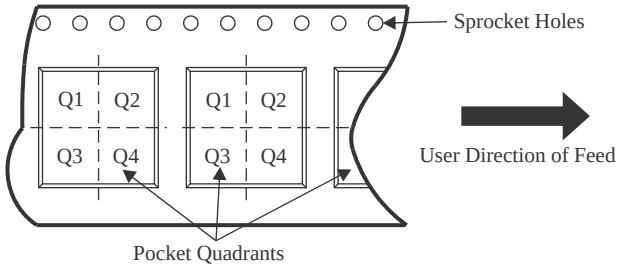



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

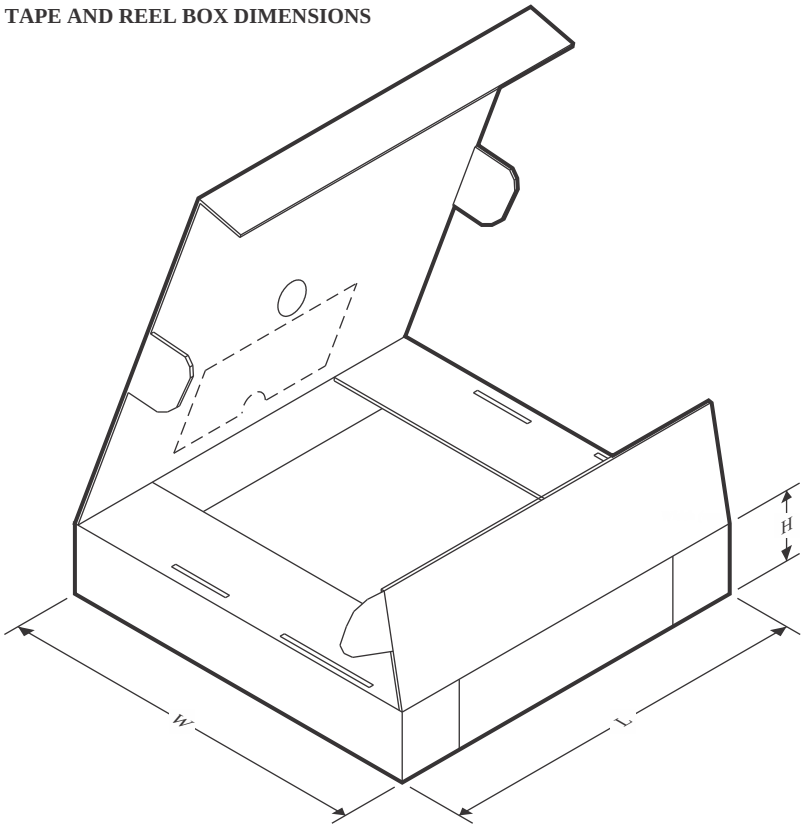
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TCAL9538DTUR | X2QFN | DTU | 16 | 3000 | 180.0 | 9.5 | 1.75 | 1.75 | 0.5 | 4.0 | 8.0 | Q1 |
| TCAL9538PWR | TSSOP | PW | 16 | 3000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TCAL9538RSVR | UQFN | RSV | 16 | 3000 | 178.0 | 13.5 | 2.1 | 2.9 | 0.75 | 4.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

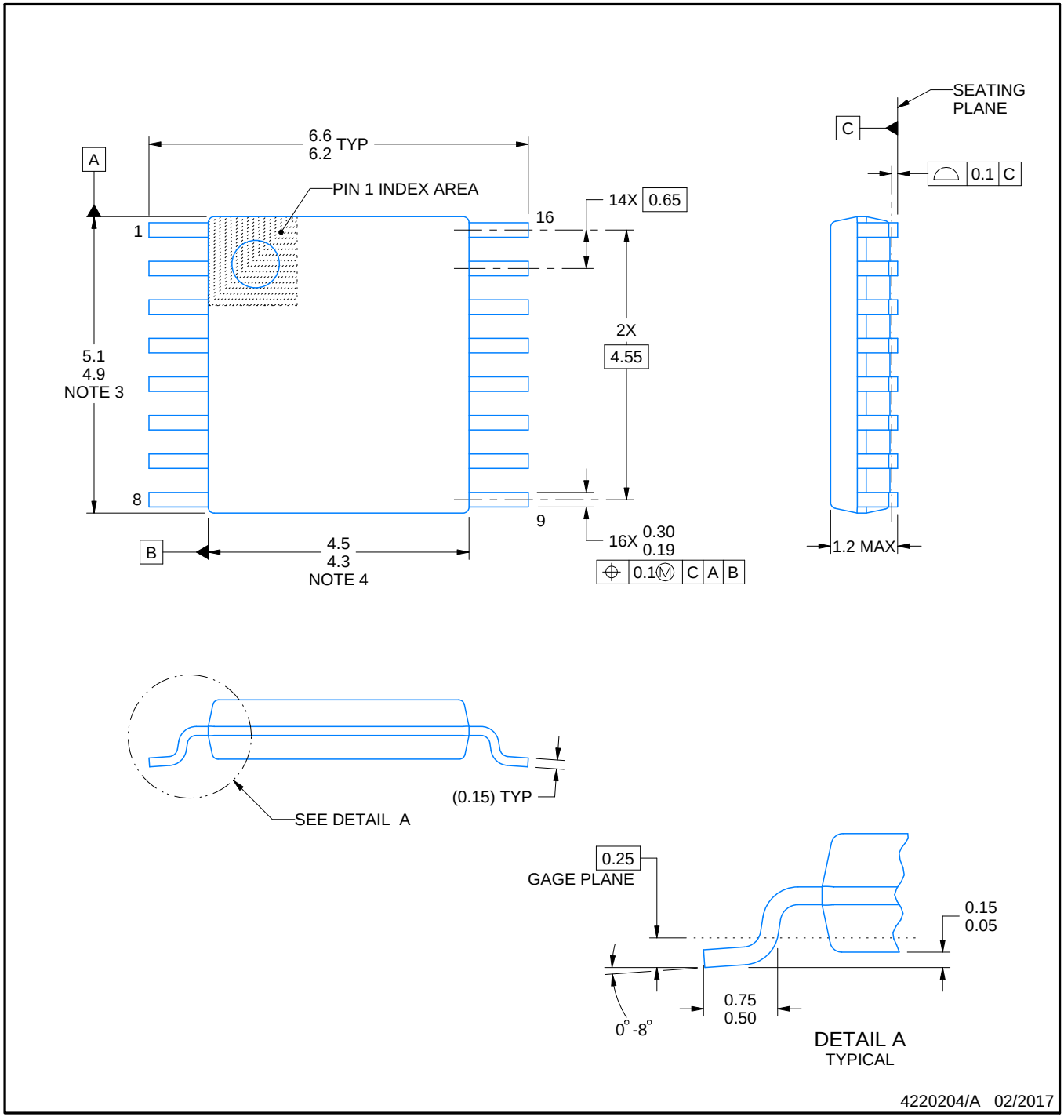
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TCAL9538DTUR | X2QFN | DTU | 16 | 3000 | 189.0 | 185.0 | 36.0 |
| TCAL9538PWR | TSSOP | PW | 16 | 3000 | 356.0 | 356.0 | 35.0 |
| TCAL9538RSVR | UQFN | RSV | 16 | 3000 | 189.0 | 185.0 | 36.0 |

# PACKAGE OUTLINE

## PW0016A

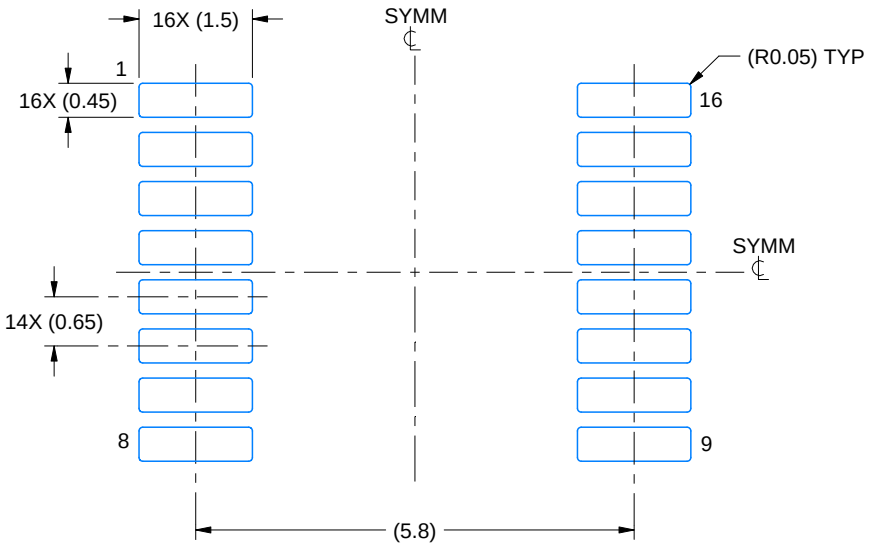
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

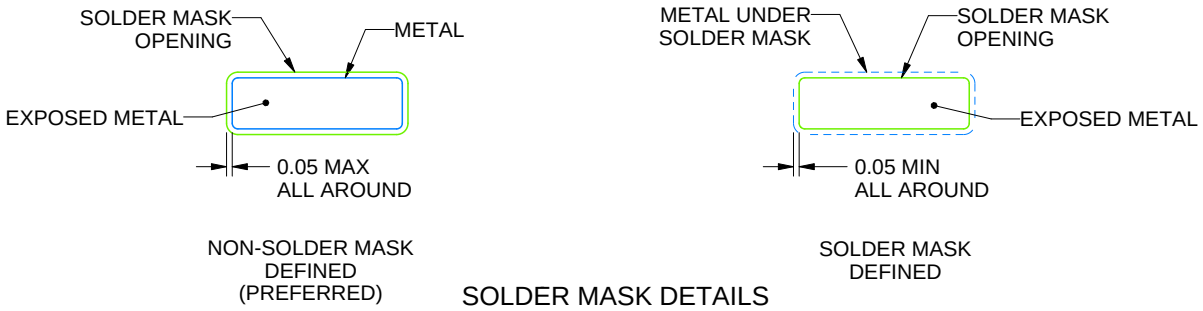



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

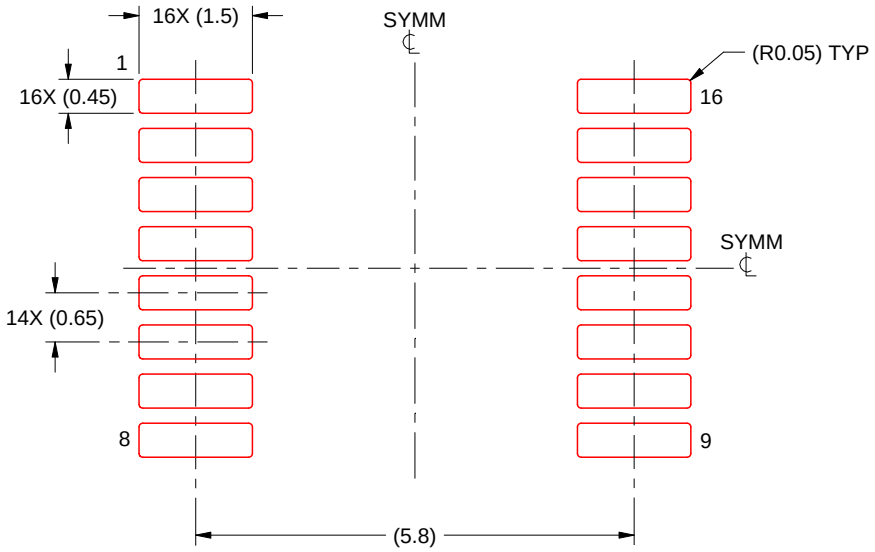



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

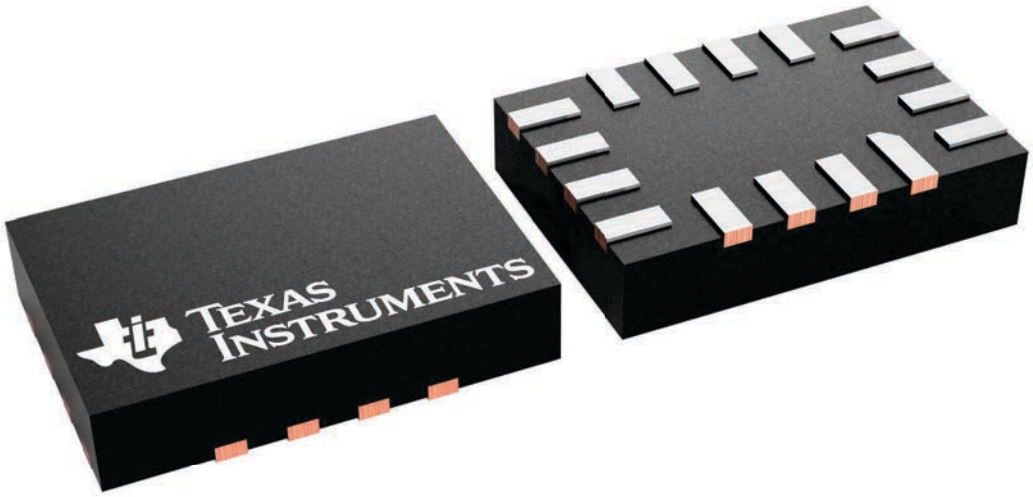
## RSV 16

## UQFN - 0.55 mm max height

**1.8 x 2.6, 0.4 mm pitch**

ULTRA THIN QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



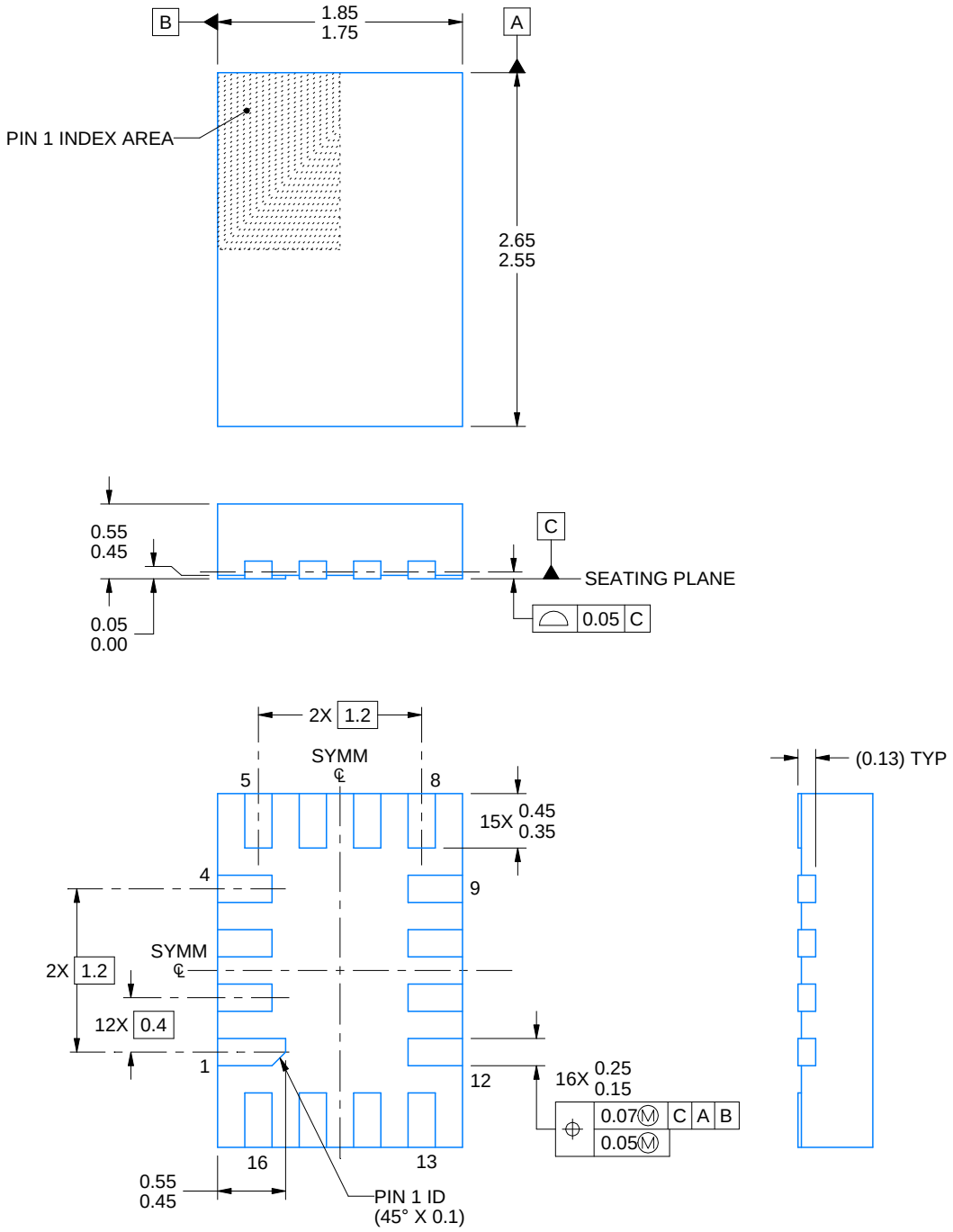

4231225/A

# RSV0016A

# PACKAGE OUTLINE

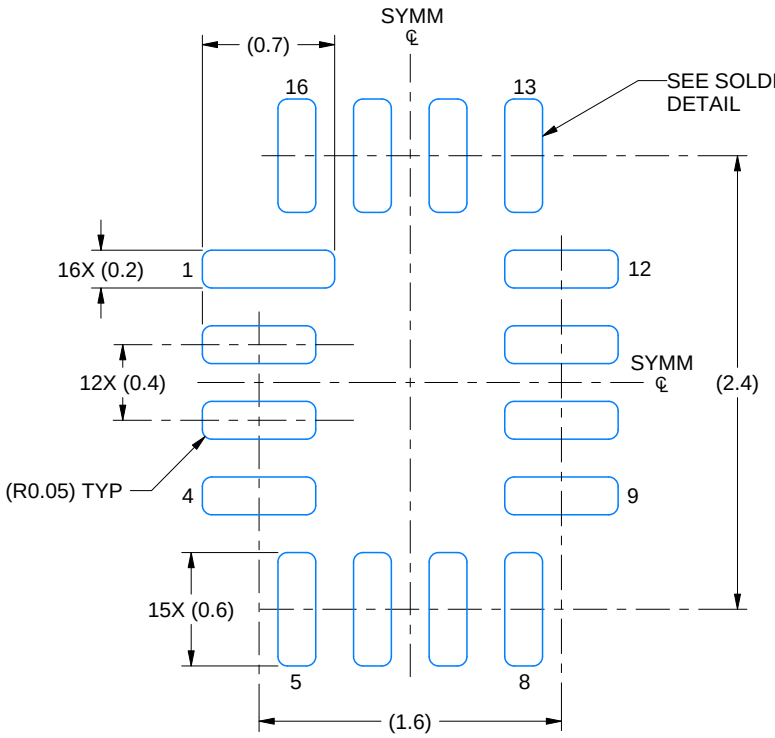
## UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD

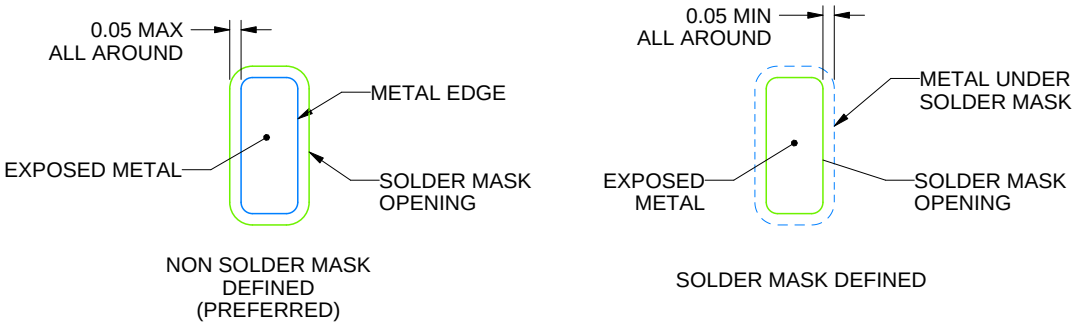



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

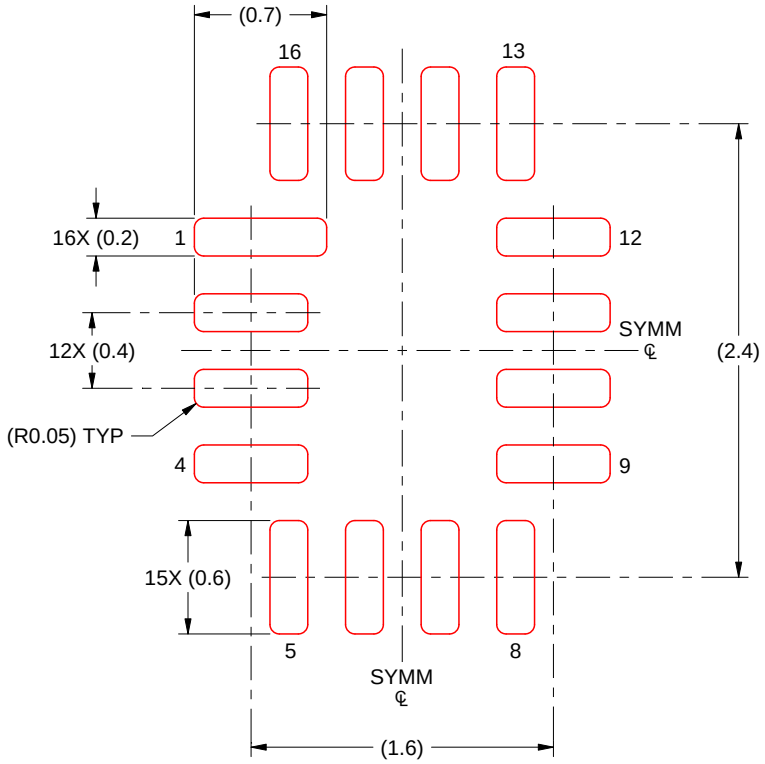



SOLDER MASK DETAILS

4220314/C 02/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).




SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 25X

4220314/C 02/2020

NOTES: (continued)

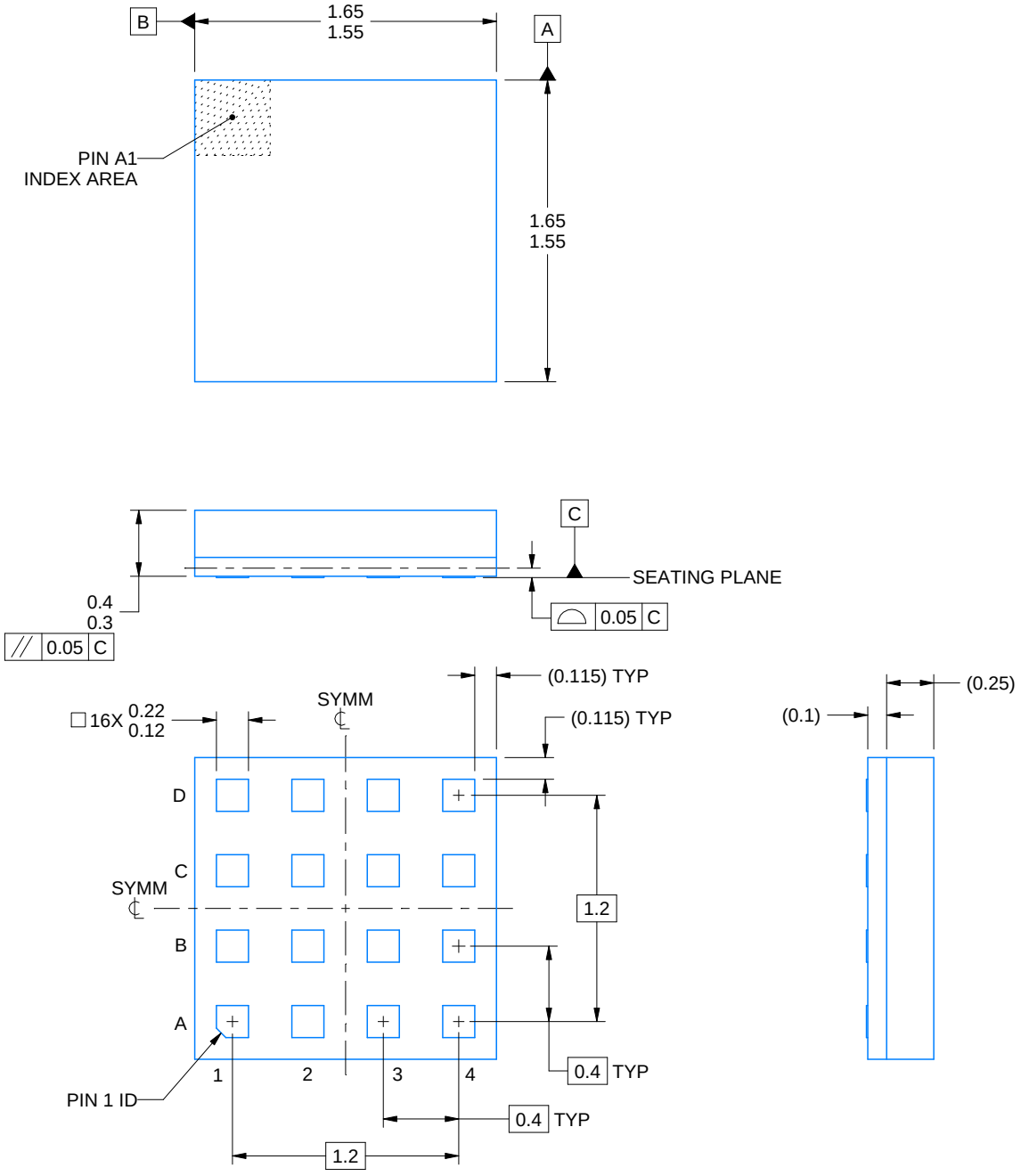
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## DTU0016A

## X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD




4228238/B 03/2022

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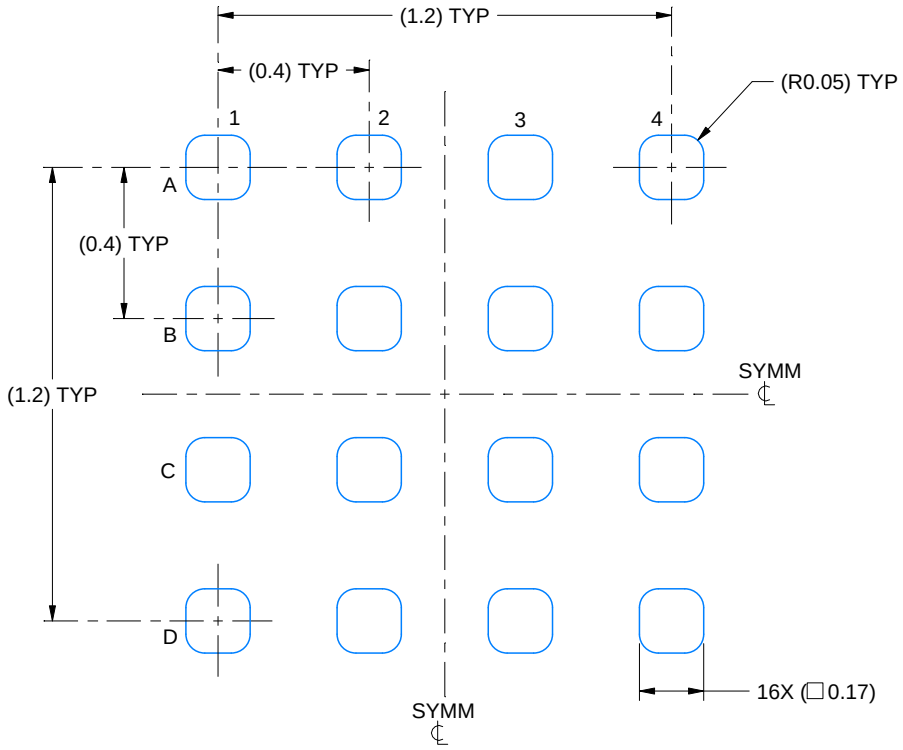
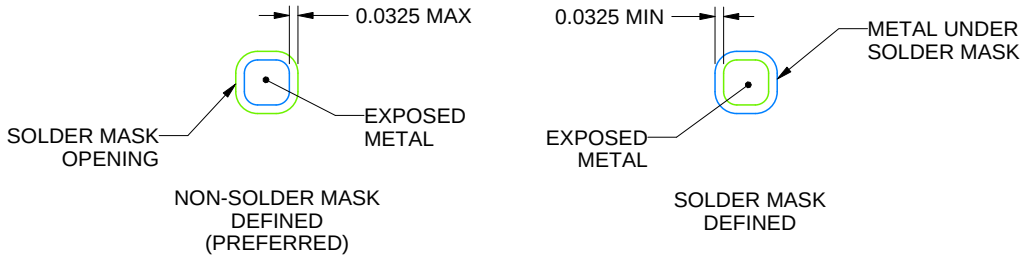
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is for Embedded Application only.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:50X

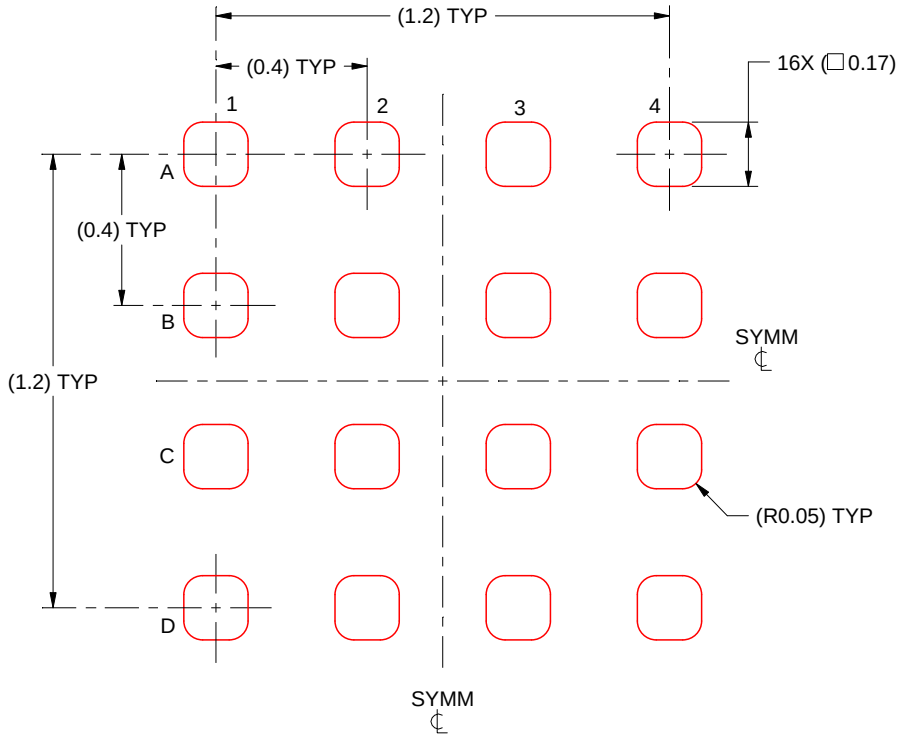



SOLDER MASK DETAILS
NOT TO SCALE

4228238/B 03/2022

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).




SOLDER PASTE EXAMPLE
BASED ON 0.0625 mm THICK STENCIL
SCALE:50X

4228238/B 03/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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