TDP20MB421 DisplayPort 2.1 24Gbps 4-Channel Linear Redriver with 2:1 MUX

1 Features

- Four channel DisplayPort 2.1 linear redriver or repeater with integrated 2:1 MUX
- Supports embedded (eDP) and DisplayPort 2.1 up to 20Gbps - RBR, HBRx, UHBRx
- Supports DP++ (also called an AC-coupled HDMI) up to 24Gbps
- Protocol agnostic, linear equalizer supporting AC coupled interfaces up to 24Gbps
- Single 3.3V supply
- Low 720mW active power for 4-channel operation
- Excellent electrical performance at 20Gbps (10GHz Nyquist):
  - 19dB equalization
  - 1.8V DC linearity, 1.08V AC linearity
  - -15dB / -16dB Rx / Tx return loss
  - -60dB NEXT, -43dB FEXT crosstalk
  - 70fs low additive RJ with PRBS data
- Low latency of 90ps
- Transparent to DisplayPort 1.4 and 2.1 link training
- Device configuration by pin control or SMBus / I^2C
  - 18EQ boost settings, 5 flat gain settings
- -40°C to 85°C temperature range
- 3.5 × 9mm 42 Pin 0.5mm pitch WQFN package

2 Applications

- Desktop PC and motherboard
- PC, notebooks, tablets
- Docking stations
- TV, gaming, home theater, and entertainment
- Pro audio, video, and signage
- Test and measurement
- Medical
- Flat panel monitors

3 Description

The TDP20MB421 is a 4-channel linear redriver with an integrated 2:1 MUX. The low-power, high-performance linear redriver is designed to support DisplayPort 2.1 up to 20Gbps.

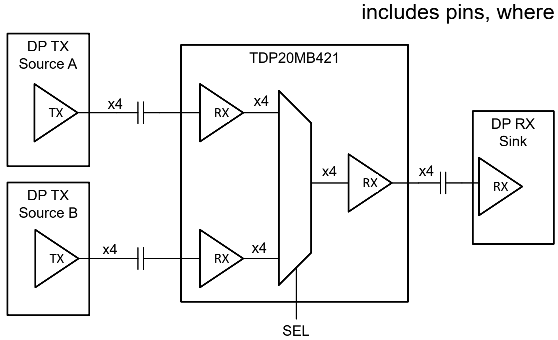
The TDP20MB421 receivers deploy continuous time linear equalizers (CTLE) to provide a programmable high-frequency boost. The equalizer opens an input eye that is completely closed due to inter-symbol interference (ISI) induced by an interconnect medium, such as PCB traces. A CTLE receiver is followed by a linear output driver. The linear data paths of TDP20MB421 preserve the characteristics of the transmit preset. High bandwidth, low channel-to-channel crosstalk, low additive jitter, and excellent return loss make the device almost a passive element in the link. The DisplayPort link training is effective through the device as the device becomes part of the passive channel between the source Tx and sink Rx. The device transparency in the link-training protocol results in the best electrical link and lowest possible latency. The data path of the device uses an internally regulated power rail that provides high immunity to supply noise on the board.

The TDP20MB421 implements high-speed testing during production for reliable, high-volume manufacturing. The device also has low AC and DC gain variation, providing consistent equalization in high-volume platform deployment.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TDP20MB421	RUA (WQFN, 42)	9mm × 3.5mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Application Use Case

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4 Pin Configuration and Functions

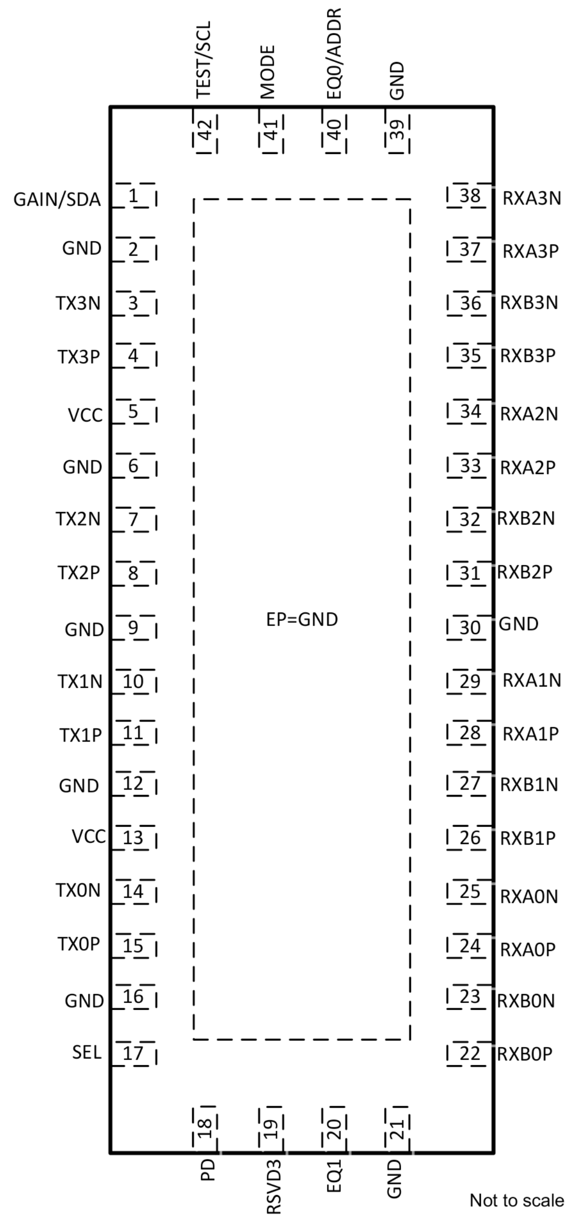


Figure 4-1. RUA Package, 42-Pin WQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
MODE	41	I, 5-level	Sets device control configuration modes. The 5-level IO pin is defined in Table 6-1. The pin is used at device power up or in normal operation mode. L0: *Pin Mode* – device control configuration is done solely by strap pins. L1 or L2: *SMBus/I^{2}C Mode* – device control configuration is done by an external controller with SMBus/I^{2}C primary. This pin along with ADDR pin set the secondary address of the device. L3 and L4 (Float): RESERVED – TI internal test modes.
EQ0 /ADDR	40	I, 5-level	In *Pin Mode:* The EQ0 and EQ1 pins sets receiver linear equalization CTLE (AC gain) for all channels according to Table 6-2. These pins are sampled at device power up only. In *SMBus/I^{2}C Mode:* The ADDR pin in conjunction with the MODE pin sets SMBus / I^{2}C secondary address according to Table 6-4. The pin is sampled at device power-up only.
EQ1	20	I, 5-level	
GAIN /SDA	1	I, 5-level / IO	*In Pin Mode*: Flat gain (broadband gain – DC and AC) from the input to the output of the device for all channels. The device also provides AC (high frequency) gain in the form of equalization controlled by EQ pins or SMBus/I^{2}C registers. The pin is sampled at device power up only. *In SMBus/I^{2}C Mode*: 3.3V SMBus/I^{2}C data. External pullup resistor such as 4.7 kΩ required for operation.
GND	EP, 2, 6, 9, 12, 16, 21, 30, 39	P	Ground reference for the device. EP: the Exposed Pad at the bottom of the QFN package. The EP is used as the GND return for the device. Connect the EP to one or more ground planes through the low resistance path. A via array provides a low impedance path to GND. The EP also improves thermal dissipation.
PD	18	I, 3.3V LVCMOS	2-level logic controlling the operating state of the redriver. Active in both *Pin Mode* and *SMBus/I^{2}C Mode*. The pin has a weak 1MkΩ internal pulldown resistor. High: power down for all channels Low: power up, normal operation for all channels
TEST /SCL	42	I, 5-level / IO	In *Pin Mode:* TI Test mode. Use external 1kΩ pulldown resistor instead. In *SMBus/I^{2}C Mode:* 3.3V SMBus/I^{2}C clock. External pullup resistor such as 4.7kΩ required for operation.
RXA3P	37	I	Inverting differential RX input – Port A, Channel 3.
RXA3N	38	I	Noninverting differential RX input – Port A, Channel 3.
RXA2P	33	I	Inverting differential RX input – Port A, Channel 2.
RXA2N	34	I	Noninverting differential RX input – Port A, Channel 2.
RXA1P	28	I	Inverting differential RX input – Port A, Channel 1.
RXA1N	29	I	Noninverting differential RX input – Port A, Channel 1.
RXA0P	24	I	Inverting differential RX input – Port A, Channel 0.
RXA0N	25	I	Noninverting differential RX input – Port A, Channel 0.
RXB3P	35	I	Inverting differential RX input – Port B, Channel 3.
RXB3N	36	I	Noninverting differential RX input – Port B, Channel 3.
RXB2P	31	I	Inverting differential RX input – Port B, Channel 2.
RXB2N	32	I	Noninverting differential RX input – Port B, Channel 2.
RXB1P	26	I	Inverting differential RX input – Port B, Channel 1.
RXB1N	27	I	Noninverting differential RX input – Port B, Channel 1.
RXB0P	22	I	Inverting differential RX input – Port B, Channel 0.
RXB0N	23	I	Noninverting differential RX input – Port B, Channel 0.

Table 4-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
SEL	17	I, 3.3V LVCMOS	Selects the mux path. Active in both *Pin Mode* and *SMBus/I²C Mode*. The pin has a weak internal pulldown resistor. Exercise the SEL pin in system implementations for mux selection between Port A vs Port B. L: Port A selected. H: Port B selected.
TX3P	4	O	Inverting differential TX output, Channel 3.
TX3N	3	O	Noninverting differential TX output, Channel 3.
TX2P	8	O	Inverting differential TX output, Channel 2.
TX2N	7	O	Noninverting differential TX output, Channel 2.
TX1P	11	O	Inverting differential TX output, Channel 1.
TX1N	10	O	Noninverting differential TX output, Channel 1.
TX0P	15	O	Inverting differential TX output, Channel 0.
TX0N	14	O	Noninverting differential TX output, Channel 0.
RSVD3	19	O	TI internal test pin. Keep no connect.
VCC	5, 13	P	Power supply, VCC = 3.3V ± 10%. Connect the VCC pins on this device through a low-resistance path to the board VCC plane.

(1) I = input, O = output, P = power, GND = ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VCC_{ABSMAX}	Supply voltage (VCC)	–0.5	4.0	V
$VIO_{CMOS,ABSMAX}$	3.3V LVCMOS and open drain I/O voltage	–0.5	4.0	V
$VIO_{5LVL,ABSMAX}$	5-level input I/O voltage	–0.5	2.75	V
$VIO_{HS\text{-}RX,ABSMAX}$	High-speed I/O voltage (RXnP, RXnN)	–0.5	3.2	V
$VIO_{HS\text{-}TX,ABSMAX}$	High-speed I/O voltage (TXnP, TXnN)	–0.5	2.75	V
$T_{J,ABSMAX}$	Junction temperature		150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2kV may actually have higher performance.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
VCC	Supply voltage, VCC to GND	DC plus AC power must not exceed these limits	3.0	3.3	3.6	V
N_{VCC}	Supply noise tolerance	DC to <50 Hz, sinusoidal(1)			250	mVpp
		50 Hz to 500 kHz, sinusoidal(1)			100	mVpp
		500 kHz to 2.5MHz, sinusoidal(1)			33	mVpp
		Supply noise, >2.5MHz, sinusoidal(1)			10	mVpp
$T_{RampVCC}$	VCC supply ramp time	From 0V to 3.0V	0.150		100	ms
T_J	Operating junction temperature		–40		115	°C
T_A	Operating ambient temperature		–40		85	°C
PW_{LVCMOS}	Minimum pulse width required for the device to detect a valid signal on LVCMOS inputs	PD and SEL	200			µs
VCC_{SMBUS}	SMBus/I²C SDA and SCL open drain termination voltage	Supply voltage for open drain pullup resistor			3.6	V
F_{SMBus}	SMBus/I²C clock (SCL) frequency in SMBus secondary mode		10		400	kHz
VID_{LAUNCH}	Source differential launch amplitude		800		1200	mVpp
DR	Data rate		1		24	Gbps

(1) Sinusoidal noise is superimposed to supply voltage with negligible impact to device function and critical performance, as shown in the Electrical Table. Take steps to ensure the combined AC plus DC supply noise meets the specified VDD supply voltage limits.

5.4 Thermal Information

THERMAL METRIC(1)		TDP20MB421	UNIT
		RUA, 42 Pins	
$R_{\theta JA\text{-High K}}$	Junction-to-ambient thermal resistance	26.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	14.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	8.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 DC Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power						
P_{ACT}	Device active power	All channels enabled (PD = L)		720	970	mW
P_{STBY}	Device power consumption in standby power mode	All channels disabled (PD = H)		23	36	mW
Control IO						
V_{IH}	High level input voltage	SDA, SCL, PD, SEL pins	2.1			V
V_{IL}	Low level input voltage	SDA, SCL, PD, SEL pins			1.08	V
V_{OH}	High level output voltage	R_{pullup} = 4.7kΩ (SDA, SCL pins)	2.1			V
V_{OL}	Low level output voltage	I_{OL} = –4mA (SDA, SCL pins)			0.4	V
$I_{IH,SEL}$	Input high leakage current for SEL pins	V_{Input} = VCC, for SEL pin			100	µA
I_{IH}	Input high leakage current	V_{Input} = VCC (SCL, SDA, PD pins)			10	µA
I_{IL}	Input low leakage current	V_{Input} = 0V (SCL, SDA, PD, SEL pins)	–10			µA
$I_{IH,FS}$	Input high leakage current for fail safe input pins	V_{Input} = 3.6V, VCC = 0V (SCL, SDA, PD, SEL pins)			200	µA
$C_{IN\text{-}CTRL}$	Input capacitance	SCL, SDA, PD, SEL pins		1.6		pF
5 Level IOs (MODE, GAIN, EQ1, EQ0, pins)						
I_{IH_5L}	Input high leakage current, 5 level IOs	VIN = 2.5V			10	µA
I_{IL_5L}	Input low leakage current for all 5 level IOs except MODE	VIN = GND	–10			µA
$I_{IL\_5L,MODE}$	Input low leakage current for MODE pin	VIN = GND	–200			µA
Receiver						
$V_{RX\text{-}DC\text{-}CM}$	RX DC common-mode voltage	Device is in an active or standby state		1.4		V
$Z_{RX\text{-}DC}$	Rx DC single-ended impedance			50		Ω
$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$	DC input CM input impedance during Reset or power-down	Inputs are at $V_{RX\text{-}DC\text{-}CM}$ voltage	20			kΩ
Transmitter						
$Z_{TX\text{-}DIFF\text{-}DC}$	DC differential Tx impedance	Impedance of Tx during active signaling, VID, diff = 1Vpp		100		Ω
$V_{TX\text{-}DC\text{-}CM}$	Tx DC common-mode voltage			1.0		V
$I_{TX\text{-}SHORT}$	Tx short-circuit current	Total current the Tx supplies when shorted to GND		70		mA

5.6 High-Speed Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver						
$RL_{RX-DIFF}$	Input differential return loss	50MHz to 1.25GHz		–22		dB
		1.25GHz to 2.5GHz		–22		dB
		2.5GHz to 4.0GHz		–22		dB
		4.0GHz to 8.0GHz		–16		dB
		8.0GHz to 12GHz		–12		dB
RL_{RX-CM}	Input common-mode return loss	50MHz to 2.5GHz		–20		dB
		2.5GHz to 8.0GHz		–14		dB
		8.0GHz to 12GHz		–10		dB
XT_{RX}	Receive-side pair-to-pair isolation	Pair-to-pair isolation (SDD21) between two adjacent receiver pairs from 10MHz to 10GHz.		–60		dB
Transmitter						
$V_{TX-AC-CM-PP}$	Tx AC peak-to-peak common mode voltage	Measured with lowest EQ, GAIN = L4; PRBS7, 20Gbps, over at least 10^6 bits using a bandpass filter from 30kHz to 500MHz			50	mVpp
$RL_{TX-DIFF}$	Output differential return loss	50MHz to 1.25GHz		–22		dB
		1.25GHz to 2.5GHz		–22		dB
		2.5GHz to 4.0GHz		–21		dB
		4.0GHz to 8.0GHz		–15		dB
		8.0GHz to 12GHz		–12		dB
RL_{TX-CM}	Output common-mode return loss	50MHz to 2.5GHz		–16		dB
		2.5GHz to 8.0GHz		–12		dB
		8.0GHz to 12GHz		–11		dB
XT_{TX}	Transmit-side pair-to-pair isolation	Minimum pair-to-pair isolation (SDD21) between two adjacent transmitter pairs from 10MHz to 10GHz.		–60		dB
Device data path						
$T_{PLHD/PHLD}$	Input-to-output latency (propagation delay) through a data channel	For either low-to-high or high-to-low transition.		90	130	ps
$L_{TX-SKEW}$	Lane-to-lane output skew	Between any two lanes within one transmitter.			20	ps
$T_{RJ-DATA}$	Additive random jitter with data	Jitter through redriver minus the calibration trace. 20Gbps PRBS15. 800mVpp-diff input swing.		70		fs
$JITTER_{TOTAL-DATA}$	Additive total jitter with data	Jitter through redriver minus the calibration trace. 20Gbps PRBS15. 800mVpp-diff input swing.		1.0		ps
FLAT-GAIN	Broadband DC and AC flat gain - input to output, measured at DC	Minimum EQ, GAIN1/0=L0		–5.6		dB
		Minimum EQ, GAIN1/0=L1		–3.8		dB
		Minimum EQ, GAIN1/0=L2		–1.2		dB
		Minimum EQ, GAIN1/0=L3		2.6		dB
		Minimum EQ, GAIN1/0=L4 (Float)		0.6		dB
$EQ-MAX_{16G}$	EQ boost at maximum setting (EQ INDEX = 19)	AC gain at 10GHz relative to gain at 100MHz.		19		dB
LINEARITY-DC	Output DC linearity	at 0dB flat gain		1700		mVpp

5.6 High-Speed Electrical Characteristics (continued)

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LINEARITY-AC	Output AC linearity at 20Gbps	at 0dB flat gain		1050		mVpp

5.7 SMBUS/I2C Timing Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Secondary Mode						
t_{SP}	Pulse width of spikes which must be suppressed by the input filter				50	ns
$t_{HD\text{-}STA}$	Hold time (repeated) START condition the first clock pulse is generated after this period		0.6			µs
t_{LOW}	LOW period of the SCL clock		1.3			µs
T_{HIGH}	HIGH period of the SCL clock		0.6			µs
$t_{SU\text{-}STA}$	Setup time for a repeated START condition		0.6			µs
$t_{HD\text{-}DAT}$	Data-hold time		0			µs
$T_{SU\text{-}DAT}$	Data-setup time		0.1			µs
t_r	Rise time of both SDA and SCL signals	Pullup resistor = 4.7kΩ, Cb = 10pF		120		ns
t_f	Fall time of both SDA and SCL signals	Pullup resistor = 4.7kΩ, Cb = 10pF		2		ns
$t_{SU\text{-}STO}$	Setup time for STOP condition		0.6			µs
t_{BUF}	Bus-free time between a STOP and START condition		1.3			µs
$t_{VD\text{-}DAT}$	Data valid time				0.9	µs
$t_{VD\text{-}ACK}$	Data valid acknowledge time				0.9	µs
C_b	Capacitive load for each bus line				400	pF

5.8 Typical Characteristics

Figure 5-1 shows typical EQ gain curves versus frequency for different EQ settings. Figure 5-2 shows EQ gain variation over temperature for maximum EQ setting of 19.

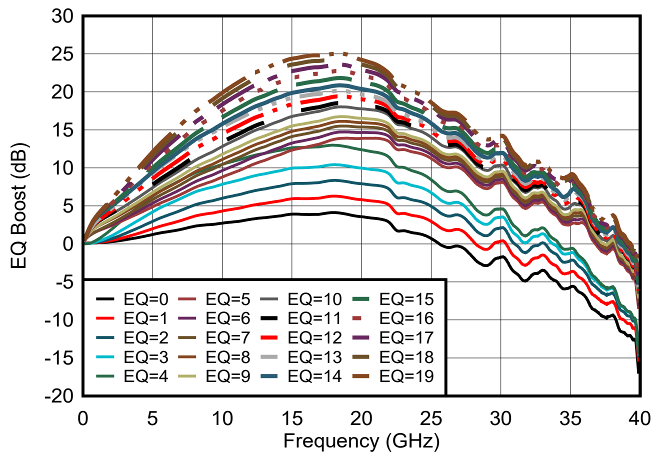


Figure 5-1. Typical EQ Boost vs Frequency

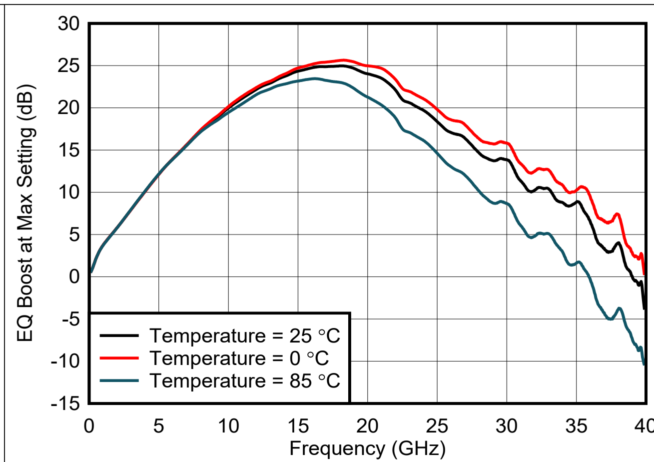


Figure 5-2. Typical EQ Boost vs Frequency at Different Temperatures with EQ=19

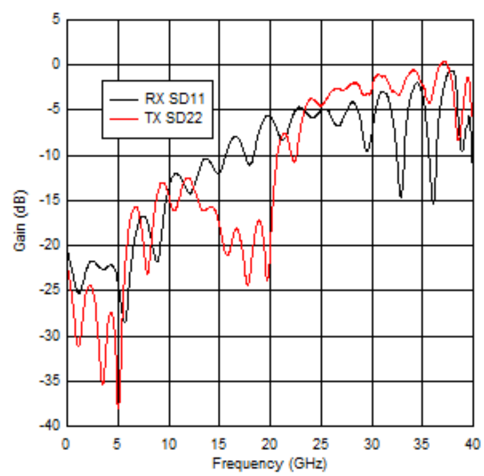


Figure 5-3. Typical Differential Return Loss

6 Detailed Description

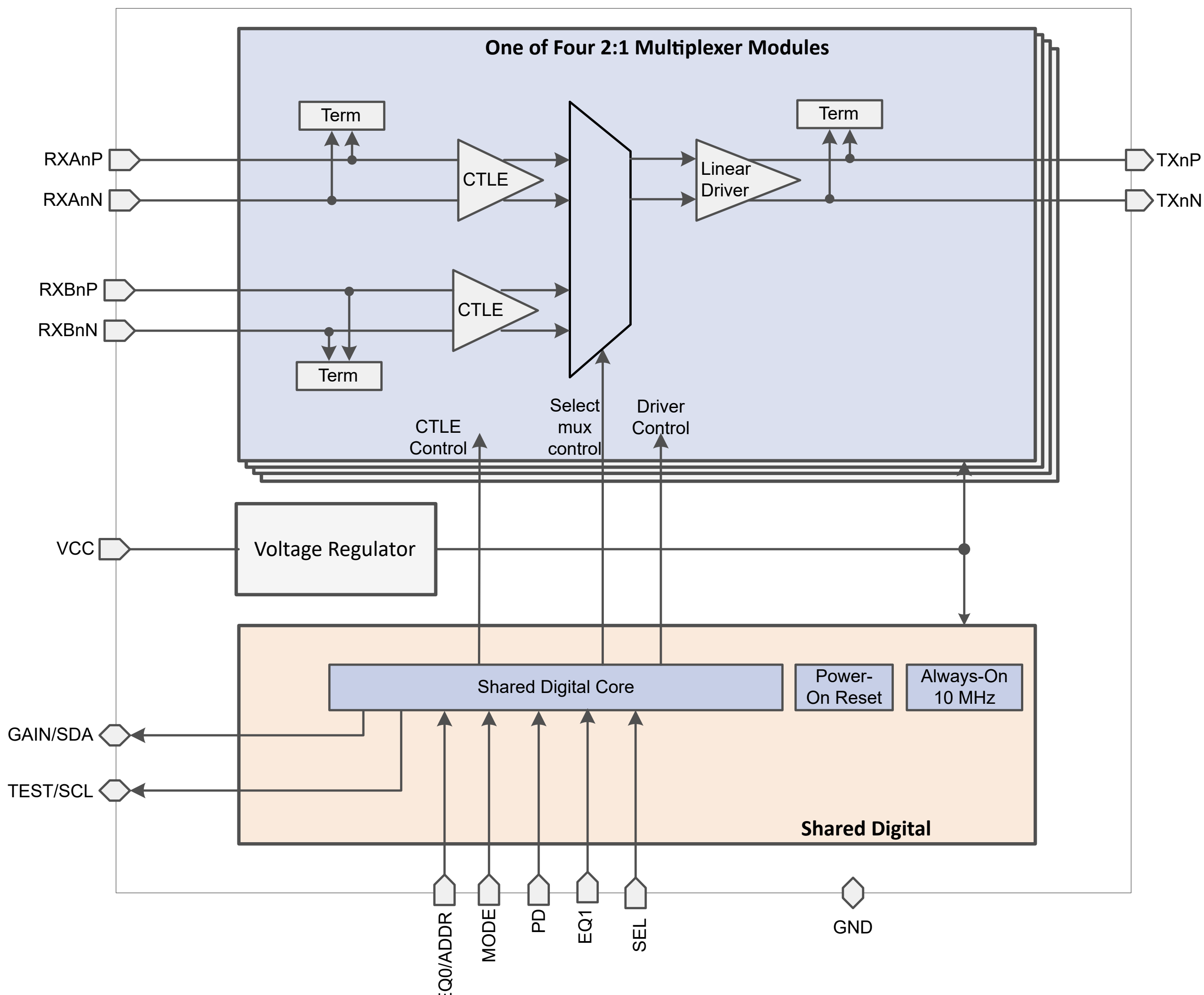
6.1 Overview

The TDP20MB421 is a 4-channel linear redriver with an integrated 2:1 MUX. The low-power, high-performance linear repeater or redriver supports DisplayPort data rates up to UHBR20. The device is a protocol agnostic linear redriver that can operate for other AC-coupled interface up to 20Gbps.

The signal channels of the TDP20MB421 operate independently. Each channel includes a continuous time linear equalizer (CTLE) and a linear output driver, which together compensate for a lossy transmission channel between the source transmitter and the final receiver. The linearity of the data path is designed to preserve transmit equalization while keeping the equalization of the DisplayPort receiver effective.

The TDP20MB421 is configurable in two ways. In Pin Mode, the device control configuration is done solely by strap pins. Pin mode is designed for many system implementation needs. SMBus/I2C Secondary Mode provides greater flexibility. SMBus/I2C Secondary Mode requires an external SMBus/I2C primary device to configure the TDP20MB421 though writing to its secondary address.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 5-Level Control Inputs

The TDP20MB421 has four 5-level inputs pins (EQ1, EQ0, GAIN, and MODE) that control the configuration of the device. These 5-level inputs use a resistor divider to set the five valid levels and provide a wider range of control settings. External resistors must have a tolerance of at least 10%. The EQ0, EQ1, and GAIN pins are sampled at power up only. The MODE pin can be exercised at device power up or in normal operation mode.

Table 6-1. 5-Level Control Pin Settings

LEVEL	SETTING
L0	1kΩ to GND
L1	8.25kΩ to GND
L2	24.9kΩ to GND
L3	75kΩ to GND
L4	F (Float)

6.3.2 Linear Equalization

The TDP20MB421 receivers feature a continuous time linear equalizer (CTLE) that applies high-frequency boost and low-frequency attenuation to equalize the frequency-dependent insertion loss effects of a passive channel. The receivers implement a 2-stage linear equalizer for a wide range of equalization capability. The equalizer stages also provide flexibility to make subtle modifications to the mid-frequency boost for the best EQ-gain profile match with a wide range of channel media characteristics. The control feature of the EQ profile is only available in SMBus/I^{2}C Mode. In Pin Mode, the settings are optimized for FR4 traces.

Table 6-2 shows available equalization boost through EQ control pins or SMBus/I^{2}C registers. In Pin Control mode, EQ1 and EQ0 pins set the equalization boost for all channels. In I^{2}C Mode, individual channels can be independently programmed for an EQ boost.

Table 6-2. Equalization Control Settings

EQUALIZATION SETTING							TYPICAL EQ BOOST (dB)
EQ INDEX	Pin mode		SMBus/I^{2}C Mode				
	EQ1	EQ0	eq_stage1_3:0	eq_stage2_2:0	eq_profile_3:0	eq_stage1_bypass	at 10 GHz
0	L0	L0	0	0	0	1	4.0
1	L0	L1	1	0	0	1	5.0
2	L0	L2	3	0	0	1	7.0
5	L1	L0	0	0	1	0	8.0
6	L1	L1	1	0	1	0	9.0
7	L1	L2	2	0	1	0	9.5
8	L1	L3	3	0	3	0	10.0
9	L1	L4	4	0	3	0	11.0
10	L2	L0	5	1	7	0	12.0
11	L2	L1	6	1	7	0	12.5
12	L2	L2	8	1	7	0	13.5
13	L2	L3	10	1	7	0	14.5
14	L2	L4	10	2	15	0	15.0
15	L3	L0	11	3	15	0	15.5
16	L3	L1	12	4	15	0	16.5

Table 6-2. Equalization Control Settings (continued)

EQUALIZATION SETTING							TYPICAL EQ BOOST (dB)
EQ INDEX	Pin mode		SMBus/I2C Mode				at 10 GHz
	EQ1	EQ0	eq_stage1_3:0	eq_stage2_2:0	eq_profile_3:0	eq_stage1_bypass	
17	L3	L2	13	5	15	0	17.0
18	L3	L3	14	6	15	0	18.0
19	L3	L4	15	7	15	0	19.0

6.3.3 Flat Gain

The GAIN pin can be used to set the overall datapath for the flat gain (broadband gain including high frequency) of the TDP20MB421 when the device is in Pin Mode. The pin GAIN sets the Flat-Gain for all channels. Each channel is independently set in I2C Mode. Table 6-3 shows the configuration settings for flat gain control. The default recommendation for most systems is GAIN = L4 (float) because it provides a flat gain of 0dB.

Set the flat gain and equalization of the TDP20MB421 so that the output signal swing at DC and high frequency does not exceed the DC and AC linearity ranges of the devices.

Table 6-3. Flat Gain Configuration Settings

Pin Mode GAIN	I^2C Mode flat_gain_2:0	Flat Gain
L0	0	−5.6dB
L1	1	−3.8dB
L2	3	−1.2dB
L3	7	+2.6dB
L4 (float)	5	+0.6dB (default recommendation)

6.4 Device Functional Modes

6.4.1 Active Mode

The TDP20MB421 is in normal operation. In this mode, the system drives the PD pin low and the TDP20MB421 redrives and equalizes RX signals to provide better signal integrity.

6.4.2 Standby Mode

The TDP20MB421 is in standby mode invoked by PD pin = H. In this mode, the device conserves power in standby mode

6.5 Programming

6.5.1 Pin Mode

The pin-strap pins fully configure the TDP20MB421. In this mode, the device uses 2-level and 5-level pins for device control and optimum settings for signal integrity.

6.5.2 SMBUS/I^2C Register Control Interface

If MODE = L2 (SMBus / I^2C secondary control mode), the TDP20MB421 is configured for best signal integrity through a standard I^2C or SMBus interface operates up to 400kHz. Pin strap settings determines the secondary address of the TDP20MB421 on the ADDR and MODE pins. Table 6-4 provides the eight possible secondary addresses (7-bit) for each channel banks of the device. In SMBus and I2C modes, the SCL and SDA pins connect to a 3.3V supply through a pullup resistor. The value of the resistor depends on the total bus capacitance. 4.7kΩ is a good first approximation for a bus capacitance of 10pF.

Table 6-4. SMBUS/I2C Secondary Address Settings

MODE	ADDR	7-bit Secondary Address Channels 2-3	7-bit Secondary Address Channels 0-1
L1	L0	0x18	0x19
L1	L1	0x1A	0x1B
L1	L2	0x1C	0x1D
L1	L3	0x1E	0x1F
X	L4	Reserved	Reserved
L2	L0	0x20	0x21
L2	L1	0x22	0x23
L2	L2	0x24	0x25
L2	L3	0x26	0x27

The TDP20MB421 has two types of registers:

- **Shared Registers:** These registers are accessible at any time and are used for device-level configuration, status read back, control, and to read the device ID information.
- **Channel Registers:** These registers control and configure specific features for each channel. All channels have the same register set and can be configured independently or as a group through broadcast writes to Bank 0 or 1.

The TDP20MB421 features two banks of channels, Bank 0 (Channels 2-3) and Bank 1 (Channels 0-1), each feature a separate register set and require a unique SMBus secondary address.

Channel Registers Base Address	Channel Bank 0 Access	Channel Bank 1 Access
0x00	Channel 3 registers	Channel 1 registers
0x20	Channel 3 registers	Channel 1 registers
0x40	Channel 2 registers	Channel 0 registers
0x60	Channel 2 registers	Channel 0 registers
0x80	Broadcast write channel Bank 0 registers, read channel 3 registers	Broadcast write channel Bank 1 registers, read channel 1 registers
0xE0	Bank 0 Share registers	Bank 1 Share registers

6.5.2.1 Shared Registers

Table 6-5. General Registers (Offset = 0xE2)

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	rst_i2c_regs	R/W/SC	0x0	Device reset control: Reset all I2C registers to default values (self-clearing).
5	rst_i2c_mas	R/W/SC	0x0	Reset I^2C Primary (self-clearing).
4-0	RESERVED	R	0x0000	Reserved

Table 6-6. DEVICE_ID0 Register (Offset = 0xF0)

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0001	Reserved
3	device_id0_3	R	0x1	Device ID0 [3:1]: 101
2	device_id0_2	R	0x0	see MSB
1	device_id0_1	R	0x1	see MSB
0	RESERVED	R	X	Reserved

Table 6-7. *DEVICE_ID1 Register (Offset = 0xF1)*

Bit	Field	Type	Reset	Description
7	device_id[7]	R	0x0	Device ID 0010 1000: TDP20MB421
6	device_id[6]	R	0x0	see MSB
5	device_id[5]	R	0x1	see MSB
4	device_id[4]	R	0x0	see MSB
3	device_id[3]	R	0x1	see MSB
2	device_id[2]	R	0x0	see MSB
1	device_id[1]	R	0x0	see MSB
0	device_id[0]	R	0x1	see MSB

6.5.2.2 Channel Registers

Table 6-8. EQ Gain Control Register (Channel Register Base + Offset = 0x01)

Bit	Field	Type	Reset	Description
7	eq_stage1_bypass	R/W	0x0	Enable EQ stage 1 bypass: 0: Bypass disabled 1: Bypass enabled
6	eq_stage1_3	R/W	0x0	EQBoost stage 1 control See Table 6-2 for details
5	eq_stage1_2	R/W	0x0	
4	eq_stage1_1	R/W	0x0	
3	eq_stage1_0	R/W	0x0	
2	eq_stage2_2	R/W	0x0	EQ Boost stage 2 control See Table 6-2 for details
1	eq_stage2_1	R/W	0x0	
0	eq_stage2_0	R/W	0x0	

Table 6-9. EQ Gain / Flat Gain Control Register (Channel Register Base + Offset = 0x03)

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	eq_profile_3	R/W	0x0	EQ mid-frequency boost profile See Table 6-2 for details
5	eq_profile_2	R/W	0x0	
4	eq_profile_1	R/W	0x0	
3	eq_profile_0	R/W	0x0	
2	flat_gain_2	R/W	0x1	Flat gain select: See Table 6-3 for details
1	flat_gain_1	R/W	0x0	
0	flat_gain_0	R/W	0x1	

Table 6-10. PD Override Register (Channel Register Base + Offset = 0x05)

Bit	Field	Type	Reset	Description
7	device_en_override	R/W	0x0	Enable power down overrides through SMBus/I^{2}C 0: Manual override disabled 1: Manual override enabled
6-0	device_en	R/W	0x111111	Manual power down of redriver various blocks – gated by device_en_override = 1 111111: All blocks are enabled 000000: All blocks are disabled

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers must validate and test their design implementation to confirm system functionality.

7.1 Application Information

The TDP20MB421 is a high-speed linear repeater with an integrated 2:1 MUX. The device extends the reach of differential channels impaired by loss from transmission media like PCBs and cables. The TDP20MB421 can be deployed in a variety of different systems. The following sections outline typical applications and their associated design considerations.

7.2 Typical Applications

The TDP20MB421 is a linear redriver that can be used as DisplayPort mainlink signal conditioner. The device can be used in a wide range of AC coupled interfaces.

7.2.1 DP 2.1 Mainlink Signal Conditioning

There are many applications for the TDP20MB421, including use in a PC motherboard, docking station, or monitor, to boost the DisplayPort mainlink signals, increasing the reach of the source and sink channel. The following sections outline the detailed procedures and design requirements for a typical DP 2.1 application. However, the design recommendations can be used in other use cases.

7.2.1.1 Design Requirements

As with any high-speed design, there are many factors influencing the overall performance. The following list indicates the critical areas to consider during the design process:

- Use 85Ω impedance traces. Perform length matching on the P and N traces on the single-ended segments of the differential pair.
- Use a uniform trace width and spacing for differential pairs.
- Place AC-coupling capacitors near to the receiver end of each channel segment to minimize reflections.
- For Gen 3.0, 4.0, and 5.0, AC-coupling capacitors of 220nF are recommended with a maximum body size of 0402 and a cutout void on the GND plane below the landing pad of the capacitor to reduce parasitic capacitance to GND.
- Back-drill connector vias and signal vias to minimize stub length.
- Use reference plane vias to ensure a low inductance path for the return current.

7.2.1.2 Detailed Design Procedure

The TDP20MB421 provides signal conditioning to four DP mainlink channels. The device is a linear redriver which is agnostic to DP link training. The DP link training negotiation between a display source and sink stays effective through the device. The redriver becomes part of the electrical channel along with passive traces, cables, and other channel elements, resulting in the optimum source and sink parameters for the best electrical link.

DisplayPort side band signals AUXp,n and HPD are bypassed. The link still has successful link training through TDP20MB421. An inverted HPD signal can control the device standby operation using the PD pin; however, provision for appropriate filtering out of HPD interrupt signals.

In some applications where a microcontroller or other link monitoring device has DP link state information, the microcontroller can exercise I^2C registers of TDP20MB421 for additional power management.

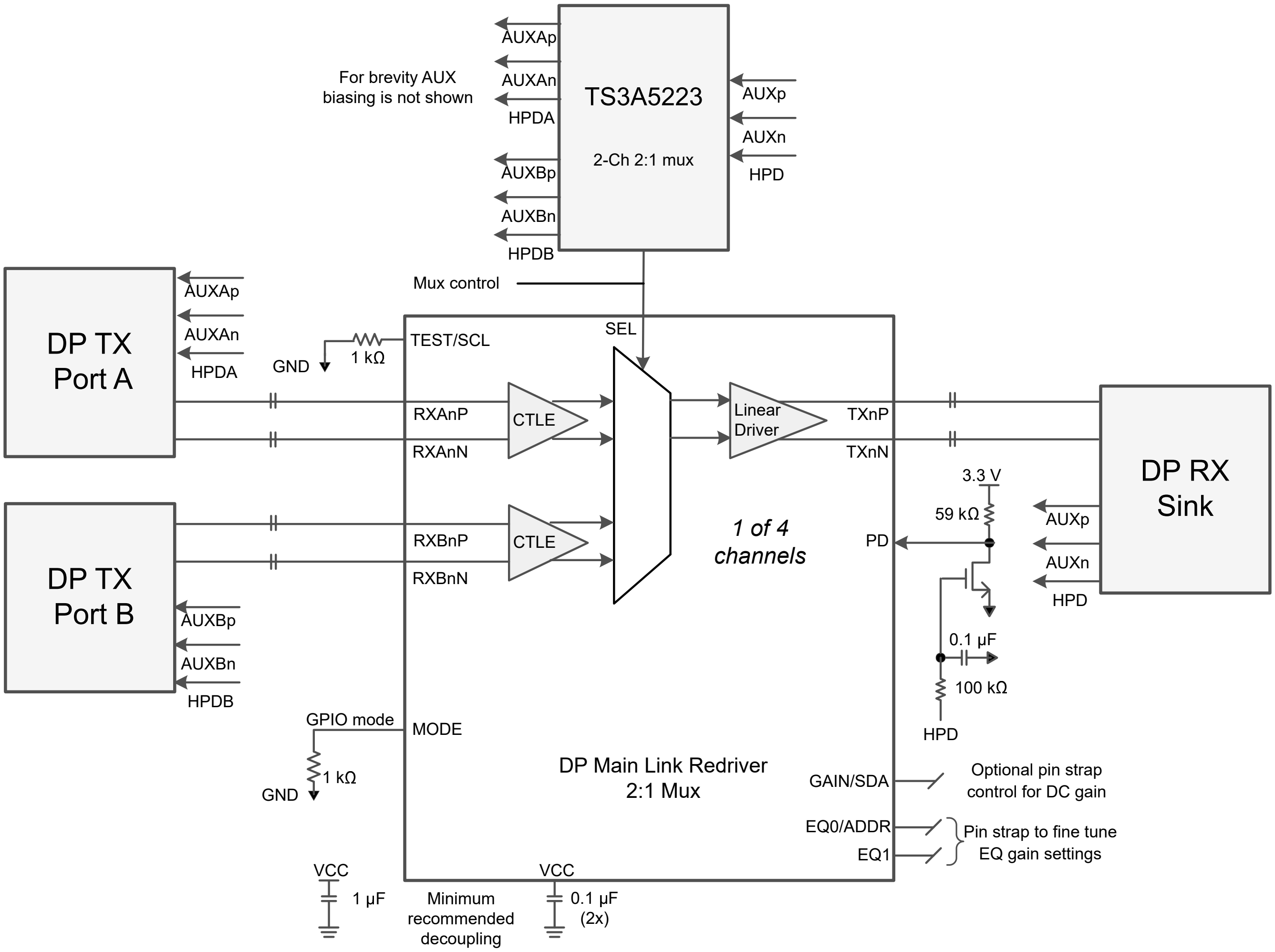


Figure 7-1. Simplified Schematic for DisplayPort Multiplexer Application

7.2.1.3 Application Curves

The TDP20MB421 is a linear redriver that can be used to extend channel reach of a DP link. The redriver can help to pass compliance by removing ISI deterministic jitter at data rates up to 20Gbps (UHBR20). Figure 7-2 through Figure 7-5 shows a typical DP 2.1 Tx compliance channel setup along with compliance Eye Diagrams at TP3_EQ with or without redriver. The comparison of eye diagrams show that TDP20MB421 can provide signal conditioning by extending horizontal and vertical eye openings that makes a failing eye to pass.

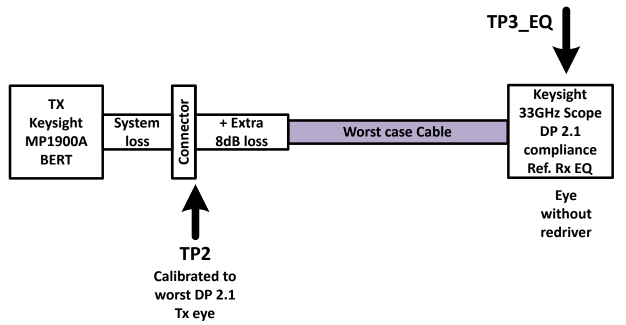


Figure 7-2. A Typical 20Gbps (UHBR20) DP 2.1 Tx Compliance Channel Setup with no Redriver

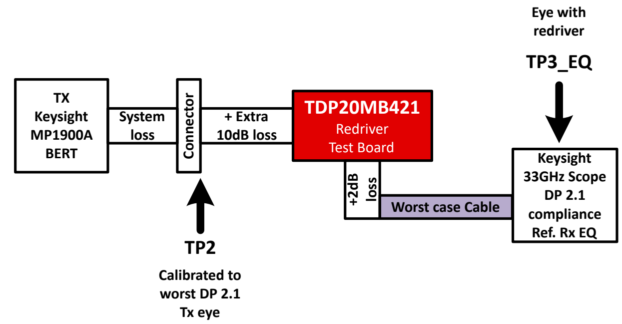


Figure 7-3. A Typical 20Gbps (UHBR20) DP 2.1 Tx Compliance Channel Setup with Redriver

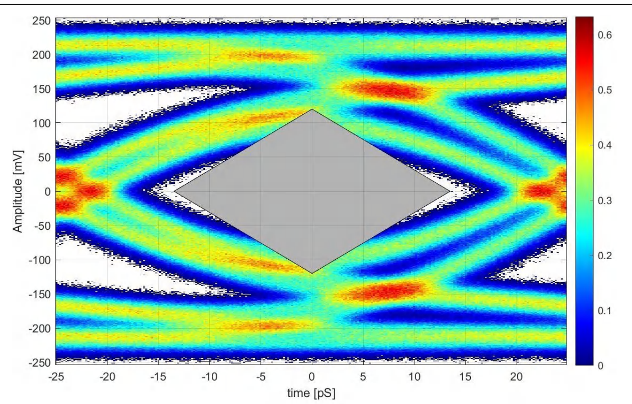


Figure 7-4. DP 2.1 Tx Compliance Eye Diagram at TP3_EQ with no Redriver

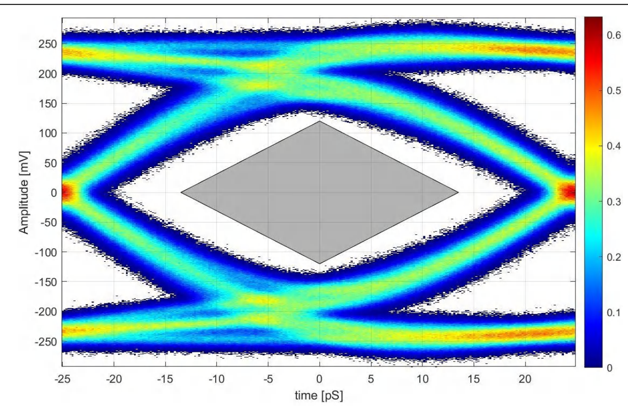


Figure 7-5. DP 2.1 Tx Compliance Eye Diagram at TP3_EQ with TDP20MB421 for Signal Conditioning

7.3 Power Supply Recommendations

Follow these general guidelines when designing the power supply:

1. Design the power supply to provide the operating conditions outlined in the recommended operating conditions section in terms of DC voltage, AC noise, and start-up ramp time.
2. The TDP20MB421 does not require any special power supply filtering, such as ferrite beads, provided that the recommended operating conditions are met. Only standard supply decoupling is required. Typical supply decoupling consists of a 0.1µF capacitor per VCC pin, one 1µF bulk capacitor per device, and one 10µF bulk capacitor per power bus that delivers power to one or more devices. Connect the local decoupling (0.1µF) capacitors as close to the VCC pins as possible and with minimal path to the device ground pad.

7.4 Layout

7.4.1 Layout Guidelines

Follow these guidelines when designing the layout:

1. Place decoupling capacitors as close to the VCC pins as possible. If possible, place the decoupling capacitors directly underneath the device.

2. Tightly couple, skew match, and impedance control the high-speed differential signals TXnP/TXnN and RXnP/RXnN.
3. Avoid vias when possible on the high-speed differential signals. Minimize the via stub when using vias, either by transitioning through most or all layers or by back drilling.
4. GND relief is used beneath the high-speed differential signal pads to improve signal integrity by counteracting the pad capacitance. Using GND relief is not required.
5. Place GND vias directly beneath the device connecting the GND plane attached to the device to the GND planes on other layers. GND vias have the added benefit of improving thermal conductivity from the device to the board.

7.4.2 Layout Example

Figure 7-6 shows TDP20MB421 layout example.

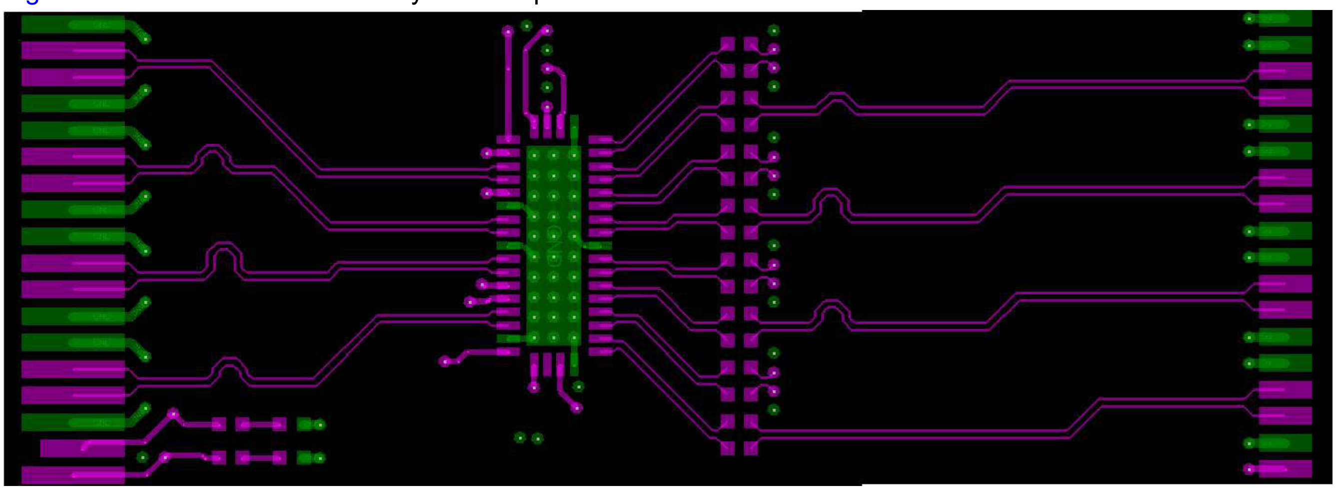


Figure 7-6. TDP20MB421 Layout Example

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2024	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TDP20MB421IRUAR	ACTIVE	WQFN	RUA	42	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	5PR421	Samples
TDP20MB421IRUAT	ACTIVE	WQFN	RUA	42	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	5PR421	Samples
TDP20MB421RUAR	ACTIVE	WQFN	RUA	42	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	5PR421	Samples
TDP20MB421RUAT	ACTIVE	WQFN	RUA	42	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	5PR421	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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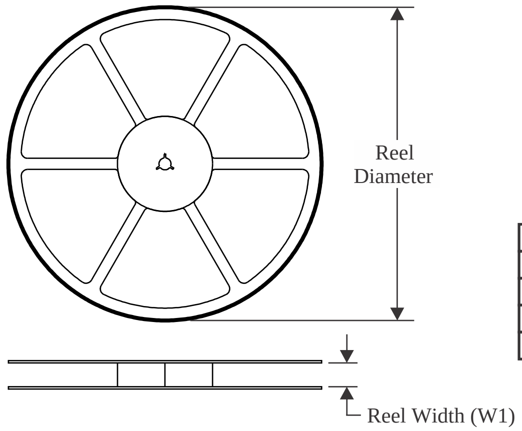
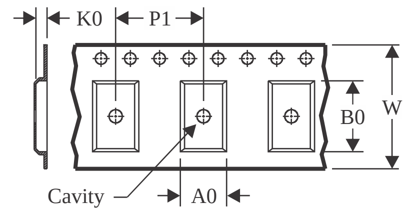
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

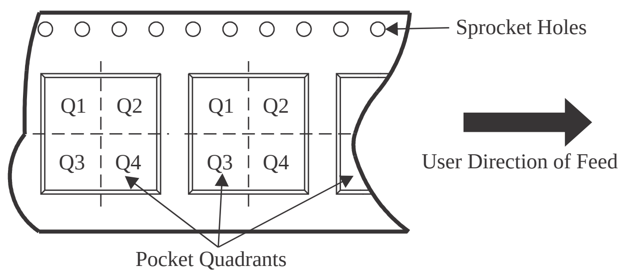


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

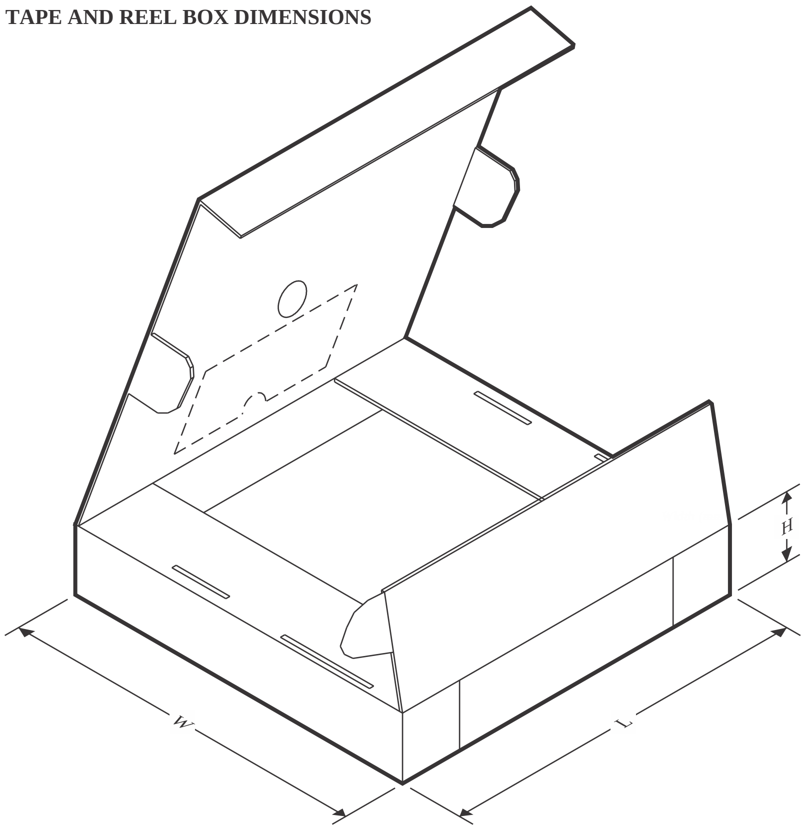
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TDP20MB421IRUAR	WQFN	RUA	42	3000	330.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1
TDP20MB421IRUAT	WQFN	RUA	42	250	180.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1
TDP20MB421RUAR	WQFN	RUA	42	3000	330.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1
TDP20MB421RUAT	WQFN	RUA	42	250	180.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TDP20MB421IRUAR	WQFN	RUA	42	3000	367.0	367.0	35.0
TDP20MB421IRUAT	WQFN	RUA	42	250	210.0	185.0	35.0
TDP20MB421RUAR	WQFN	RUA	42	3000	367.0	367.0	35.0
TDP20MB421RUAT	WQFN	RUA	42	250	210.0	185.0	35.0

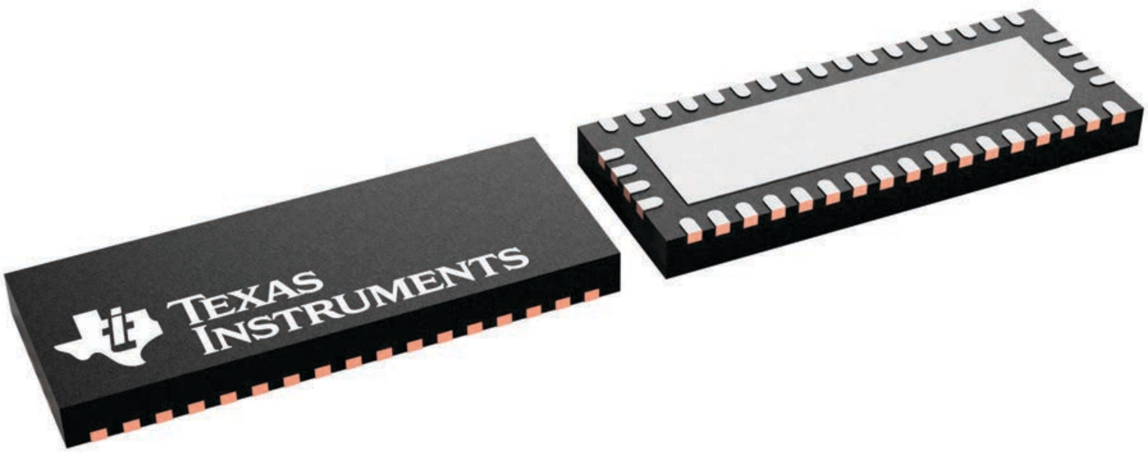
RUA 42

WQFN - 0.8 mm max height

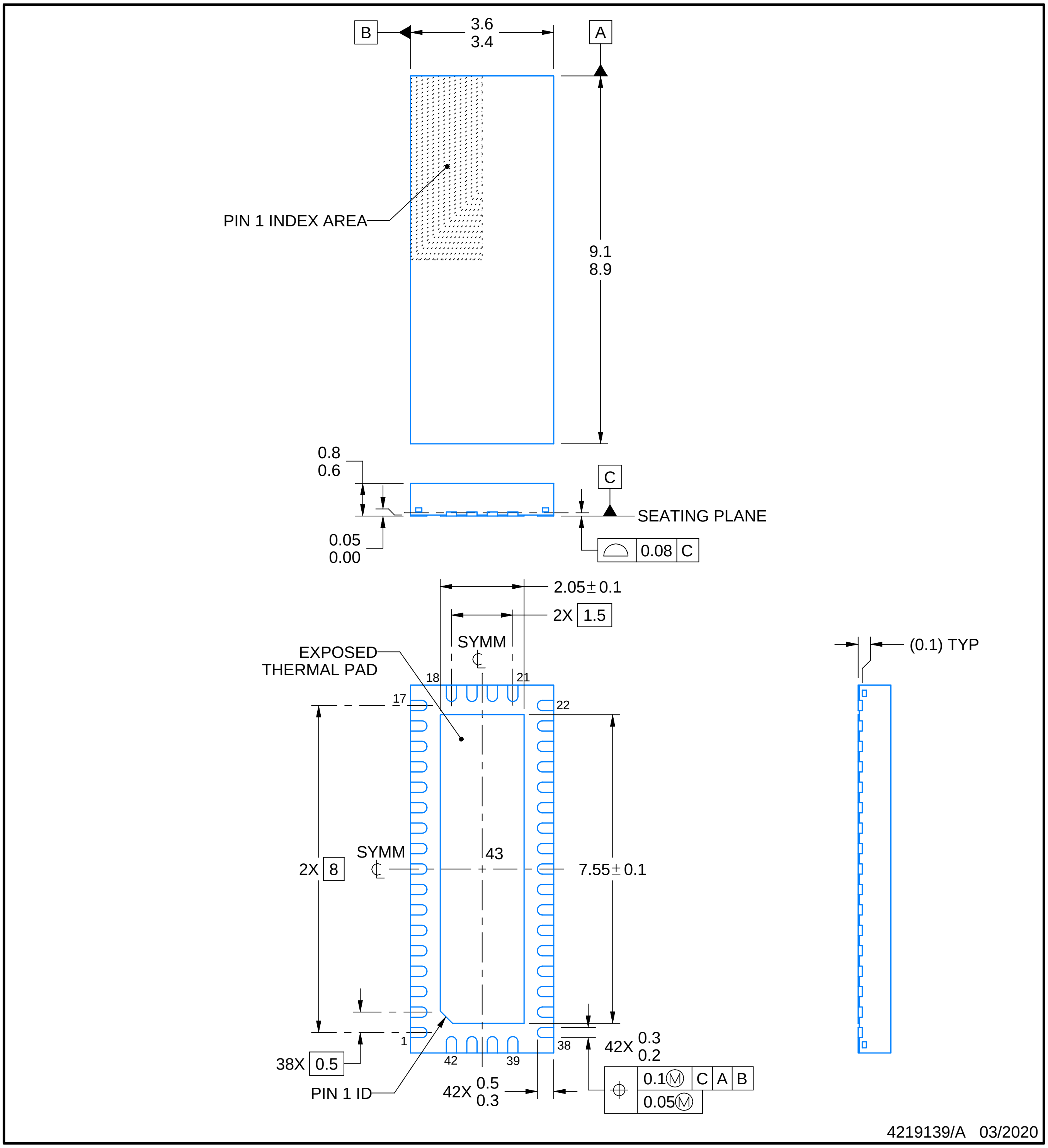
9 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

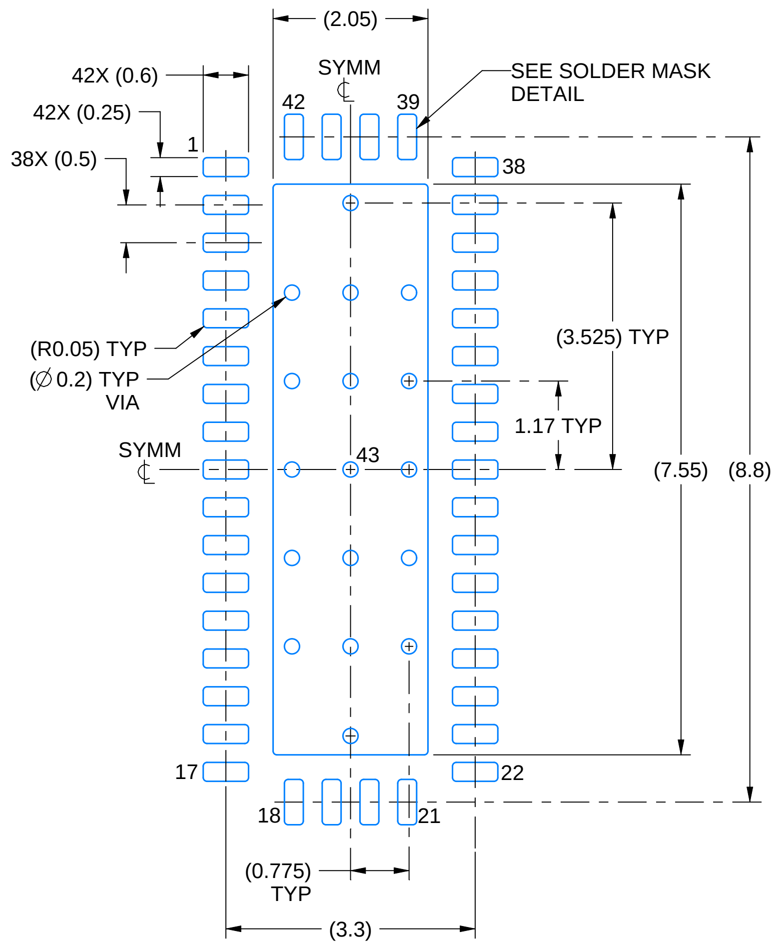


4226504/A

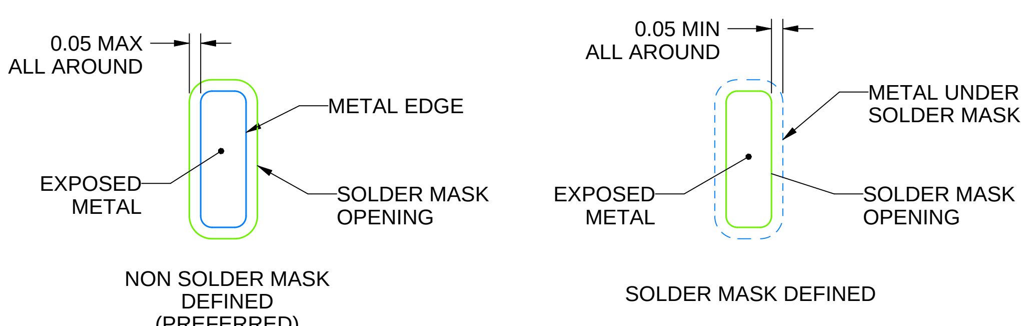


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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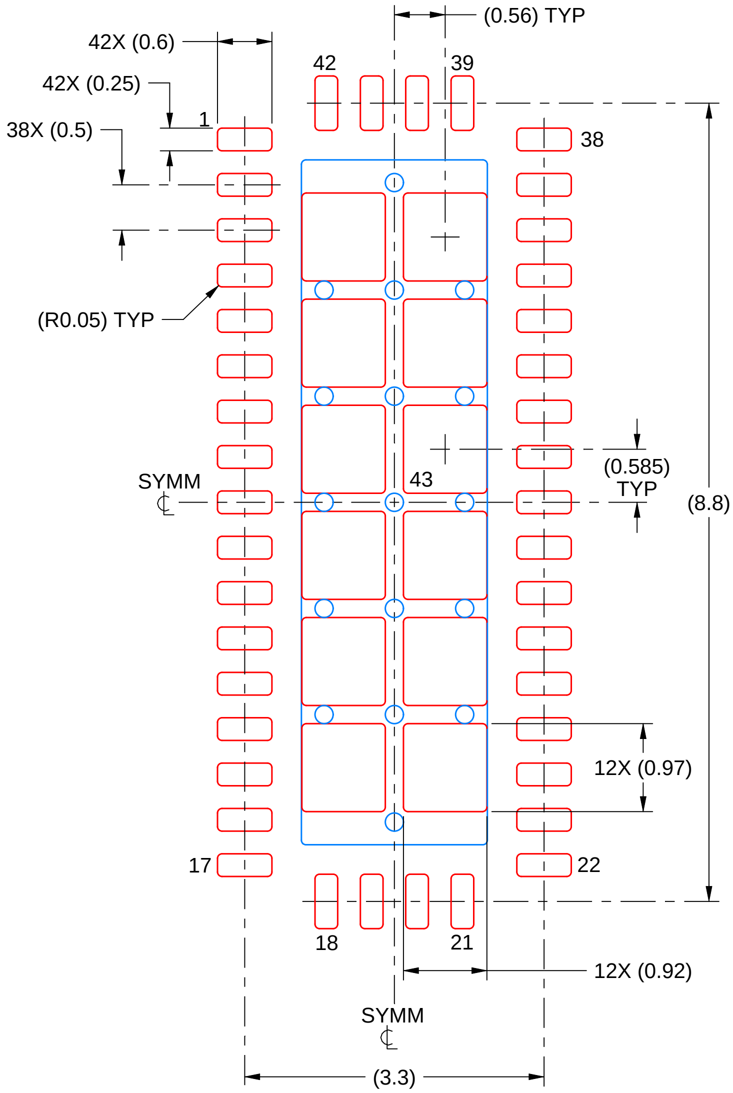
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 12X

EXPOSED PAD 43
69% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.