

## TPIC6596 Power Logic 8-bit Shift Register

### 1 Features

- Low  $r_{DS(on)}$ : 1.3 $\Omega$  Typical
- Avalanche energy: 75mJ
- Eight power DMOS transistor outputs of 250mA Continuous Current
- 1.5A pulsed current per output
- Output clamp voltage at 45V
- Enhanced cascading for multiple stages all registers cleared with single input
- Low power consumption

### 2 Applications

- Instrumentation clusters
- Tell-tale lamps
- LED illumination and controls
- Automotive relay or solenoids drivers

### 3 Description

The TPIC6596 is a monolithic, high-voltage, high-current power 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK) respectively. The storage register transfers data to the output buffer when shift-register clear ( $\overline{SRCLR}$ ) is high. Write data and read data are valid only when RCK is low. When  $\overline{SRCLR}$  is low, all registers in the device are cleared. When output enable ( $\overline{G}$ ) is held high, all data in the output buffers is held low and all drain outputs are off. When  $\overline{G}$  is held low, data from the storage register is transparent to the output buffers. The serial output (SER OUT) is clocked out of the device on the falling edge of SRCK to provide additional hold time for cascaded applications. This provides improved performance for applications where clock signals can be skewed, devices are not located near one another, or the system must tolerate electromagnetic interference.

Outputs are low-side, open-drain DMOS transistors with output ratings of 45V and 250mA continuous sink current capability. When data in the output buffers is low, the DMOS-transistor outputs are off. When data

is high, the DMOS-transistor outputs have sink current capability.

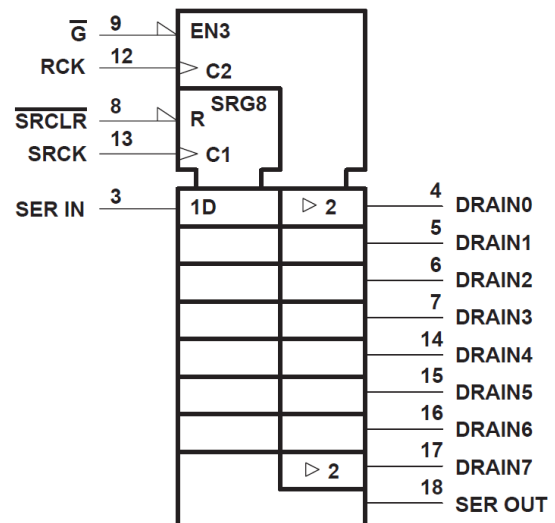
Separate power and logic level ground pins are provided to facilitate maximum system flexibility. Pins 1, 10, 11, and 20 are internally connected, and each pin must be externally connected to the power system ground to minimize parasitic inductance. A single-point connection between pin 19, logic ground (LGND), and pins 1, 10, 11, and 20, power grounds (PGND), must be externally made in a manner that reduces crosstalk between the logic and load circuits. The TPIC6596 is characterized for operation over the operating case temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

#### Device Information

PART NUMBER <sup>(1)</sup>	PACKAGE	BODY SIZE (NOM)
TPIC6596	SOIC (20)	12.80mm × 7.50mm
	PDIP (20)	25.40mm × 6.35mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.

#### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### Typical Application



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## 4 Pin Configuration and Functions

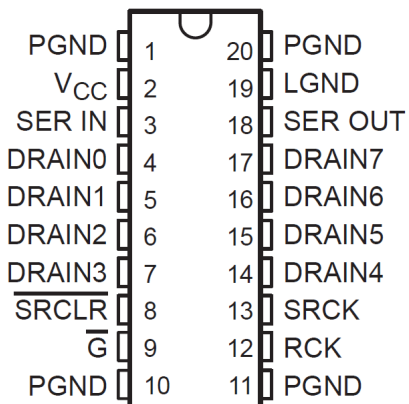


Figure 4-1. DW or N Package, 20-pin SOIC (Top- View)

Table 4-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
DRAIN0	4	O	Open-drain output
DRAIN1	5		
DRAIN2	6		
DRAIN3	7		
DRAIN4	14		
DRAIN5	15		
DRAIN6	16		
DRAIN7	17		
$\overline{G}$	9	I	Output enable, active-low
LGND	19	-	Logic ground
PGND	1, 10, 11, 20	-	Power ground
RCK	12	I	Register clock
SER IN	3	I	Serial data input
SER OUT	18	O	Serial data output
SRCK	13	I	Shift register clock
SRCLR	8	I	Shift register clear, active-low
V <sub>CC</sub>	2	I	Power supply

(1) P: Power Pin; I: Input Pin; I/O: Input/Output Pin; O: Output Pin.

## 5 Specifications

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

### 5.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
$V_{CC}$	Logic supply voltage		7	V
$V_I$	Logic input voltage range	-0.3	7	V
$V_{DS}$	Power DMOS drain-to-source voltage		45	V
	Continuous source-drain diode anode current		1	A
	Pulsed source-drain diode anode current		2	A
	Pulsed drain current, each output, all outputs on, see also <sup>(3)</sup>		750	mA
$I_{Dn}$	Continuous drain current, each output, all outputs on, $T_A = 25^\circ$		250	mA
$I_{DM}$	Peak drain current single output, $T_A = 25^\circ\text{C}$ (See <sup>(3)</sup> )		2	A
$E_{AS}$	Single-pulse avalanche energy (See <sup>(4)</sup> )		75	mJ
$I_{AS}$	Avalanche current (See <sup>(4)</sup> )		1	A
	Continuous total power dissipation	see Section 5.2		<sup>(5)</sup>
$T_J$	Operating virtual junction temperature range	-40	150	$^\circ\text{C}$
$T_{slg}$	Storage temperature	-65	150	$^\circ\text{C}$
	Lead temperature 1, 6mm (1/16 inch) from case for 10 seconds		260	$^\circ\text{C}$

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values are with respect to network ground terminal GND.
- (3) Pulse duration  $\leq 100\mu\text{s}$ , duty cycle  $\leq 2\%$
- (4) DRAIN supply voltage = 15V, starting junction temperature ( $T_{JS}$ ) =  $25^\circ\text{C}$ ,  $L = 100\text{mH}$ ,  $I_{AS} = 1\text{A}$  (see Figure 5-1).
- (5) See Dissipation Table

### 5.2 Dissipation Rating Table

PACKAGE	$T_C \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_C = 25^\circ\text{C}$	$T_C = 125^\circ\text{C}$ POWER RATING
DW	1125mW	9.0mW/ $^\circ\text{C}$	225mW
N	1150mW	9.2mW/ $^\circ\text{C}$	230mW

over operating free-air temperature range (unless otherwise noted)

### 5.3 Recommended Operating Conditions

		MIN	MAX	UNIT
$V_{CC}$	Logic supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	$0.85V_{CC}$		V
$V_{IL}$	Low-level input voltage		$0.15V_{CC}$	V
	Pulsed drain output current, $T_C = 25^\circ\text{C}$ , $V_{CC} = 5\text{V}$ See <sup>(1)</sup> , <sup>(2)</sup>	-1.8	1.5	A
$t_{su}$	Setup time, SER IN high before SRCK $\uparrow$ , see Figure 6-2	10		ns
$t_h$	Hold time, SER IN high after SRCK $\uparrow$ , see Figure 6-2	10		ns
$t_w$	Pulse duration, see Figure 6-2	20		ns
$T_C$	Operating case temperature	-40	125	$^\circ\text{C}$

- (1) Pulse duration  $\leq 100\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- (2) Technique must limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum.

over operating free-air temperature range ( $V_{CC} = 5V$ ,  $T_C = 25^\circ C$ , unless otherwise noted)

## 5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-source breakdown voltage	$I_D = 1mA$	45			V
$V_{SD}$	Source-drain diode forward voltage	$I_F = 250mA$ , see (1)		0.85	1	V
$V_{OH}$	High-level output voltage, High-level output voltage, SER OUT	$I_{OH} = -20mA$ , $V_{CC} = 4.5V$	4.4	4.49		V
		$I_{OH} = -4mA$ , $V_{CC} = 4.5V$	4.1	4.3		
$V_{OL}$	Low-level output voltage, SER OUT	$I_{OH} = 20mA$ , $V_{CC} = 4.5V$		0.002	0.1	V
		$I_{OH} = 4mA$ , $V_{CC} = 4.5V$		0.2	0.4	
$V_{(hys)}$	Input hysteresis	$V_{DS} = 15V$		1.3		V
$I_{IH}$	High-level input current	$V_{CC} = 5.5V$ , $V_I = V_{CC}$			1	$\mu A$
$I_{IL}$	Low-level input current	$V_{CC} = 5.5V$ , $V_I = 0$			-1	$\mu A$
$I_{CCL}$	Logic supply current	$I_O = 0$ , All inputs low		15	100	$\mu A$
$I_{CC(FRQ)}$	Logic supply current frequency	$f_{SRCK} = 5MHz$ , $I_O = 0$ , $CL = 30pF$ See Figure 6-1, Figure 6-2, and Figure 5-2		0.6	5	mA
$I_N$	Nominal current	$V_{DS(on)} = 0.5V$ , $I_N = I_D$ , $T_C = 85^\circ C$ . See (2), (3), and (4)		250		mA
$I_{DSX}$	Off-state drain current	$V_{DS} = 40V$		0.05	1	$\mu A$
		$V_{DS} = 40V$ ; $T_C = 125^\circ C$		0.15	5	
$r_{DS(on)}$	Static drain-source on-state resistance	$I_D = 250mA$ , $V_{CC} = 4.5V$ See (2), (3), Figure 5-5 and Figure 5-6		1.3	2	$\Omega$
		$I_D = 250mA$ , $V_{CC} = 4.5V$ , $T_C = 125^\circ C$ .		2	3.2	
		$I_D = 500mA$ , $V_{CC} = 4.5V$		1.3	2	

- (1) Pulse duration  $\leq 100\mu s$ , duty cycle  $\leq 2\%$ .  
(2) Technique must limit  $T_J - T_C$  to  $10^\circ C$  maximum.  
(3) These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.  
(4) Nominal current is defined for a consistent comparison between devices from different sources. The current produces a voltage drop of 0.5V at  $T_C = 85^\circ C$ .

over operating free-air temperature range (unless otherwise noted)

## 5.5 Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay time, low-to-high-level output from G	$C_{LL} = 30pF = 30pF$ , $I_{DD} = 250mA$ , See Figure 6-1, Figure 6-2, and Figure 5-7		650		ns
$t_{PHL}$	Propagation delay time, high-to-low-level output from G			200		ns
$t_r$	Rise time, drain output			230		ns
$t_f$	Fall time, drain output			170		ns
$t_{PD}$	Propagation delay time, SRCK <sub>I</sub> to SER OUT	$C_L = 30pF$ , $I_D = 250mA$ , See (3)		50		ns
$f_{SRCK}$	Serial clock frequency	$C_L = 30pF$ , $I_D = 250mA$ , See Figure 6-2			5	MHz
$t_a$	Reverse-recovery-current rise time	$I_{FF} = 250mA$ , $di/dt = 20A/\mu s$ . See (1), (2), and Figure 6-3		100		ns
$t_{rr}$	Reverse-recovery time			300		

- (1) Technique must limit  $T_J - T_C$  to  $10^\circ C$  maximum.  
(2) These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.  
(3) This is the maximum serial clock frequency assuming cascaded operation where serial data is passed from one stage to a second stage. The clock period allows SRCK  $\rightarrow$  SER OUT propagation delay and setup time plus some timing margin

## 5.6 Thermal Resistance Characteristics

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	DW	All eight outputs with equal power		111	$^{\circ}\text{C}/\text{W}$
		N			108	

## 5.7 Typical Characteristics

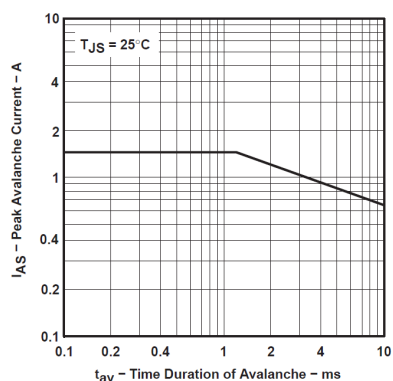


Figure 5-1. Peak Avalanche Current vs. Time Duration of Avalanche

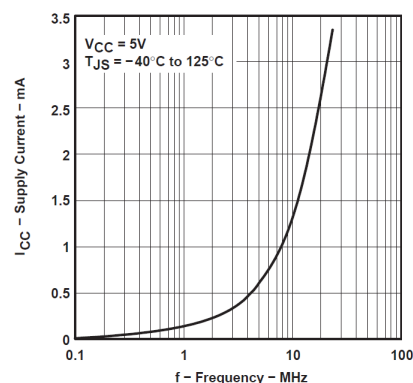


Figure 5-2. Supply Current vs. Frequency

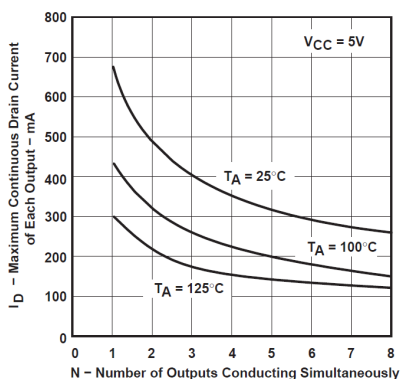


Figure 5-3. Maximum Continuous Drain Current of Each Output vs. Number Of Outputs Conducting Simultaneously

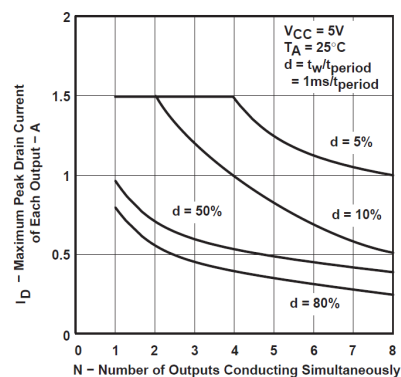
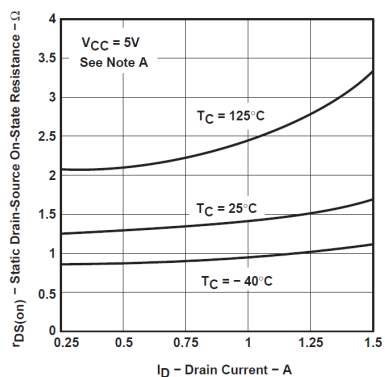
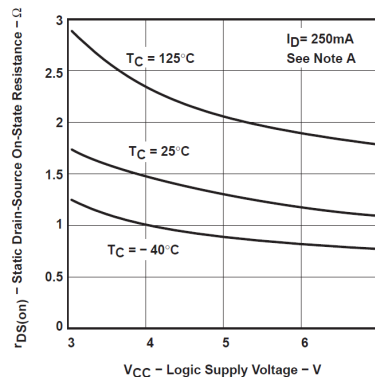


Figure 5-4. Maximum Peak Drain Current of Each Output vs. Number of Outputs Conducting Simultaneously

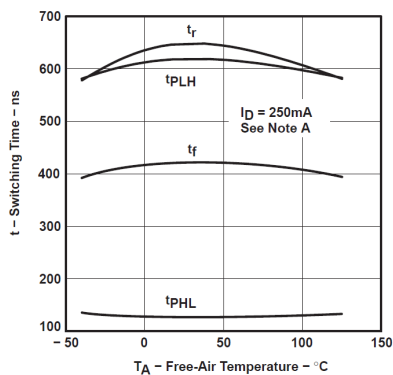
## 5.7 Typical Characteristics (continued)



**Figure 5-5. Static Drain-source On-state Resistance vs. Drain Current**

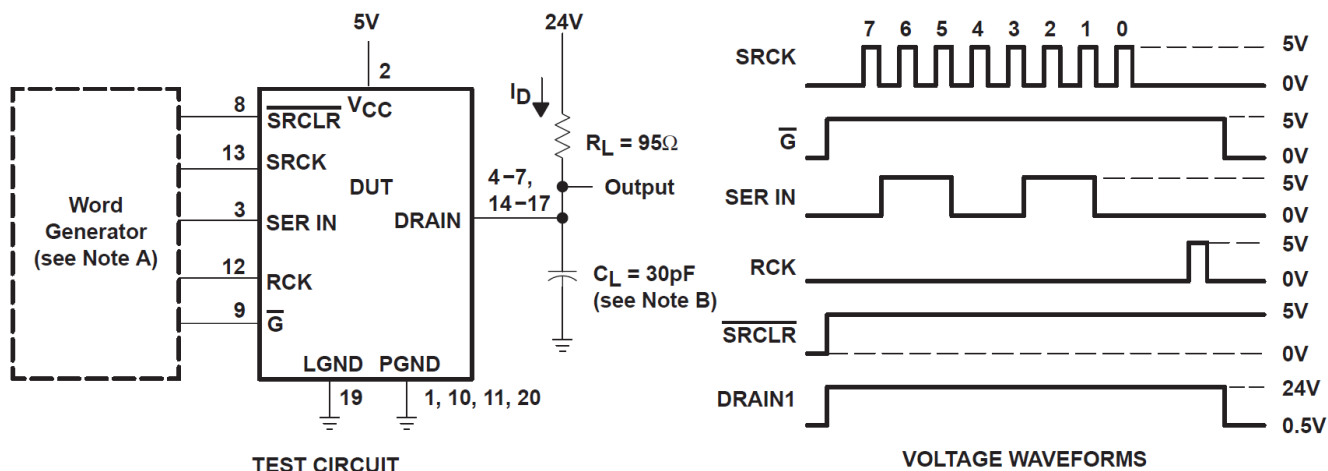


**Figure 5-6. Static Drain-source On-state Resistance vs. Logic Supply Voltage**



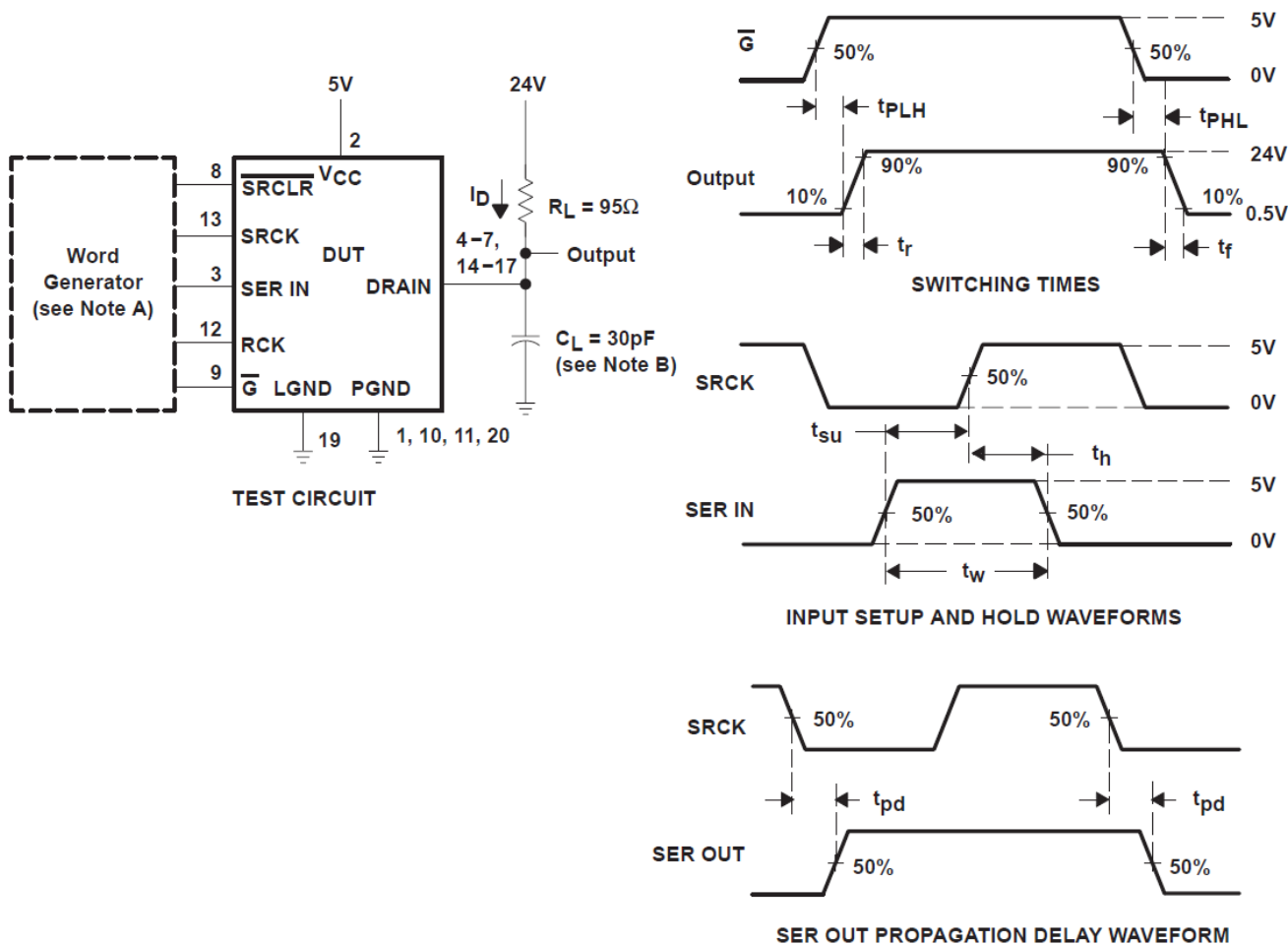
**Figure 5-7. Switching Time vs. Free-air Temperature**

## 6 Parameter Measurement Information



A. Write data and read data are valid only when RCK is low

**Figure 6-1. Resistive Load Operation**

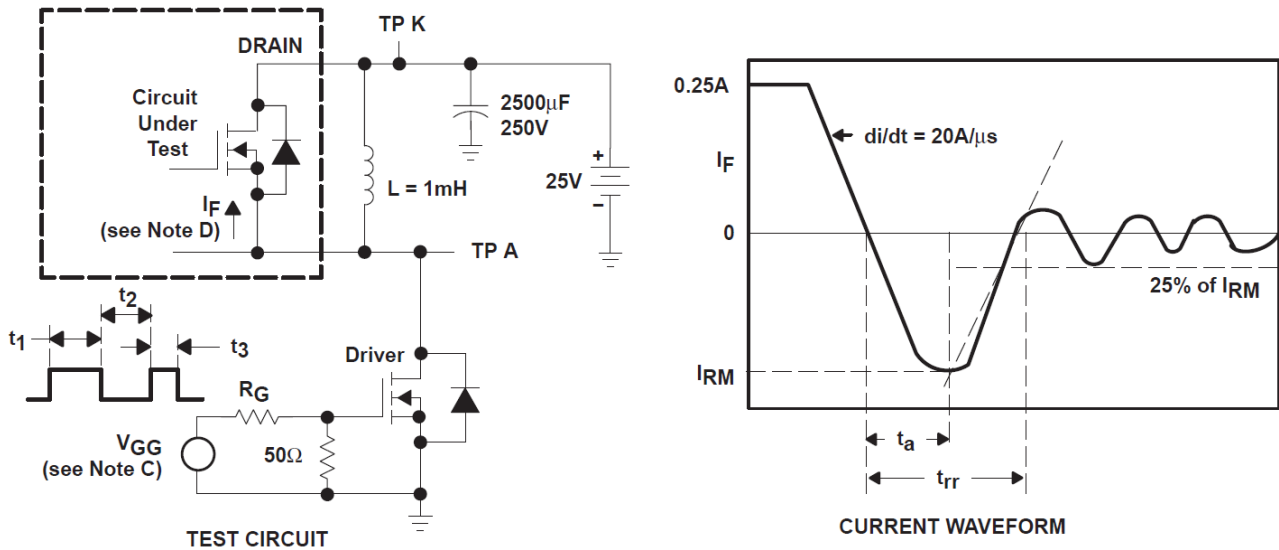


A.  $C_L$  includes probe and jig capacitance.



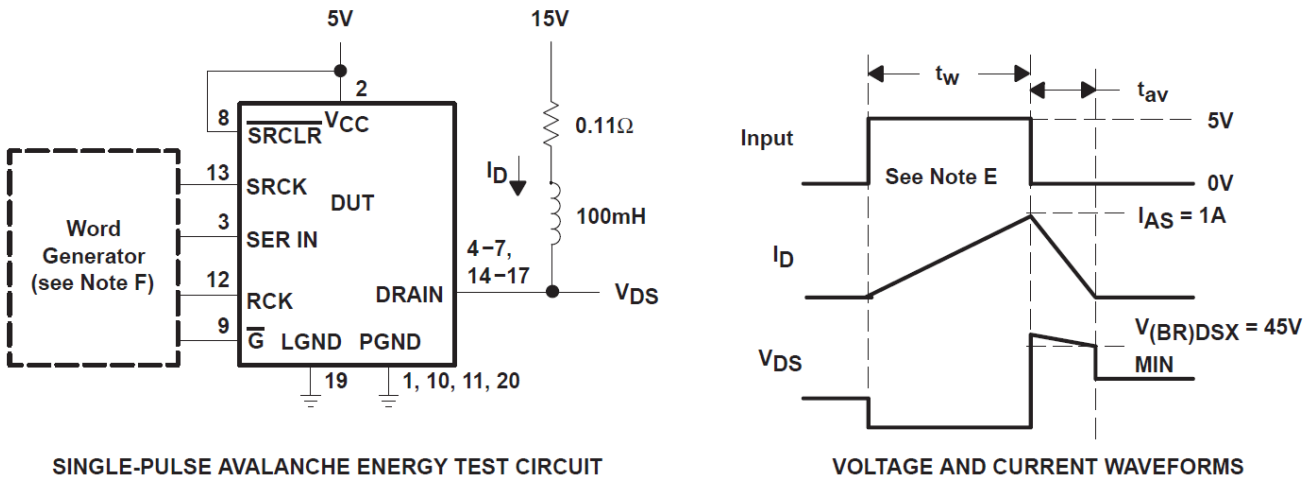
- B. Outputs DRAIN 1, 2, 5, and 6 low (PGND), all other DRAIN outputs are at 24V. The word generator has the following characteristics:  $t_r \leq 10\text{ns}$ ,  $t_f \leq 10\text{ns}$ ,  $t_w = 300\text{ns}$ , pulsed repetition rate (PRR) = 5kHz,  $Z_O = 50\Omega$ .

**Figure 6-2. Test Circuit, Switching Times, and Voltage Waveforms**



- A. The  $V_{GG}$  amplitude and  $R_G$  are adjusted for  $di/dt = 20\text{A}/\mu\text{s}$ . A  $V_{GG}$  double-pulse train is used to set  $I_F = 0.25\text{A}$ , where  $t_1 = 10\mu\text{s}$ ,  $t_2 = 7\mu\text{s}$ , and  $t_3 = 3\mu\text{s}$ .
- B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

**Figure 6-3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode**



- A. The word generator has the following characteristics:  $t_r \leq 10\text{ns}$ ,  $t_f \leq 10\text{ns}$ ,  $Z_O = 50\Omega$ .
- B. Input pulse duration,  $t_w$ , is increased until peak current  $I_{AS} = 1\text{A}$ . Energy test level is defined as  $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2 = 75\text{mJ}$ , where  $t_{av}$  = avalanche time.

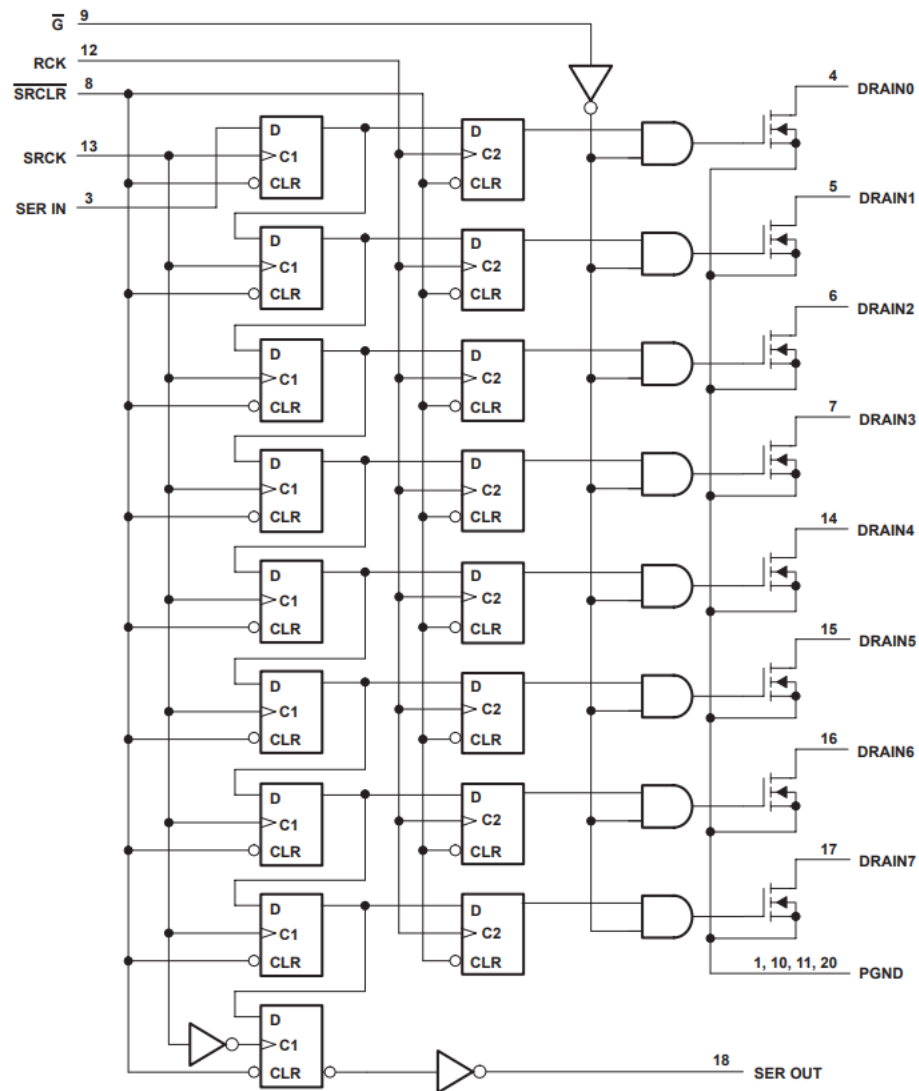
**Figure 6-4. Single-Pulse Avalanche Energy Test Circuit and Waveforms**

## 7 Detailed Description

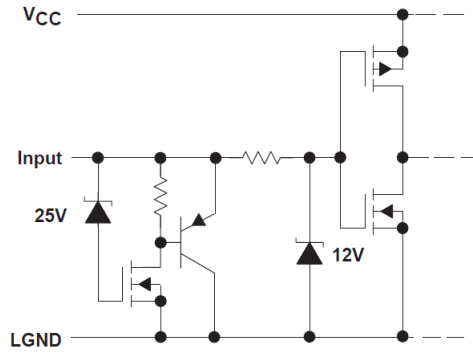
## 7.1 Overview

The TPIC6596 is a monolithic, high-voltage, highcurrent power 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads.

## 7.2 Functional Block Diagram

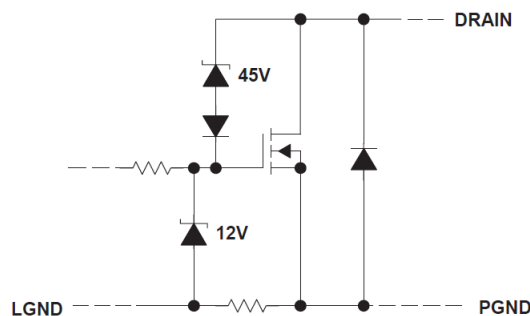


### Figure 7-1. Functional Block Diagram



**Equivalent of Each Input Schematic**

TYPICAL OF ALL DRAIN OUTPUTS



**Typical of All Drain Outputs Schematic**

## 7.3 Feature Description

### 7.3.1 Serial-In Interface

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK) respectively. Write data and read data are valid only when RCK is low. The storage register transfers data to the output buffer when shift register clear ( $\overline{\text{SRCLR}}$ ) is high.

### 7.3.2 Clear Register

A logical low on ( $\overline{\text{SRCLR}}$ ) clears all registers in the device. TI suggests clearing the device during power up or initialization.

### 7.3.3 Output Control

When output enable (G) is held high, all data in the output buffers is held low and all drain outputs are off. Holding ( $\overline{\text{G}}$ ) low makes data from the storage register transparent to the output buffers. When data in the output buffers is low, the DMOS transistor outputs are OFF. When data is high, the DMOS transistor outputs have sink-current capability. This pin can also be used for global PWM dimming.

### 7.3.4 Cascaded Application

The serial output (SER OUT) is clocked out of the device on the falling edge of SRCK to provide additional hold time for cascaded applications. This will provide improved performance for applications where clock signals may be skewed, devices are not located near one another, or the system must tolerate electromagnetic interference. Connect the device (SER OUT) pin to the next device (SER IN) for daisy Chain.

### 7.3.5 Current Limit Function

Outputs are low-side, open-drain DMOS transistors with output ratings of 45V and 250mA continuous sink current capability

## 7.4 Device Functional Modes

### 7.4.1 Operating with $V_{CC} < 4.5V$

This device works normally during  $4.5V \leq V_{CC} \leq 5.5V$ , when operation voltage is lower than 4.5V, correct behavior of the device, including communication interface and current capability, is not assured.

### 7.4.2 Operating with $5.5V < V_{CC} \leq 7V$

The device works normally in this voltage range, but reliability issues can occur if the device works for a long time in this voltage range.

## 8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2000) to Revision B (March 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Changed SRCLR timing diagram.....	8

Changes from Revision * (May 2005) to Revision A (April 2000)	Page
• Changed SRCLR timing diagram.....	1

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPIC6596DWG4	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI		TPIC6596	
TPIC6596DWRG4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		TPIC6596	Samples
TPIC6596N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TPIC6596N	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPIC6596DWRG4	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TPIC6596DWRG4	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPIC6596DWRG4	SOIC	DW	20	2000	350.0	350.0	43.0
TPIC6596DWRG4	SOIC	DW	20	2000	350.0	350.0	43.0

## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TPIC6596N	N	PDIP	20	20	506	13.97	11230	4.32

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

**DW0020A****PACKAGE OUTLINE****SOIC - 2.65 mm max height**

SOIC



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**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

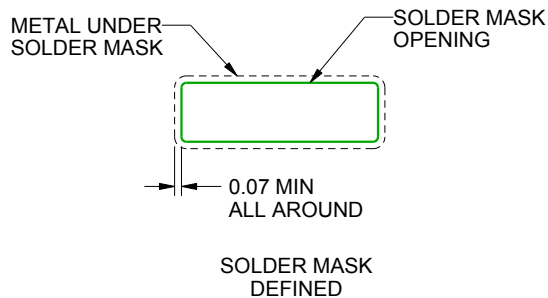
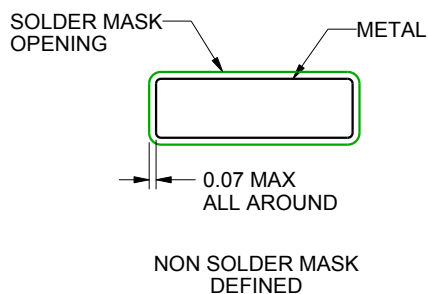
**DW0020A**

## SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



## SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.  
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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