

## TPIC6A596 Power Logic 8-Bit Shift Register

### 1 Features

- Low  $r_{DS(on)}$ : 1 $\Omega$  (Typical)
- Output short-circuit protection
- Avalanche energy: 75mJ
- Eight 350mA DMOS outputs
- 50V Switching capability
- Enhanced cascading for multiple stages
- All registers cleared with single input
- Low power consumption

### 2 Application

- Instrumentation Clusters
- Tell-Tale Lamps
- LED Illumination and Controls
- Automotive Relay or Solenoids Drivers

### 3 Description

The TPIC6A596 is a monolithic, high-voltage, high-current power logic 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium- current or high-voltage loads. Each open-drain DMOS transistor features an independent chopping current-limiting circuit to prevent damage in the case of a short circuit.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit, D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift-register clear (SRCLR) is high. Write data and read data are valid only when RCK is low. When SRCLR is low, all registers in the device are cleared. When output enable  $\overline{G}$  is held high, all data in the output buffers is held low and all drain outputs are off. When  $\overline{G}$  is held low, data from the storage register is transparent to the output buffers. The serial output (SER OUT) is clocked out of the device on the falling edge of SRCK to provide additional hold time for cascaded applications. This will provide improved performance for applications where clock signals may be skewed, devices are not located near one another, or the system must tolerate electromagnetic interference.

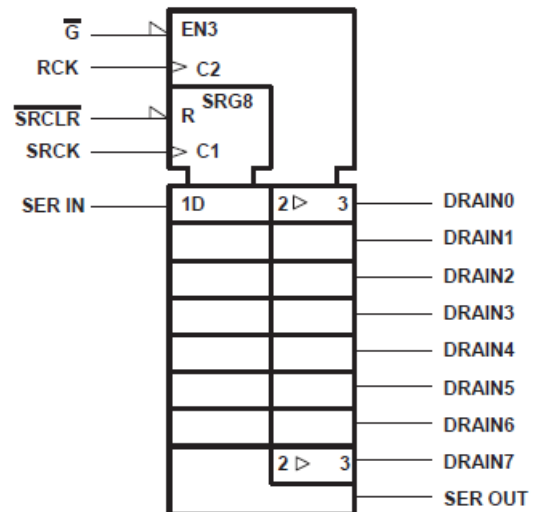
Outputs are low-side, open-drain DMOS transistors with output ratings of 50V and a 350mA continuous sink current capability. When data in the output buffers is low, the DMOS-transistor outputs are off. When data is high, the DMOS-transistor outputs have sink current capability.

Separate power ground (PGND) and logic ground (LGND) terminals are provided to facilitate maximum system flexibility. All PGND terminals are internally connected, and each PGND terminal must be externally connected to the power system ground to minimize parasitic impedance. A single-point connection between LGND and PGND must be made externally in a manner that reduces crosstalk between the logic and load circuits.

The TPIC6A596 is offered in a thermally-enhanced dual-in-line (NE) package and a wide-body surface-mount (DW) package. The TPIC6A596 is characterized for operation over the operating case temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

**Table 3-1. Device Information**

| PART NUMBER | PACKAGE  | BODY SIZE(NOM)   |
|-------------|----------|------------------|
| TPIC6A596   | PDIP(20) | 24.00mm × 6.86mm |
|             | SOIC(24) | 15.40mm × 7.50mm |



This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### Logic Symbol



## Table of Contents

|  |    |  |    |
|--|----|--|----|
| <b>1 Features</b> .....                          | 1  | 7.2 Functional Block Diagram.....                                | 12 |
| <b>2 Application</b> .....                       | 1  | 7.3 Feature Description.....                                     | 13 |
| <b>3 Description</b> .....                       | 1  | <b>8 Device Functional Modes</b> .....                           | 14 |
| <b>4 Pin Configuration and Functions</b> .....   | 2  | 8.1 Operating with $V_{CC} < 4.5V$ .....                         | 14 |
| <b>5 Specifications</b> .....                    | 4  | 8.2 Operating with $5.5V < V_{CC} \leq 7V$ .....                 | 14 |
| 5.1 Absolute Maximum Ratings .....               | 4  | <b>9 Device and Documentation Support</b> .....                  | 15 |
| 5.2 Dissipation Rating Table.....                | 4  | 9.1 Documentation Support.....                                   | 15 |
| 5.3 Recommended Operating Conditions.....        | 4  | 9.2 Receiving Notification of Documentation Updates....          | 15 |
| 5.4 Electrical Characteristics.....              | 5  | 9.3 Support Resources.....                                       | 15 |
| 5.5 Switching Characteristics .....              | 6  | 9.4 Trademarks.....  | 15 |
| 5.6 Thermal Resistance .....                     | 6  | 9.5 Electrostatic Discharge Caution.....                         | 15 |
| 5.7 Typical Characteristics.....                 | 6  | 9.6 Glossary.....  | 15 |
| <b>6 Parameter Measurement Information</b> ..... | 8  | <b>10 Revision History</b> .....                                 | 15 |
| <b>7 Detailed Description</b> .....              | 12 | <b>11 Mechanical, Packaging, and Orderable Information</b> ..... | 15 |
| 7.1 Overview.....                                | 12 |  |    |

## 4 Pin Configuration and Functions

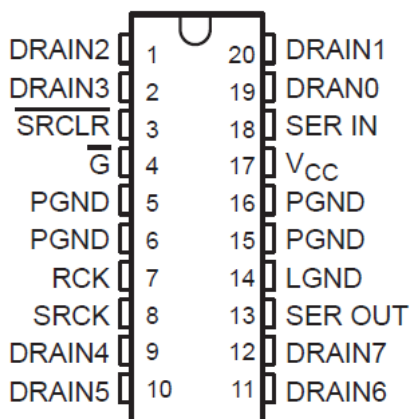


Figure 4-1. NE package 20-Pin PDIP Top View

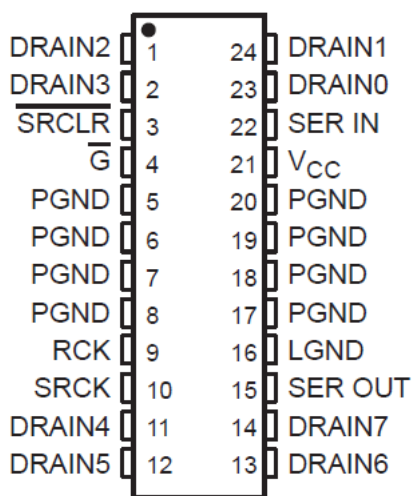


Figure 4-2. DW package 24-Pin SOIC Top View

## Pin Function

**Table 4-1. PDIP Pin Function**

| PIN            |              | I/O | DESCRIPTION                      |
|----------------|--------------|-----|----------------------------------|
| Name           | NO.          |     |                                  |
| DRAIN0         | 19           | O   | Open-drain output                |
| DRAIN1         | 20           |     |                                  |
| DRAIN2         | 1            |     |                                  |
| DRAIN3         | 2            |     |                                  |
| DRAIN4         | 9            |     |                                  |
| DRAIN5         | 10           |     |                                  |
| DRAIN6         | 11           |     |                                  |
| DRAIN7         | 12           |     |                                  |
| $\overline{G}$ | 4            | I   | Output enable, active-low        |
| PGND           | 5, 6, 15, 16 | -   | Power ground                     |
| LGND           | 14           | -   | Line ground                      |
| RCK            | 7            | I   | Register clock                   |
| SERIN          | 18           | I   | Serial data input                |
| SEROUT         | 13           | O   | Serial data output               |
| SRCK           | 8            | I   | Shift register clock             |
| SRCLR          | 3            | I   | Shift register clear, active-low |
| VCC            | 17           | I   | Power supply                     |

**Table 4-2. SOIC Pin Function**

| PIN            |                            | I/O | DESCRIPTION                      |
|----------------|----------------------------|-----|----------------------------------|
| Name           | NO.                        |     |                                  |
| DRAIN0         | 23                         | O   | Open-drain output                |
| DRAIN1         | 24                         |     |                                  |
| DRAIN2         | 1                          |     |                                  |
| DRAIN3         | 2                          |     |                                  |
| DRAIN4         | 11                         |     |                                  |
| DRAIN5         | 12                         |     |                                  |
| DRAIN6         | 13                         |     |                                  |
| DRAIN7         | 14                         |     |                                  |
| $\overline{G}$ | 4                          | I   | Output enable, active-low        |
| PGND           | 5, 6, 7, 8, 17, 18, 19, 20 | -   | Power ground                     |
| LGND           | 16                         | -   | Line ground                      |
| RCK            | 9                          | I   | Register clock                   |
| SERIN          | 22                         | I   | Serial data input                |
| SEROUT         | 15                         | O   | Serial data output               |
| SRCK           | 10                         | I   | Shift register clock             |
| SRCLR          | 3                          | I   | Shift register clear, active-low |
| VCC            | 21                         | I   | Power supply                     |

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over recommended operating case temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |  | MIN                   | MAX | UNIT |
|------------------|--|-----------------------|-----|------|
| V <sub>CC</sub>  | Logic supply voltage <sup>(2)</sup>                              |                       | 7   | V    |
| V <sub>I</sub>   | Logic input voltage range  | -0.3                  | 7   | V    |
| V <sub>DS</sub>  | Power DMOS drain-to-source voltage <sup>(3)</sup>                |                       | 50  | V    |
|                  | Continuous source-drain diode anode current                      |                       | 1   | A    |
|                  | Pulsed source-drain diode anode current <sup>(4)</sup>           |                       | 2   | A    |
| I <sub>Dn</sub>  | Pulsed drain current, each output, all outputs on <sup>(4)</sup> | T <sub>A</sub> = 25°C | 1.1 | A    |
| I <sub>Dn</sub>  | Continuous drain current, each output, all outputs on            | T <sub>A</sub> = 25°C | 350 | mA   |
|                  | Peak drain current, single output <sup>(4)</sup>                 | T <sub>A</sub> = 25°C | 1.1 | A    |
| E <sub>AS</sub>  | Single-pulse avalanche energy (see Figure 6-6)                   |                       | 75  | mJ   |
| I <sub>AS</sub>  | Avalanche current <sup>(5)</sup>                                 |                       | 600 | mA   |
|                  | Continuous total dissipation                                     | See Section 5.2       |     |      |
| T <sub>C</sub>   | Operating case temperature range                                 | -40                   | 125 | °C   |
| T <sub>J</sub>   | Operating virtual junction temperature range                     | -40                   | 150 | °C   |
| T <sub>stg</sub> | Storage temperature range  | -65                   | 150 | °C   |
|                  | Lead temperature 1,6mm (1/16 inch) from case for 10 seconds      |                       | 260 | °C   |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to LGND and PGND.
- (3) Each power DMOS source is internally connected to PGND.
- (4) Pulse duration ≤ 100μs and duty cycle ≤ 2%.
- (5) DRAIN supply voltage = 15V, starting junction temperature (T<sub>JA</sub>) = 25°C, L = 210mH, I<sub>AS</sub> = 600mA (see Figure 6-6).

### 5.2 Dissipation Rating Table

| PACKAGE | T <sub>C</sub> ≤ 25°C<br>POWER RATING | DERATING FACTOR<br>ABOVE T <sub>C</sub> = 25°C | T <sub>C</sub> = 125°C<br>POWER RATING |
|---------|---------------------------------------|--|--|
| DW      | 1750mW                                | 14mW/°C  | 350mW                                  |
| NE      | 2500mW                                | 20mW/°C  | 500mW                                  |

### 5.3 Recommended Operating Conditions

|                 |   | MIN                  | MAX                  | UNIT |
|-----------------|---|----------------------|----------------------|------|
| V <sub>CC</sub> | Logic supply voltage  | 4.5                  | 5.5                  | V    |
| V <sub>IH</sub> | High-level input voltage  | 0.85 V <sub>CC</sub> | V <sub>CC</sub>      | V    |
| V <sub>IL</sub> | Low-level input voltage   | 0                    | 0.15 V <sub>CC</sub> | V    |
|                 | Pulsed drain output current, T <sub>C</sub> = 25°C, V <sub>CC</sub> = 5V <sup>(1) (2)</sup> | -1.8                 | 0.6                  | A    |
| t <sub>su</sub> | Setup time, SER IN high before SRCK (see Figure 6-2)  | 10                   |                      | ns   |
| t <sub>h</sub>  | Hold time, SER IN high after SRCK (see Figure 6-2)  | 10                   |                      | ns   |
| t <sub>w</sub>  | Pulse duration, (see Figure 6-2)  | 20                   |                      | ns   |
| T <sub>C</sub>  | Operating case temperature  | -40                  | 125                  | °C   |

- (1) Pulse duration ≤ 100μs and duty cycle ≤ 2%.
- (2) Technique should limit T<sub>J</sub>– T<sub>C</sub> to 10°C maximum.

## 5.4 Electrical Characteristics

$V_{CC} = 5V$ ,  $T_C = 25^\circ C$  (unless otherwise noted)

| PARAMETER     |   | TEST CONDITIONS                             |   | MIN   | TYP            | MAX | UNIT    |
|---------------|---|---|---|---|----------------|-----|---------|
| $V_{(BR)DSX}$ | Drain-to-source breakdown voltage       | $I_D = 1mA$                                 |   | 50  |                |     | V       |
| $V_{SD}$      | Source-to-drain diode forward voltage   | $I_F = 350mA$ ,                             | See <sup>(1)</sup>  |   | 0.8            | 1.1 | V       |
| $V_{OH}$      | High-level output voltage, SER OUT      | $I_{OH} = -20\mu A$                         |   | $V_{CC} - 0.1$  | $V_{CC}$       |     | V       |
|               |   | $I_{OH} = -4mA$                             |   | $V_{CC} - 0.5$  | $V_{CC} - 0.2$ |     |         |
| $V_{OL}$      | Low-level output voltage, SER OUT       | $I_{OL} = 20\mu A$                          |   |   | 0              | 0.1 | V       |
|               |   | $I_{OL} = 4mA$                              |   |   | 0.2            | 0.5 |         |
| $I_{IH}$      | High-level input current                | $V_I = V_{CC}$                              |   |   |                | 1   | $\mu A$ |
| $I_{IL}$      | Low-level input current                 | $V_I = 0$                                   |   |   |                | -1  | $\mu A$ |
| $I_{O(chop)}$ | Output current at which chopping starts | $T_C = 25^\circ C$ ,                        | See Figure 6-3 and Figure 6-4 <sup>(2)</sup>                            | 0.6   | 0.8            | 1.1 | A       |
| $I_{CC}$      | Logic supply current                    | $I_O = 0$ ,                                 | $V_I = V_{CC}$ or 0   |   | 0.5            | 5   | mA      |
| $I_{CC(FRQ)}$ | Logic supply current at frequency       | $f_{SRCK} = 5MHz$ ,<br>$V_I = V_{CC}$ or 0, | $I_O = 0$ ,<br>$V_{CC} = 5V$ ,<br>$C_L = 30 pF$ ,<br>See Figure 5-1     |   | 1.3            |     | mA      |
| $I_{(nom)}$   | Nominal current                         | $V_{DS(on)} = 0.5V$ ,<br>$V_{CC} = 5V$ ,    | $I_{(nom)} = I_D$ ,<br>See <sup>(2)</sup> <sup>(3)</sup> <sup>(4)</sup> |   | 350            |     | mA      |
| $I_D$         | Drain current, off-state                | $V_{DS} = 40V$ ,                            |   | $T_C = 25^\circ C$  |                | 0.1 | 1       |
|               |   | $V_{DS} = 40V$ ,                            |   | $T_C = 125^\circ C$   |                | 0.2 | 5       |
| $r_{DS(on)}$  | Static drain-source on-state resistance | $I_D = 350mA$ ,                             | $T_C = 25^\circ C$  | See Figure 5-4 and Figure 5-5 <sup>(2)</sup> <sup>(3)</sup> |                | 1   | 1.5     |
|               |   | $I_D = 350mA$ ,                             | $T_C = 125^\circ C$   |   |                | 1.7 | 2.5     |

- (1) Pulse duration  $\leq 100\mu s$  and duty cycle  $\leq 2\%$ .
- (2) Technique should limit  $T_J - T_C$  to  $10^\circ C$  maximum.
- (3) These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
- (4) Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of  $0.5V$  at  $T_C = 85^\circ C$ .

## 5.5 Switching Characteristics

 $V_{CC} = 5\text{ V}$ ,  $T_C = 25^\circ\text{C}$ 

| PARAMETER    |   | TEST CONDITIONS  |                                    | MIN | TYP | MAX | UNIT |
|--------------|---|--|------------------------------------|-----|-----|-----|------|
| $t_{PHL}$    | Propagation delay time, high-to-low-level output from G | $C_L = 30\text{pF}$ ,<br>See Figure 6-1, Figure 6-2 and Figure 5-6 | $I_D = 350\text{mA}$ ,             |     | 30  |     | ns   |
| $t_{PLH}$    | Propagation delay time, low-to-high-level output from G |  |                                    |     | 125 |     | ns   |
| $t_r$        | Rise time, drain output                                 |  |                                    |     | 60  |     | ns   |
| $t_f$        | Fall time, drain output                                 |  |                                    |     | 30  |     | ns   |
| $t_{pd}$     | Propagation delay time, SRCK $\downarrow$ to SEROUT     | $C_L = 30\text{pF}$ ,<br>See Figure 6-2                            | $I_D = 350\text{mA}$ ,             |     | 20  |     | ns   |
| $f_{(SRCK)}$ | Serial clock frequency                                  | $C_L = 30\text{pF}$ ,<br>See <sup>(3)</sup>                        | $I_D = 350\text{mA}$ ,             |     |     | 10  | MHz  |
| $t_a$        | Reverse-recovery-current rise time                      | $I_F = 350\text{mA}$ ,   | $di/dt = 20\text{A}/\mu\text{s}$ , |     | 100 |     | ns   |
| $t_{rr}$     | Reverse-recovery time                                   | See Figure 6-5 <sup>(1)</sup> <sup>(2)</sup>                       |                                    |     | 300 |     | ns   |

(1) Technique should limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum.

(2) These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

(3) This is the maximum serial clock frequency assuming cascaded operation where serial data is passed from one stage to a second stage. The clock period allows for SRCK @ SEROUT propagation delay and setup time plus some timing margin.

## 5.6 Thermal Resistance

| PARAMETER       |   | TEST CONDITIONS |                                    | MIN | MAX | UNIT                      |
|-----------------|---|-----------------|------------------------------------|-----|-----|---------------------------|
| $R_{\theta JC}$ | Thermal resistance, junction-to-case    | DW              | All eight outputs with equal power |     | 10  | $^\circ\text{C}/\text{W}$ |
|                 |   | NE              |                                    |     | 10  |                           |
| $R_{\theta JA}$ | Thermal resistance, junction-to-ambient | DW              | All eight outputs with equal power |     | 50  | $^\circ\text{C}/\text{W}$ |
|                 |   | NE              |                                    |     | 50  |                           |

## 5.7 Typical Characteristics

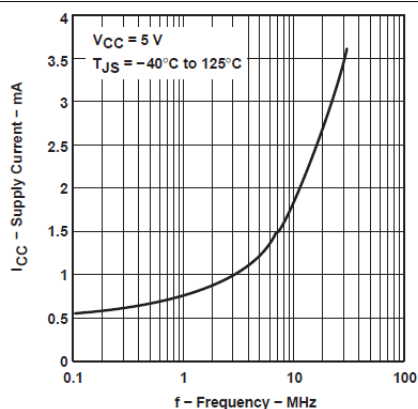


Figure 5-1. Supply Current vs Frequency

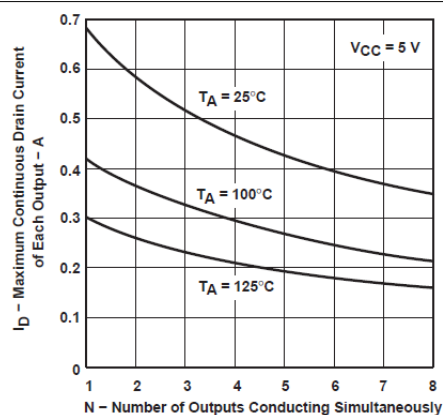
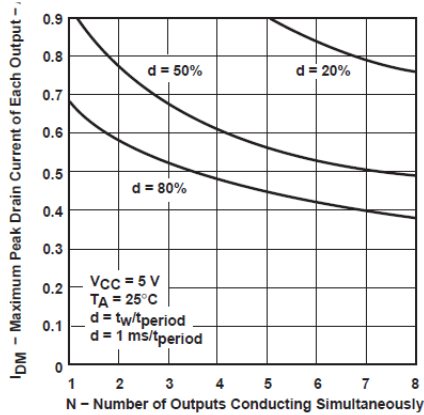
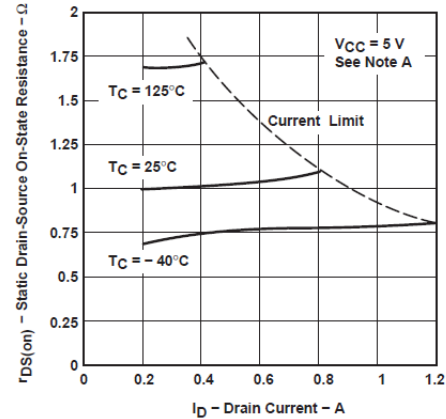


Figure 5-2. Maximum Continuous Drain Current of Each Output vs Number of Outputs Conducting Simultaneously

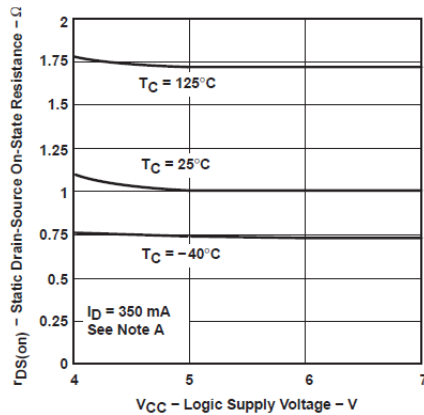
## 5.7 Typical Characteristics (continued)



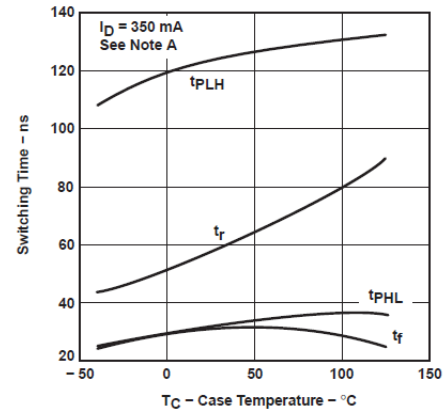
**Figure 5-3. Maximum Peak Drain Current of Each Output vs Number of Outputs Conducting Simultaneously**



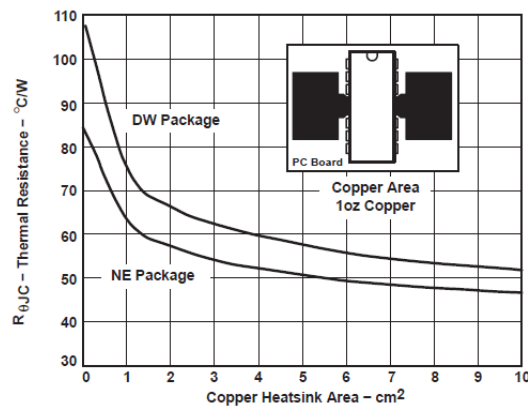
Technique should limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum.  
**Figure 5-4. Static Drain-Source On-State Resistance vs Drain Current**



Technique should limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum.  
**Figure 5-5. Static Drain-Source On-State Resistance vs Logic Supply Voltage**

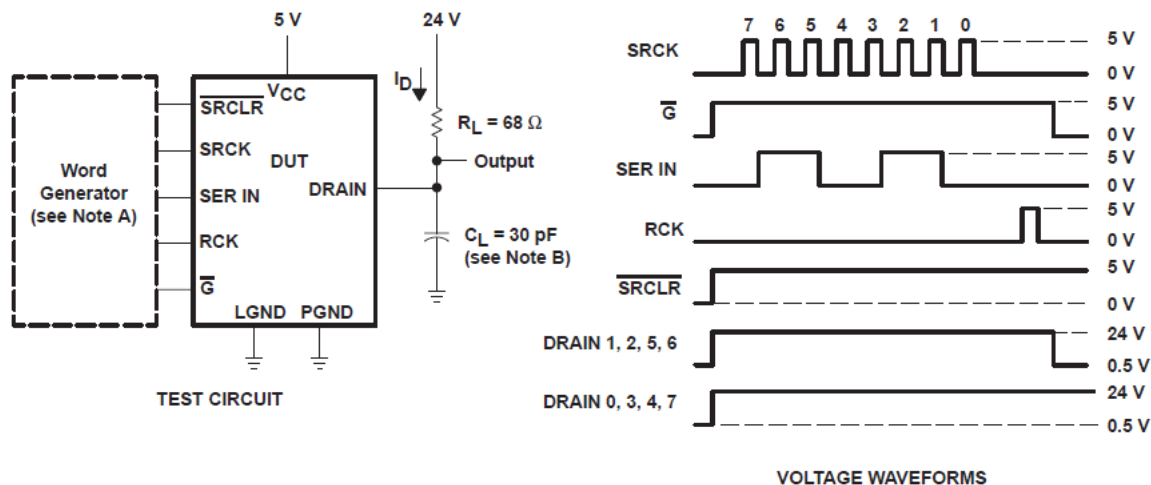


**Figure 5-6. Switching Time vs Case Temperature**



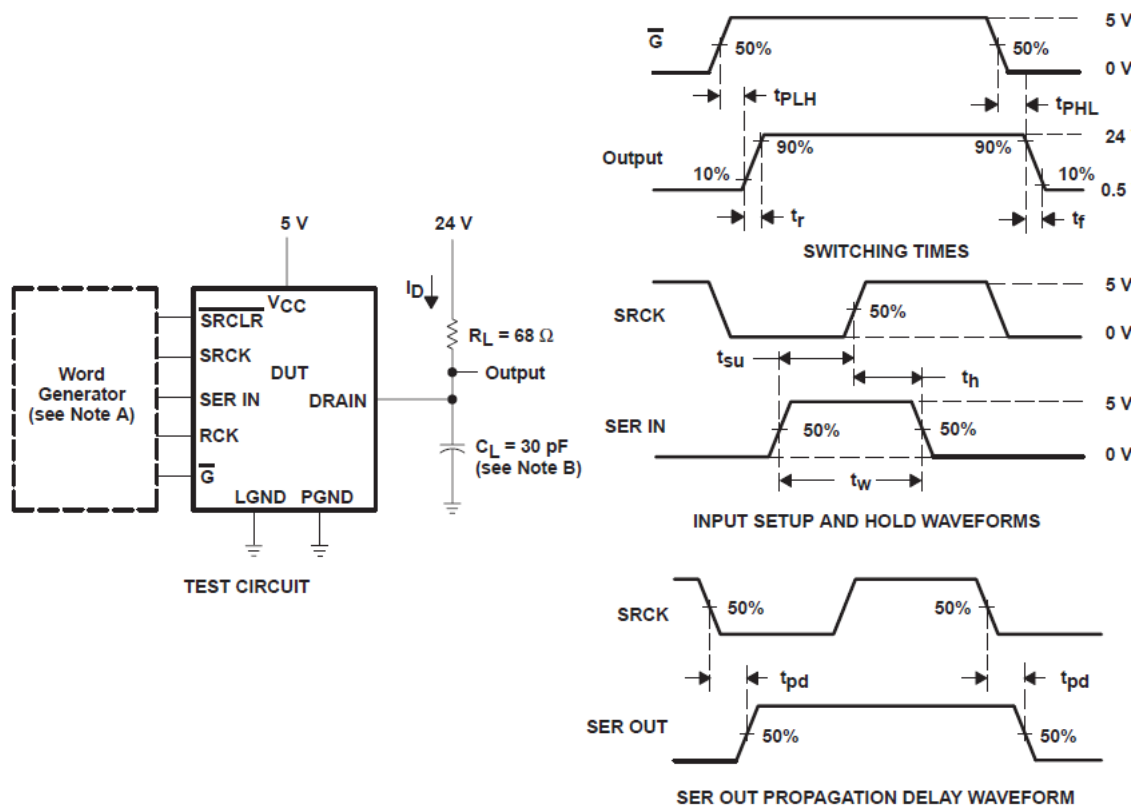
**Figure 5-7. Typical  $R_{\theta JA}$  Thermal Resistance vs On Board Heatsink Area**

## 6 Parameter Measurement Information



- A. The word generator has the following characteristics:  $t_r \leq 10\text{ns}$ ,  $t_f \leq 10\text{ns}$ ,  $t_w = 300\text{ns}$ , pulsed repetition rate (PRR) = 5kHz,  $Z_O = 50\Omega$ .
- B.  $C_L$  includes probe and jig capacitance.
- C. Write data and read data are valid only when RCK is low

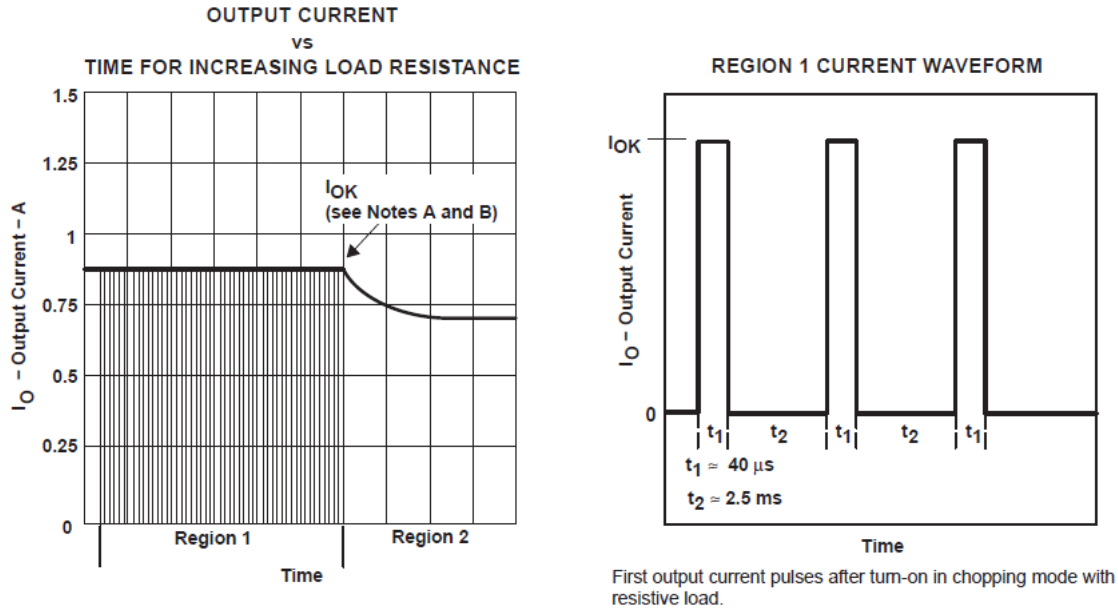
**Figure 6-1. Resistive Load Operation**



- A. The word generator has the following characteristics:  $t_r \leq 10\text{ns}$ ,  $t_f \leq 10\text{ns}$ ,  $t_w = 300\text{ns}$ , pulsed repetition rate (PRR) = 5kHz,  $Z_O = 50\Omega$ .
- B.  $C_L$  includes probe and jig capacitance.

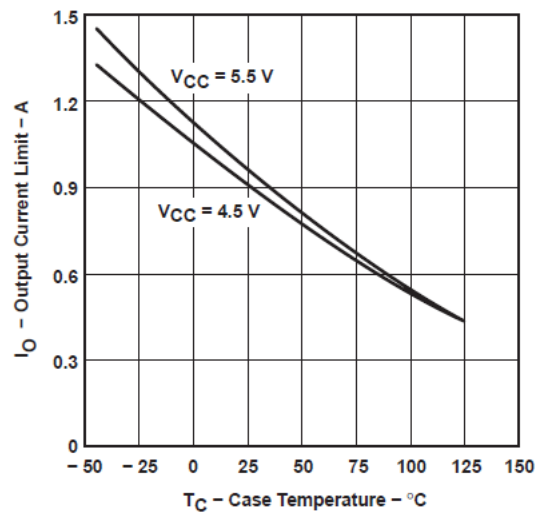
**Figure 6-2. Test Circuit, Switching Times, and Voltage Waveforms**



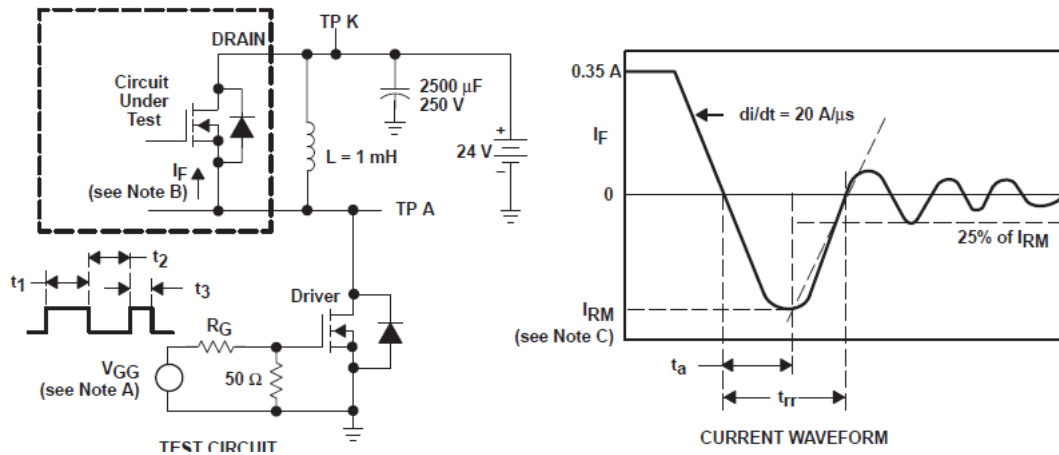


- A. The image above illustrates the output current characteristics of the device energizing a load having initially low, increasing resistance, e.g., an incandescent lamp. In region 1, chopping occurs and the peak current is limited to  $I_{OK}$ . In region 2, output current is continuous. The same characteristics occur in reverse order when the device energizes a load having an initially high, decreasing resistance.
- B. Region 1 duty cycle is approximately 2%.

**Figure 6-3. Chopping-Mode Characteristics**

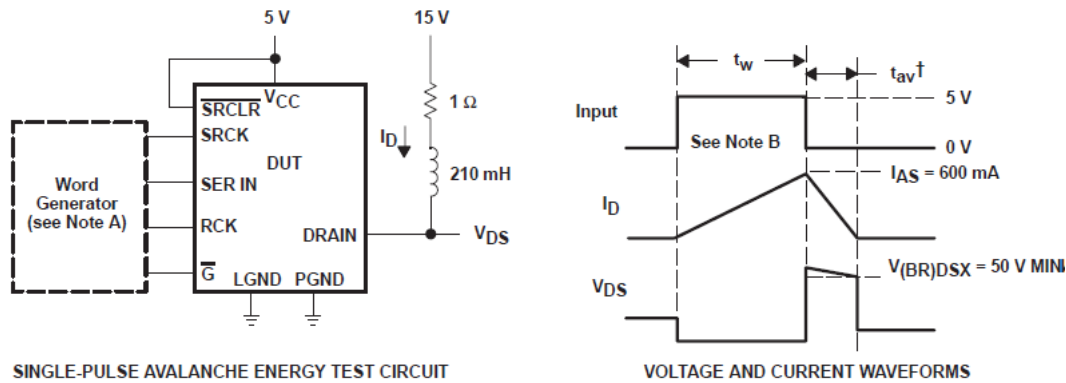


**Figure 6-4. Output Current Limit vs Case Temperature**



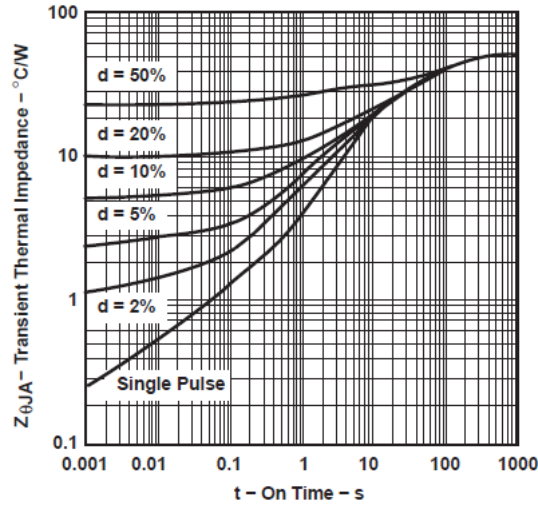
- The  $V_{GG}$  amplitude and  $R_G$  are adjusted for  $di/dt = 20A/\mu s$ . A  $V_{GG}$  double-pulse train is used to set  $I_F = 0.35A$ , where  $t_1 = 10\mu s$ ,  $t_2 = 7\mu s$ , and  $t_3 = 3\mu s$ .
- The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TPA test point.
- $I_{RM}$  = maximum recovery current.

**Figure 6-5. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode**



- Non JEDEC symbol for avalanche time.
- The word generator has the following characteristics:  $t_r \leq 10ns$ ,  $t_f \leq 10ns$ ,  $Z_O = 50\Omega$ .
- Input pulse duration,  $t_w$ , is increased until peak current  $I_{AS} = 600mA$ .  
Energy test level is defined as  $E_{AS} = (I_{AS} \times V_{(BR)DSX} \times t_{av})/2 = 75mJ$ .

**Figure 6-6. Single-Pulse Avalanche Energy Test Circuit and Waveforms**



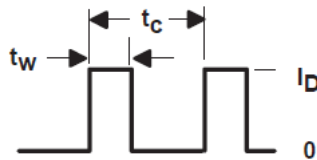
**Figure 6-7. NE Package Transient Thermal Impedance vs On Time**

The single-pulse curve represents measured data. The curves for various pulse durations are based on the following equation:

$$Z_{\theta JA} = \left| \frac{t_w}{t_c} \right| R_{\theta JA} + \left| 1 - \frac{t_w}{t_c} \right| Z_{\theta}(t_w + t_c) + Z_{\theta}(t_w) - Z_{\theta}(t_c) \quad (1)$$

where:

- $Z_{\theta}(t_w)$  = the single-pulse thermal impedance for  $t = t_w$  seconds
- $Z_{\theta}(t_c)$  = the single-pulse thermal impedance for  $t = t_c$  seconds
- $Z_{\theta}(t_w + t_c)$  = the single-pulse thermal impedance for  $t = t_w + t_c$  seconds
- $d = t_w/t_c$

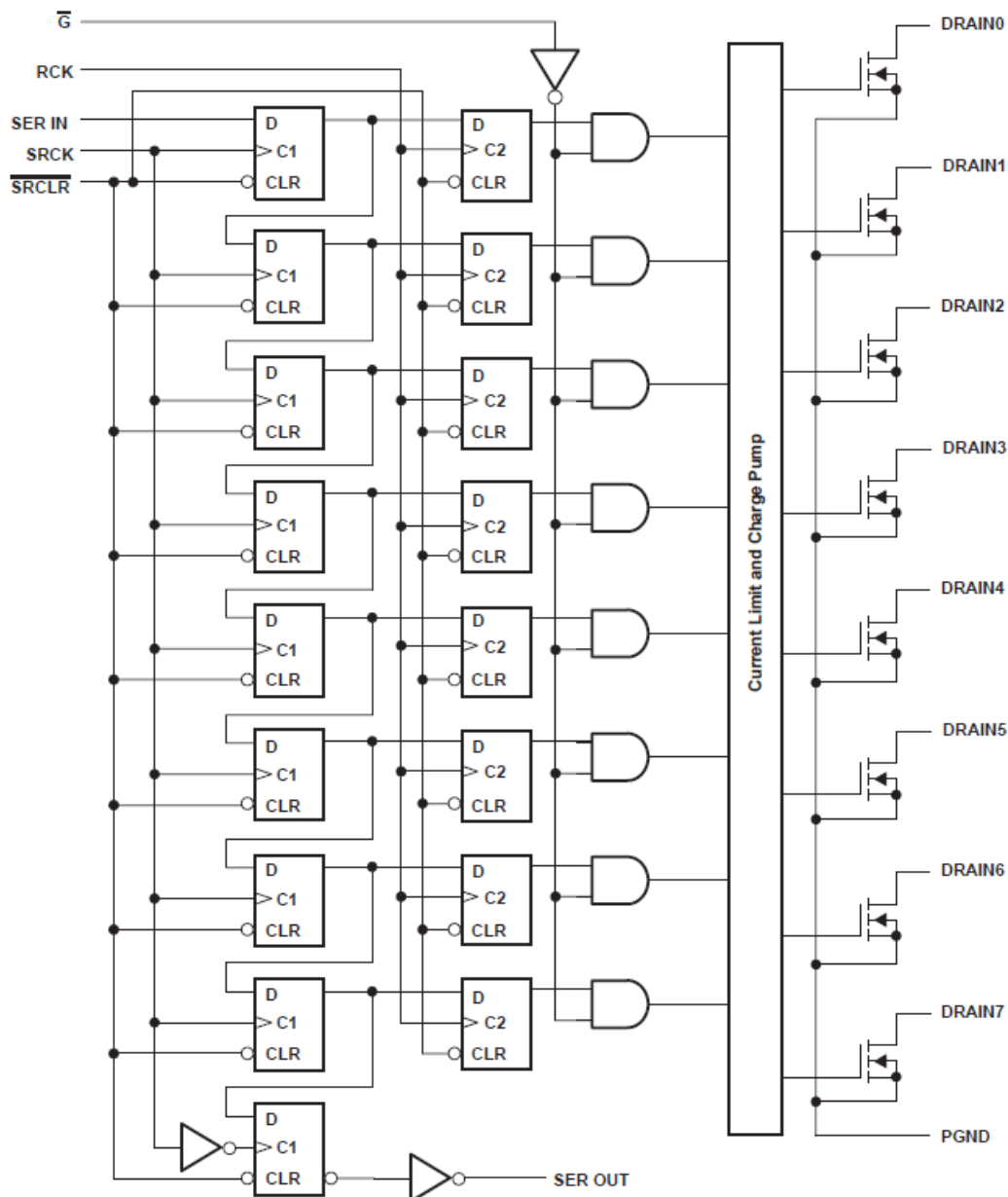


## 7 Detailed Description

### 7.1 Overview

The TPIC6A596 device is a monolithic, high-voltage, medium-current power 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection, so it can also drive relays, solenoids, and other medium-current or high-voltage loads.

### 7.2 Functional Block Diagram



Functional Block Diagram

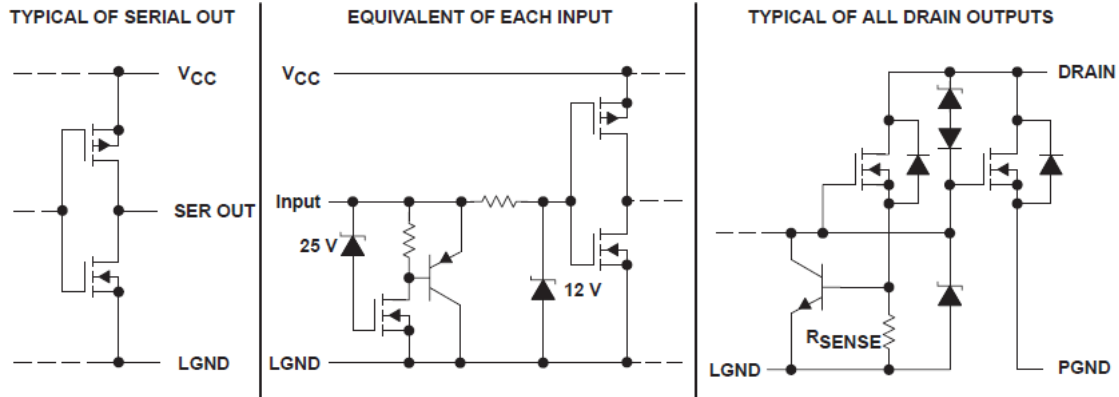


Figure 7-1. Functional Block Diagram (continued)

## 7.3 Feature Description

### 7.3.1 Serial-In Interface

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift register clock (SRCK) and the register clock (RCK), respectively. Write data and read data are valid only when RCK is low. The storage register transfers data to the output buffer when shift register clear (SRCLR) is high.

### 7.3.2 Clear Register

A logical low on ( $\overline{\text{SRCLR}}$ ) clears all registers in the device. TI suggests clearing the device during power up or initialization.

### 7.3.3 Output Control

Holding the output enable ( $\overline{\text{G}}$ ) high holds all data in the output buffers low, and all drain outputs are off. Holding ( $\overline{\text{G}}$ ) low makes data from the storage register transparent to the output buffers. When data in the output buffers is low, the DMOS transistor outputs are OFF. When data is high, the DMOS transistor outputs have sink-current capability. This pin can also be used for global PWM dimming.

### 7.3.4 Cascaded Application

The serial output (SER OUT) allows for cascading of the data from the shift register to additional devices. The serial output (SER OUT) is clocked out of the device on the falling edge of SRCK to provide additional hold time for cascaded applications. This will provide improved performance for applications where clock signals may be skewed, devices are not located near one another, or the system must tolerate electromagnetic interference. Connect the device (SER OUT) pin to the next device (SER IN) for daisy Chain.

### 7.3.5 Current Limit Function

Outputs are low-side, open-drain DMOS transistors with output ratings of 50V and a 350mA continuous sink current capability. Each open-drain DMOS transistor features an independent chopping current-limiting circuit to prevent damage in the case of a short circuit.

## 8 Device Functional Modes

### 8.1 Operating with $V_{CC} < 4.5V$

This device works normally during  $4.5V \leq V_{CC} \leq 5.5V$ , when operation voltage is lower than 4.5V, correct behavior of the device, including communication interface and current capability, is not assured.

### 8.2 Operating with $5.5V < V_{CC} \leq 7V$

The device works normally in this voltage range, but reliability issues can occur if the device works for a long time in this voltage range.

## 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (May 2015) to Revision B (March 2025) | Page |
|---|------|
| • Updated Applications section.....                           | 1    |

| Changes from Revision * (March 2000) to Revision A (May 2015)  | Page |
|--|------|
| • Changed $\overline{\text{SRCLR}}$ timing diagram and changed title on Draining timing diagram for <a href="#">Figure 6-1</a> ..... | 8    |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| TPIC6A596DW      | OBSOLETE      | SOIC         | DW                 | 24   |                | TBD             | Call TI                              | Call TI              | -40 to 125   | TPIC6A596               |         |
| TPIC6A596DWRG4   | ACTIVE        | SOIC         | DW                 | 24   | 2000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | TPIC6A596               | Samples |
| TPIC6A596NE      | ACTIVE        | PDIP         | NE                 | 20   | 20             | RoHS & Green    | NIPDAU                               | N / A for Pkg Type   | -40 to 125   | TPIC6A596NE             | Samples |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.



In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPIC6A596DWRG4 | SOIC         | DW              | 24   | 2000 | 330.0              | 24.4               | 10.75   | 15.7    | 2.7     | 12.0    | 24.0   | Q1            |
| TPIC6A596DWRG4 | SOIC         | DW              | 24   | 2000 | 330.0              | 24.4               | 10.75   | 15.7    | 2.7     | 12.0    | 24.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPIC6A596DWRG4 | SOIC         | DW              | 24   | 2000 | 350.0       | 350.0      | 43.0        |
| TPIC6A596DWRG4 | SOIC         | DW              | 24   | 2000 | 350.0       | 350.0      | 43.0        |

## TUBE

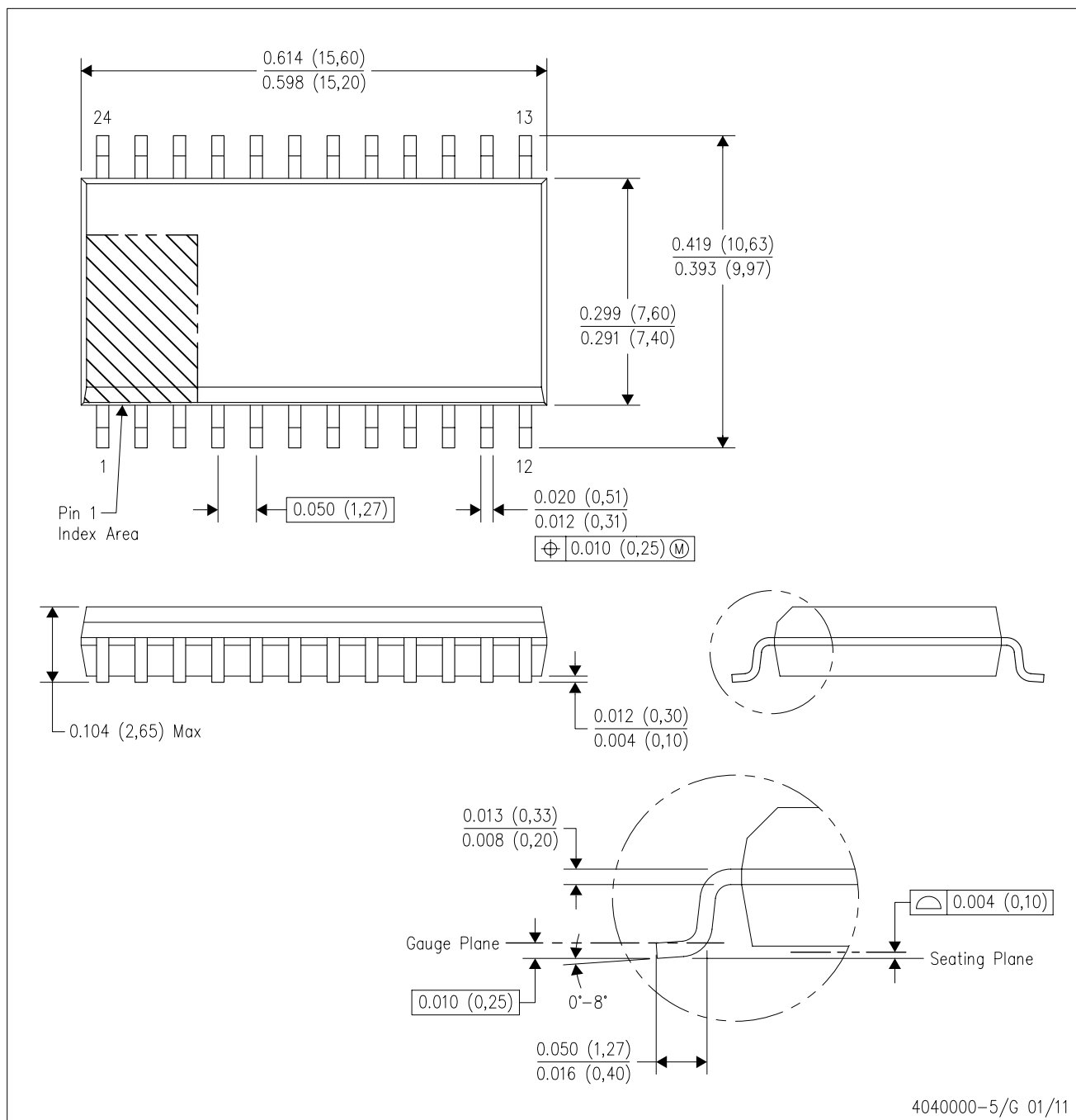


\*All dimensions are nominal

| Device      | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| TPIC6A596NE | NE           | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2025, Texas Instruments Incorporated