



TPS22924D 3.6-V, 2-A, 18.3-mΩ On-Resistance Load Switch

1 Features

- Integrated Single-Channel Load Switch
- Input Voltage: 0.75 V to 3.6 V
- On-Resistance
 - $r_{ON} = 18.3 \text{ m}\Omega$ at $V_{IN} = 3.6 \text{ V}$
 - $r_{ON} = 18.5 \text{ m}\Omega$ at $V_{IN} = 2.5 \text{ V}$
 - $r_{ON} = 19.6 \text{ m}\Omega$ at $V_{IN} = 1.8 \text{ V}$
 - $r_{ON} = 19.4 \text{ m}\Omega$ at $V_{IN} = 1.2 \text{ V}$
 - $r_{ON} = 20.3 \text{ m}\Omega$ at $V_{IN} = 1.0 \text{ V}$
 - $r_{ON} = 22.7 \text{ m}\Omega$ at $V_{IN} = 0.75 \text{ V}$
- Small CSP-6 package
0.9 mm x 1.4 mm, 0.5-mm Pitch
- 2-A Maximum Continuous Switch Current
- Low Shutdown Current
- Low Threshold Control Input
- Controlled Slew Rate to Avoid Inrush Currents
- Quick Output Discharge Transistor
- ESD Performance Tested Per JESD 22
 - 5000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)

2 Applications

- Battery Powered Equipment
- Portable Industrial Equipment
- Portable Medical Equipment
- Portable Media Players
- Point of Sales Terminal
- GPS Devices
- Digital Cameras
- Notebooks / Tablet PCs / eReaders
- Smartphones

3 Description

The TPS22924D is a small, low R_{ON} load switch with controlled turn on. The device contains a N-channel MOSFET that can operate over an input voltage range of 0.75 V to 3.6 V. An integrated charge pump biases the NMOS switch to achieve a minimum switch ON resistance. The switch is controlled by an on/off input (ON), which is capable of interfacing directly with low-voltage control signals.

A 1250 Ω on-chip load resistor is added for output quick discharge when the switch is turned off. The rise time of the device is internally controlled to avoid inrush current. The TPS22924D features a rise time of 6200 μs at 3.6 V.

The TPS22924D is available in an ultra-small, space-saving 6-pin CSP package and is characterized for operation over the free-air temperature range of -40°C to 85°C .

Device Information ⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22924D	DSBGA (6)	0.9 mm x 1.4 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Diagram

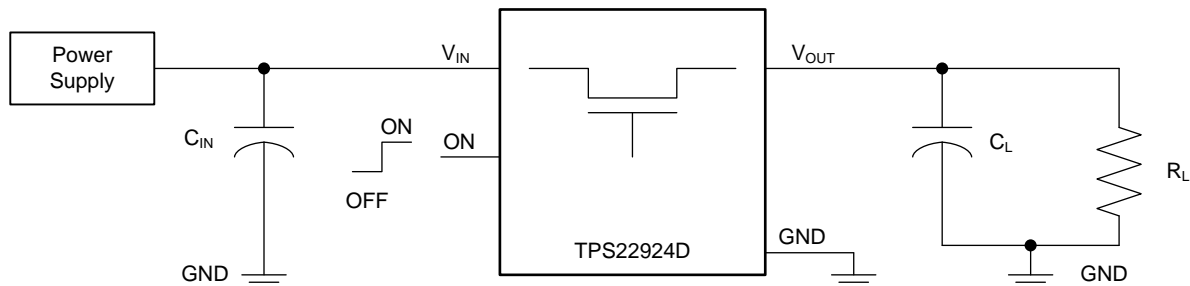


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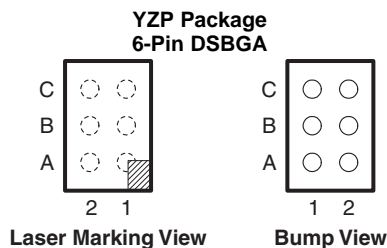
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (May 2013) to Revision A	Page
<ul style="list-style-type: none"> Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section 	1

5 Pin Configuration and Functions



Pin Assignments (YZP Package)

C	GND	ON
B	VOUT	VIN
A	VOUT	VIN
	1	2

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	C1	—	Ground
ON	C2	I	Switch control input, active high. Do not leave floating
VIN	A2, B2	I	Switch input. Place a decoupling capacitor from VIN to GND. See Application Information section for details about input capacitors.
VOUT	A1, B1	O	Switch output

6 Specifications

6.1 Absolute Maximum Ratings ⁽¹⁾

		MIN	MAX	UNIT
V _{IN}	Input voltage	−0.3	4	V
V _{OUT}	Output voltage		V _{IN} + 0.3	V
V _{ON}	ON pin voltage	−0.3	4	V
I _{MAX}	Maximum continuous switch current, T _A = −40°C to 85°C		2	A
I _{PLS}	Maximum pulsed switch current, 100-μs pulse, 2% duty cycle, T _A = −40°C to 85°C		4	A
T _A	Operating free-air temperature	−40	85	°C
T _{stg}	Storage temperature	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	
		±5000	
		±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{IN}	Input voltage	0.75	3.6	V
V_{OUT}	Output voltage		V_{IN}	V
V_{IH}	High-level input voltage, ON	$V_{IN} = 2.5\text{ V to }3.6\text{ V}$	1.2	3.6
		$V_{IN} = 0.75\text{ V to }2.5\text{ V}$	0.9	3.6
V_{IL}	Low-level input voltage, ON	$V_{IN} = 2.5\text{ V to }3.6\text{ V}$		0.6
		$V_{IN} = 0.75\text{ V to }2.49\text{ V}$		0.4
C_{IN}	Input capacitance	1 ⁽¹⁾		μF

(1) See the *Input Capacitor* section in Application Information.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS22924D	UNIT
		YZP (DSBGA)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	123	$^{\circ}\text{C/W}$
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.6	$^{\circ}\text{C/W}$
$R_{\theta JB}$	Junction-to-board thermal resistance	22.8	$^{\circ}\text{C/W}$
Ψ_{JT}	Junction-to-top characterization parameter	5.7	$^{\circ}\text{C/W}$
Ψ_{JB}	Junction-to-board characterization parameter	22.6	$^{\circ}\text{C/W}$
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	$^{\circ}\text{C/W}$

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

 $V_{IN} = 0.75\text{ V to }3.6\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	MIN	TYP ⁽¹⁾	MAX	UNIT
$I_{Q, VIN}$ Quiescent current	$V_{OUT} = \text{open}, V_{IN} = V_{ON}$	$V_{IN} = 3.6\text{ V}$		75	160	μA
		$V_{IN} = 2.5\text{ V}$		42	100	
		$V_{IN} = 1.8\text{ V}$		50	350	
		$V_{IN} = 1.2\text{ V}$		95	200	
		$V_{IN} = 1.0\text{ V}$		65	120	
		$V_{IN} = 0.75\text{ V}$		35	80	
$I_{SD, VIN}$ Shutdown current	$V_{ON} = \text{GND}, V_{OUT} = 0\text{ V}$	Full			4.0	μA
R_{ON} ON-state resistance	$I_{OUT} = -200\text{ mA}$	$V_{IN} = 3.6\text{ V}$	25 $^{\circ}\text{C}$	18.3	22.8	$\text{m}\Omega$
			Full		26.8	
		$V_{IN} = 2.5\text{ V}$	25 $^{\circ}\text{C}$	18.5	23.0	
			Full		27.2	
		$V_{IN} = 1.8\text{ V}$	25 $^{\circ}\text{C}$	19.6	24.1	
			Full		28.1	
		$V_{IN} = 1.2\text{ V}$	25 $^{\circ}\text{C}$	19.4	23.9	
			Full		28.0	
		$V_{IN} = 1.0\text{ V}$	25 $^{\circ}\text{C}$	20.3	24.8	
			Full		29.0	
		$V_{IN} = 0.75\text{ V}$	25 $^{\circ}\text{C}$	22.7	27.2	
			Full		34.8	
R_{PD} Output pulldown resistance ⁽²⁾	$V_{IN} = 3.3\text{ V}, V_{ON} = 0, I_{OUT} = 1\text{ mA}$	25 $^{\circ}\text{C}$	450		1400	Ω

(1) Typical values are at $V_{IN} = 3.3\text{ V}$ and $T_A = 25^{\circ}\text{C}$.

(2) See [Output Pulldown](#).

Electrical Characteristics (continued)

 $V_{IN} = 0.75\text{ V to }3.6\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	MIN	TYP ⁽¹⁾	MAX	UNIT
I_{ON} ON-pin input leakage current	$V_{ON} = 0.9\text{ V to }3.6\text{ V or GND}$	Full			0.1	μA

6.6 Switching Characteristics: $V_{IN} = 3.6\text{ V}$

 $V_{IN} = 3.6\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON} Turn-ON time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $V_{IN} = 3.6\text{ V}$		7400		μs
t_{OFF} Turn-OFF time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $V_{IN} = 3.6\text{ V}$		2.5		μs
t_r V_{OUT} rise time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $V_{IN} = 3.6\text{ V}$		6200		μs
t_f V_{OUT} fall time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $V_{IN} = 3.6\text{ V}$		2		μs

6.7 Switching Characteristics: $V_{IN} = 0.9\text{ V}$

 $V_{IN} = 0.9\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON} Turn-ON time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $V_{IN} = 0.9\text{ V}$		6300		μs
t_{OFF} Turn-OFF time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $V_{IN} = 0.9\text{ V}$		12		μs
t_r V_{OUT} rise time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $V_{IN} = 0.9\text{ V}$		3200		μs
t_f V_{OUT} fall time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $V_{IN} = 0.9\text{ V}$		3		μs

6.8 Dissipation Ratings

BOARD	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A < 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$	$T_A = 85^\circ\text{C}$
High-K ⁽¹⁾	- 8.1063 mW/ $^\circ\text{C}$	810.63 mW	445.84 mW	324.25 mW

(1) The JEDEC high-K (2s2p) board used to derive this data was a 3- × 3-inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

6.9 Typical Characteristics

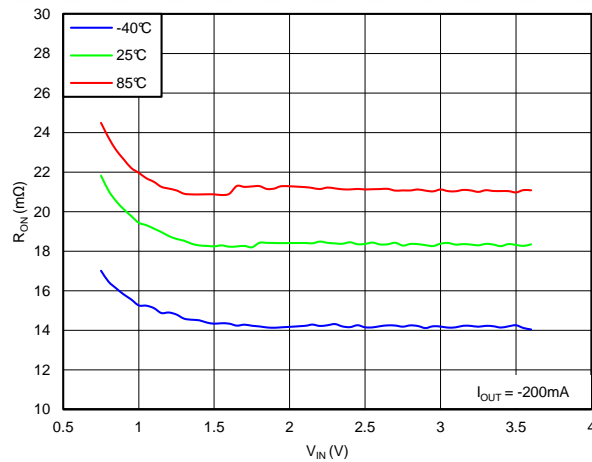


Figure 1. On-State Resistance vs Input Voltage

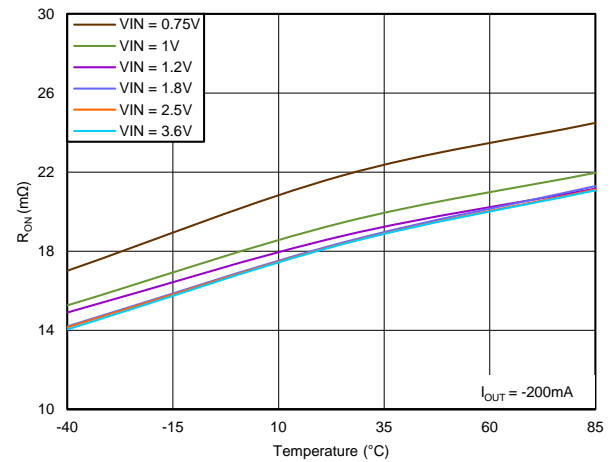


Figure 2. On-State Resistance vs Temperature

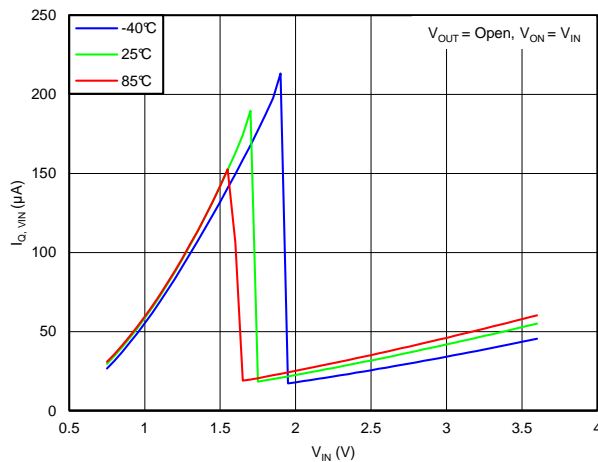


Figure 3. Quiescent Current vs Input Voltage

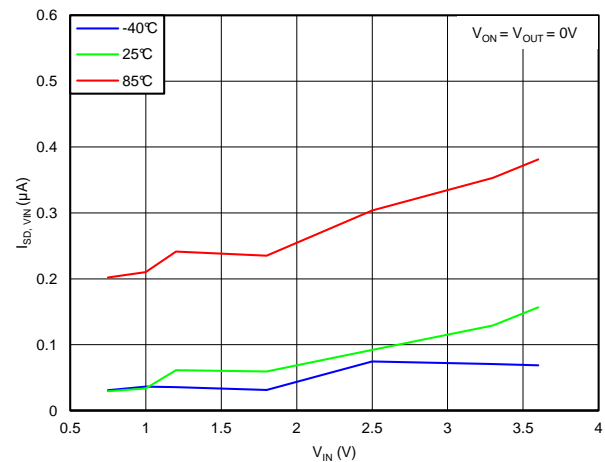


Figure 4. Shutdown Current vs Input Voltage

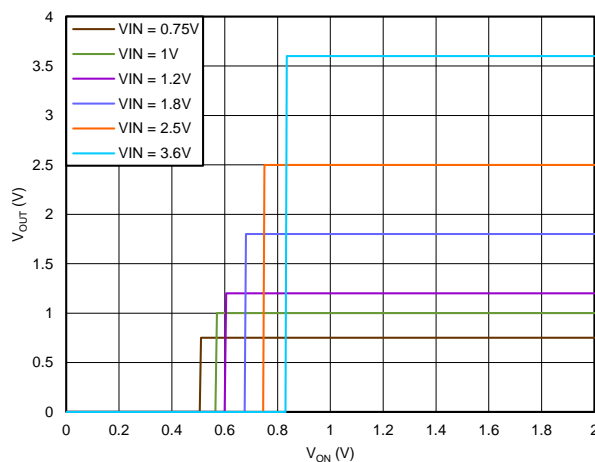


Figure 5. On Input Threshold

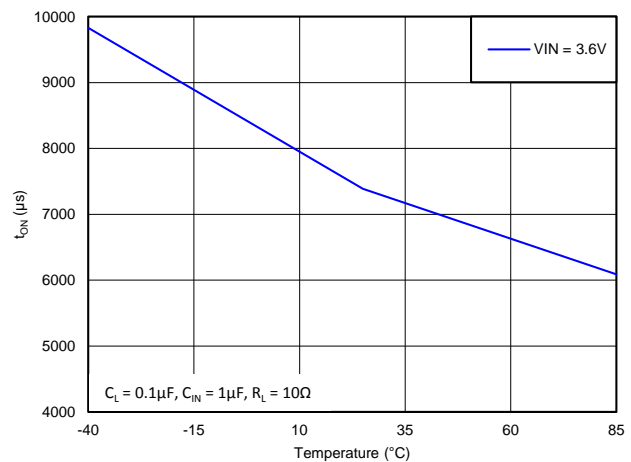


Figure 6. Turnon Time vs Temperature
($V_{IN} = 3.6\text{ V}$, $C_L = 0.1\text{ }\mu\text{F}$, $R_L = 10\text{ }\Omega$)

Typical Characteristics (continued)

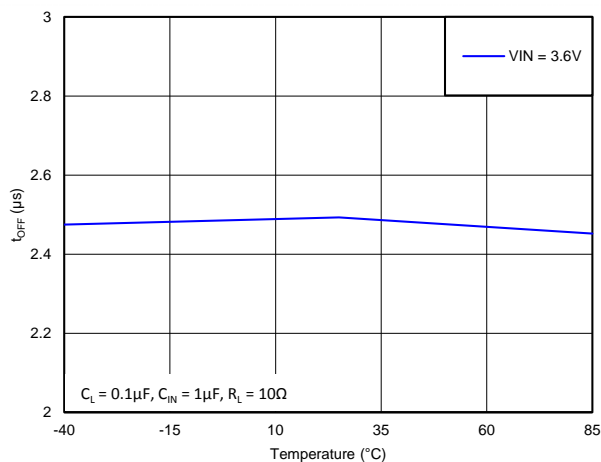


Figure 7. Turnoff Time vs Temperature
($V_{IN} = 3.6\text{ V}$, $C_L = 0.1\text{ }\mu\text{F}$, $R_L = 10\text{ }\Omega$)

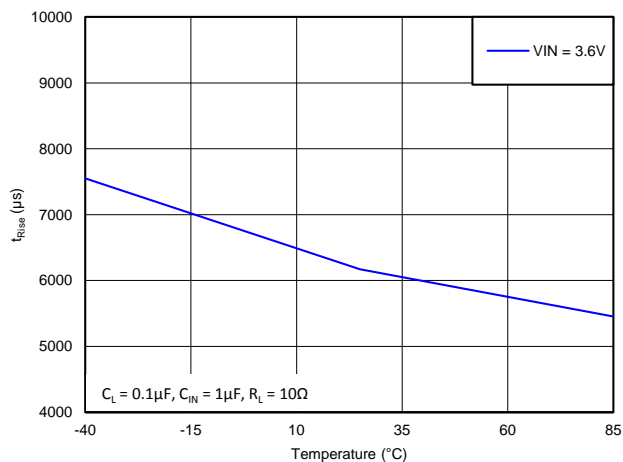


Figure 8. Rise Time vs Temperature
($V_{IN} = 3.6\text{ V}$, $C_L = 0.1\text{ }\mu\text{F}$, $R_L = 10\text{ }\Omega$)

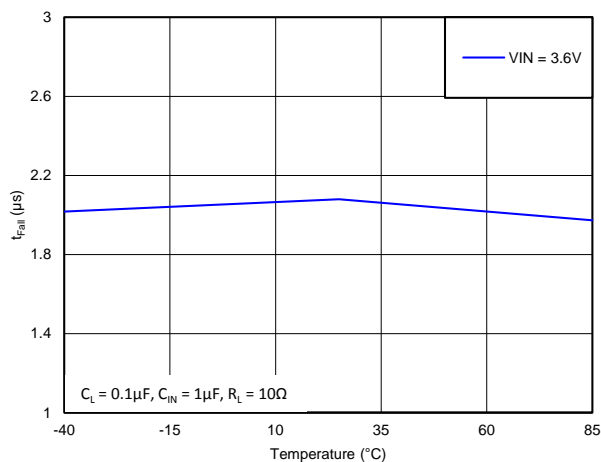


Figure 9. Fall Time vs Temperature
($V_{IN} = 3.6\text{ V}$, $C_L = 0.1\text{ }\mu\text{F}$, $R_L = 10\text{ }\Omega$)

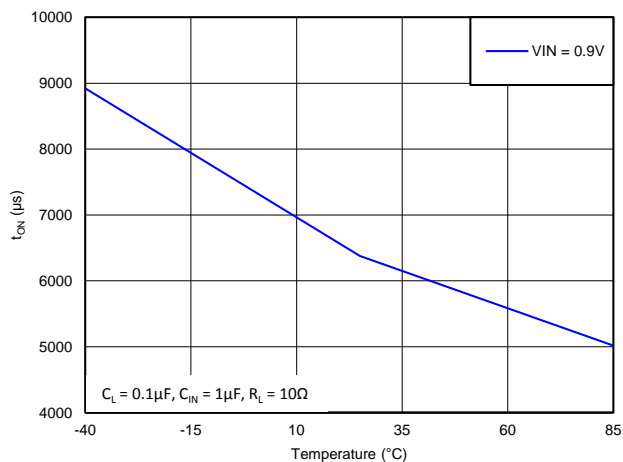


Figure 10. Turnon Time vs Temperature
($V_{IN} = 0.9\text{ V}$, $C_L = 0.1\text{ }\mu\text{F}$, $R_L = 10\text{ }\Omega$)

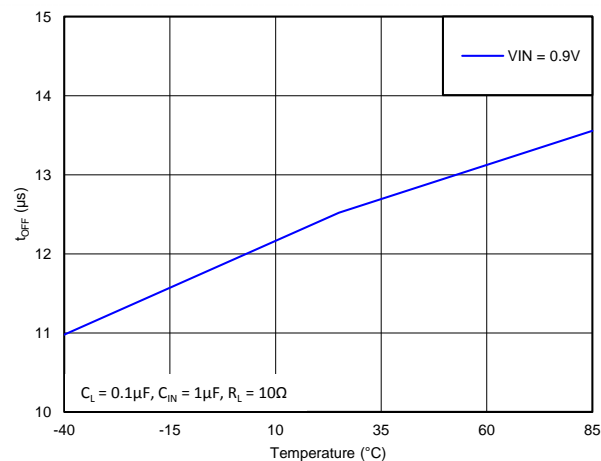


Figure 11. Turnoff Time vs Temperature
($V_{IN} = 0.9\text{ V}$, $C_L = 0.1\text{ }\mu\text{F}$, $R_L = 10\text{ }\Omega$)

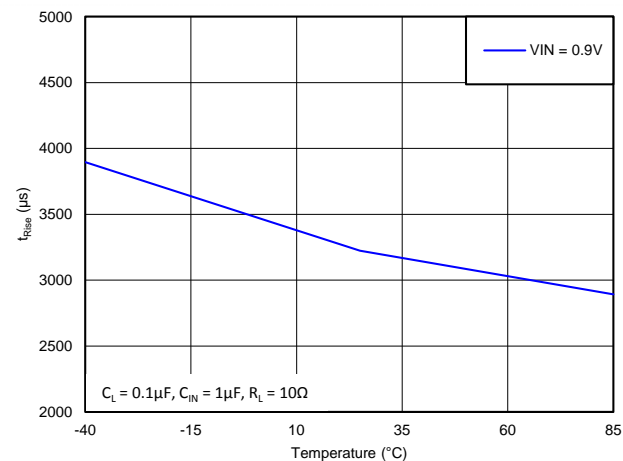


Figure 12. Rise Time vs Temperature
($V_{IN} = 0.9\text{ V}$, $C_L = 0.1\text{ }\mu\text{F}$, $R_L = 10\text{ }\Omega$)

Typical Characteristics (continued)

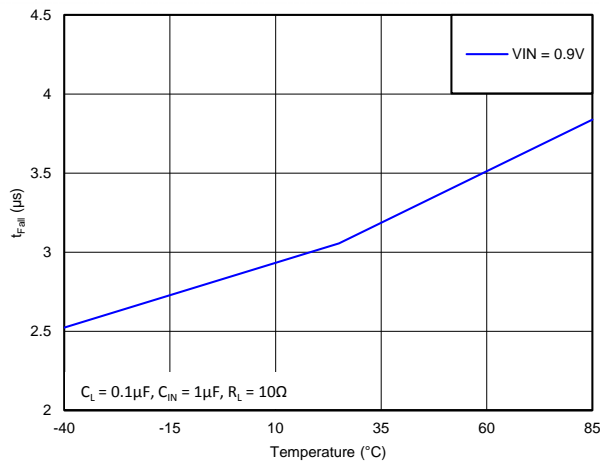


Figure 13. Fall Time vs Temperature
($V_{IN} = 0.9\text{ V}$, $C_L = 0.1\text{ }\mu\text{F}$, $R_L = 10\text{ }\Omega$)

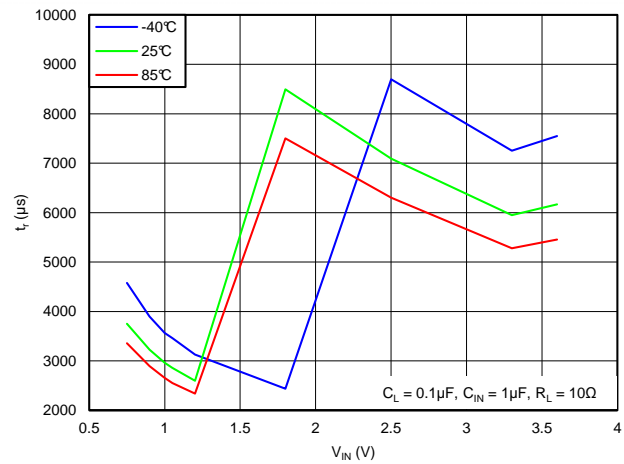


Figure 14. Rise Time vs Input Voltage
($C_L = 0.1\text{ }\mu\text{F}$, $R_L = 10\text{ }\Omega$, $V_{ON} = 1.8\text{ V}$)

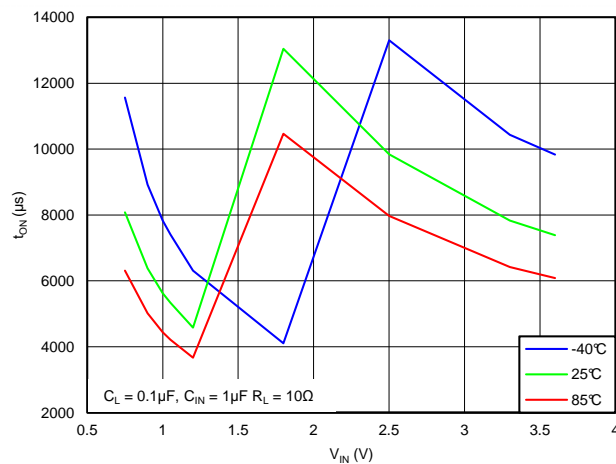


Figure 15. Turnon Time vs Input Voltage
($C_L = 0.1\text{ }\mu\text{F}$, $R_L = 10\text{ }\Omega$, $V_{ON} = 1.8\text{ V}$)

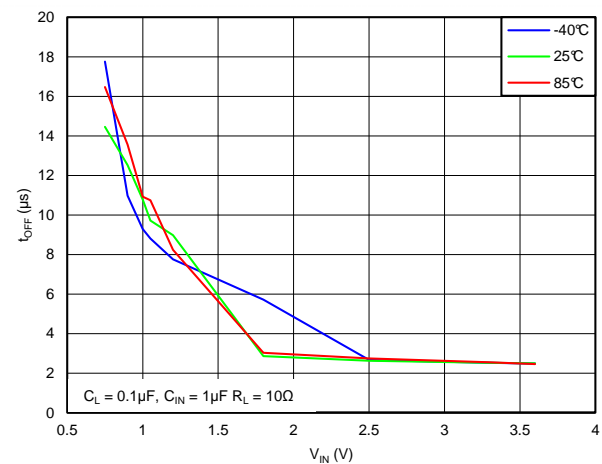


Figure 16. Turnoff Time vs Input Voltage
($C_L = 0.1\text{ }\mu\text{F}$, $R_L = 10\text{ }\Omega$, $V_{ON} = 1.8\text{ V}$)

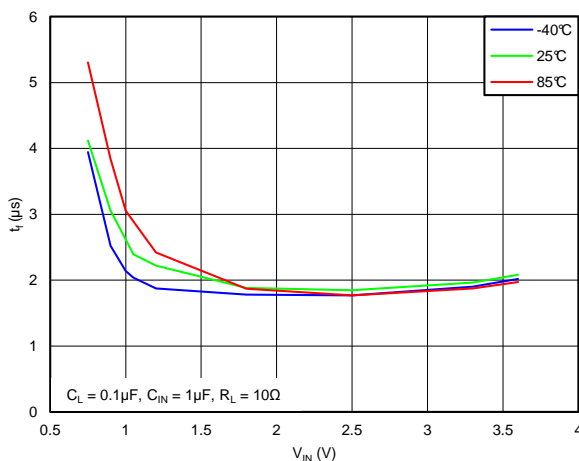


Figure 17. Fall Time vs Input Voltage
($C_L = 0.1\text{ }\mu\text{F}$, $R_L = 10\text{ }\Omega$, $V_{ON} = 1.8\text{ V}$)

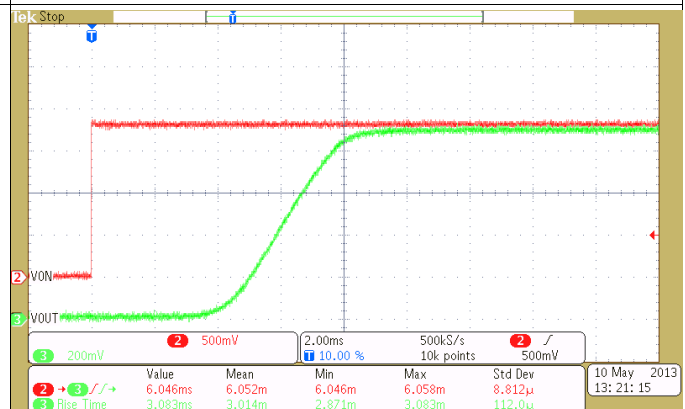


Figure 18. Turnon Response
($C_{IN} = 1\text{ }\mu\text{F}$, $C_L = 0.1\text{ }\mu\text{F}$, $R_L = 10\text{ }\Omega$, $V_{IN} = 0.9\text{ V}$, $T_A = 25^\circ\text{C}$)

Typical Characteristics (continued)

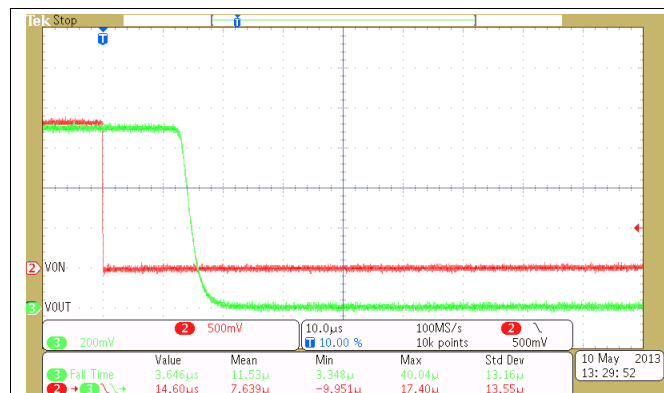


Figure 19. Turnoff Response
($C_{IN} = 1 \mu F$, $C_L = 0.1 \mu F$, $R_L = 10 \Omega$, $V_{IN} = 0.9 V$, $T_A = 25^\circ C$)

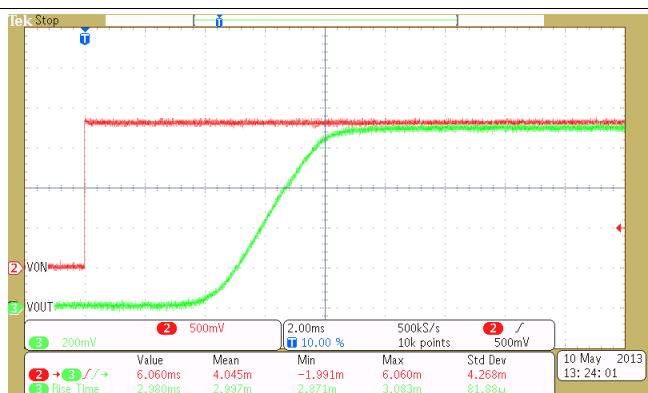


Figure 20. Turnon Response
($C_{IN} = 10 \mu F$, $C_L = 1 \mu F$, $R_L = 10 \Omega$, $V_{IN} = 0.9 V$, $T_A = 25^\circ C$)

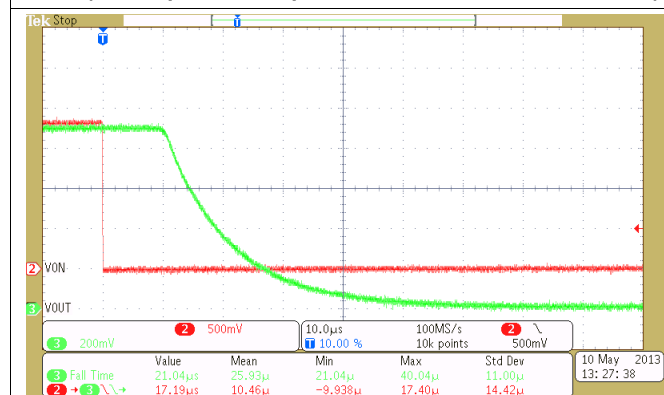


Figure 21. Turnoff Response
($C_{IN} = 10 \mu F$, $C_L = 1 \mu F$, $R_L = 10 \Omega$, $V_{IN} = 0.9 V$, $T_A = 25^\circ C$)

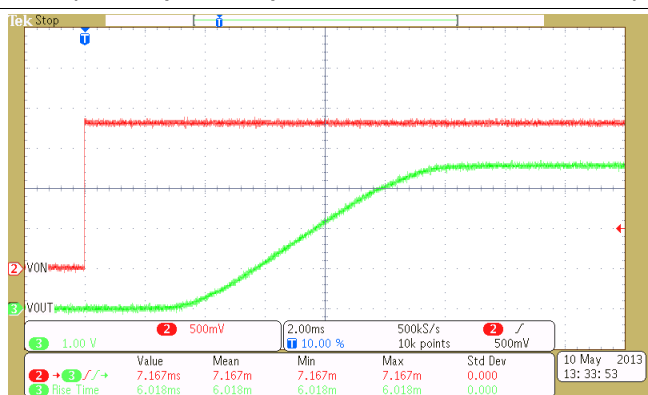


Figure 22. Turnon Response
($C_{IN} = 1 \mu F$, $C_L = 0.1 \mu F$, $R_L = 10 \Omega$, $V_{IN} = 3.6 V$, $T_A = 25^\circ C$)

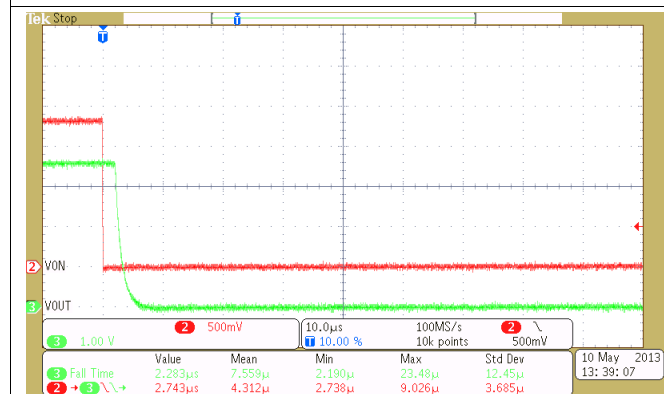


Figure 23. Turnoff Response
($C_{IN} = 1 \mu F$, $C_L = 0.1 \mu F$, $R_L = 10 \Omega$, $V_{IN} = 3.6 V$, $T_A = 25^\circ C$)

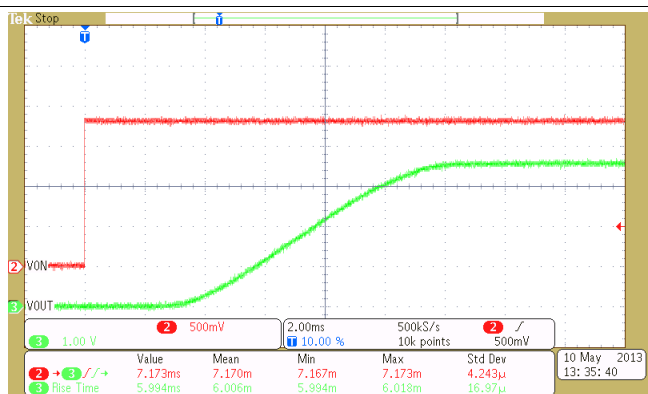


Figure 24. Turnon Response
($C_{IN} = 10 \mu F$, $C_L = 1 \mu F$, $R_L = 10 \Omega$, $V_{IN} = 3.6 V$, $T_A = 25^\circ C$)

Typical Characteristics (continued)

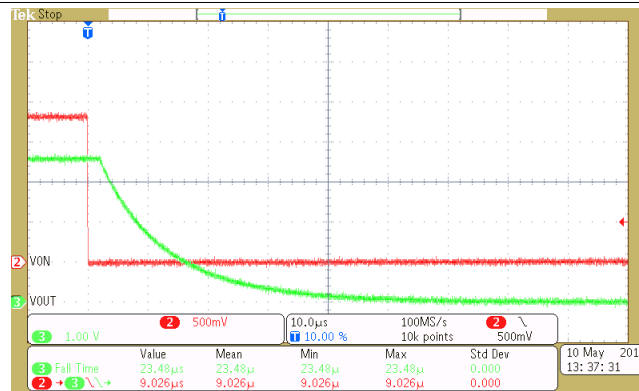
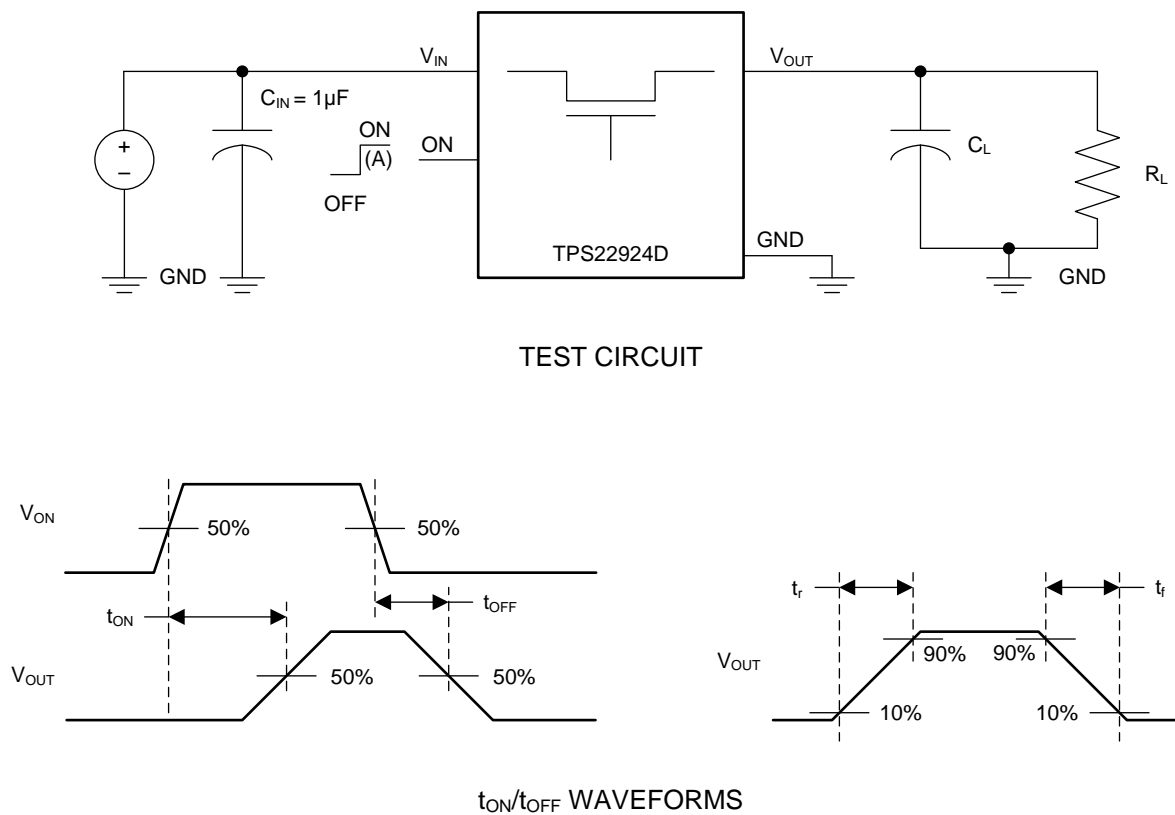


Figure 25. Turnoff Response
($C_{IN} = 10\ \mu\text{F}$, $C_L = 1\ \mu\text{F}$, $R_L = 10\ \Omega$, $V_{IN} = 3.6\ \text{V}$, $T_A = 25^\circ\text{C}$)

7 Parametric Measurement Information



A. Rise and fall times of the control signal is 100ns

Figure 26. Test Circuit and t_{ON}/t_{OFF} Waveforms

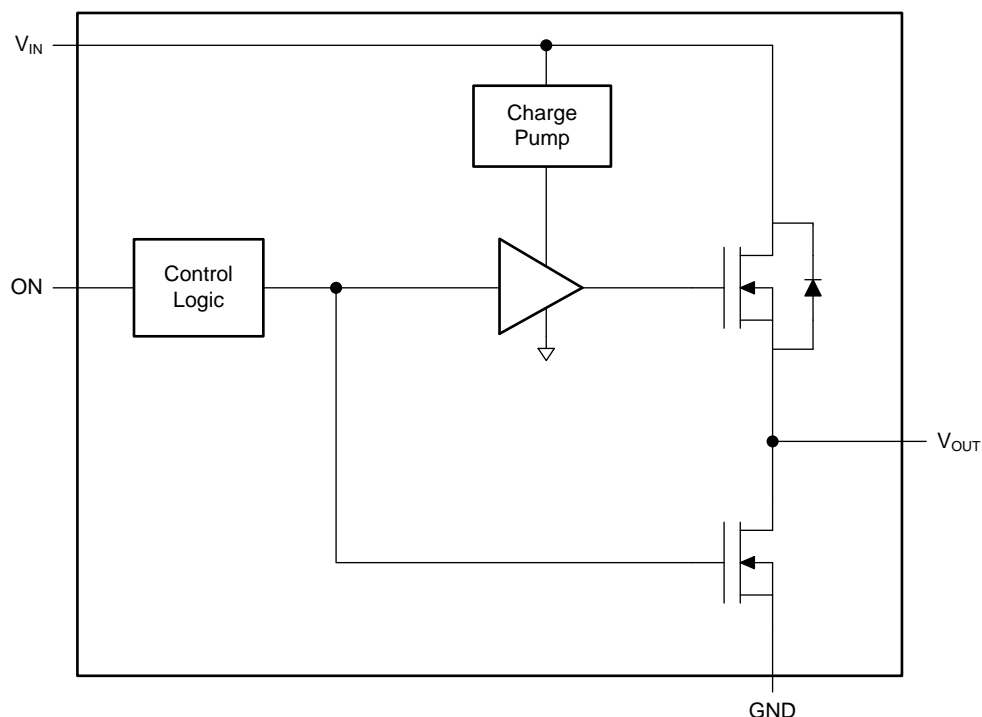
8 Detailed Description

8.1 Overview

The TPS22924D is a single channel, 2-A load switch in a small, space-saving CSP-6 package. This device implements a low resistance N-channel MOSFET with a controlled rise time for applications that need to limit the inrush current.

This device is also designed to have very low leakage current during off state. This prevents downstream circuits from pulling high standby current from the supply. Integrated control logic, driver, power supply, and output discharge FET eliminates the need for additional external components, which reduces solution size and bill of materials (BOM) count.

8.2 Functional Block Diagram



8.3 Feature Description

Table 1 lists the features of the TPS22924D device.

Table 1. Feature List

DEVICE	r_{ON} (TYP) AT 3.6 V	SLEW RATE (TYP) AT 3.6 V	QUICK OUTPUT DISCHARGE ⁽¹⁾	MAXIMUM OUTPUT CURRENT	ENABLE
TPS22924D	18.3 mΩ	6200 μs	Yes	2 A	Active high

(1) This feature discharges the output of the switch to ground through a 1250-Ω resistor, preventing the output from floating. See the *Output Pulldown* section in Application Information.

8.3.1 ON/OFF Control

The ON pin controls the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V or 3.3-V GPIOs.

8.3.2 Output Pulldown

The output pulldown is active when the user is turning off the main pass FET. The pulldown discharges the output rail to approximately 10% of the rail, then the output pulldown is automatically disconnected to optimize the shutdown current.

8.4 Device Functional Modes

[Table 2](#) lists the functional modes of the TPS22924D device.

Table 2. Function Table

ON (Control Signal)	VIN to VOUT	VOUT to GND ⁽¹⁾
L	OFF	ON
H	ON	OFF

(1) See [Output Pulldown](#).

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 VIN to VOUT Voltage Drop

The VIN to VOUT voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the VIN condition of the device. Refer to the R_{ON} specification of the device in the Electrical Characteristics table of this datasheet. Once the R_{ON} of the device is determined based upon the VIN conditions, use [Equation 1](#) to calculate the VIN to VOUT voltage drop:

$$\Delta V = I_{LOAD} \times R_{ON}$$

where

- ΔV = Voltage drop from VIN to VOUT
- I_{LOAD} = Load current
- R_{ON} = On-resistance of the device for a specific VIN
- An appropriate I_{LOAD} must be chosen such that the I_{MAX} specification of the device is not violated. (1)

9.1.2 Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between VIN and GND. A 1- μ F ceramic capacitor, C_{IN} , placed close to the pins is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop.

9.1.3 Output Capacitor

Due to the integrated body diode in the NMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN} . A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup.

9.2 Typical Application

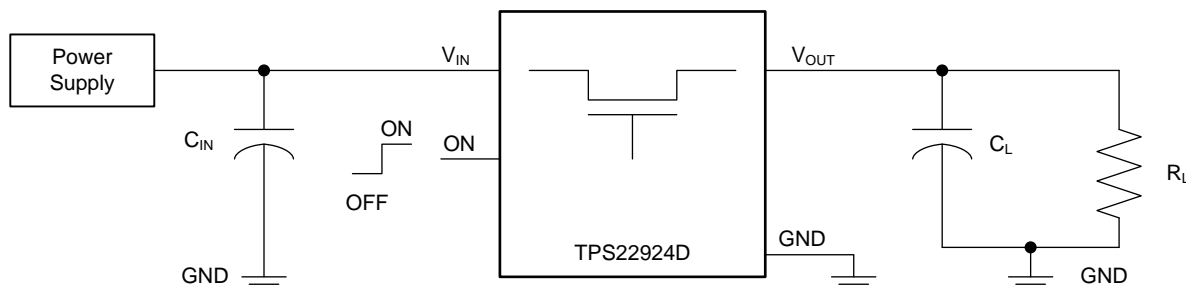


Figure 27. TPS22924D Typical Application

Typical Application (continued)

9.2.1 Design Requirements

Table 3 shows the design requirements for this application.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V _{IN}	3.6 V
C _L	100 µF
Maximum Acceptable Inrush Current	100 mA

9.2.2 Detailed Design Procedure

9.2.2.1 Managing Inrush Current

When the switch is enabled, the output capacitors must be charged up from 0 V to V_{IN}. This charge arrives in the form of inrush current. Inrush current can be calculated using the following equation:

$$\text{Inrush Current} = C \times \frac{dv}{dt}$$

where

- C = Output capacitance
- dv = Output voltage
- dt = Rise time

(2)

The TPS22924D offers a very slow controlled rise time for minimizing inrush current. This device can be selected based upon the maximum acceptable slew rate which can be calculated using the design requirements and the inrush current equation. An output capacitance of 100 µF will be used since the amount of inrush increases with output capacitance:

$$100\text{mA} = 100\mu\text{F} \times (3.6\text{V} / dt)$$

(3)

$$dt = 3600\mu\text{s}$$

(4)

To ensure an inrush current of less than 100 mA, a device with a rise time greater than 3600 µs must be used.

The TPS22924D has a typical rise time of 6200 µs at 3.6 V. This meets the above design requirements.

9.2.3 Application Curve

Figure 28 shows the TPS22924D turning on into a 100 µF load.

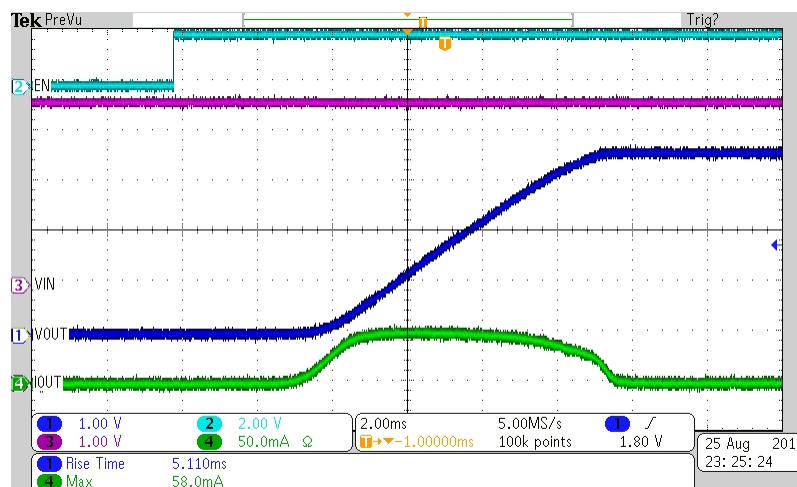


Figure 28. TPS22924D Inrush Current With a 100µF Load

10 Power Supply Recommendations

The device is designed to operate with a V_{IN} range of 0.75 V to 3.6 V. This supply must be well regulated and placed as close to the device terminal as possible with the recommended 1 μ F bypass capacitor. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 10 μ F may be sufficient.

11 Layout

11.1 Layout Guidelines

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation. Using wide traces for V_{IN} , V_{OUT} , and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

11.2 Layout Example

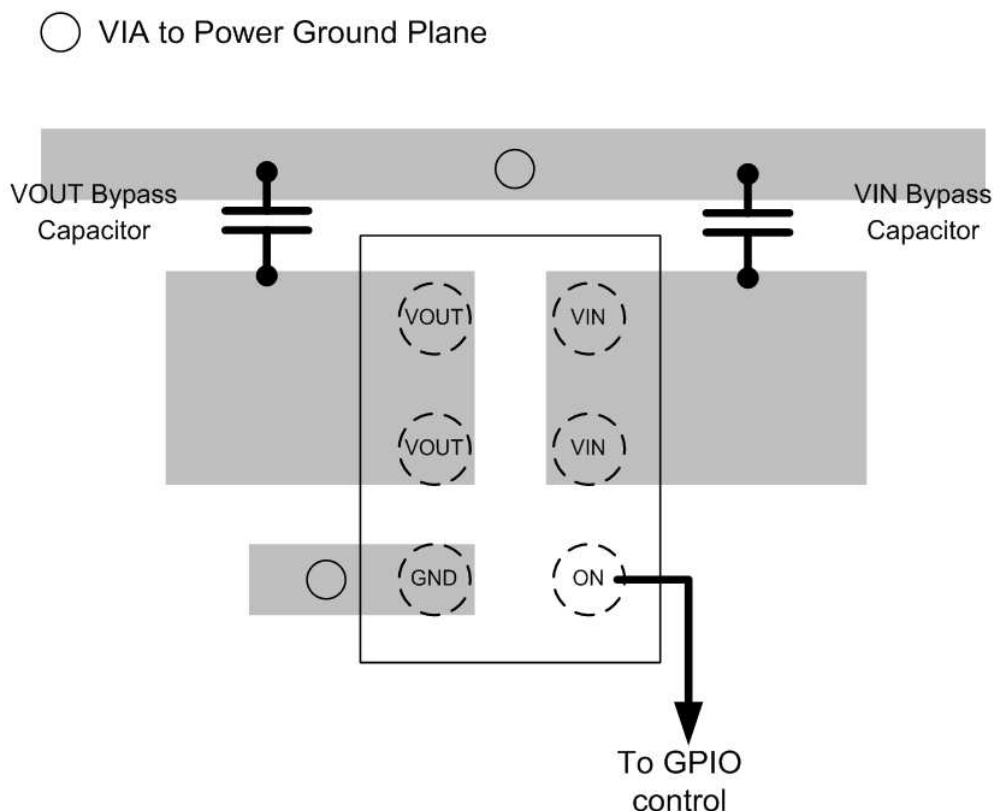


Figure 29. TPS22924D Layout Example

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22924DYZPR	ACTIVE	DSBGA	YZP	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	DL	Samples
TPS22924DYZPT	ACTIVE	DSBGA	YZP	6	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	DL	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22924DYZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1
TPS22924DYZPT	DSBGA	YZP	6	250	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

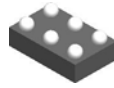
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22924DYZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0
TPS22924DYZPT	DSBGA	YZP	6	250	220.0	220.0	35.0

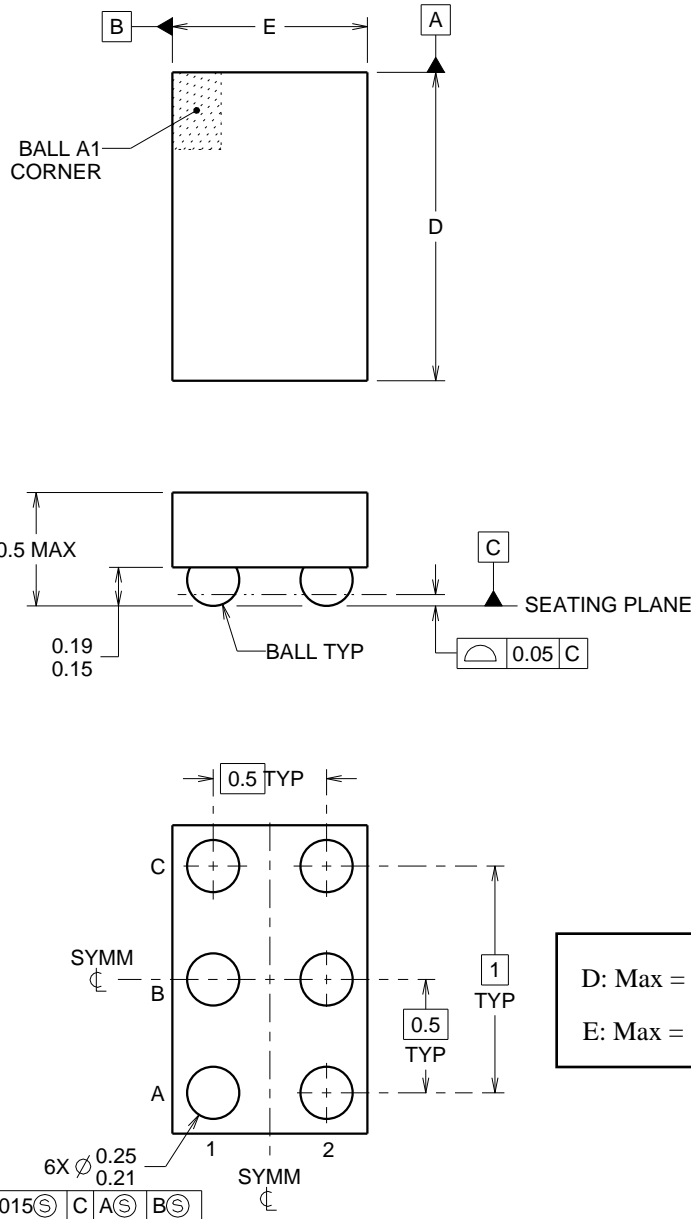
YZP0006



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



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NOTES:

NanoFree Is a trademark of Texas Instruments.

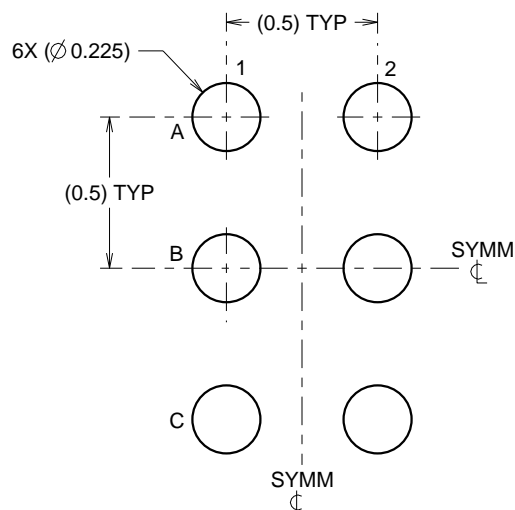
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

EXAMPLE BOARD LAYOUT

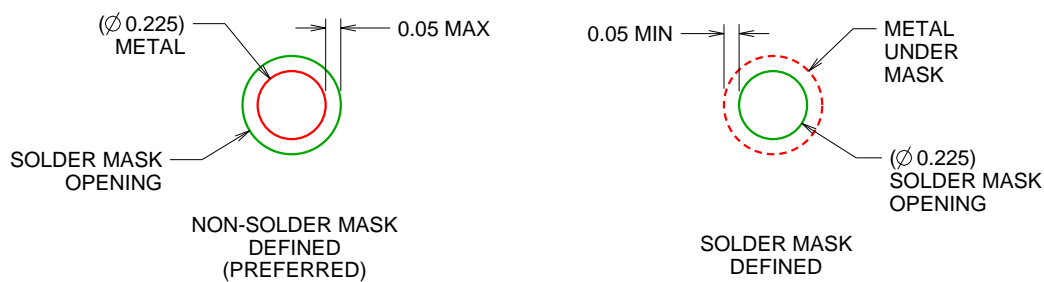
YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

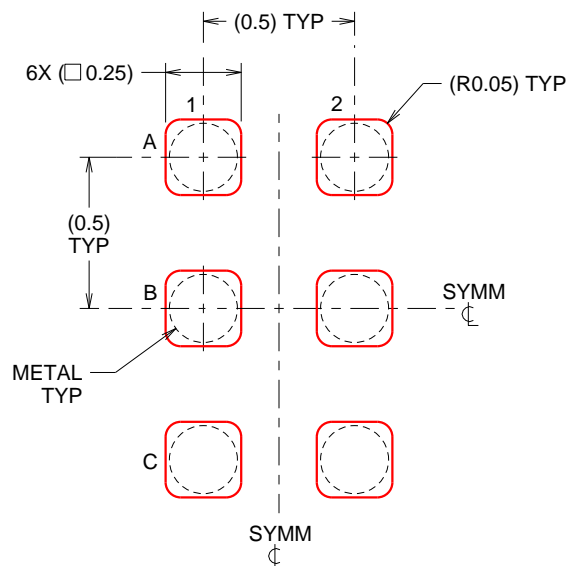
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

EXAMPLE STENCIL DESIGN

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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