TPS22948 5.5-V, 240-mA Current Limited Load Switch with Reverse Current Blocking

1 Features

- Input operating voltage range (V_{IN}): 2.5 V to 5.5 V
- Output current limit (I_{LIMIT}): 240 mA (typical)
- Thermal shutdown (TSD)
- ON-Resistance (R_{ON}): 300 mΩ (typical)
- Slow Turn ON timing limits inrush current (typical):
  - Turn ON time (t_{ON}): 820 us at 6.6 mV/µs
- Always-ON Reverse Current Blocking (RCB):
  - ON State activation current (I_{RCB}): –200 mA (typical)
- Fault indication (FLT)
- Smart ON pin pull down ($R_{PD,ON}$):
  - ON V_{IH} (I_{ON}): 25 nA (maximum)
  - ON V_{IL} ($R_{PD,ON}$): 500 kΩ (typical)
- Low power consumption:
  - ON State (I_Q): 50 uA (typical)
  - OFF State (I_{SD}): 0.3 uA (typical)

2 Applications

- Personal electronics
- Set top box
- HDMI output ports
- Notebook, desktop PC
- Docking stations

3 Description

The TPS22948 device is a small, single channel load switch with robust protection against fault cases with output current limiting, reverse current blocking, and thermal shutdown.

The switch ON state is controlled by a digital input that is capable of interfacing directly with low-voltage control signals. When power is first applied, a smart pull down is used to keep the ON pin from floating until system sequencing is complete. Once the pin is deliberately driven high (>VIH), the smart pull down will be disconnected to prevent unnecessary power loss.

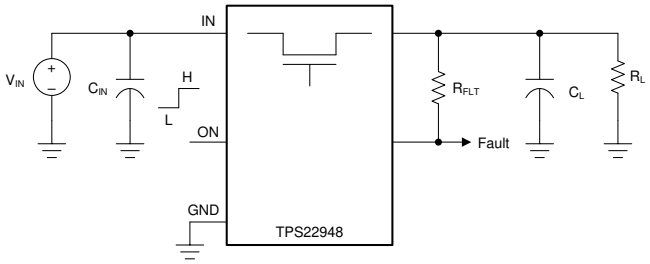
TPS22948 is available in a standard SC-70 package characterized for operation over a temperature range of –40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22948	SC-70 (6)	2.1 mm x 2.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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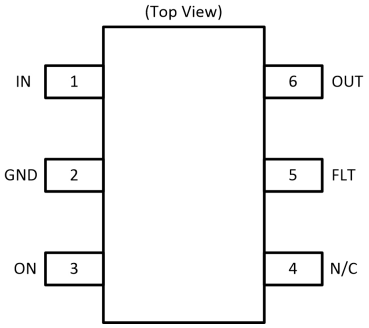
4 Revision History

Changes from Original (March 2019) to Revision A	Page
• Changed from Advance Information to Production Data	1
• FIrst Public Release	1

5 Pin Configuration and Functions

DCK Package
6-Pin SC-70
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IN	I	Switch input
2	GND	–	Device ground
3	ON	I	Active high switch control input. Do not leave floating.
4	N/C	–	No connect pin, leave floating or GND
5	FLT	O	Open-drain output, pulled low during thermal shutdown or reverse current-conditions.
6	OUT	O	Switch output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Maximum Input Voltage Range	–0.3	6	V
V_{OUT}	Maximum Output Voltage Range	–0.3	6	V
V_{ON}	Maximum ON Pin Voltage Range	–0.3	6	V
V_{FLT}	Maximum FLT Pin Voltage	–0.3	6	V
I_{MAX}	Maximum Output Current	Internally Limited		A
T_J	Junction temperature	Internally Limited		°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Maximum Lead Temperature (10 s soldering time)		300	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, allpins(1)	±2000	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less is possible with the necessary precautions. Pins listed may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage Range	2.5		5.5	V
V_{OUT}	Output Voltage Range	0		5.5	V
V_{IH}	ON Pin High Voltage Range	1		5.5	V
V_{IL}	ON Pin Low Voltage Range	0		0.35	V
I_{OUT}	Output Current Range	0		130	mA
C_{OUT} (1)	Output Capacitance		18		nF
T_A	Ambient temperature	–40		125	°C

(1) The recommended output capacitance is the capacitance placed next to the output of the device that will provide optimal hard short performance across different load cable lengths.

6.4 Thermal Information

THERMAL METRIC(1)		TPS22948 DCK (SC-70) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	213.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	148.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	66.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	50.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	66.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

Unless otherwise noted, the characteristics in the following table applies at 5 V with a load of C_L = 0.1 µF, R_L = 100 Ω. Typical Values are at 25°C.

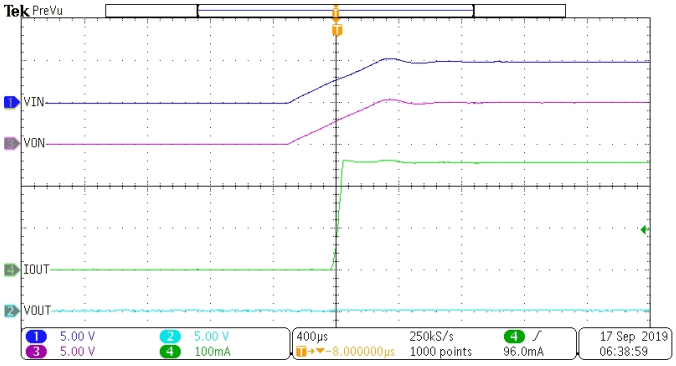
PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
Input Supply (VIN)								
$I_{Q, VIN}$	VIN Quiescent Current	$V_{ON} \geq V_{IH}$, VOUT = Open		-40°C to 125°C		50	85	µA
$I_{SD, VIN}$	VIN Shutdown Current	$V_{ON} \leq V_{IL}$, VOUT = GND		-40°C to 125°C		0.3	5	µA
ON-Resistance (RON)								
R_{ON}	ON-State Resistance	I_{OUT} = -50 mA		25°C		300	350	mΩ
				-40°C to 85°C			450	
				-40°C to 125°C			500	
Output Current Limit (ILIM)								
I_{LIM}	Output Current Limit			-40°C to 125°C	130	240	350	mA
t_{LIM}	Current Limit Response Time	Output hard short ($I_{OUT} > I_{LIM}$)		-40°C to 125°C		2		µs
Reverse Current Blocking (RCB)								
V_{RCB}	Activation Threshold	V_{OUT} Rising; $V_{OUT} > V_{IN}$		-40°C to 125°C		60		mV
	Release Threshold	V_{OUT} Falling; $V_{OUT} > V_{IN}$		-40°C to 125°C		44		mV
t_{RCB}	Response Time	$V_{OUT} = V_{IN}$ + 1V		-40°C to 125°C		3		µs
$I_{Q, RCB}$	RCB Quiescent Current (VIN)	$V_{ON} \leq V_{IL}$ $V_{OUT} - V_{IN}$ = 1V	$V_{ON} \leq V_{IL}$ $V_{OUT} - V_{IN}$ = 1V	-40°C to 125°C			15	µA
Fault Indication (FLT)								
$V_{OL, FLT}$	Output Low Voltage	I_{FLT} = 1 mA		-40°C to 125°C			0.1	V
$t_{DG,FLT}$	Fault Delay Time	$V_{ON} \geq V_{IH}$		-40°C to 125°C		10		µs
I_{FLT}	Off State Leakage	$V_{ON} \leq V_{IL}$		-40°C to 125°C			25	nA
Enable Pin (ON)								
$R_{PD, ON}$	Smart Pull Down Resistance	$V_{ON} \leq V_{IL}$		-40°C to 85°C		500		kΩ
I_{ON}	ON Pin Leakage	$V_{ON} \geq V_{IH}$		-40°C to 125°C			25	nA
Thermal Shutdown (TSD)								
TSD	Thermal Shutdown	Rising		N/A	130	150	170	°C
		Falling (Hysteresis)		N/A	100	120	140	°C

6.6 Switching Characteristics

Unless otherwise noted, the typical characteristics in the following table applies at 5 V and 25°C

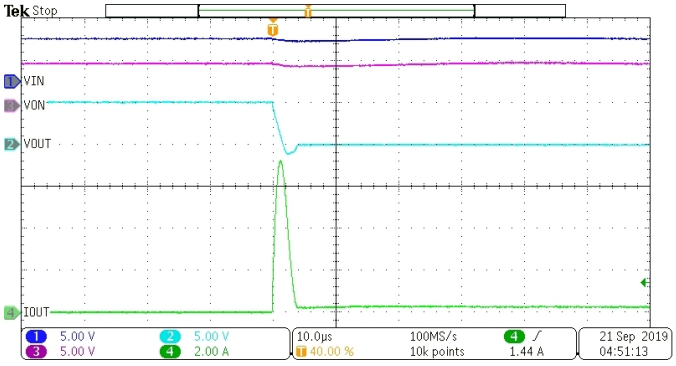
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Turn ON Time	C_L = 18 nF, R_L = 100 Ω		820		µs
t_R	Output Rise Time	C_L = 18 nF, R_L = 100 Ω		600		µs
SR_{ON}	Turn ON Slew Rate	C_L = 18 nF, R_L = 100 Ω		6.6		mV/µs
t_{OFF}	Turn OFF Time	C_L = 18 nF, R_L = 100 Ω		15		µs
t_{FALL}	Output Fall Time	C_L = 18 nF, R_L = 100 Ω		6.9		µs

6.7 Typical Characteristics



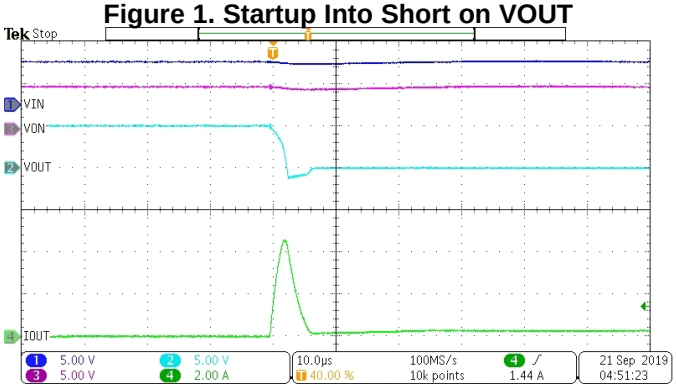
V_{IN} = 5 V T_A = 25 °C V_{OUT} = 0 V

Figure 1. Startup Into Short on VOUT



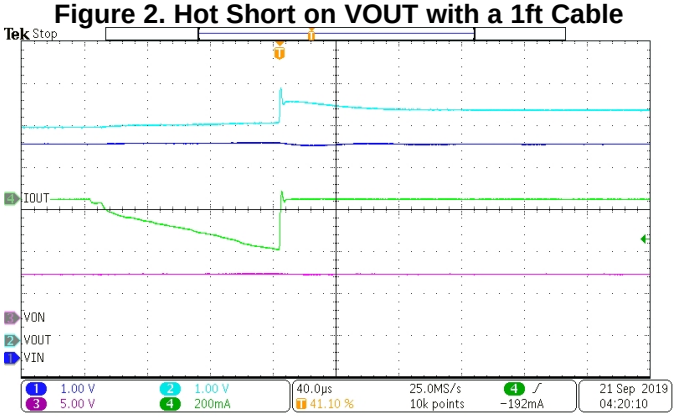
V_{IN} = 5 V T_A = 25 °C C_{OUT} = 18 nF

Figure 2. Hot Short on VOUT with a 1ft Cable



V_{IN} = 5 V T_A = 25 °C C_{OUT} = 18 nF

Figure 3. Hot Short on VOUT with a 3ft Cable



V_{IN} = 5 V T_A = 25 °C

Figure 4. Reverse Current Blocking Behavior

7 Parameter Measurement Information

7.1 Timing Waveform Diagram

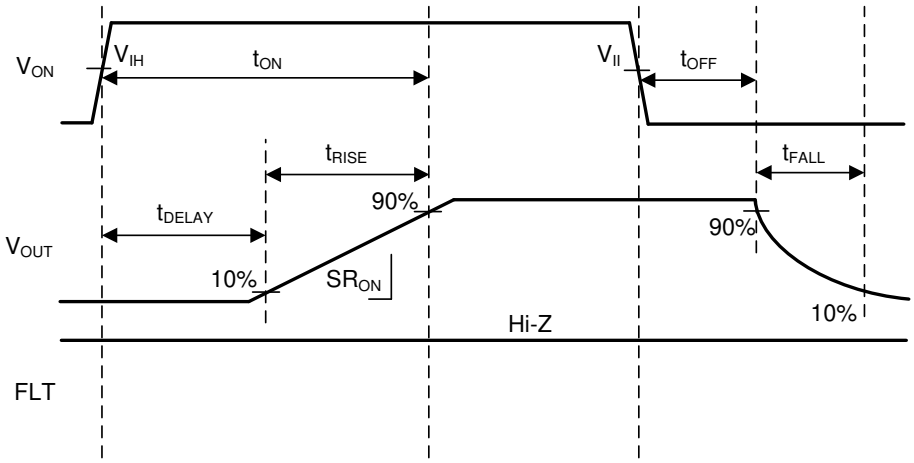


Figure 5. Timing Waveforms

8 Detailed Description

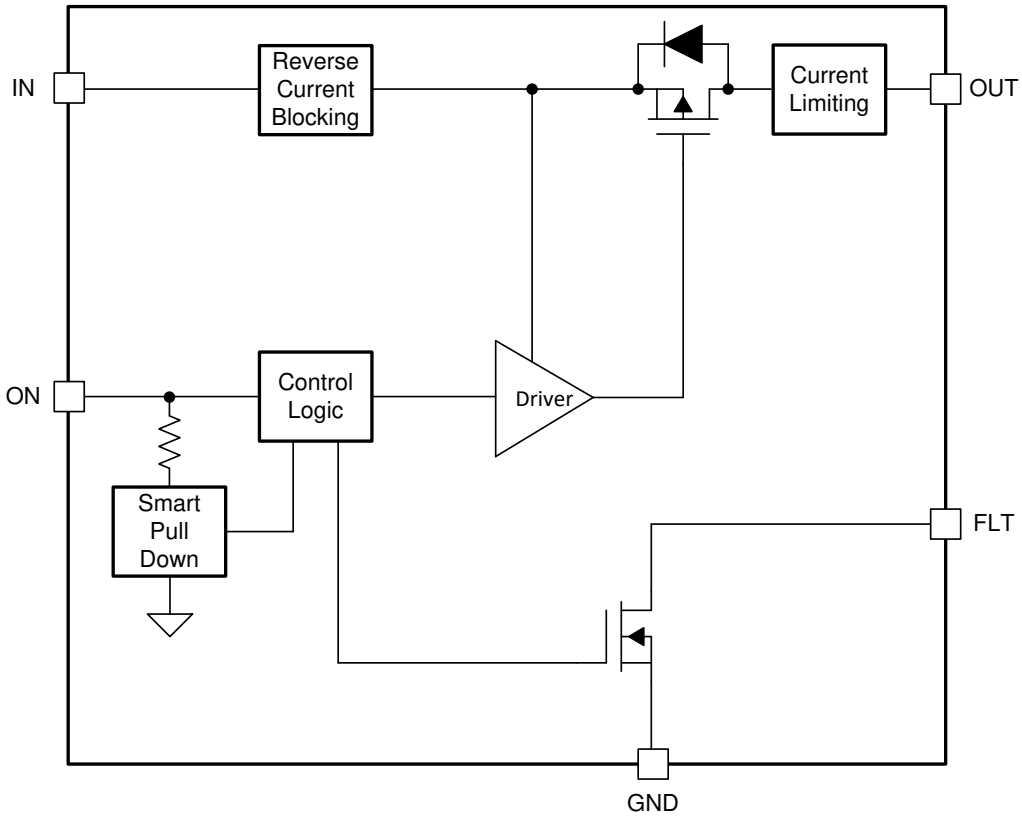
8.1 Overview

The TPS22948 device is a 5.5-V, 240-mA current limited load switch in a 6-pin SC-70 package. The 300-mΩ P-channel FET is used to switch power from input to output with minimal voltage drop across the device.

The TPS22948 device has a slow slew rate which helps reduce or eliminate power supply droop because of large inrush currents. During shutdown, the device has very low leakage currents, thereby reducing unnecessary leakages for downstream modules during standby. Integrated control logic, and driver eliminates the need for any external components which reduces solution size and bill of materials (BOM) count.

The TPS22948 load switch also provides protection features such as reverse current blocking, output current limiting and thermal shutdown.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 On and Off Control

The ON pin controls the state of the switch. The ON pin is compatible with standard GPIO logic threshold so it can be used in a wide variety of applications. When power is first applied to VIN, a smart pull down is used to keep the ON pin from floating until system sequencing is complete. Once the ON pin is deliberately driven high ($\geq V_{IH}$), the smart pull down is disconnected to prevent unnecessary power loss. See Table 1 when the ON pin smart pull down is active.

Table 1. Smart-ON Pull Down

VON	Pull Down
≤ V_{IL}	Connected
≥ V_{IH}	Disconnected

8.3.2 Fault Indication (FLT)

The FLT pin is an open drain output that acts as a status indication for the device. It is pulled low during thermal shutdown or reverse-current events. The behavior of the FLT pin is shown in Figure 6.

8.3.3 Current Limiting (V_{SC})

The TPS22948 responds to overcurrent conditions by limiting its output current to the ILIM level shown in Figure 6.

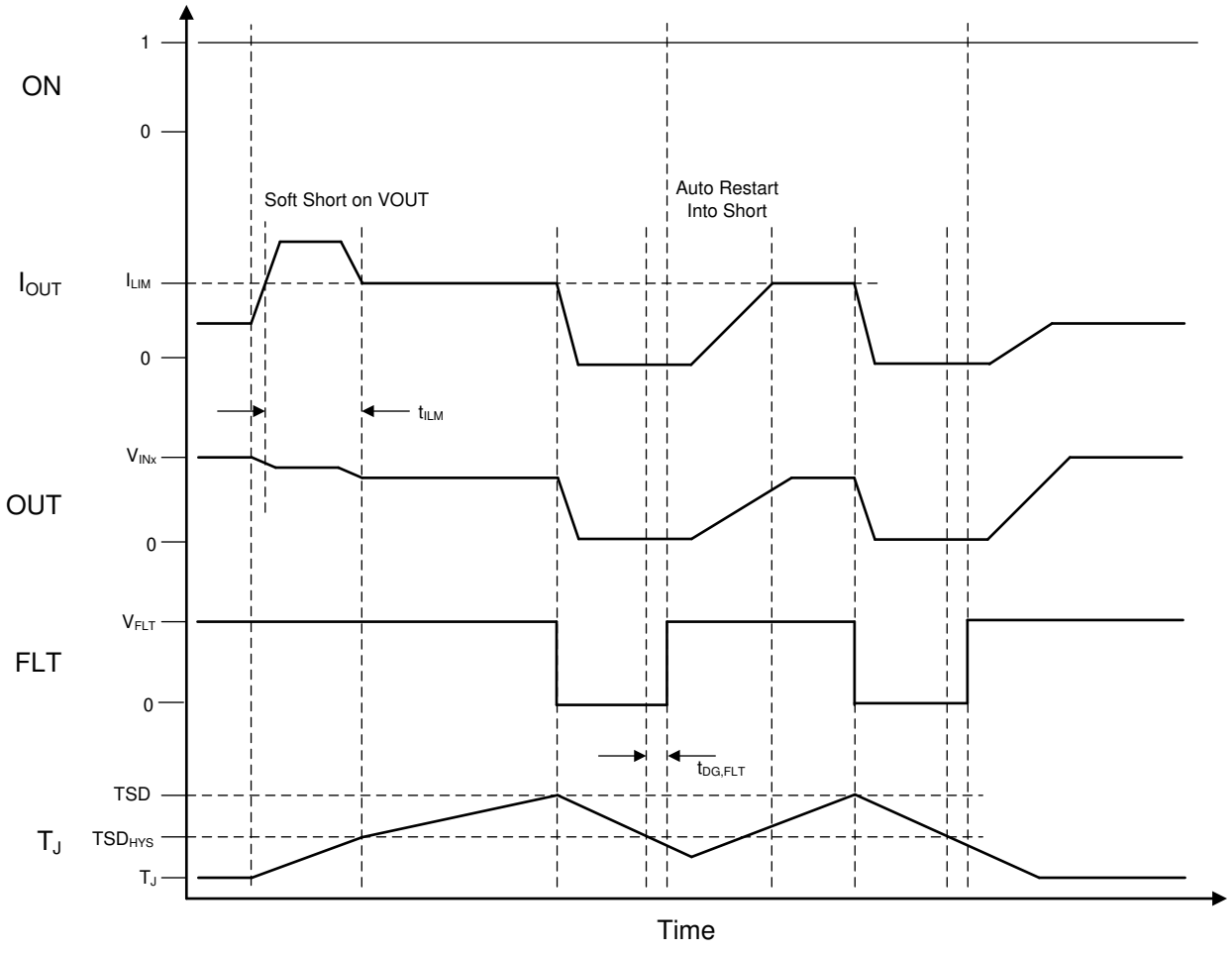


Figure 6. TPS22948 Current Limiting Behavior

When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Two possible overload conditions can occur.

The first condition is when a short circuit or partial short circuit is present on the output and the ON pin is toggled high, turning the device on. The output voltage is held near zero potential with respect to ground and the TPS22948 ramps the output current to I_{LIM}. The TPS22948 device will limit the current to I_{LIM} until the overload condition is removed or the internal junction temperature of the device reaches thermal shutdown and the device turns itself off. The device remains off until the junction temperature has lowered by TSD_{HYS}, and the device will turn itself back on. This will cycle until the overload condition is removed.

The second condition is when a short circuit, partial short circuit, or transient overload occurs after the device has been fully powered on. The device responds to the overcurrent condition within time t_{LIM} (see Figure 7), and before this time, the current is able to exceed I_{LIM}. In the case of a fast transient, the current-sense amplifier is overdriven and momentarily disables the internal power FET. The current-sense amplifier recovers and limits the output current to I_{LIM}. Similar to the previous case, the TPS22948 limits the current to I_{LIM} until the overload condition is removed or the internal junction temperature of the device reaches thermal shutdown and begins thermally cycling on and off.

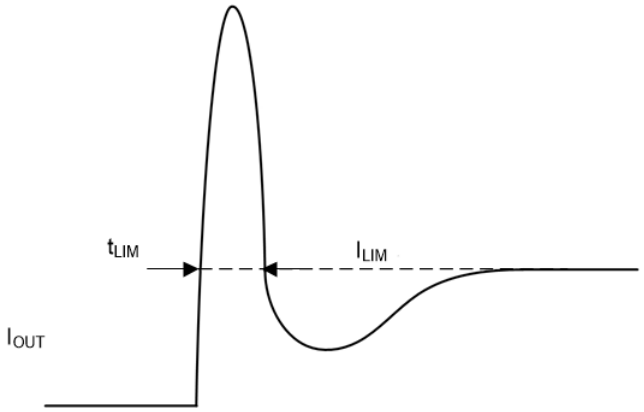


Figure 7. Transient Current Limit Waveform

8.3.4 Reverse Current Blocking (RCB)

In a scenario where the device is enabled and VOUT is greater than VIN, there is potential for reverse current to flow through the pass FET or the body diode. When the reverse current threshold is exceeded (about 200 mA), there is a delay time (t_{RCB}) before the switch turns off to stop the current flow. The switch will remain off and block reverse current as long as the reverse voltage condition exists. Once VOUT has dropped below the release voltage threshold (V_{RCB}) the device will turn back on. When the ON pin is pulled low, the device will constantly block reverse current.

8.4 Device Functional Modes

Table 2 describes the connection of the VOUT pin depending on the state of the ON pin.

Table 2. VOUT Connection

ON	TPS22919 VOUT
L	Open
H	VIN

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications.

9.2 Typical Application

This typical application demonstrates how the TPS22948 device can be used to power downstream modules.

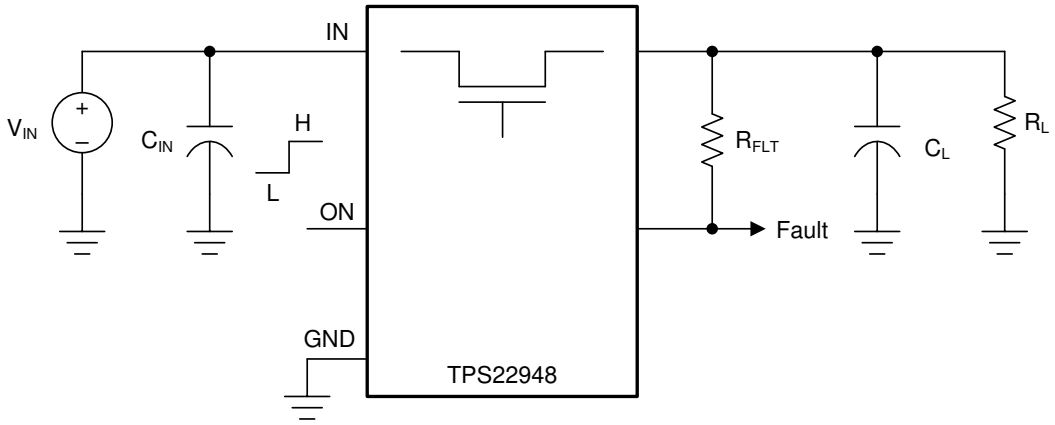


Figure 8. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the values listed in Table 3 as the design parameters:

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage (V_{IN})	5 V
Load Current / Resistance (R_L)	1 kΩ
Load Capacitance (C_L)	10 µF
Maximum Inrush Current (I_{INRUSH})	100 mA

Although the load capacitance is 10 µF, this is assumed to be at the end of a cable or closer to the load. An 18nF capacitance close to the output of the device is recommended for optimal performance during short circuit conditions.

9.2.2 Detailed Design Procedure

9.2.2.1 Limiting Inrush Current

Use Equation 1 to find the maximum output capacitance for a given inrush current requirement.

$$C_L = I_{INRUSH} \times t_R \div (0.8 \times V_{IN})$$

where

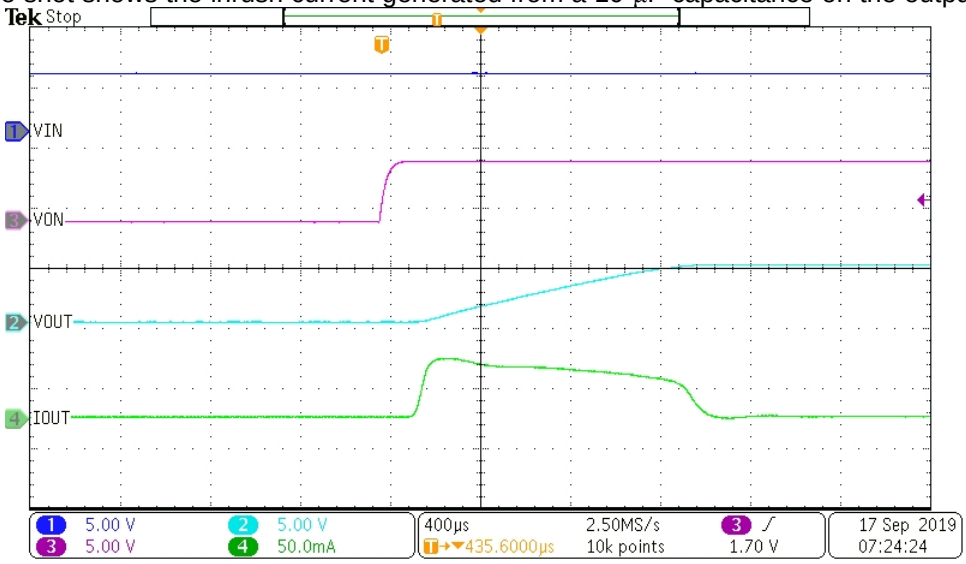
- C_L = capacitance on VOUT (µF)
- I_{INRUSH} = maximum acceptable inrush current (A)
- t_R = rise time of the TPS22948 (µs)

- V_{IN} = input voltage (V) (1)

Based on Equation 1, the maximum output capacitance that limits the inrush current to 100 mA is 12.5 µF. Therefore, the desired 10-µF load capacitance will not exceed the inrush current design requirement during turn on.

9.2.3 Application Curves

The below scope shot shows the inrush current generated from a 10-µF capacitance on the output.



A.

VIN = 5 V CL = 10 µF

Figure 9. TPS22948 Inrush Current Control with Slow Rise Time

10 Power Supply Recommendations

The device is designed to operate with a VIN range of 2.5 V to 5.5 V. The VIN power supply must be well regulated and placed as close to the device terminal as possible. The power supply must be able to withstand all transient load current steps. In most situations, using an input capacitance (CIN) of 1 μF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input. A 18nF capacitance close to the output of the device is recommended for optimal performance during short circuit conditions.

11 Layout

11.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects.

11.2 Layout Example

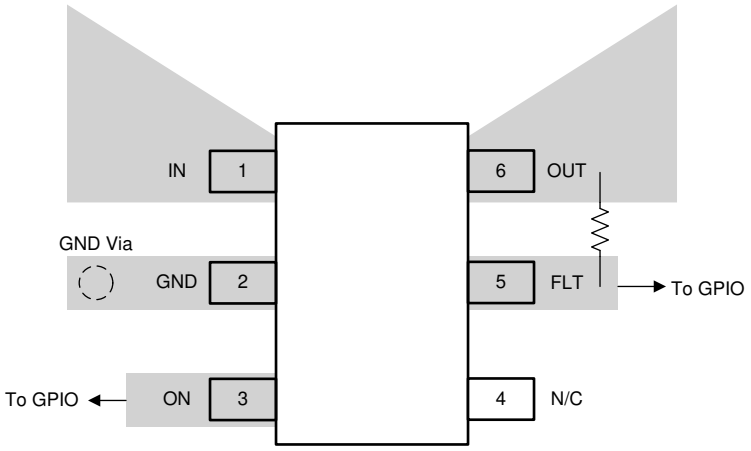


Figure 10. Recommended Board Layout

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

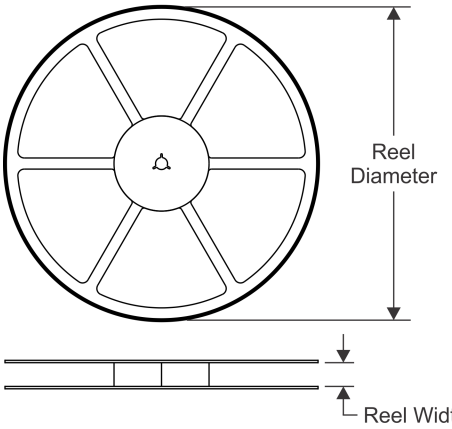
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

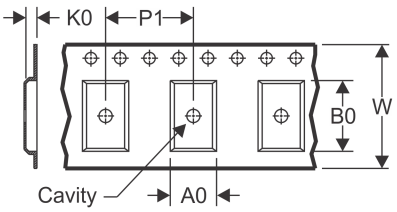
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

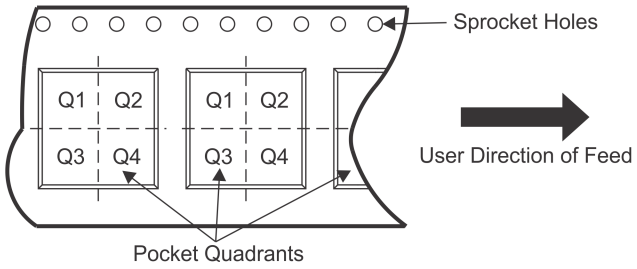


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

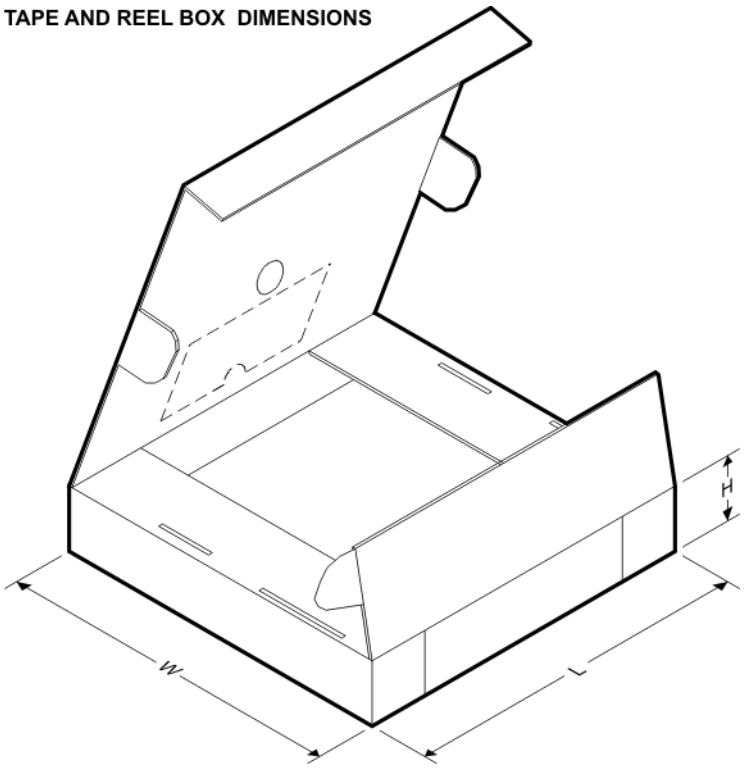
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22948DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

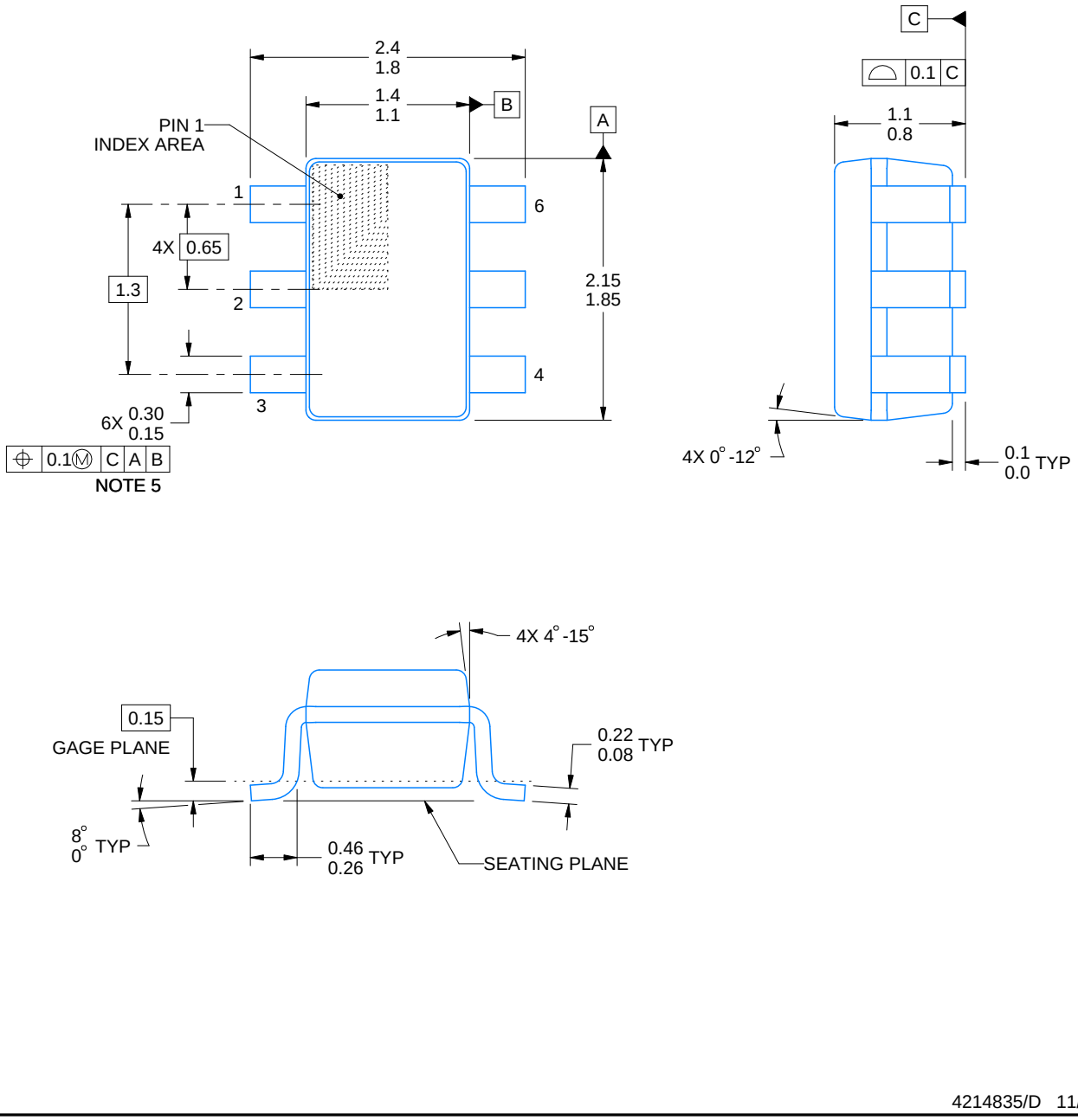
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22948DCKR	SC70	DCK	6	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DCK0006A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



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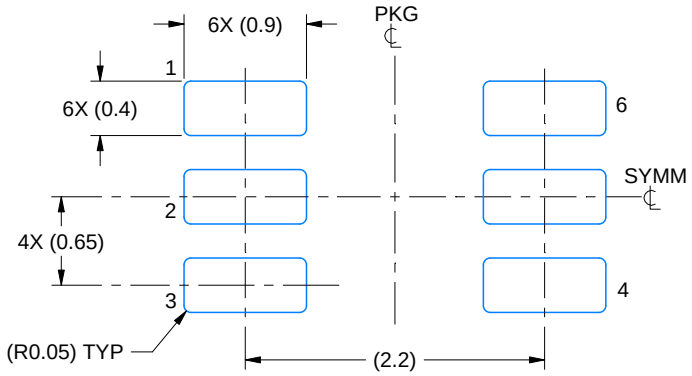
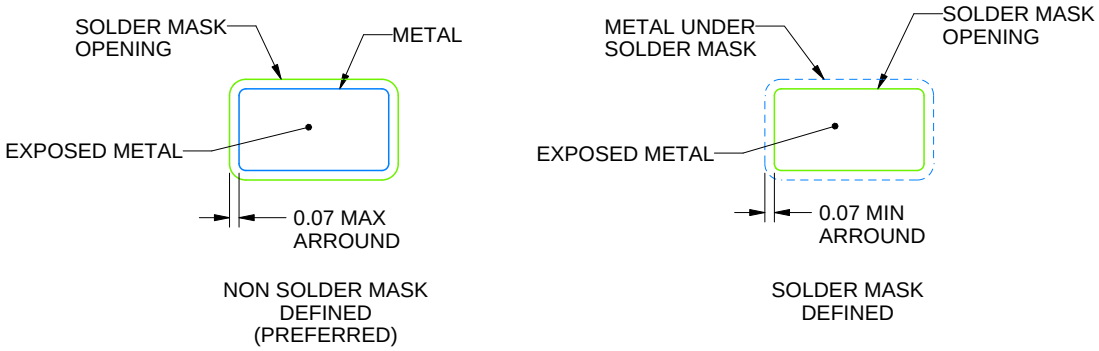
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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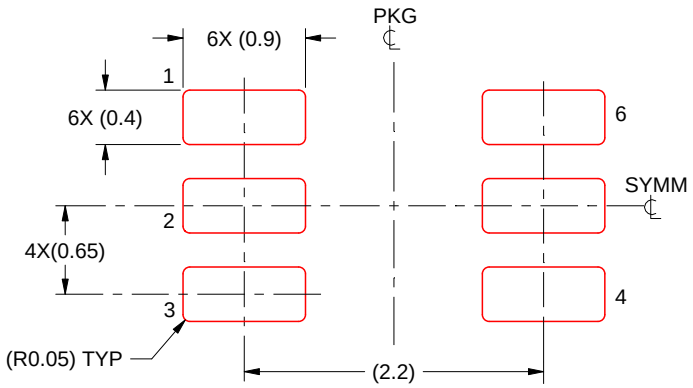
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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