36-V Hotswap Controller with Precision I²C Power Monitoring

Check for Samples: TPS2482, TPS2483

FEATURES

- **9-V to 36-V Input Range, 40 V Abs. Max**
- **Current, Voltage and Power Monitor**
- **±0.5% Accurate Current Monitoring (-25°C < T_J < 85°C)**
- **16 Programmable I²C™ Addresses**
- **Configurable Averaging Options**
- **Programmable MOSFET SOA protection**
- **High Side Gate Drive for External N-FET**
- **Programmable Fault Timer**
- **Open-Drain Power-Good Output**
- **20-Pin TSSOP Package**

APPLICATIONS

- **RRH (Remote Radio Heads)**
- **Storage Networks**
- **Plug-In Modules**
- **Base Station 24 V Antenna Power**
- **Industrial 24 V - 28 V Power**

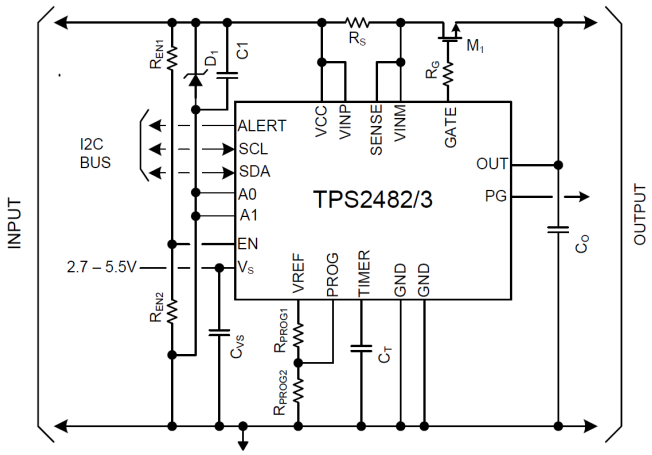
DESCRIPTION

The TPS2482 and TPS2483 provide hotswap control and precision monitoring for 9-V to 36-V applications. Accurate voltage, current, and power monitoring is provided by a 16-bit A/D converter with a serial interface that is compatible with I²C and SMBus. Voltage and current measurements are interleaved and multiplied internally to provide concurrent power calculations. These devices have high current monitoring accuracy over temperature and a broad load range. This makes them well suited for applications where load identity and health is determined by current profile, such as remote radio heads or cellular antennae.

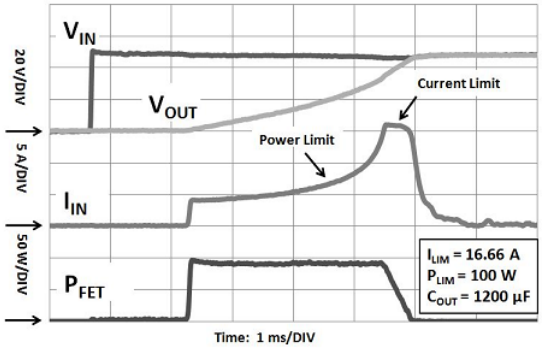
The hotswap section drives N-channel MOSFETs, with timed inrush and fault-current limiting. Advanced MOSFET safe operating area (SOA) protection is achieved by programmable constant-power foldback and a fixed current limit. This results in an exponential inrush current profile as shown in the start-up figure below. As V_{OUT} ramps up and the V_{DS} of the MOSFET is reduced the current increases keeping MOSFET power dissipation within its SOA at all times. The TPS2482 latches off after a hard fault, while the TPS2483 automatically attempts to restart after a cool-off delay.

The TPS2482 and TPS2483 can be dropped into existing TPS2480 and TPS2481 sockets to provide improved accuracy and operating voltage range. This can be accomplished with no PCB changes and minor software modifications.

Simplified Application Diagram



Example Start-Up Waveforms



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

While the standard monitoring function is limited to 36 V, with a few external components it is possible to monitor buses as high as 80 V. See special application description in High Voltage Application Example.

DEVICE INFORMATION (1)

DEVICE	AMBIENT TEMPERATURE	PACKAGE	FUNCTION	MARKING
TPS2482	-40°C to 85°C	PW20	Latch Off on Fault	TPS2482
TPS2483	-40°C to 85°C	PW20	Auto Retry on Fault	TPS2483

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the TI web-site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1) (2)

over recommended operating temperature range (unless otherwise noted)

	VALUES		UNIT
	MIN	MAX	
Input voltage range, VCC, SENSE, EN, OUT	-0.3	100	V
Supply voltage, V_S	-0.3	6	
Input voltage, common mode, VINP, VINM	-0.3	40	
Input voltage, differential, VINP, VINM	-40	40	
Input voltage range, PROG	-0.3	6	
Output voltage range, GATE, PG	-0.3	100	
Output voltage range, TIMER(3), VREF(3)	-0.3	6	
Sink current, PG		10	mA
Source current, VREF		2	
Sink current, PROG		2	
SDA, ALERT	-0.3	6	V
SCL	-0.3	(V_S + 0.3)	
Current into SENSE	-1	1	mA
Current into SDA, SCL, V_S, VINP, VINM, A0, A1, ALERT		5	
Open-drain digital output current into SDA, ALERT		10	
ESD rating, HBM		2000	V
ESD rating, CDM		500	
Maximum operating junction temperature, T_J		150	°C
Storage temperature range, T_{stg}	-40	150	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND unless otherwise noted.
(3) Do not apply external voltage to these pins.

RECOMMENDED OPERATING CONDITIONS

over recommended junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VCC	Hotswap section bias-supply voltage range	9		80	V
V_S	Monitor section bias-supply voltage range	2.7		5.5	
VINP, VINM	Monitor section sensing input voltage range	0		36	
PROG	Power-limit programming voltage range	0.4 (1)		4	
VREF	Reference source current	0		1	mA
T_J	Operating junction temperature	-40		125	°C

(1) V_{PROG} may be set below this minimum with reduced power-limit accuracy.

THERMAL INFORMATION

THERMAL METRIC (1)		TPS2482 and TPS2483	UNITS
		PW	
		20 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	99.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	33.6	
θ_{JB}	Junction-to-board thermal resistance	50.4	
ψ_{JT}	Junction-to-top characterization parameter	2.2	
ψ_{JB}	Junction-to-board characterization parameter	49.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS (Hotswap Section)

Unless otherwise noted, minimum and maximum limits apply across the recommended operating junction temperature and voltage ranges, typical specifications are at T_J = 25°C, V_{VCC} = 48 V, V_{PROG} = 2 V, V_{TIMER} = 0 V, all outputs unloaded. Voltages are with respect to GND and positive currents are into pins.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Hotswap Supply (VCC)						
I_{VCC}	Hotswap section enabled	V_{EN} = Hi, V_{SENSE} = V_{VCC}, V_{OUT} = V_{VCC}		450	1000	µA
	Hotswap section disabled	V_{EN} = Lo, V_{SENSE} = V_{VCC}, V_{OUT} = 0 V		90	250	
	UVLO turn-on threshold	VCC rising		8.4	8.8	V
	UVLO turn-off threshold	VCC falling	7.2	8.3		
	UVLO threshold hysteresis			75		mV
Current Sense Input (SENSE)						
I_{SENSE}	Input bias current	V_{SENSE} = V_{VCC}, V_{OUT} = V_{VCC}		7.5	20	µA
Reference Voltage Output (VREF)						
V_{VREF}	Reference voltage	0 mA < I_{VREF} < 1 mA	3.9	4	4.1	V
Power Limiting Input (PROG)						
I_{PROG}	Input bias current; device enabled; sourcing or sinking	0 V < V_{PROG} < 4 V, V_{EN} = 48 V			5	µA
R_{PROG}	Pulldown resistance; device disabled	I_{PROG} = 200 µA, V_{EN} = 0 V		375	600	Ω
Power Limiting and Current Limiting (SENSE)						
V_{CL_PL}	Current-sense threshold $V_{(VCC-SENSE)}$, with power-limit active	[V_{PROG} = 2.4 V and V_{OUT} = 0 V] or [V_{PROG} = 0.9 V and V_{OUT} = 30 V]	17	25	33	mV
V_{CL}	Current-sense threshold $V_{(VCC-SENSE)}$, with power-limit inactive	V_{PROG} = 4 V, V_{OUT} = V_{SENSE}	45	50	55	
t_{F_TRIP}	Response time, from large overload to GATE low	V_{PROG} = 4 V, V_{OUT} = V_{SENSE}, $C_{(GATE-OUT)}$ = 2 nF, $V_{(VCC-SENSE)}$ = 0 V → 200 mV, $V_{(GATE-OUT)}$ = 1 V			1.2	µs
Timer Operation (TIMER)						
I_{SOURCE}	Charge current (sourcing)	V_{TIMER} = 0 V	15	25	34	µA
		V_{TIMER} = 0 V, T_J = 25°C	20	25	30	
I_{SINK}	Discharge current (sinking)	V_{TIMER} = 5 V	1.5	2.5	3.7	
		V_{TIMER} = 5 V, T_J = 25°C	2.1	2.5	3.1	
V_{TMRHI}	TIMER upper threshold voltage		3.9	4.0	4.1	V
V_{TMRLO}	TIMER lower threshold voltage	TPS2483 only	0.96	1.0	1.04	
D_{RETRY}	Fault retry duty-cycle	TPS2483 only	0.5%	0.75%	1%	
Gate Drive Output (GATE)						
I_{GATE}	GATE sourcing current	V_{EN} = Hi, V_{SENSE} = V_{VCC}, $V_{(GATE-OUT)}$ = 7 V	15	22	35	µA
	GATE sinking current	V_{EN} = Lo, V_{GATE} = V_{VCC}	1.8	2.4	2.8	mA
		V_{EN} = Hi, V_{GATE} = V_{VCC}, $V_{(VCC-SENSE)}$ = 200 mV	75	125	250	
$V_{GATE-OUT}$	GATE output voltage	V_{GATE} with respect to V_{OUT}	12		16	V
t_{D_ON}	Propagation delay: EN going true to GATE output high	V_{EN} = 0 V → 2.5 V (t_{RISE} < 0.1 µs), 50% of V_{EN} to 50% of V_{GATE}, V_{OUT} = V_{VCC}, $R_{(GATE-OUT)}$ = 1 MΩ		25	40	µs
t_{D_OFF}	Propagation delay: EN going false to GATE output low	V_{EN} = 2.5 V → 0 V (t_{FALL} < 0.1 µs), 50% of V_{EN} to 50% of V_{GATE}, V_{OUT} = V_{VCC}, $R_{(GATE-OUT)}$ = 1 MΩ		0.5	1	
	Propagation delay: TIMER expires to GATE output low	V_{TIMER} = 0 V → 5 V (t_{RISE} < 0.1 µs), 50% of V_{TIMER} to 50% of V_{GATE}, V_{OUT} = V_{VCC}, $R_{(GATE-OUT)}$ = 1 MΩ		0.8	1	

ELECTRICAL CHARACTERISTICS (Hotswap Section) (continued)

Unless otherwise noted, minimum and maximum limits apply across the recommended operating junction temperature and voltage ranges, typical specifications are at T_J = 25°C, V_{VCC} = 48 V, V_{PROG} = 2 V, V_{TIMER} = 0 V, all outputs unloaded. Voltages are with respect to GND and positive currents are into pins.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power-Good Output (PG)						
V_{PG_OL}	Output voltage (sinking), PG = false	V_{OUT} = 0 V, I_{PG} = 2 mA		0.1	0.25	V
		V_{OUT} = 0 V, I_{PG} = 4 mA		0.25	0.5	
V_{PGTL}	PG = true threshold voltage	V_{SENSE} = V_{VCC}, V_{OUT} rising, $V_{(SENSE-OUT)}$ decreasing	0.8	1.25	1.7	
V_{PGTH}	PG = false threshold voltage	V_{SENSE} = V_{VCC}, V_{OUT} falling, $V_{(SENSE-OUT)}$ increasing	2.2	2.7	3.2	
V_{HYST_PG}	PG threshold hysteresis	V_{SENSE} = V_{VCC}		1.4		
t_{DPG}	PG deglitch delay, detection to output, rising and falling edges	V_{SENSE} = V_{VCC}	5	9	15	ms
	Output leakage current, PG = true	V_{PG} = V_{VCC}			10	µA
Output Voltage Feedback Input (OUT)						
I_{OUT}	Input bias current	V_{OUT} = V_{VCC}, V_{EN} = Hi; (sinking)		8	20	µA
		V_{OUT} = 0 V, V_{EN} = Lo; (sourcing)		18	40	
Enable Input (EN)						
V_{EN_H}	Threshold V_{EN} rising		1.32	1.35	1.38	V
V_{EN_L}	Threshold V_{EN} falling		1.20	1.25	1.30	
	EN threshold hysteresis			100		mV
I_{EN}	Input bias current	V_{EN} = 30 V			1	µA

ELECTRICAL CHARACTERISTICS (Monitor Section)

Boldface limits apply over the recommended junction temperature range, otherwise limits apply at T_A = 25°C. Unless otherwise noted, V_S = 3.3 V, VINP = 12 V, V_{SHUNT} = (VINP – VINM) = 0 mV, default power-on mode. Voltages are with respect to GND and positive currents are into pins.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
Monitor Supply (V_S)						
Operating supply range			2.7		5.5	V
Quiescent current, default operating mode		No SCL clock		330	420	µA
Quiescent current, power-down mode		No SCL clock		0.5	2	µA
Monitor Sense Inputs (VINP, VINM)						
Shunt voltage input range			-81.9175		81.9175	mV
Bus voltage input range[1]			0		36	V
Common-mode rejection	CMRR	V_{VINP} = 0 V to 36 V	126	140		dB
Shunt offset voltage, RTI[2]	V_{OS}			±2.5	±10	µV
vs Temperature				***0.1***	***0.4***	***µV/°C***
vs Power supply	PSRR	V_S = 2.7 V to 5.5 V		2.5		µV/V
Bus offset voltage, RTI[2]	V_{OS}			±1.25	±7.5	mV
vs Temperature				***10***	***40***	***µV/°C***
vs Power supply	PSRR	V_S = 2.7 V to 5.5 V		0.5		mV/V
Input bias current	I_{VINP}			10		µA
Input bias current, plus parallel resistance	I_{VINM} + R_{VINM}			10µA || 830kΩ		

(1) While the input range is limited to 36 V, the full-scale range of the ADC scaling is 40.96 V. See the Basic ADC Functions section. Do not apply more than 36 V.
(2) RTI = Referred-to-input.

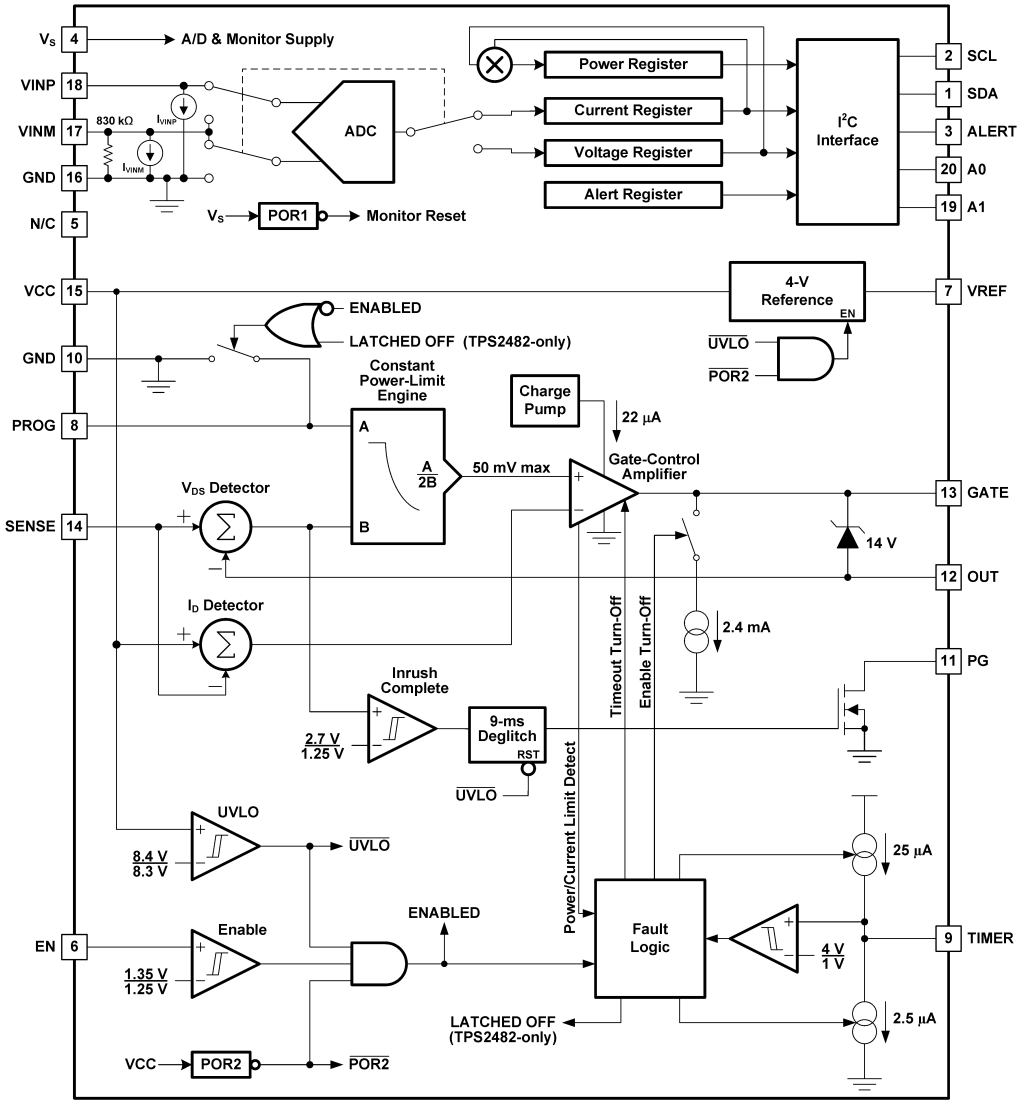
ELECTRICAL CHARACTERISTICS (Monitor Section) (continued)

Boldface limits apply over the recommended junction temperature range, otherwise limits apply at T_A = 25°C. Unless otherwise noted, V_S = 3.3 V, VINP = 12 V, V_{SHUNT} = (VINP – VINM) = 0 mV, default power-on mode. Voltages are with respect to GND and positive currents are into pins.

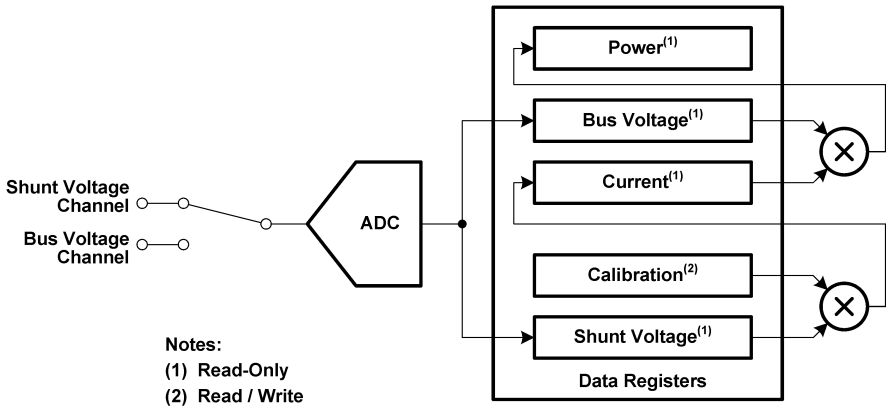
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
Input leakage(3)		(VINP Pin) + (VINM Pin), Power-down mode, excluding VINM resistance		0.1	0.5	µA
Conversion DC Accuracy						
ADC native resolution				16		Bits
1 LSB step size, Shunt voltage				2.5		µV
1 LSB step size, Bus voltage				1.25		mV
Shunt voltage gain error				0.02	0.1	%
vs Temperature				***10***	***50***	***ppm/°C***
Bus voltage gain error				0.02	0.1	%
vs Temperature				***10***	***50***	***ppm/°C***
Differential nonlinearity				±0.1		LSB
ADC conversion time, shunt or bus voltage		CT bits = 000		140	154	µs
		CT bits = 001		204	224	
		CT bits = 010		332	365	
		CT bits = 011		588	646	
		CT bits = 100 (default)		1.1	1.21	ms
		CT bits = 101		2.116	2.328	
		CT bits = 110		4.156	4.572	
		CT bits = 111		8.244	9.068	
Serial-Bus Characteristics (SDA, SCL, ALERT, A0, A1)						
Input capacitance				3		pF
Input leakage current		$0 \le V_{IN} \le V_S$		0.1	1	µA
Input logic high level	V_{IH}		$0.7(V_S)$		V_S	V
Input logic low level	V_{IL}		–0.3		$0.3(V_S)$	V
Input hysteresis level	Hysteresis			500		mV
Output logic low level SDA, ALERT	V_{OL}	I_{OL} = 3 mA	0		0.4	V
Bus timeout(4)		V_{SCL} = 0 V		28	35	ms

(3) Input leakage is positive (current flowing into the pin) for the conditions shown at the top of this table. Negative leakage currents can occur under different input conditions.
(4) Serial-Bus timeout in the TPS2482 and TPS2483 reset the bus interface any time SCL is low for more than the specified limit.

FUNCTIONAL BLOCK DIAGRAM



Register Block Diagram



Pinout Diagram
20-Pin TSSOP
PW Package
(Top View)

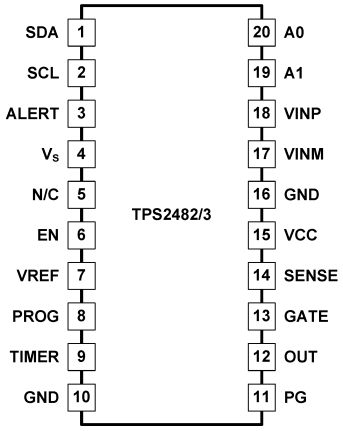


Table 1. PIN FUNCTIONS

NAME	NUMBER	I/O	DESCRIPTION
A0	20	I	Serial-bus address input. Connect to GND, SCL, SDA, or V_S. Table 8 shows pin settings and corresponding addresses.
A1	19	I	Serial-bus address input. Connect to GND, SCL, SDA, or V_S. Table 8 shows pin settings and corresponding addresses.
ALERT	3	O	Serial-bus multi-function alert signal, open-drain output.
EN	6	I	Hotswap section enable input.
GATE	13	O	Pass-MOSFET gate-drive output.
GND	10	-	GND; common reference for all other input and output voltages.
GND	16	-	GND; common reference for all other input and output voltages.
N/C	5	-	No connection; tie to GND or float.
OUT	12	I	Input to sense pass-MOSFET source voltage for power-limit protection and PG state determination.
PG	11	O	Open-drain power-good output signal based on V_{SENSE} - V_{OUT}.
PROG	8	I	Pass-MOSFET power-limit programming input. Typically apply 0.4 to 4 V with a resistor divider from VREF.
SCL	2	I	Serial-bus clock line, high impedance input.
SDA	1	I/O	Serial-bus data line, open-drain input/output.
SENSE	14	I	Input to sense pass-MOSFET drain voltage for power-limit protection, and for sensing current-shunt voltage.
TIMER	9	I	Connect the fault timing capacitor from TIMER to GND.
VCC	15	I	Hotswap section bias-supply input and the positive reference for sensing current-shunt voltage.
VINM	17	I	Negative differential shunt voltage input. Connect to negative side of shunt resistor. Bus voltage is also measured from this pin to GND.
VINP	18	I	Positive differential shunt voltage input. Connect to positive side of shunt resistor.
VREF	7	O	Reference voltage output, used to set power-limit threshold on PROG input.
V_S	4	I	Monitor section bias-supply input.

Pin Function Detailed Descriptions

A0, A1: Address bits for setting the TPS2482 and TPS2483 serial-bus address. Each input may be tied to one of four pins (GND, SDA, SCL, V_S) which provides a total of 16 different available addresses, as shown in Table 8.

ALERT: The ALERT pin is associated with the serial bus, similar to the SMBus Alert function. ALERT is an open-drain multi-function logic signal that can be programmed to go low if a user-defined threshold has been exceeded.

EN: The GATE driver is enabled when the internal POR2 and UVLO thresholds have been satisfied and the EN upper threshold is exceeded. Hysteresis between the upper and lower thresholds of EN helps to avoid enable/disable chatter if a slowly changing voltage is applied. EN can be used as a logic-level control input, an analog input voltage monitor as illustrated by R_{EN1}/R_{EN2} in the Simplified Application Diagram, or it can be tied to VCC to always enable the TPS2482 and TPS2483. The hysteresis associated with the internal comparator makes this a stable method of detecting a low input voltage condition and shutting off the downstream circuit(s). A TPS2482 that has latched off can be reset by cycling EN below its lower threshold and back high.

GATE: Provides the high-side (above VCC) gate drive for the external N-channel MOSFET pass-transistor (pass-MOSFET). It is controlled by the internal gate drive amplifier, which provides a pull-up current of 22 µA from an internal charge pump and a strong pull-down to ground of at least 75 mA. The pull-down current is a non-linear function of the amplifier overdrive; it provides less drive for small overloads, but higher overdrive for fast reaction to an output short-circuit. There is a separate pull-down of about 2.4 mA to shut off the pass-MOSFET when either EN or UVLO fall below their respective lower thresholds.

An internal clamp protects the gate of the pass-MOSFET (to OUT) and generally eliminates the need for an external clamp in almost all cases for devices with a $V_{GS(max)}$ rating ≥ 20 V; an external Zener diode may be required to protect the gate of high-C_{GD} devices with $V_{GS(max)}$ < 16 V. A small series resistance of 10 Ω should be inserted in the gate lead if the C_{ISS} of the pass-MOSFET > 200 pF, otherwise use 33 Ω for small MOSFETs.

A capacitor can be connected from GATE to ground to create a slower inrush with a constant current profile without affecting the amplifier stability. Add a series resistor of about 1 kΩ to the gate capacitor to maintain the gate clamping and current limit response time.

GND: These pins are connected to the system ground.

OUT: This pin is an input used by the constant power-limit engine and the PG comparator to measure V_{DS} of the pass-MOSFET as $V_{(SENSE-OUT)}$. Internal protection circuits leak a small current from this pin when it is low. If the load circuit can drive OUT below ground, connect a clamp (or freewheel) diode from OUT (cathode) to GND (anode) to keep V_{OUT} > -0.3 V.

PG: This open-drain output is intended to interface to downstream dc/dc converters or monitoring circuits to provide a "power-good" indication when load capacitor charge-up is essentially complete. PG goes open-drain (high voltage with a pull-up) after V_{DS} of the pass-MOSFET has fallen below 1.25 V and a 9-ms deglitch time period has elapsed. PG is false (low or low-resistance to ground) whenever V_{DS} of the pass-MOSFET is above 2.7 V or UVLO is active. PG can also be viewed as having an input and output voltage monitor function. The 9-ms deglitch circuit serves to filter short events that could cause PG to go inactive (low) such as a momentary overload or input voltage step. However, the 9-ms delay is immediately reset whenever UVLO is active. V_{PG} can be greater than V_{VCC} because its ESD protection is only with respect to ground.

PROG: The voltage applied to this pin (normally 0.4 V to 4.0 V) programs the power dissipation limit for the pass-MOSFET by the constant power-limit engine. Applying a voltage lower than 0.4 V may result in wide variations in power-limiting performance. Typically, a resistor divider R_{PROG1}/R_{PROG2} is connected from VREF to PROG to set the power limit according to the following equation:

$$V_{PROG} = \frac{P_{LIM}}{(10 \times I_{LIM})} \quad (1)$$

where P_{LIM} is the desired power dissipation limit for the pass-MOSFET and I_{LIM} is the current limit setpoint (see SENSE). P_{LIM} is determined by the allowable thermal stress on the pass-MOSFET:

$$P_{LIM} < \frac{T_{J(max)} - T_{S(max)}}{R_{\theta JC(max)}} \quad (2)$$

where $T_{J(max)}$ is the maximum desired transient junction temperature of the pass-MOSFET and $T_{S(max)}$ is its maximum case temperature just prior to a power-limiting event (such as a start or restart). $R_{\theta JC(max)}$ is the transient junction-to-case thermal resistance of the pass-MOSFET corresponding to the event interval.

V_{PROG} is used in conjunction with V_{DS} to compute the (scaled) drain current, $I_{D\_ALLOWED}$, by the constant power-limit engine. $I_{D\_ALLOWED}$ is compared by the gate amplifier to the actual I_D and used to generate a gate drive. If $I_D < I_{D\_ALLOWED}$, the amplifier turns the gate of the pass-MOSFET full on because there is no overload condition; otherwise GATE is regulated to maintain the $I_D = I_{D\_ALLOWED}$ relationship.

A capacitor may be tied from PROG to ground to alter the natural constant power inrush current shape. If properly designed, the effect is to cause the leading step of current in Figure 30 to look like a ramp. PROG is internally pulled to ground whenever EN, POR2, or UVLO are not satisfied, or the TPS2482 is latched off. This feature serves to discharge any capacitance connected to the pin. Do not apply voltages greater than 4 V to PROG. If the constant power limit is not used, PROG should be tied to VREF through a 47-kΩ resistor.

SCL: This pin is the clock input for the serial-bus interface.

SDA: This pin is the data input for the serial-bus interface.

SENSE: Monitors the input voltage at the drain of the pass-MOSFET, and the downstream side of R_S providing the constant power limit engine with feedback of both the pass-MOSFET current (I_D) and voltage (V_{DS}). Voltage is determined by the difference between SENSE and OUT, while the current analog is the difference between VCC and SENSE. The constant power engine uses V_{DS} to compute the allowed I_D and is clamped to 50 mV, acting like a traditional current limit at low V_{DS}. The maximum current limit is set by the following equation:

$$I_{LIM} = 50\ mV / R_S \quad (3)$$

Design the connections to SENSE to minimize R_S voltage sensing errors. Don't drive SENSE to a large voltage difference from VCC because there is a non-linear internal impedance between them. The current limit function can be disabled by connecting SENSE to VCC.

TIMER: An integrating capacitor, C_T, connected to the TIMER pin provides a timing function that controls the allowable fault-time for both versions and the retry interval for the TPS2483. The timer charges at 25 µA whenever the TPS2482 and TPS2483 are in power limit or current limit and discharges at 2.5 µA otherwise. The charge-to-discharge current ratio is constant with temperature even though there is a positive temperature coefficient to both. If TIMER reaches 4 V, the TPS2482 pulls GATE to ground, latches off, and discharges C_T. The TPS2483 pulls GATE to ground and attempts a restart (re-enable GATE) after a timing sequence consisting of discharging C_T down to 1 V followed by 15 more charge and discharge cycles. The TPS2482 can be reset by either cycling the EN pin or the UVLO (e.g. power cycling). TIMER discharges when EN is low or UVLO or the internal POR2 (power-on reset) are active. The TIMER pin should be tied to ground if this feature is not used. The general equation for fault retry time as a function of C_T and retry-application information is found in Applications Using the Retry Feature (TPS2483).

VCC: Power supply input for the hotswap section, which provides three functions:

1. biasing power to the integrated circuit,
2. input to the hotswap section power-on reset (POR2) and under voltage lockout (UVLO) functions, and
3. voltage sense at one terminal of R_S for the pass-MOSFET current measurement.

The voltage must exceed the POR2 threshold (about 6 V for approximately 400 µs) and the internal UVLO turn-on threshold (about 8.4 V) before normal operation (driving the GATE output) may begin. Connections to VCC should be designed to minimize R_S voltage sensing errors and to maximize the effect of C_1 and D_1; place C_1 at R_S rather than at the device pin to eliminate transient sensing errors. GATE, PROG, PG, and TIMER are held low when either UVLO or POR2 are active.

VINM: This pin is Kelvin connected to the negative (load) side of the current sensing resistor.

VINP: This pin is Kelvin connected to the positive (source) side of the current sensing resistor.

V_S: Power supply input for the monitoring section power-on reset (POR1), control logic, ADC, and serial-bus interface. Typically between 2.7 V and 5.5 V.

VREF: Provides a 4.0-V reference voltage for use in conjunction with the resistor divider of a typical application circuit to set the voltage on the PROG pin. The reference voltage is available once the internal POR2 and UVLO turn-on thresholds have been met. It is not designed as a general-purpose supply voltage for other external circuitry, therefore ensure that no more than 1 mA is drawn from this output. Although not typically required, capacitance up to 1000 pF may be placed on this pin.

TYPICAL CHARACTERISTICS

At T_A = 25°C, V_S = 3.3 V, VINP = 12 V, V_{SHUNT} = (VINP – VINM) = 0 mV, unless otherwise noted.

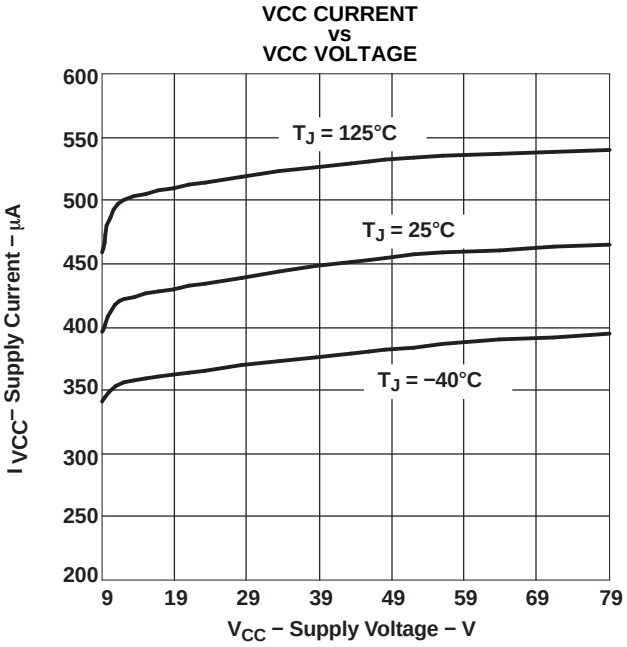


Figure 1.

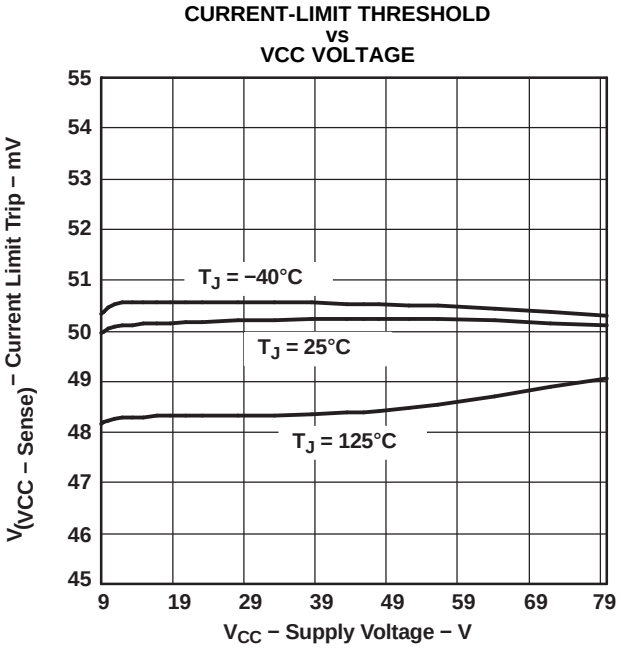


Figure 2.

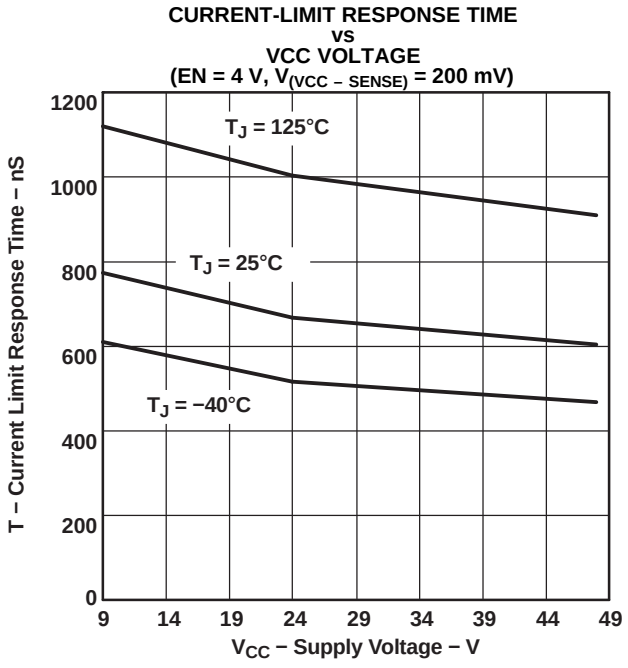


Figure 3.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_S = 3.3 V, VINP = 12 V, V_{SHUNT} = (VINP – VINM) = 0 mV, unless otherwise noted.

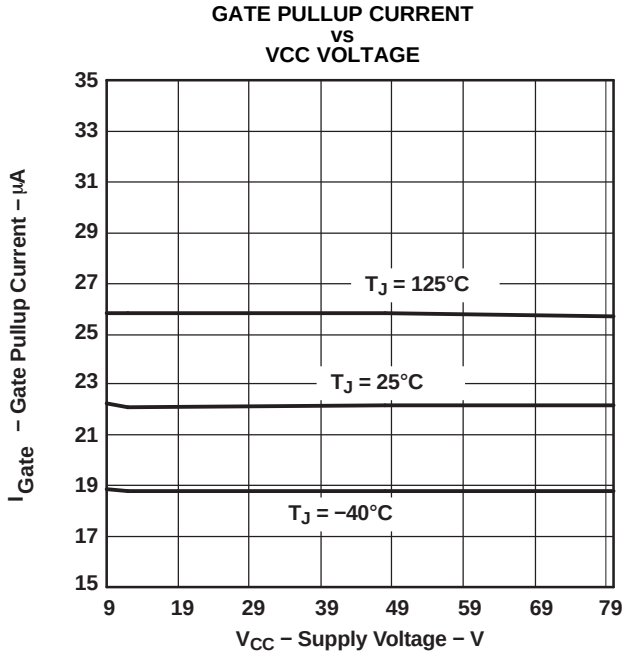


Figure 4.

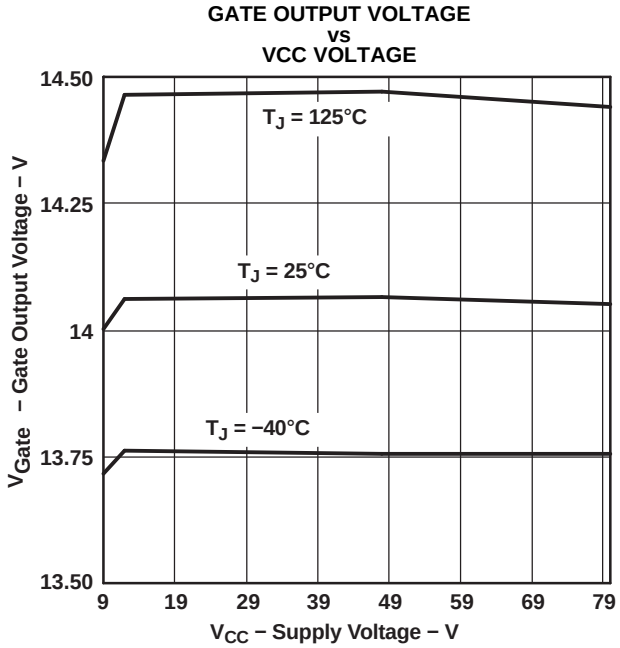


Figure 5.

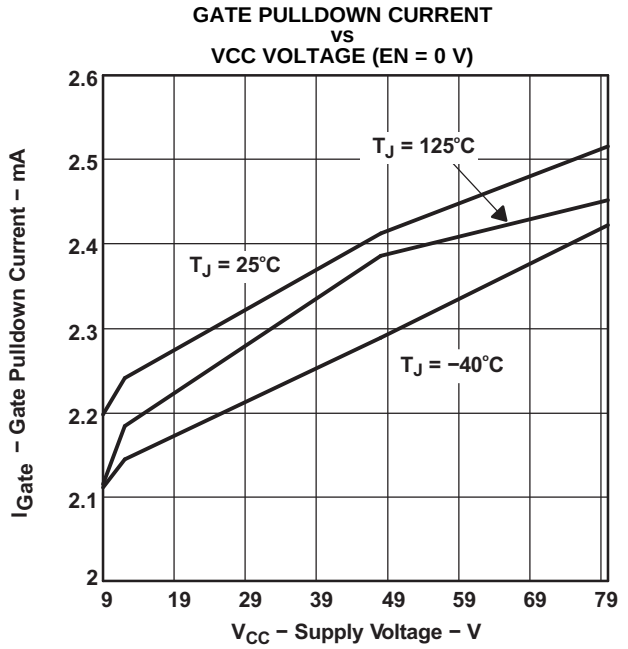


Figure 6.

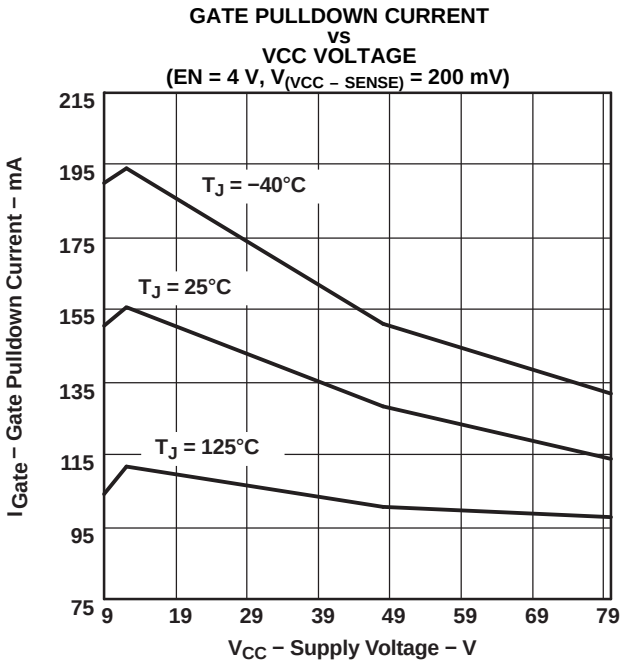


Figure 7.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_S = 3.3 V, VINP = 12 V, V_{SHUNT} = (VINP – VINM) = 0 mV, unless otherwise noted.

TIMER PULLUP CURRENT vs VCC VOLTAGE

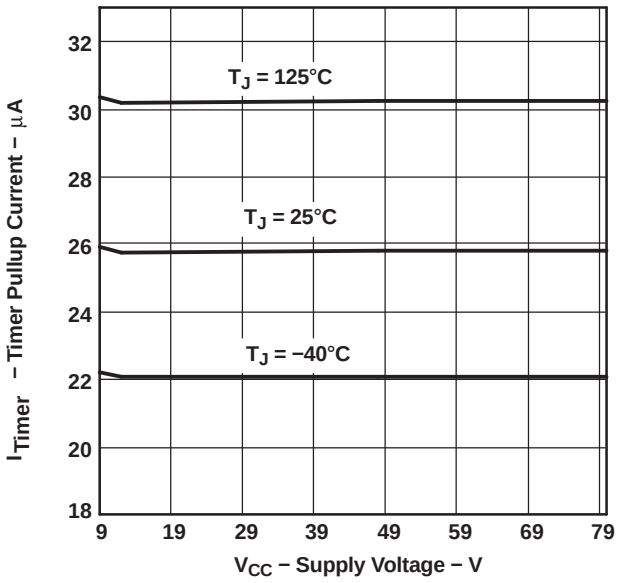


Figure 8.

TIMER CHARGE/DISCHARGE RATIO vs VCC VOLTAGE AND TEMPERATURE

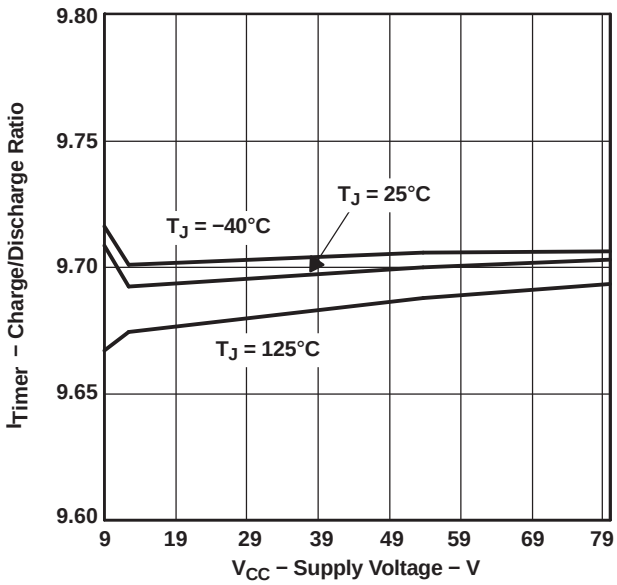


Figure 9.

EN THRESHOLD VOLTAGE (RISING) vs VCC VOLTAGE

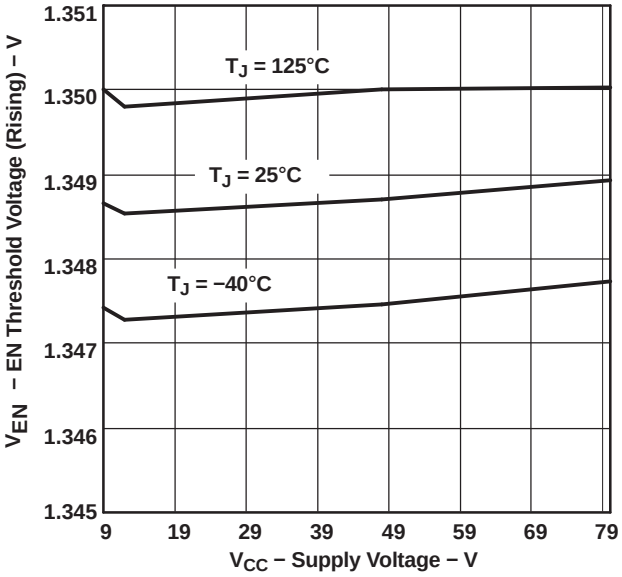


Figure 10.

EN THRESHOLD VOLTAGE (FALLING) vs VCC VOLTAGE

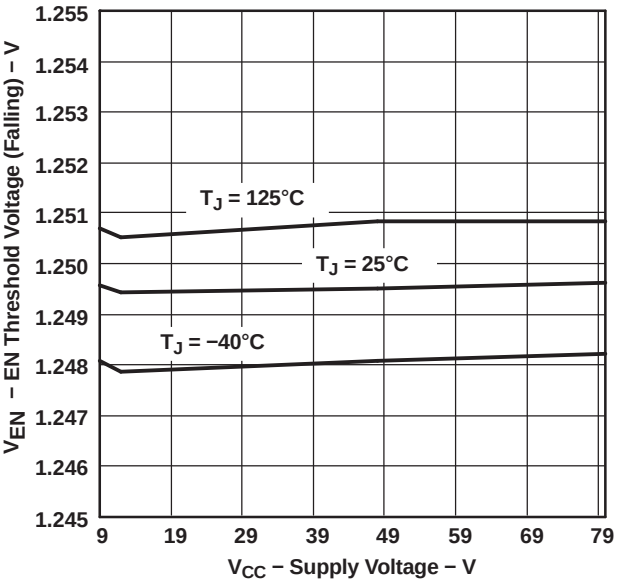


Figure 11.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_S = 3.3 V, VINP = 12 V, V_{SHUNT} = (VINP – VINM) = 0 mV, unless otherwise noted.

SHUNT MEASUREMENT INPUT OFFSET VOLTAGE PRODUCTION DISTRIBUTION

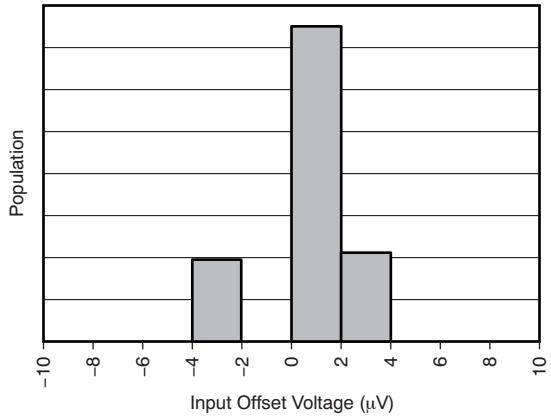


Figure 12.

SHUNT MEASUREMENT INPUT OFFSET VOLTAGE vs TEMPERATURE

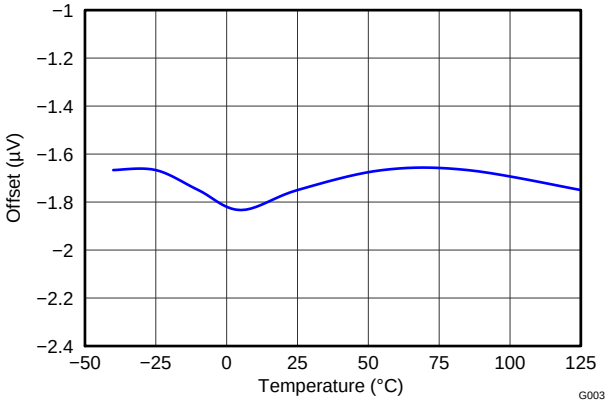


Figure 13.

SHUNT MEASUREMENT INPUT GAIN ERROR PRODUCTION DISTRIBUTION

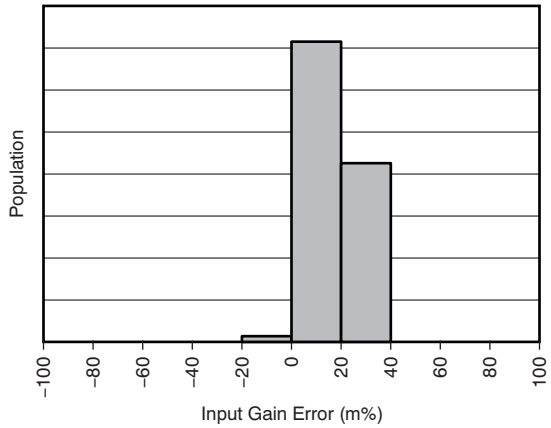


Figure 14.

SHUNT MEASUREMENT INPUT GAIN ERROR vs TEMPERATURE

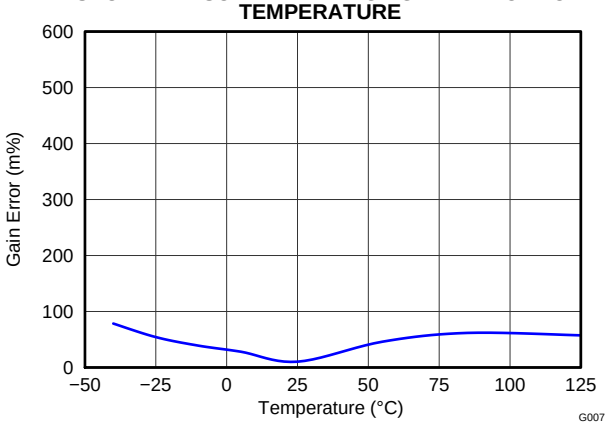


Figure 15.

SHUNT MEASUREMENT INPUT GAIN ERROR vs COMMON-MODE VOLTAGE

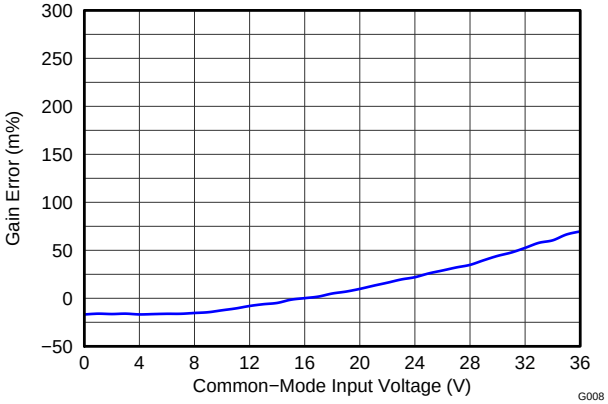


Figure 16.

SHUNT MEASUREMENT INPUT COMMON-MODE REJECTION RATIO vs TEMPERATURE

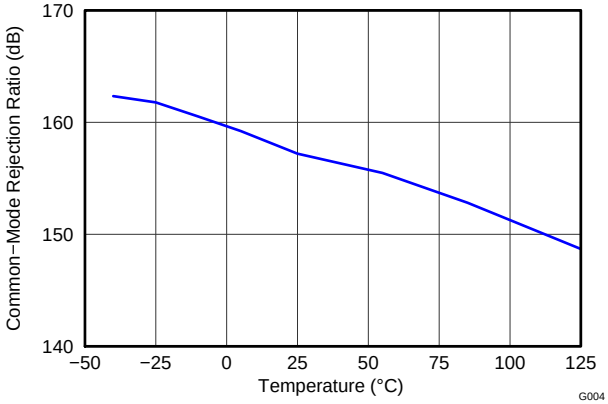


Figure 17.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_S = 3.3 V, VINP = 12 V, V_{SHUNT} = (VINP – VINM) = 0 mV, unless otherwise noted.

BUS MEASUREMENT INPUT OFFSET VOLTAGE PRODUCTION DISTRIBUTION

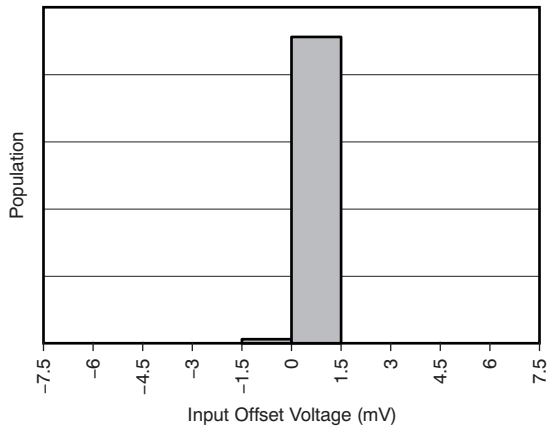


Figure 18.

BUS MEASUREMENT INPUT OFFSET VOLTAGE vs TEMPERATURE

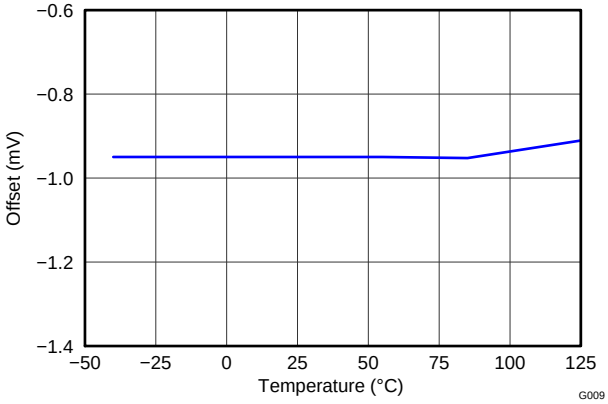


Figure 19.

BUS MEASUREMENT INPUT GAIN ERROR PRODUCTION DISTRIBUTION

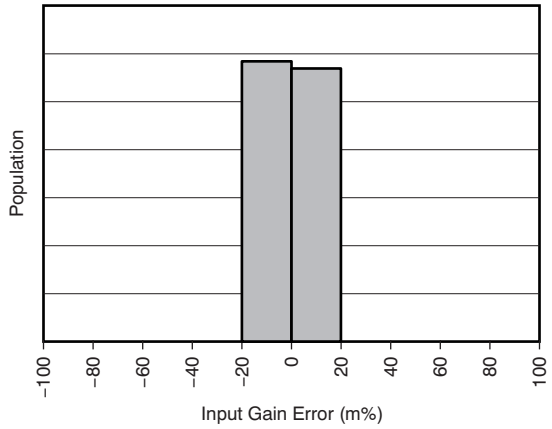


Figure 20.

BUS MEASUREMENT INPUT GAIN ERROR vs TEMPERATURE

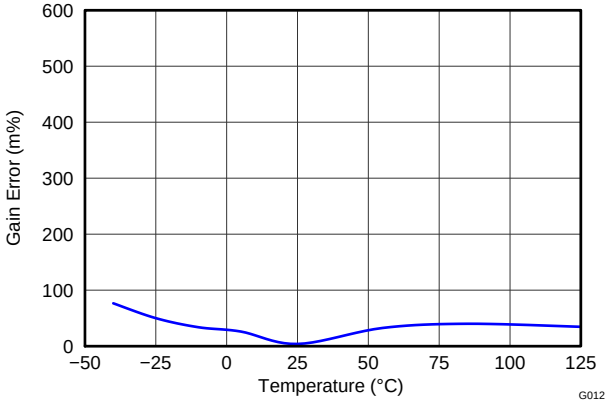


Figure 21.

VINP+VINM INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

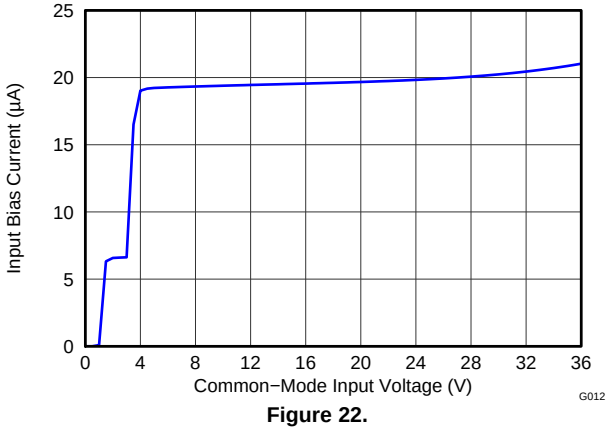


Figure 22.

VINP+VINM INPUT BIAS CURRENT vs TEMPERATURE

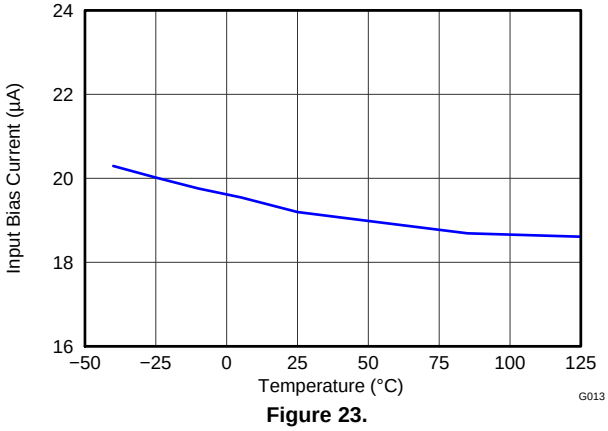


Figure 23.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_S = 3.3 V, VINP = 12 V, V_{SHUNT} = (VINP – VINM) = 0 mV, unless otherwise noted.

VINP+VINM INPUT BIAS CURRENT vs TEMPERATURE, POWER-DOWN MODE

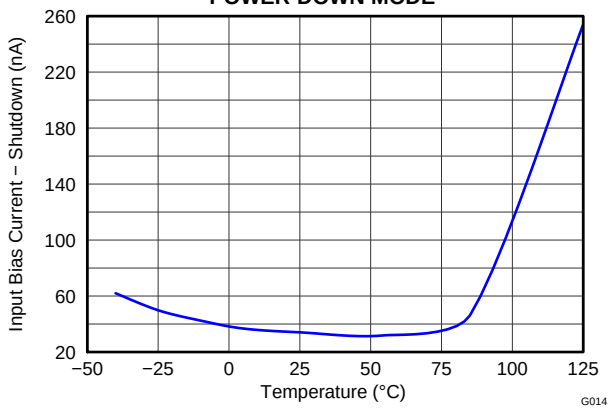


Figure 24.

SAMPLING FREQUENCY RESPONSE (POR DEFAULT SETTINGS)

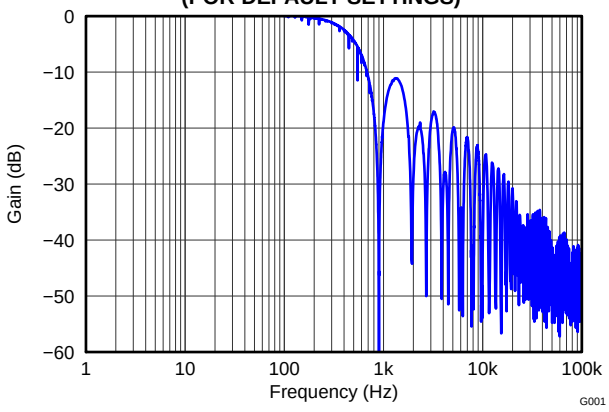


Figure 25.

ACTIVE I_{Q-VS} vs I^2C CLOCK FREQUENCY

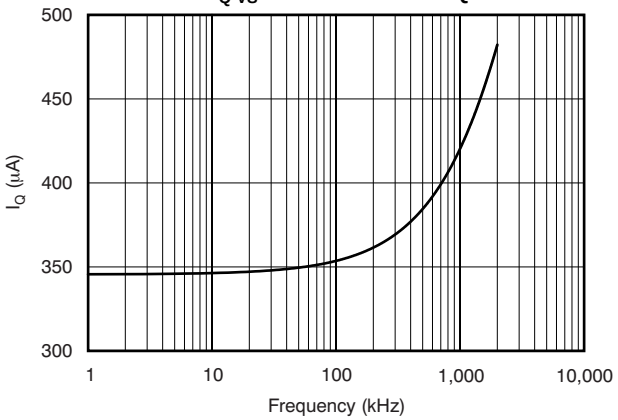


Figure 26.

ACTIVE I_{Q-VS} vs TEMPERATURE (NO I^2C CLOCK)

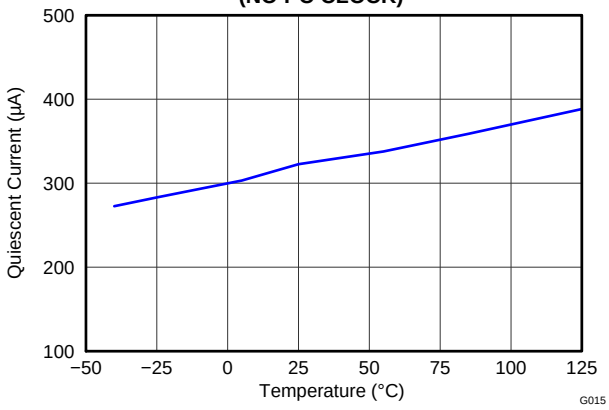


Figure 27.

SHUTDOWN I_{Q-VS} vs I^2C CLOCK FREQUENCY

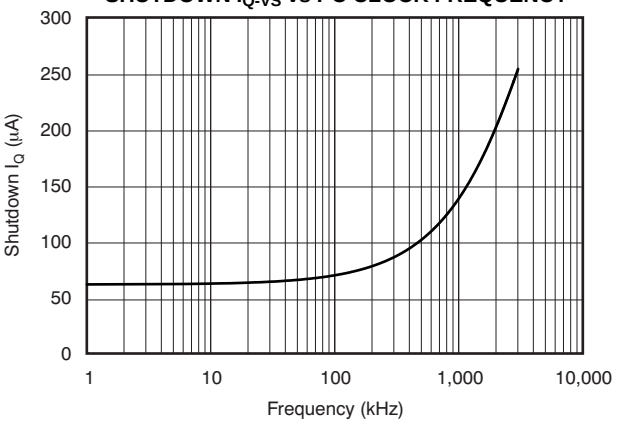


Figure 28.

SHUTDOWN I_{Q-VS} vs TEMPERATURE (NO I^2C CLOCK)

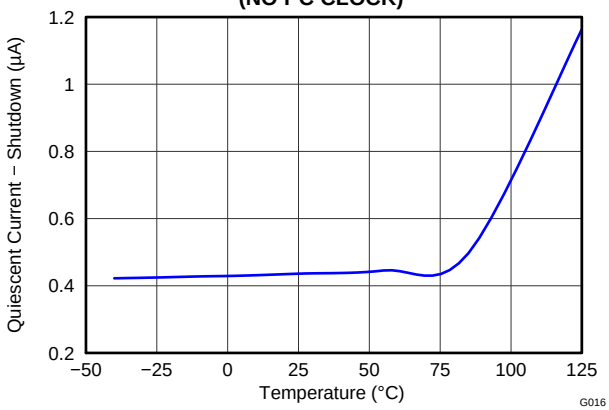


Figure 29.

HOTSWAP APPLICATION INFORMATION

Upgrading TPS2480 with TPS2482 and TPS2481 with TPS2483

The TPS2482 and TPS2483 are pin-compatible with the TPS2480 and TPS2481 with the exception that the VINP and VINM inputs are reversed in position. The TPS2482 and TPS2483 may be installed on a circuit board designed for the TPS2480/1 and operated successfully. The effect of the pin reversal will be to make the input current appear negative. This can be corrected in the interface software per the procedure discussed in Shunt Voltage Register 01h (Read-Only). This is not the only change required in the interface software as the data acquisition engine is different, requiring different configuration and calibration values.

Basic TPS2482 and TPS2483 Operation

The TPS2482 and TPS2483 provide all the features needed for a positive-voltage hotswap controller and monitor.

These features include:

1. Under-voltage lockout;
2. Adjustable (system-level) enable;
3. Turn-on inrush limit;
4. High-side gate drive for an external N-channel MOSFET;
5. MOSFET over-current and power dissipation protection;
6. Adjustable overload timeout;
7. Charge-complete indicator for downstream converter sequencing;
8. Optional automatic restart mode; and
9. Serial-bus interface to monitor voltage, current, and power to the load.

The TPS2482 and TPS2483 feature superior pass-MOSFET power-limiting protection that allows independent control of the current limit (to set maximum full-load current), power-limit and overload time (to keep the MOSFET within its SOA), and overload recovery time (to control case temperature rise). Oscilloscope waveforms from a typical 24-V application circuit, seen in Figure 30 through Figure 35, demonstrate many of the functions described above.

EN can be used as a logic-level control input or as an analog input voltage monitor as illustrated by R_{EN1}/R_{EN2} in the Simplified Application Diagram. The hysteresis associated with the internal comparator makes this a stable method of detecting a low input voltage condition and shutting off the pass-MOSFET. EN may also be tied directly to VCC to always enable the TPS2482 and TPS2483.

Board Plug-In (Figure 30)

Only the bypass capacitor charge current and small bias currents are evident when a board is first plugged in. A startup cycle is ready to take place after POR2 stabilization. The TPS2482 and TPS2483 are held inactive and GATE, PROG, TIMER, and PG are held low for less than 1 ms while internal voltages stabilize.

GATE, PROG, TIMER, and PG are released after stabilization if both the internal UVLO threshold and the external EN (enable) thresholds have been exceeded. After an RC-filter delay on EN passes, the device begins sourcing current from the GATE pin and M_1 begins to turn on while the voltage across it, measured as $V_{(SENSE–OUT)}$, and current through it, measured as $V_{(VCC–SENSE)}$, are monitored and controlled. Once V_{GS} has charged to the pass-MOSFET threshold voltage, current initially rises to the value which satisfies the power-limit engine, that is. (P_{LIM} / V_{VCC}), as seen on the trace labeled I-IN. The entire input voltage VCC is impressed across M_1 since the output load capacitor, C_O, was initially discharged.

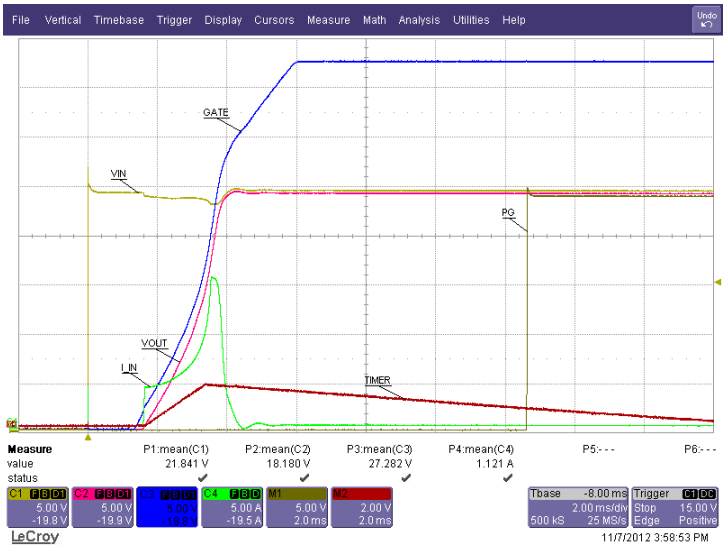


Figure 30. Basic Board Insertion

TIMER and PG Operation (Figure 30)

The TIMER pin charges C_T as long as limiting action continues, and discharges at 1/10 of the charge rate when all limiting stops (see trace labeled TMR). If the voltage on C_T reaches 4 V while limiting is still active, the pass-MOSFET is turned off and either a latch-off or restart cycle commences, depending on the controller type. The open-drain PG output provides a deglitched end-of-charge indication which is based on the voltage across the pass-MOSFET. PG is useful to prevent a downstream DC-to-DC converter from starting while C_O is still charging. PG goes active (open-drain) about 9 ms after C_O is charged. This delay allows the pass-MOSFET to fully turn on and any transient disturbances in the power circuits to settle before the converter is allowed to start up. The resistor pull-up shown on pin PG in the typical application diagram illustrates an example operation only; the actual interface network to a converter depends on the specific application.

C_T charge can appear to terminate early in some designs (usually with high-C_{RSS} MOSFETs) if operation transitions out of the power-limit mode into a gate-charge-limited mode at mid to low V_{DS} values. This can occur when I_{GATE} is insufficient to drive C_{ISS} of the MOSFET at a rate that would sustain operation in either P_{LIM} or I_{LIM}. In this situation, dV_{DS}/dt is limited by I_{GATE}/C_{RSS}.

Action of the Constant Power-Limit Engine (Figure 31)

The calculated power dissipated in the pass-MOSFET, V_{DS} x I_D, is computed under the startup conditions previously seen in Figure 30. The current of the pass-MOSFET, labeled I-IN, initially rises to the value that satisfies the constant power-limit engine; in this case it is 90 W / 24 V = 3.75A. The 90-W value is programmed into the engine by setting the PROG voltage using Equation 1. V_{DS} of the pass-MOSFET, which is measured as $V_{(SENSE-OUT)}$, decreases as C_O charges, thus allowing the pass-MOSFET drain current to increase. This is the result of the internal constant-power engine adjusting the current-limit reference to the GATE amplifier as C_O charges and V_{DS} falls. The calculated device power dissipation shown in Figure 31 is flat-topped and constant within the limitations of circuit tolerance and acquisition noise. A fixed current limit is implemented by clamping the constant power-limit engine output to 50 mV when V_{DS} is low. This protection technique can be viewed as a specialized form of foldback limiting; the benefit over a linear foldback technique is that it yields the maximum output current from a device over the full range of V_{DS} and still protects the device.

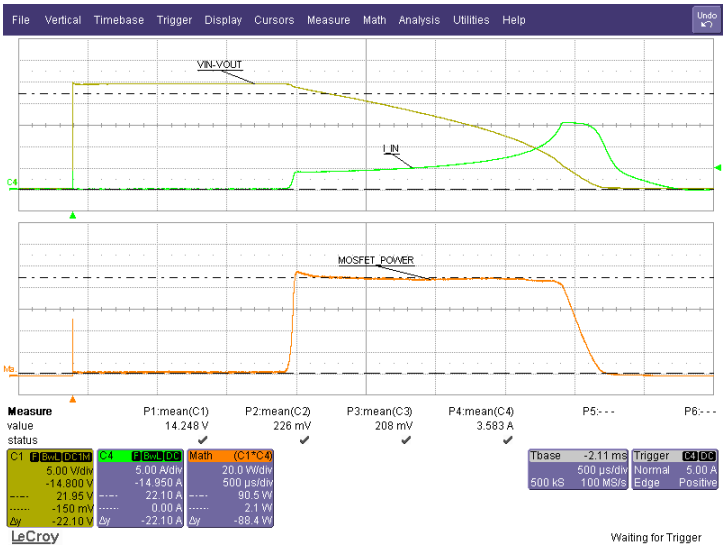


Figure 31. Computation of the Pass-MOSFET Stress During Startup

Response to a Hard Output Short (Figure 32 and Figure 33)

Figure 32 shows the short-circuit response over the full time-out interval. This interval begins when an output short-circuit is applied and ends when the pass-MOSFET is turned off. The pass-MOSFET current is actively controlled by the power-limit engine and gate amplifier circuit while the TIMER pin charges C_T to the 4-V threshold. Once this threshold is reached, the TPS2482 and TPS2483 disable and shut off the pass-MOSFET. The TPS2482 remains latched off until either the VCC voltage drops below the UVLO threshold or EN is cycled through the false (low) state. The TPS2483 will automatically retry C_O charging (attempt a restart) after going through a 16-count time-out cycle.

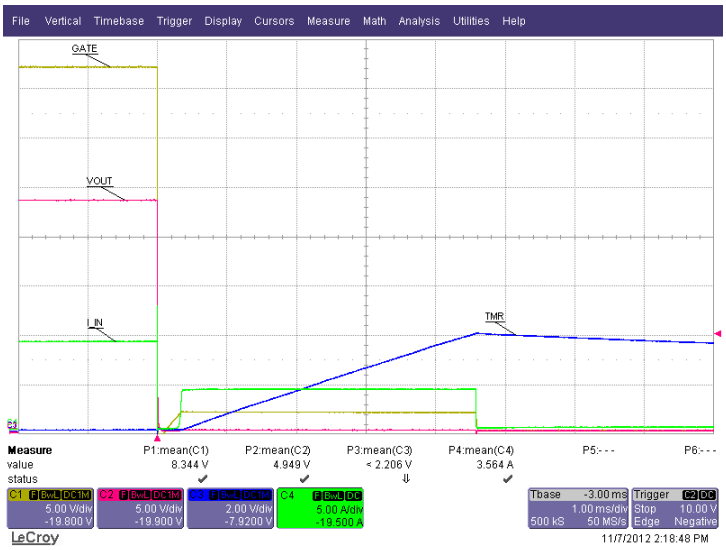


Figure 32. Current Limit Overview

The TPS2482 and TPS2483 respond rapidly to the short-circuit as seen in Figure 33 (horizontal time base is 1 µs/div). The falling OUT voltage is the result of the pass-MOSFET and C_O currents through the short-circuit impedance. The internal GATE diode clamp causes the GATE voltage to follow the output limits the negative V_{GS} to 1~2 V. The rapidly rising fault current (not shown) overdrives the GATE amplifier causing it to overshoot and rapidly turn the pass-MOSFET off by sinking current to ground. The pass-MOSFET eventually turns back on as the GATE amplifier recovers and settles to an equilibrium operating point determined by the power-limit engine.

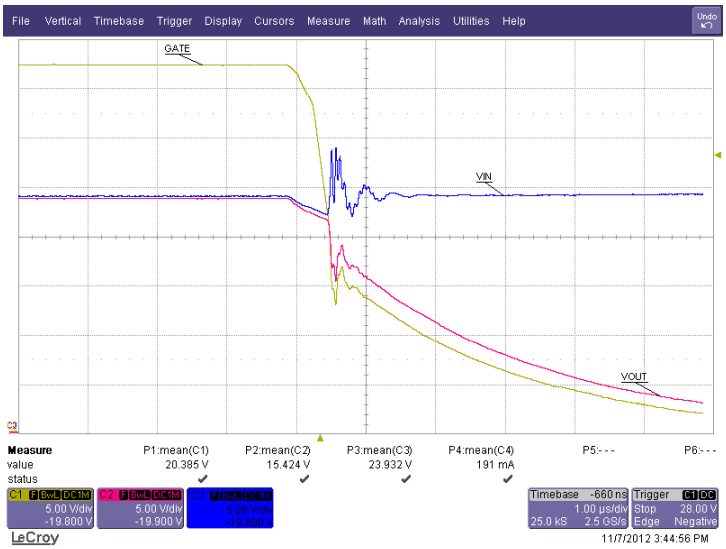


Figure 33. Current Limit Onset

Minimal input voltage overshoot appears in Figure 33 because a local 100-µF input bypass capacitor and very short input leads were used. In a typical application, as the input current abruptly drops, the input voltage may overshoot significantly due to stored energy in the input distribution inductance. The exact waveforms seen in an application depend upon many factors including parasitics of the voltage distribution, circuit layout, and the nature of the overload or short-circuit itself.

Automatic Retry on Fault (Figure 34 and Figure 35)

The TPS2483 automatically initiates a delayed restart attempt after a fault has caused it to turn off the pass-MOSFET. Internal control circuits use C_T to count 16 charge/discharge cycles before re-enabling the pass-MOSFET. This sequence repeats if the fault persists. The TIMER has a 10:1 charge-to-discharge current ratio, and uses a 1-V lower threshold. TPS2483 will attempt to restart indefinitely, until a restart is successful or input power is removed. The fault-retry duty-cycle specification, D_{RETRY}, quantifies this behavior. This small duty cycle often reduces the average short-circuit power dissipation in the MOSFET to levels associated with normal operation and reduces the need for additional thermal measures or derating.

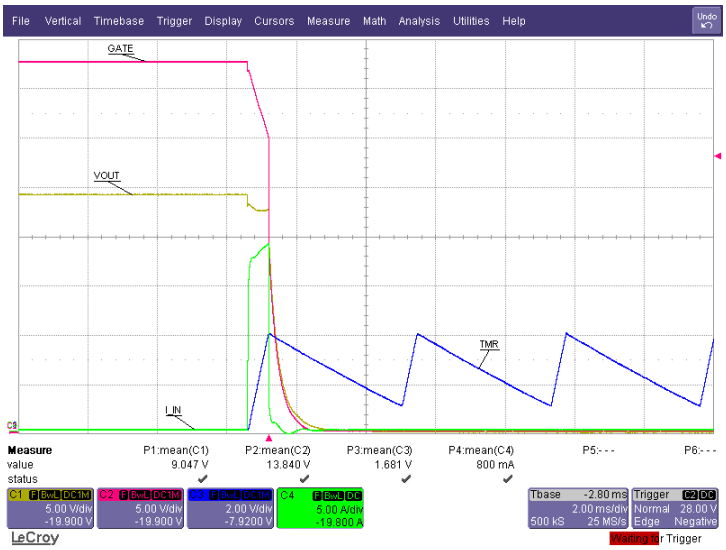


Figure 34. TPS2483 Retry-Cycle Timing Detail

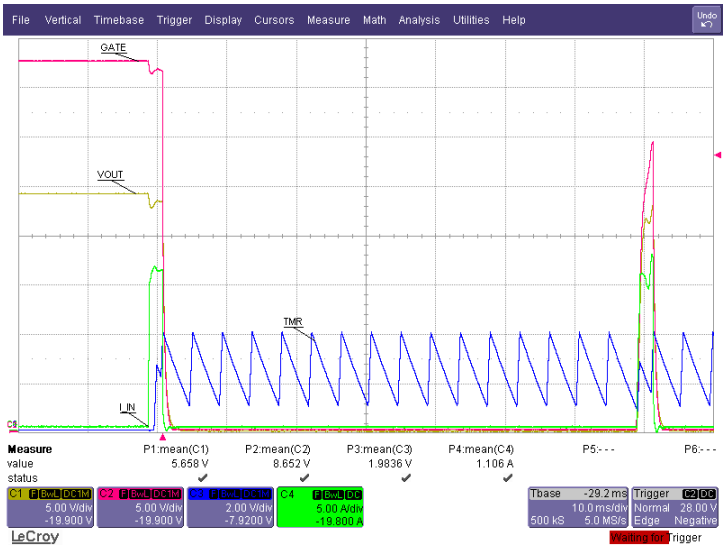


Figure 35. TPS2483 Full Retry-Cycle Timing

24-V, 10-A Application Design Example

The following example illustrates the design and component selection process for a 24-V, 10-A hotswap application. Figure 36 shows an example schematic for the TPS2482 and TPS2483 application.

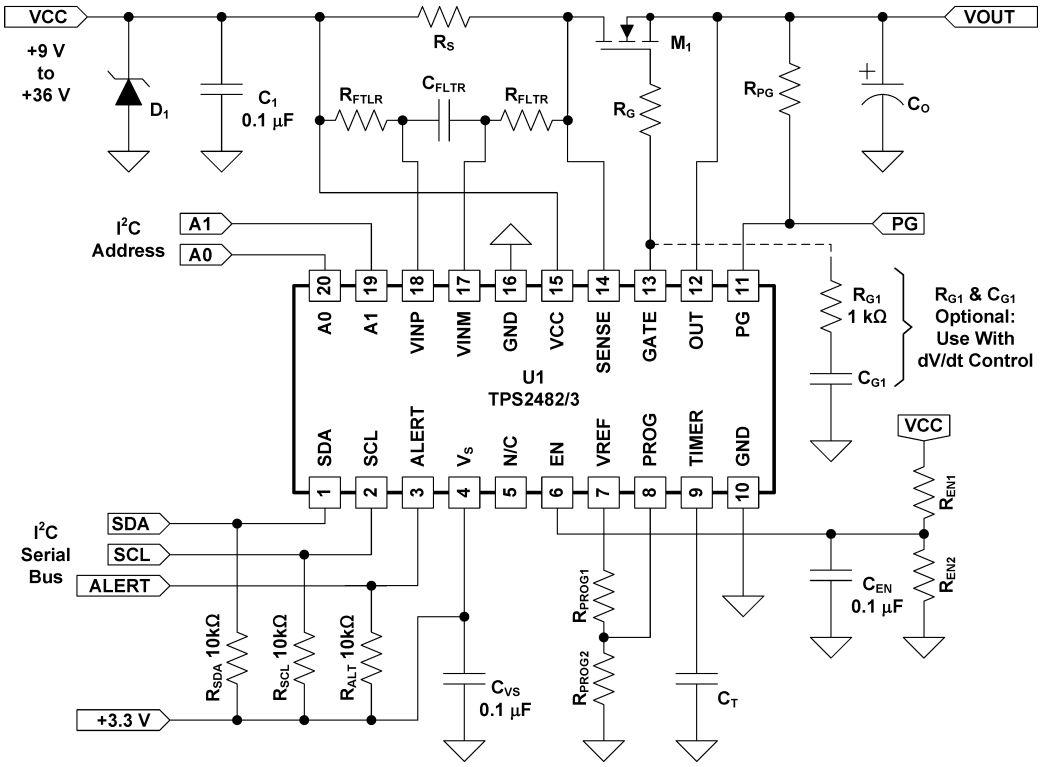


Figure 36. TPS2482 and TPS2483 Example Schematic

1. Choose Shunt Resistor R_S

The following equation includes a margin factor of 1.2 (20%) to account for current limit threshold (V_{CL}) and R_S tolerances along with some additional margin. I_{MAX} is the maximum continuous load current.

$$R_S = \frac{V_{SENSE}}{1.2 \times I_{MAX}} = \frac{50mV}{1.2 \times 10A} = 4.17\ m\Omega \quad (4)$$

- Where practical, select a standard value; choose R_S = 4 mΩ.

$$P_{R_S(MAX)} = I^2_{MAX} \times R_S = (10A)^2 \times 3m\Omega = 0.3W \quad (5)$$

Pick a sense resistor with a power rating of 0.5 W or 1 W to allow some margin. Ensure sufficient heatsinking.

2. Choose Pass-MOSFET, M_1

Select the V_{DS}-rating of M_1 allowing for peak input voltage, including transients and ringing. Then select an operating-$R_{DS(on)}$, device package, and cooling method to control the steady-state operating temperature. Most manufacturers list $R_{DS(on)(MAX)}$ at 25°C and provide an adjustment curve from which on-resistance at other temperatures can be derived. The next equation can be used to estimate desired $R_{DS(on)(MAX)}$ at the maximum operating junction temperature of $T_{J(MAX1)}$ (usually 50°C below absolute maximum). $T_{A(MAX)}$ is the maximum expected ambient temperature.

$$T_{J1(MAX)} = 100C,\ T_{A(MAX)} = 60C,\ R_{\theta JA} = 31\frac{C}{W},\ I_{(MAX)} = 10A$$

$$R_{DS(ON)} < \frac{T_{J1(MAX)} - T_{A(MAX)}}{R_{\theta JA} \times I^2_{MAX}} = \frac{100C - 60C}{31\frac{C}{W} \times (10A)^2} = 12.9\ m\Omega \quad (6)$$

The junction-to-ambient thermal resistance, $R_{\theta JA}$, depends upon the package style chosen and the details of heat-sinking and cooling including the PCB. Actual "in-system" temperature measurements will be required to validate heat-sinking and cooling performance. Based on the above requirements CSD18503Q5A was chosen for M_1. It has a V_{DS} rating of 40 V and $R_{DS(ON)(MAX)}$ of 6.5 mΩ at 100°C meeting both the voltage and $R_{DS(ON)}$ requirements.

3. Choose the Power Limit, P_{LIM}, and the PROG Resistors, R_{PROG1} and R_{PROG2}

M_1 dissipates large amounts of power during the brief power-up or output short-circuit events. Power limit, P_{LIM} should be set to prevent M_1 junction temperature from exceeding a short-term maximum temperature, $T_{J2(MAX)}$. It is recommended to set $T_{J2(MAX)}$ 25°C below the maximum junction temperature specified by the manufacturer to allow some margin.

$$T_{J(MAX2)} = 125C, T_{A(MAX)} = 60C, R_{\theta CA} = 30\frac{C}{W}, R_{\theta JC} = 1\frac{C}{W}, Z_{\theta JC} = 0.3, R_{DS(ON)(MAX)} = 6.45m\Omega$$

$$P_{LIM} = \frac{0.7 \times (T_{J(MAX2)} - R_{\theta CA} \times I^2_{MAX} \times R_{DSON(MAX)} - T_{A(MAX)})}{R_{\theta JC} \times Z_{\theta JC}} = 106.5W \quad (7)$$

where, $R_{\theta CA}$ is M_1 junction-to-case thermal resistance (computed by subtracting $R_{\theta JC}$ from $R_{\theta JA}$), $Z_{\theta JC}$ is the normalized thermal impedance, $R_{DS(ON)(MAX)}$ is the channel resistance at the maximum operating temperature, and the factor of 0.7 accounts for the tolerance of the constant power engine. For CSD18503Q5A, $Z_{\theta JC}$ of 0.3 can be used for fault times below 10 ms. This assumption will be verified once the timer capacitor is chosen.

The maximum power limit obtainable from the constant power-limit engine, $P_{LIM(MAX)}$, and nominal output power $P_{OUT(NOM)}$ for this example system are calculated with the following equations:

$$V_{REF} = 4V, R_S = 4m\Omega, V_{OUT(NOM)} = 24V, I_{LIMIT(NOM)} = 12.5A$$

$$P_{LIM(MAX)} = \frac{1V \times V_{REF}}{2 \times R_S} = 500W$$

$$P_{OUT(NOM)} = V_{OUT(NOM)} \times I_{LIMIT(NOM)} = 24V \times 12.5A = 300W \quad (8)$$

The PROG resistors should be chosen using the smallest of P_{LIM}, $P_{LIM(MAX)}$, or $P_{OUT(NOM)}$ values.

Choose R_{PROG2} = 20kΩ. Choose R_{PROG1} as shown in Equation 9.

$$P_{LIM(ACT)} = 106.5W, R_S = 4m\Omega,\ R_{PROG2} = 20k\Omega$$

$$V_{PROG} = \frac{2 \times P_{LIM(ACT)} \times R_S}{1V} = \frac{2 \times 106.5W \times 4m\Omega}{1V} = 0.852V$$

$$R_{PROG1} = R_{PROG2} \times \left(\frac{V_{REF}}{V_{PROG}} - 1\right) = 73.9k\Omega \quad (9)$$

- Choose R_{PROG1} = 73.2 kΩ, for a standard value.

The current and power limit curve for this configuration is shown in Figure 37.

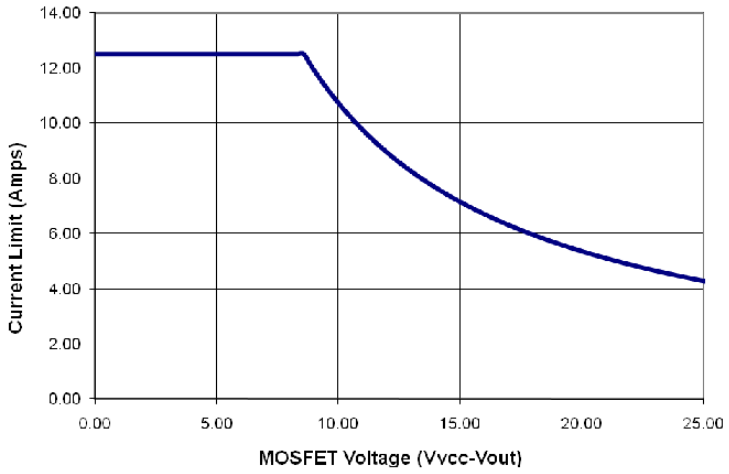


Figure 37. Design Example Current and Power Limit Curve

4. Choose the Timer Capacitor, C_T

The turn on time t_{ON}, represents the time it takes the circuit to charge up the output capacitance C_O. C_T programs the fault time and should be chosen so that the fault timer does not terminate prior to completion of start up. Assuming that all of the current is going towards charging C_O, t_{ON} can be computed as follows:

$$For\ P_{LIM(ACT)} < V_{VCC(MAX)} \times I_{LIMIT(NOM)}: t_{ON} = \frac{C_O \times P_{LIM(ACT)}}{2 \times I^2_{LIMIT(NOM)}} + \frac{C_O \times V^2_{VCC(MAX)}}{2 \times P_{LIM(ACT)}}$$

$$For\ P_{LIM(ACT)} \geq V_{VCC(MAX)} \times I_{LIMIT(NOM)}: t_{ON} = \frac{C_O \times V_{VCC(MAX)}}{I_{LIMIT(NOM)}} \quad (10)$$

C_T should be set to accommodate the worst case on time $t_{ON(MAX)}$, which can be computed as follows:

$$P_{LIM(MIN)} = 0.7 \times P_{LIM(ACT)} = 75.1W,\ I_{LIMIT(MIN)} = 0.9 \times I_{LIMIT(ACT)} = 11.25A,$$

$$V_{VCC(MAX)} = 26V,\ C_O = 330\mu F$$

$$t_{ON(MAX)} = \frac{C_{O,MAX} \times P_{LIM(MIN)}}{2 \times I^2_{LIMIT(MIN)}} + \frac{C_{O,MAX} \times V^2_{VCC(MAX)}}{2 \times P_{LIM(MIN)}}$$

$$= \frac{330\mu F \times 75.1W}{2 \times (11.25A)^2} + \frac{C330\mu F \times (26V)^2}{2 \times 75.1W} = 1.58ms \quad (11)$$

The next equation allows C_T to be selected assuming that only C_O draws current during startup. Account for the TPS2482 and TPS2483 timer current source and capacitor tolerances.

$$I_{SOURCE(MAX)} = 34\mu A, V_{TMR\text{-}TH(MIN)} = 3.9V,\ C_{O\text{-}TOL} = 20\%, C_{T\text{-}TOL} = 10\%$$

$$C_T = \frac{I_{SOURCE(MAX)}}{V_{TMR\text{-}TH(MIN)}} \times t_{ON(MAX)} \times (1 + C_{O\text{-}TOL} + C_{T\text{-}TOL})$$

$$C_T = \frac{34\mu A}{3.9V} \times 1.58ms \times (1 + 0.2 + 0.1) = 17.9nF \quad (12)$$

- Choose C_T = 0.022 µF standard value.

Once C_T is selected, it is prudent to back-calculate the longest fault-time which M_1 must endure to validate that it remains properly within its SOA during a limiting event. If not, some previously-chosen system parameter(s) must be adjusted until M_1 operates safely for both $t_{ON(max)}$ and $t_{FAULT(max)}$, which can be computed as follows.

$$I_{SOURCE(MIN)} = 15\underline{m}A, V_{TMR\text{-}TH(MAX)} = 4.1V, C_{T\text{-}TOL} = 10\%$$

$$t_{FAULT(MAX)} = \frac{V_{TMR\text{-}TH(MAX)} \times C_T}{I_{SOURCE(MIN)}} \times (1 + C_{T\text{-}TOL}) = 6.6ms \quad (13)$$

Note that $t_{FAULT(MAX)}$ is under 10 ms, supporting the use of $Z_{\theta JC}$ = 0.3.

5. Choose the Turn-On Voltage, V_{ON}, and the EN Resistors, R_{EN1} and R_{EN2}

When the EN pin is used as an analog control, the desired input turn-on voltage, V_{ON}, can be used to select the EN resistors. The size of R_{EN1} and R_{EN2} need to be reasonable to avoid inaccuracy due to leakage current. First choose R_{EN2} = 10 kΩ, and compute R_{EN2} as follows:

$$V_{ON} = 18V,\ V_{EN\_H} = 1.35V, V_{EN\_L} = 1.25V, R_{EN2} = 10k\Omega$$

$$R_{EN1} = R_{EN2} \times \left(\frac{V_{ON}}{V_{EN\_H}} - 1\right) = 123.33k\Omega \quad (14)$$

- Choose R_{EN1} = 124 kΩ standard value.

The actual turn-on and turn-off voltages, V_{ON} and V_{OFF}, can be calculated as follows:

$$V_{ON(MAX)} = V_{EN\_H} \times \frac{R_{EN1} + R_{EN2}}{R_{EN2}} = 18.09V$$

$$V_{OFF(MIN)} = V_{EN\_L} \times \frac{R_{EN1} + R_{EN2}}{R_{EN2}} = 16.75V \quad (15)$$

Miscellaneous Design Considerations

The serial bus will require pullup resistors (R_{SCL}, R_{SDA}, R_{ALT}). These are placed at the end of the bus. Typical values are 10 kΩ to a 3.3-V supply.

C_{VS} must be placed adjacent to the TPS2482 and TPS2483 to bypass noise at the V_S input. 0.1 µF is a good choice.

C_1 provides a local source of bias currents and aids in controlling the dV/dt and overshoot on VCC. The size of C_1 might be controlled by inrush energy considerations during board plug-in.

PG and R_{PG} are not necessary for TPS2482 and TPS2483 operation. However, the PG output can be used to minimize loading from downstream DC/DC circuits during inrush. R_{PG} serves as a placeholder for some type of interface to those downstream circuits.

D_1 may be required for some systems. See Input and Output Transient Protection below.

Note: In some cases, start-up may transition out of power-limited and current-limited operating modes before C_O is fully charged, and C_T begins to discharge as depicted in Figure 30. In such situations, V_{GS} of the pass-MOSFET is held nearly constant by the output dV/dt and C_O charging continues due to the high transconductance of the MOSFET. The circuit behaves like a source-follower, but the remaining time to fully charge C_O is dependent on variable MOSFET parameters. The actual turn-on time used to determine C_T (in Equation 12) may be longer than the time calculated by Equation 10. Prototype testing is necessary to identify this situation and validate the proper choice for C_T.

Alternative Inrush Designs

Gate Capacitor (dV/dt) Control

The TPS2482 and TPS2483 can be configured to provide a controlled linear dV_{OUT}/dt turn-on characteristic. The load-capacitor charging current, I_{CHARGE}, is controlled by an R-C network (R_{G1} - C_{G1}) from the GATE terminal to ground. M_1 operates as a source follower (which follows the gate voltage) in this implementation. Choose a dV/dt-controlled charge time, t_{ON_G1}, based on the load capacitor, C_O, input voltage VCC, and desired charge current. When power-limiting is used ($V_{PROG} < V_{VREF}$), choose I_{CHARGE} to be less than P_{LIM} / V_{VCC} to prevent the fault timer from starting. The fault timer starts only if power limit or current limit is invoked. It is assumed there is no downstream load current during this charge-up time.

$$t_{ON\_G1} = \frac{C_O \times V_{VCC}}{I_{CHARGE}} \tag{16}$$

Use the following equation to select the external gate capacitance, C_G. As shown in Figure 36, an R_{G1} of about 1 kΩ should be used in series with C_G.

$$C_G = \left(I_{GATE} \times \frac{\Delta t}{V_{VCC}} \right) - C_{RS} \tag{17}$$

I_{GATE} is the nominal gate charge current. This equation assumes that the MOSFET C_{GD} is the controlling element as the gate and output voltage rise. Since, C_{GD} is non-linear with applied V_{GD} an averaged estimate (C_{RS}) should be used when computing using C_G. Divide the MOSFET Q_{GD} by V_{IN} to obtain C_{RS}. Since neither power nor current-limit faults are invoked during turn on, C_T can be chosen for fast transient turn off response using the M1 SOA curve. Choose the single pulse time conservatively from the M1 SOA curve using maximum operating voltage and maximum trip current.

High Voltage Application Example

The TPS2482 and TPS2483 can be used to monitor current from a voltage source greater than 36 V by using a "high-side" Op-Amp circuit, as shown in Figure 38. This circuit translates the high-side current shunt voltage to a ground-referenced signal within the monitor section's operational rating. Voltage and power monitoring are lost in this configuration. Except for the high-side translation circuit, the system design and component selection process is the same as for the 24-V, 10-A Application Design Example.

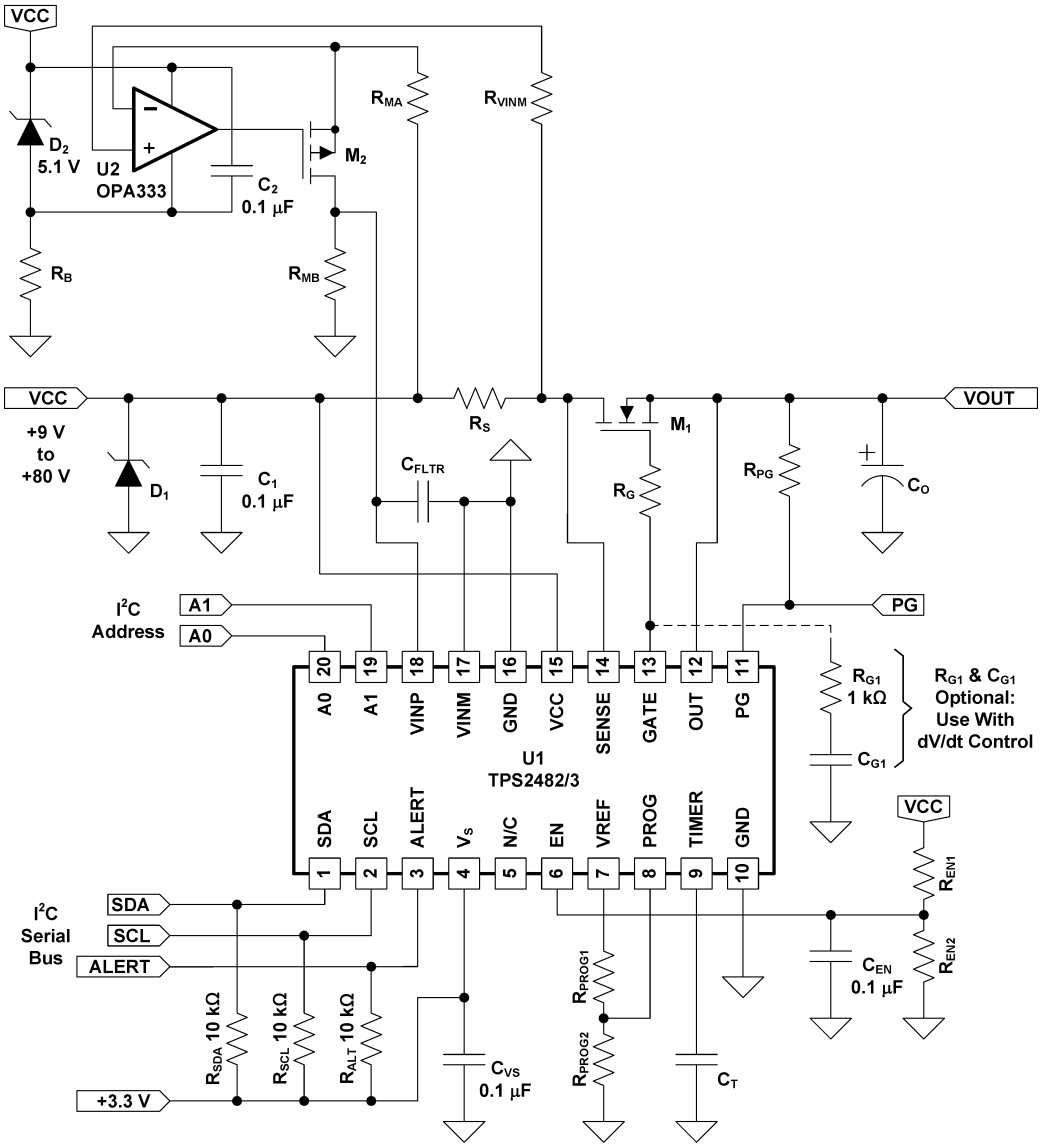


Figure 38. TPS2482 and TPS2483 High Voltage Application Diagram

The basic operating principle of U_2, M_2, R_{MA}, and R_{MB} is to mirror the voltage seen across R_S from a VCC-referenced voltage to a GND-referenced voltage. As load current flows through R_S, the voltage at the (+) input of U_2 decreases and U_2 drives M_2 to cause its source voltage at the (-) input to follow the (+) input. Ideally then, the voltage across R_{MA} mirrors the voltage drop of R_S. Current flow though R_{MB} will mirror current through R_{MA}, and if $R_{MB} = R_{MA}$, then the shunt voltage across R_S is mirrored at VINP.

Since only small voltages will be across R_{MA} and R_{MB}, their nominal values should be fairly low to avoid input bias-current effects (I_{VINP}). While discrete resistors may provide acceptable performance, well-matched network-type resistors with temperature coefficient tracking for R_{MA} and R_{MB} will provide the most accurate solution.

U_2 should be a high-quality, low-drift operational amplifier, such as the OPA333, which provides low input voltage offset and very low drift over time and temperature. U_2 is referenced to VCC through D_2 and R_B and its output can operate from rail to rail. P-channel MOSFET M_2 can be a small-signal device rated for the maximum input voltage, such as Si2325DS or similar.

Additional Design Considerations

Use of PG Output

Use the PG pin to control and sequence a downstream DC/DC converter. If this is not done, a long time delay may be needed on the converter to allow C_O to fully charge before the converter starts.

Output Clamp Diode

Inductive loads on the output may drive the OUT pin below GND when the circuit is unplugged or during sudden current limit. Protect the OUT pin from excessive negative voltage excursions with a clamp diode from OUT to GND. The diode must be sized to carry the peak fault current .

Gate Clamp Diode

The TPS2482 and TPS2483 have a relatively well-regulated gate voltage of 12 V to 16 V, even at low supply voltages. If V_{GS} of the pass-MOSFET is rated below 20 V, an external Zener clamp-diode, such as a BZX84C7V5, is recommended from gate to source.

High Gate Capacitance Applications

An external gate clamp Zener diode is recommended if the total gate capacitance of M_1 exceeds 4000 pF, to aid in controlling the MOSFET peak V_{GS} if the source is abruptly pulled to ground. without the external clamp, excess V_{GS} voltage may occur as a result of the C_{DG}/C_{GS} divider in M_1. When gate-capacitor dV/dt control is used, a 1-kΩ resistor in series with C_{G1} is recommended, as shown in Figure 36. If the series R-C combination is used for MOSFETs with C_{ISS} less than 3000 pF, then an external Zener diode is usually not required.

Input and Output Transient Protection

Hotswap systems experience positive-going transients on their input during hotswap or rapid turn-off events due to inductance in the input circuit. These same systems experience negative-going transients on the output during rapid turn-off due to inductance in the output circuit. The location of transients experienced by the TPS2482 and TPS2483 will depend on the application; one example is a hotswap input protector, and a second example is short circuit protection for an output cable.

When used as an input hotswap protector, input voltage overshoots are a primary concern. Absolute Maximum Voltage (V_{ABS}) ratings of the VINM and VINP pins will control the maximum operating voltage and the choice of transient protection. The use of a transient voltage suppressor (TVS) across the input power line is recommended to sink the over-current. Consider the SMCJ28A TVS as an example. The breakdown voltage is 31.1 V to 34.4 V at 1 mA, and its clamp voltage is 45 V at 33.1 A. Considering the worst case, the TVS can be modeled as an ideal 34.4 V diode in series with a 0.32 Ω resistor. The model indicates the SMCJ28A will conduct at least 17.5 A of current at 40 V. This device can provide sufficient protection from an inductive current spike that is less than 17.5 A. Overall, the magnitude of these spikes is very system dependent and should be evaluated in a real system. As a rule of thumb, pick a TVS to support a current spike twice the operating current. Then test the circuit in a fully loaded system, observe the maximum transient voltage (V_{MAX}), and ensure that the difference between V_{MAX} and V_{ABS} is at least 3 volts to account for variation in the break down voltage of the TVS. If this difference is too small, pick a TVS with a larger die area or use two in parallel.

When the TPS2482 and TPS2483 are used as an output protector with sufficient input capacitance these transient spikes are not as big of a concern. In this case, a 4 V margin between the VINP and VINM operating voltage and absolute max should be sufficient.

An output voltage clamp to GND may be required to limit negative transients if the local output capacitance does not provide adequate control. An example of this is a system with significant output bus inductance and little local capacitance. In this case, select a schottky diode with low forward voltage drop at the anticipated current during an output short-circuit shut-down event.

Output Short-Circuit Measurements

Repeatable short-circuit testing results are difficult to obtain. The many details of source bypassing, input leads, circuit layout and component selection, output shorting method, relative location of the short-circuit, and instrumentation all contribute to varying results. The actual short-circuit itself exhibits a certain degree of randomness as it microscopically bounces and arcs. Care in test configuration and methods must be used to obtain realistic results. Do not expect to see waveforms exactly like those in the data sheet since every setup differs.

Applications Using the Retry Feature (TPS2483)

Applications using the retry feature may want to estimate fault retry time. The TPS2483 will retry (enable M_1 to attempt turn-on to restart the load) once for every 16 TIMER charge/discharge cycles (1 segment between 0 V and 1 V, and 16 cycles from 1 V to 4 V back to 1V). However, in the case of an immediate fault upon each retry attempt, the minimum retry interval is found by Equation 18, when the voltage on C_T does not fall appreciably below 1V at the end of each retry interval. Although most retry intervals are likely to be slightly longer, using this retry equation in thermal analysis will help achieve conservative results.

$$t_{RETRY} = C_T \times \left[16 \times \left(V_{TMRHI} - V_{TMRLO} \right) \times \left(\frac{1}{I_{SOURCE}} + \frac{1}{I_{SINK}} \right) \right] \quad (18)$$

$$t_{RETRY} = C_T \times 21.12 M\Omega \quad (19)$$

NOTE

Equation 19 is simplified - assumes no error, nominal conditions, and immediate fault on retry. Resistance shown is an effective mathematical value, not a true resistance.

PCB Layout Considerations

Good layout practice arranges the power devices D_1, R_S, M_1, and C_O so that power flows in a sequential, linear fashion. A ground plane under the positive current path and the TPS2482 and TPS2483 are desirable. The TPS2482 and TPS2483 should be placed close to the sense resistor and MOSFET, using Kelvin-type connections to achieve accurate voltage sensing across R_S. A low-impedance GND connection is required because the TPS2482 and TPS2483 can momentarily sink current greater than 100 mA from the gate of M_1. The GATE amplifier has high bandwidth while active, so keep the GATE trace-length short. The PROG, TIMER, and EN pins have high input impedances, therefore keep their input leads short. Oversize power traces and power-device connections to assure low voltage drop and good thermal performance.

MONITORING APPLICATION INFORMATION

The TPS2482 and TPS2483 incorporate a digital monitor with a serial-bus interface compatible with I^2C and SMBus. It provides digital current, voltage, and power readings necessary for accurate decision-making in precisely-controlled systems. Programmable registers allow flexible configuration for measurement resolution as well as continuous-versus-triggered operation. Detailed register information appears at the end of this data sheet, beginning with Table 3. See the Register Block Diagram for a high-level overview of the TPS2482 and TPS2483 monitoring section.

Each data register contains a value stored as a binary number (often abbreviated in the hexadecimal format in the text) which represents the magnitude of the respective register measurement or calculation. Each of these registers also has a corresponding unit weighting for the least significant bit (LSB) of the respective register, which is used to scale that register's decimal equivalent value to the actual real-world magnitude in the units for that parameter. The Shunt Voltage Register and the Bus Voltage Register have fixed internal LSB-weights of 2.5 µV/bit and 1.25 mV/bit, respectively. The Current Register's LSB-weight is determined using the process discussed in PROGRAMMING THE TPS2482 and TPS2483 MONITOR SECTION. The Power Register's LSB-weight is internally determined based on the Current Register's LSB-weight.

Reading a register via the serial-bus for a particular parameter of interest returns the value stored in that register. Multiplying the register's decimal value by its corresponding LSB-weight yields the actual magnitude of that register's measured or calculated parameter.

BASIC ADC FUNCTIONS

The TPS2482 and TPS2483 monitoring section performs two measurements on the input power-supply bus of interest. The load current that flows through a shunt resistor develops a shunt voltage that is measured at the VINP and VINM pins. The shunt resistor is used by both the hotswap and monitoring sections. The device also measures the input bus voltage at the VINM input with respect to ground.

The monitoring section is typically powered by a separate power supply that can range from 2.7 V to 5.5 V. The input bus can be monitored over a range of 0 V to 36 V. It is important to note here that based on the fixed 1.25-mV LSB for the Bus Voltage Register, a full-scale register would result in a value of 40.96 V. **The actual voltage that is applied to the VINP and VINM pins of the TPS2482 and TPS2483 should not exceed 36 V.** There are no special considerations for power-supply sequencing because the common-mode input range and power-supply voltage are independent of each other; therefore, the bus voltage can be present with the supply voltage off, and vice-versa.

As noted, the TPS2482 and TPS2483 take two measurements, shunt voltage and bus voltage. It then converts the shunt measurement to current based on the Calibration Register value, and thereafter calculates power. Refer to the Configure/Measure/Calculate Example section for additional information on programming the Calibration Register.

Monitoring can operate in one of two conversion modes, continuous or triggered, which determine how the ADC proceeds following a measurement conversion. When the TPS2482 and TPS2483 are in the normal continuous operating mode (that is, MODE bits of the Configuration Register are set to '111'), it continuously converts a shunt voltage reading followed by a bus voltage reading. After each shunt voltage reading, the current value is calculated (based on Equation 22). This current value is then used to calculate the power result (using Equation 23). These values are subsequently stored in an accumulator, and the measurement/calculation sequence repeats until the number of averaging samples set in the Configuration Register is reached. Following every sequence, the present set of values measured and calculated are appended to previously collected values. Once all of the averaging has been completed, the final values for shunt voltage, bus voltage, current, and power are updated in the corresponding registers that can then be read. These values remain in the data output registers until they are replaced by the next fully-averaged conversion results. Reading the data output registers does not affect a conversion in progress.

The Mode control in the Configuration Register also permits selecting modes to convert only the shunt voltage or only the bus voltage in order to allow the user to configure the monitoring function to fit the specific application requirements.

All current and power calculations are performed in the background and do not contribute to conversion time.

To operate in triggered mode, writing any of the triggered-convert modes into the Configuration Register (that is, MODE bits of the Configuration Register are set to ‘001’, ‘010’, or ‘011’) triggers a single-shot conversion. This action produces a single set of measurements; thus, to trigger another single-shot conversion, the Configuration Register must be written to a subsequent time, even if the mode does not change.

In addition to the two operating modes (continuous and triggered), the TPS2482 and TPS2483 also have a power-down mode that reduces the section quiescent current and turns off the bias currents into VINP and VINM (except for the 830 kΩ on VINM), reducing the impact of supply drain when the monitoring section is not being used. The registers of the TPS2482 and TPS2483 can be written to and read from while the device is in power-down mode. The device remains in power-down mode until one of the active modes settings are written into the Configuration Register. Power-on reset for the monitoring section (POR1) configures continuous shunt and bus monitoring as default. Full recovery from POR1 or power-down mode requires about 40 µs.

Although the TPS2482 and TPS2483 can be read at any time, and the data from the last conversion remain available, the Conversion Ready Flag bit (Mask/Enable Register, CVRF bit) is provided to help coordinate one-shot or triggered conversions. The Conversion Ready Flag bit is set after all conversions, averaging, and multiplication operations are complete.

The Conversion Ready Flag bit clears under these conditions:

1. Writing to the Configuration Register, except when configuring the MODE bits for power-down mode; or
2. Reading the Status Register.

Power Calculation

The Current and Power values are calculated following shunt voltage and bus voltage measurements as shown in Figure 39. Current is calculated following each shunt voltage measurement based on the value set in the Calibration Register. If there is no value loaded into the Calibration Register, the current value stored is zero. Power is calculated following each bus voltage measurement based on the previous current calculation and that bus voltage measurement. If there is no value loaded in the Calibration Register, the power value stored is also zero. Again, these calculations are performed in the background and do not add to the overall conversion time. These current and power values are considered intermediate results (unless the averaging is set to '1') and are stored in an internal accumulation register set, not the corresponding output registers. Following every measured sample, the newly-calculated values for current and power are appended to this accumulation register set until all of the samples have been measured and averaged based on the number of samples set in the Configuration Register.

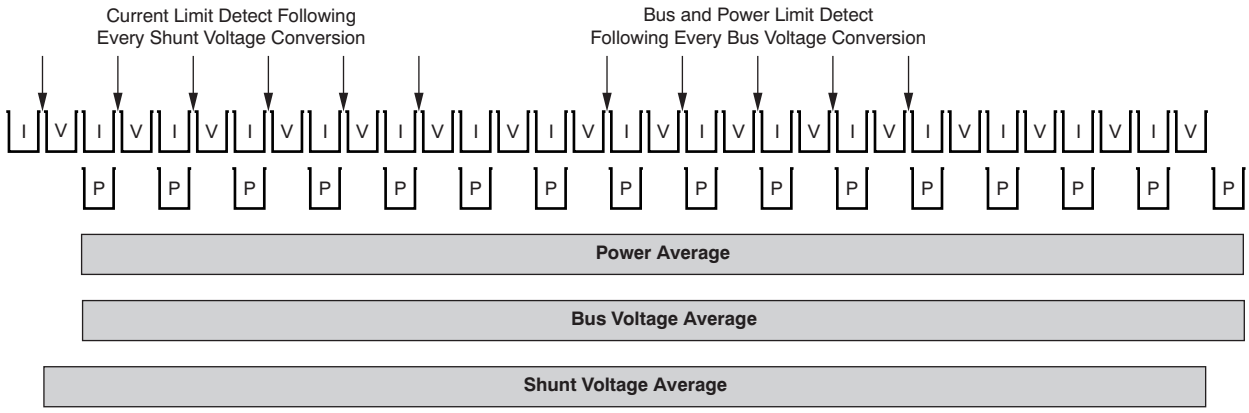


Figure 39. Power Calculation Scheme

In addition to the current and power values accumulating after every sample, the shunt and bus voltage measurements are also collected. Once all of the samples have been measured and the corresponding current and power calculations have been made, the accumulated average for each of these parameters is then loaded to their corresponding output registers, where they can then be read. Figure 39 illustrates an averaging of 16 samples. Also indicated in Figure 39 is the relative timing of the various current, voltage, and power limit detection functions associated with the ALERT pin. Details of the Alert functions can be found in the ALERT PIN section.

Averaging and Conversion Time Considerations

The TPS2482 and TPS2483 have programmable conversion times for both the shunt voltage and bus voltage measurements. The conversion times for these measurements can be selected from as fast as 140 µs to as long as 8.244 ms. The conversion time settings, along with the programmable averaging mode, allow the TPS2482 and TPS2483 to be configured to optimize the available timing requirements in a given application. For example, if a system requires that data be read every 5 ms, the TPS2482 and TPS2483 could be configured with the conversion times set to 588 µs and the averaging mode set to '4'. This configuration results in the data updating approximately every 4.7 ms. The TPS2482 and TPS2483 could also be configured with a different conversion time setting for the shunt and bus voltage measurements. This type of approach is common in applications where the bus voltage tends to be relatively stable. This situation can allow for the time focused on the bus voltage measurement to be reduced relative to the shunt voltage measurement. The shunt voltage conversion time could be set to 4.156 ms with the bus voltage conversion time set to 588 µs, with the averaging mode set to '1'. This configuration also results in data updating approximately every 4.7 ms.

There are trade-offs associated with the settings for conversion time and the averaging mode used. The averaging feature can significantly improve the measurement accuracy by effectively filtering the signal. This approach allows the TPS2482 and TPS2483 to reduce any noise in the measurement that may be caused by noise coupling into the signal. A greater number of averages enables the TPS2482 and TPS2483 to be more effective in reducing the noise component of the measurement.

The conversion times selected can also have an impact on the measurement accuracy. This effect can seen in Figure 40. Multiple conversion times are shown here to illustrate the impact of noise on the measurement. In order to achieve the highest accuracy measurement possible, a combination of the longest allowable conversion times and highest number of averages should be used, based on the timing requirements of the system.

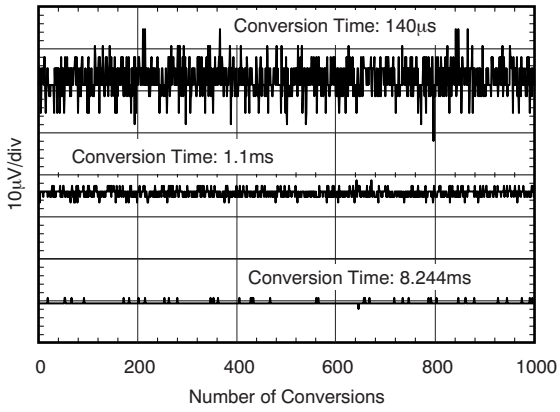


Figure 40. Noise vs Conversion Time

Filtering and Input Considerations

Measuring current is often noisy, and such noise can be difficult to define. The TPS2482 and TPS2483 offer several options for filtering by allowing the conversion times and number of averages to be selected independently in the Configuration Register. The conversion times can be set independently for the shunt voltage and bus voltage measurements to allow added flexibility in configuring the monitoring of the power-supply bus.

The internal ADC is based on a delta-sigma (ΔΣ) front-end with a 500 kHz (±30%) typical sampling rate. This architecture has good inherent noise rejection; however, transients that occur at or very close to the sample-rate harmonics can cause problems. Because these signals are at 1 MHz and higher, they can be managed by incorporating simple R-C filtering at VINP and VINM. The high frequency enables the use of low-value series resistors on the filter with negligible effects on measurement accuracy. In general, filtering the TPS2482 and TPS2483 monitoring input is only necessary if there are transients at exact harmonics of the 500 kHz (±30%) sampling rate (greater than 1 MHz). Filter using the lowest possible series resistance (typically 10 Ω for R_{FLTR}) and a ceramic capacitor, C_{FLTR}. Recommended values for C_{FLTR} are 0.1 µF to 1.0 µF. Figure 41 shows the TPS2482 and TPS2483 with an additional filter added at the input.

A short circuit on the hotswap output can create an input voltage overshoot. This occurs as the input circuit inductance discharges when the MOSFET, M_1, turns off. These transients could exceed the 40-V common-mode rating of VINP and VINM if not controlled. See Input and Output Transient Protection for guidance.

In applications that do not have large energy storage electrolytics on one or both sides of the shunt, an input overstress condition may result from an excessive dV/dt of the voltage applied to VINP and VINM. A hard physical short is the most likely cause of this event. This problem occurs because an excessive dV/dt can activate the ESD protection. The addition of 10-Ω resistors in series with VINP and VINM will protect the monitor inputs against this dV/dt failure up to their maximum 40-V ratings.

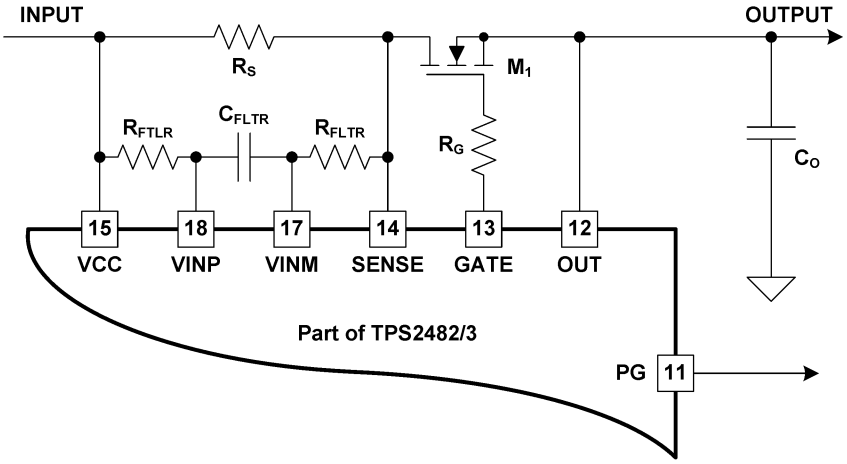


Figure 41. TPS2482 and TPS2483 with Input Filtering

ALERT PIN

The TPS2482 and TPS2483 have a single Alert Limit Register, 07h, that allows the ALERT pin to be programmed to respond to a single user-defined event or to a conversion ready notification if desired. The Mask/Enable Register allows the user to select from one of the five available functions to monitor and/or set the conversion ready bit to control the response of the ALERT pin. Based on the function being monitored, the user would then enter a value into the Alert Limit Register to set the corresponding threshold value that asserts the ALERT pin.

The ALERT pin allows for one of several available Alert functions to be monitored to determine if a user-defined threshold has been exceeded. The five Alert functions that can be monitored are:

- Shunt Voltage Over Limit (SOL)
- Shunt Voltage Under Limit (SUL)
- Bus Voltage Over Limit (BOL)
- Bus Voltage Under Limit (BUL)
- Power Over Limit (POL)

The ALERT pin is an open-drain output. This pin is asserted when the value of the Alert function selected in the Mask/Enable Register exceeds the value programmed into the Alert Limit Register. Only one of these Alert functions can be enabled and monitored at a time. If multiple Alert functions are enabled, the selected function in the highest significant bit position takes priority and exclusively responds to the Alert Limit Register value. For example, if the Shunt Voltage Over Limit and the Shunt Voltage Under Limit are both selected, the ALERT pin asserts only when the Shunt Voltage Over Limit Register exceeds the value in the Alert Limit Register.

The Conversion Ready state of the device can also be monitored at the ALERT pin to inform the user when the device has completed the previous conversion and is ready to begin a new conversion. Conversion Ready can be monitored at the ALERT pin simultaneously with one of the Alert functions. If an Alert function and the Conversion Ready are both enabled to be monitored at the ALERT pin, after the ALERT pin is asserted, the Mask/Enable Register must be read following the Alert to determine the source of the Alert. By reading the Conversion Ready Flag (CVRF), bit D3, and the Alert Function Flag (AFF), bit D4 in the Mask/Enable Register, the source of the Alert can be determined. If the Conversion Ready feature is not desired and the CNVR bit is not set, the ALERT pin only responds to an exceeded Alert limit based on the Alert function enabled.

If the Alert function is not used, the ALERT pin can be left floating without affecting the operation of the device.

Refer to Figure 39 to see the relative timing of when the value in the Alert Limit Register is compared to the corresponding Alert function value. For example, if the Alert function that is enabled is Shunt Voltage Over Limit (SOL), following every shunt voltage conversion the value in the Alert Limit Register is compared to the measured shunt voltage to determine if the measurement has exceeded the programmed limit. The AFF, bit 4 of the Mask/Enable Register, asserts high any time the measured voltage exceeds the value programmed into the Alert Limit Register. In addition to the AFF being asserted, the ALERT pin logic polarity is asserted based on the Alert Polarity Bit (APOL, bit 1 of the Mask/Enable Register). If the Alert Latch is enabled, the AFF and ALERT pin remain asserted until either the Configuration Register is written to or the Mask/Enable Register is read.

The Shunt Voltage Alert functions compare the measured Shunt Voltage Register value to the Alert Limit Register value following every shunt voltage conversion and assert the AFF bit and ALERT pin if the programmed limit threshold is exceeded.

The Bus Voltage Alert functions compare the measured Bus Voltage Register value to the Alert Limit Register value following every bus voltage conversion and assert the AFF bit and ALERT pin if the programmed limit threshold is exceeded.

The Power Over Limit Alert function compares the calculated Power Register value to the Alert Limit Register value following every bus voltage conversions and asserts the AFF bit and ALERT pin if the programmed limit threshold is exceeded.

PROGRAMMING THE TPS2482 and TPS2483 MONITOR SECTION

An important aspect of the TPS2482 and TPS2483 is that they do not measure current or power directly. The TPS2482 and TPS2483 measure both the differential shunt voltage applied between the VINP and VINM input pins and the bus voltage applied from the VINM pin to GND. In order for the TPS2482 and TPS2483 to report both current and power values, the user must program the resolution of the Current Register and the value of the shunt resistor used in the application. The Power_LSB, corresponding to the Power Register, is internally set to be 25 times the programmed Current_LSB. Both the Current_LSB and shunt-resistor value are used in the calculation of the Calibration Register value which the TPS2482 and TPS2483 use to calculate the corresponding current and power values based on the shunt and bus voltage measurements.

The Calibration Register value is calculated using Equation 21. CAL(ibration) is the factor used to convert the value in the Shunt Voltage Register to the value representing current in the Current Register. This equation includes the Current_LSB term, which is a rounded value for the LSB-weight of the Current Register. The highest resolution for the Current Register can be obtained by using the exact Current_LSB value, based on the maximum expected current, as determined by Equation 20. While this value will yield the highest resolution, it is common practice to select a value for the Current_LSB to the nearest round number above this value to simplify the conversion of the Current Register and Power Register values to amperes and watts, respectively. The R_{SHUNT} term is the value of the external shunt resistor used to generate the differential voltage across the input pins. The 0.00512 term in Equation 21 is a constant factor used to scale the external values to the proper internal levels.

$$\text{Current\_LSB} = \frac{I_{MAX}}{2^{15} - 1} = \frac{I_{MAX}}{32767} \tag{20}$$

$$\text{CalibrationRegValue} = \text{CAL} = \frac{0.00512}{\text{Current\_LSB} \times R_{SHUNT}} \tag{21}$$

Once the Calibration Register has been programmed, the Current Register and Power Register will be updated accordingly based on the corresponding shunt voltage and bus voltage averaged measurements. Until the Calibration Register is programmed, the Current and Power Registers remain at zero.

CONFIGURE/MEASURE/CALCULATE EXAMPLE

In this example, shown in Figure 42, a nominal 40-A load current creates a differential voltage of 40 mV across a 1-mΩ shunt resistor. The bus voltage for the TPS2482 and TPS2483 is measured from VINM to GND. In this case, the VINM pin measures 11.96 V as a consequence of the voltage drop across the shunt resistor.

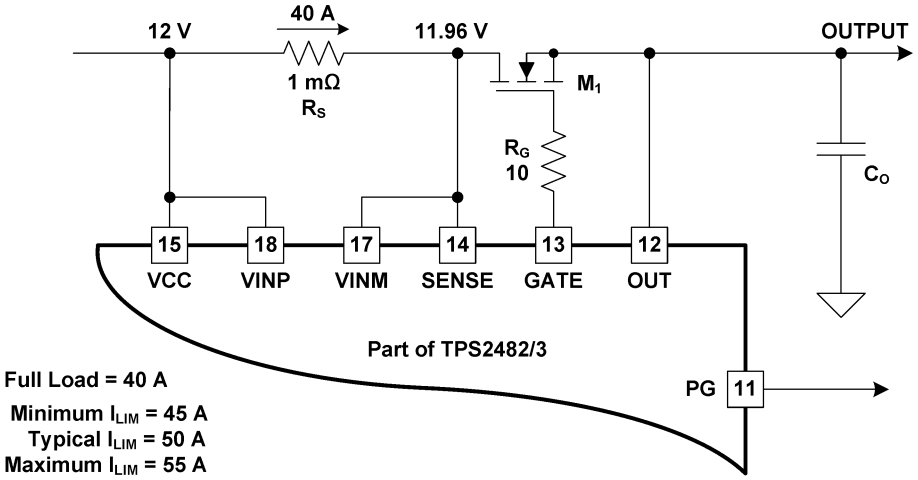


Figure 42. Example Circuit Configuration

For this example, assuming a maximum expected current of 55 A (based on the I_{LIM} tolerance), the exact Current_LSB is calculated to be 1.679 mA/bit using Equation 20. Choosing a rounded-up Current_LSB value of 2 mA/bit would significantly simplify the mental conversion of the Current Register and Power Register values to amperes and watts. Using a rounded value for the Current_LSB does trade off a small amount of resolution for having a simpler calculation process on the part of the user. With a Current_LSB of 2 mA/bit and a shunt resistance of 1-mΩ in this example, using Equation 21 results in a Calibration Register value of 2560, or A00h.

The Current Register value is then calculated by multiplying the decimal value of the Shunt Voltage Register contents by the decimal value of the Calibration Register and dividing by 2048 (another internal scaling factor), as shown in Equation 22. For this example, the Shunt Voltage Register contains a value of 16000, which is multiplied by the Calibration Register value of 2560 and then divided by 2048 to yield a decimal value for the Current Register of 20000, or 4E20h. Multiplying this value by 2 mA/bit results in the original 40-A current level stated at the beginning of this example.

$$\text{CurrentRegValue} = \frac{\text{ShuntVoltageRegValue} \times \text{CAL}}{2048} \tag{22}$$

The LSB for the Bus Voltage Register is internally fixed at 1.25 mV/bit, which means that the 11.96 V present at the V_{VINM} pin results in a register representation value of 2560h, or a decimal equivalent of 9568. Note that the MSB of the Bus Voltage Register is always zero because the V_{VINM} pin is only able to measure positive voltages.

The Power_LSB has a fixed ratio to the Current_LSB of 25 W/bit to 1 A/bit. For this example, a programmed Current_LSB of 2 mA/bit automatically results in a Power_LSB of 50 mW/bit (((25 W/bit) / (1 A/bit)) * 2 mA/bit). The 25-W/A ratio is internally programmed to ensure that the results of the power calculation falls within an acceptable representation range for the Power Register.

The Power Register value is calculated by multiplying the decimal value of the Current Register, 20000, by the decimal value of the Bus Voltage Register, 9568, and then dividing by 20000, as defined in Equation 23. For this example, the result for the Power Register is 2560h, or a decimal equivalent of 9568. Multiplying this value by the Power_LSB results in a calculation of (9568 × 50 mW/bit), or 478.4 W of actual power. To verify the example, a manual calculation for the power being delivered to the load uses the bus voltage of 11.96 V (12 V source – 40 mV shunt drop) multiplied by the load current of 40 A to give a result of 478.4 W.

$$\text{Power RegValue} = \frac{\text{CurrentRegValue} \times \text{BusVoltageRegValue}}{20000} \quad (23)$$

Table 2 shows the steps for configuring, measuring, and calculating the values for current and power for this device.

Table 2. Configure/Measure/Calculate Example(1)

STEP #	REGISTER NAME	ADDRESS	CONTENT REPRESENTATION		LSB-WEIGHT	ACTUAL VALUE
			HEXADECIMAL	DECIMAL		
Step 1	Configuration	00h	4127h	—	—	—
Step 2	Shunt Voltage	01h	3E80h	16000	2.5 µV/bit	40 mV
Step 3	Bus Voltage	02h	2560h	9568	1.25 mV/bit	11.96 V
Step 4	Calibration	05h	A00h	2560	—	—
Step 5	Current	04h	4E20h	20000	2 mA/bit	40 A
Step 6	Power	03h	2560h	9568	50 mW/bit	478.4W

(1) Conditions: R_{SHUNT} = 1 mΩ, load current = 40 A, V_{CM} = 12 V, and V_{VINM} = 12 V.

PROGRAMMING THE TPS2482 and TPS2483 POWER MEASUREMENT ENGINE

Calibration Register and Scaling

The Calibration Register makes it possible to set the scaling of the Current and Power Registers to whatever values are most useful for a given application. One strategy may be to set the Calibration Register such that the largest possible number is generated in the Current Register or Power Register at the expected full-scale point. This approach would yield the highest resolution based on using the previously-calculated exact Current_LSB in the equation for the Calibration Register. The Calibration Register value can also be selected to produce values in the Current and Power Registers that either provide direct decimal equivalents of the values being measured, or yield a rounded LSB-value for each respective register.

After these choices have been made, the programmable Calibration Register also offers possibilities for end-user system-level calibration. By physically measuring the current with an accurate external ammeter, the exact current is known. The calculated value for the Calibration Register can then be adjusted, based on the measured-current result of the TPS2482 and TPS2483, to cancel the total system error as shown in Equation 24. Store the Corrected_CAL value (rounded to the nearest whole number) in place of the previously-stored (exact or rounded) CAL value. If necessary, iterate this process until the current reported by the TPS2482 and TPS2483 is equal to the ammeter measurement.

$$\text{Corrected\_CAL} = \text{round}\left(\text{CAL} \times \frac{\text{Ammeter\_Measured\_Current}}{\text{TPS2482/3\_Reported\_Current}}\right) \quad (24)$$

Simple Current Shunt Monitor Usage (No Programming Necessary)

The TPS2482 and TPS2483 can be used without any programming if it is only necessary to read a shunt voltage drop and bus voltage with the default power-on reset configuration and continuous conversion of shunt and bus voltage.

Without programming the TPS2482 and TPS2483 Calibration Register, the device is unable to provide either a valid current or power value, because these outputs are both derived using the values loaded into the Calibration Register.

Default TPS2482 and TPS2483 Settings

The default power-up states of the registers are shown in the REGISTER DETAILS section of this data sheet. These registers are volatile, and if programmed to a value other than the default values shown in Table 3, they must be re-programmed at every device power-up. Detailed information on programming the Calibration Register specifically is given in the Configure/Measure/Calculate Example section and calculated based on Equation 21.

REGISTER INFORMATION

The TPS2482 and TPS2483 monitoring section uses a bank of registers for programming and holding configuration settings, measurement results, minimum/maximum limits, and status information. Table 3 summarizes all of the TPS2482 and TPS2483 registers. Refer to the Register Block Diagram for a simplified illustration of the measurement data registers.

Table 3. Summary of Register Set

POINTER ADDRESS			POWER-ON RESET DEFAULT SETTINGS		
HEX	REGISTER NAME	FUNCTION	BINARY	HEX	TYPE (1)
0	Configuration Register	Configures all-register reset, shunt voltage and bus voltage ADC conversion times and averaging, operating mode.	01000001 00100111	4127	R/$\overline{W}$
1	Shunt Voltage	Shunt voltage averaged measurement data.	00000000 00000000	0000	R
2	Bus Voltage	Bus voltage averaged measurement data.	00000000 00000000	0000	R
3	Power (2)	Contains the value of the calculated power being delivered to the load.	00000000 00000000	0000	R
4	Current (2)	Contains the value of the calculated current flowing through the shunt resistor.	00000000 00000000	0000	R
5	Calibration	Sets full-scale range and LSB value of current and power measurements. Overall system calibration.	00000000 00000000	0000	R/$\overline{W}$
6	Mask/Enable	Alert configuration and Conversion Ready flag.	00000000 00000000	0000	R/$\overline{W}$
7	Alert Limit	Contains the limit value to compare to the selected Alert function.	00000000 00000000	0000	R/$\overline{W}$
FF	Die ID	Contains unique die identification number.	ASCII	ASCII	R

(1) Type: **R** = Read-Only, **R/$\overline{W}$** = Read/Write.
(2) The Current Register defaults to '0' because the Calibration Register defaults to '0', yielding zero current and power values until the Calibration Register is programmed.

REGISTER DETAILS

All 16-bit registers in the TPS2482 and TPS2483 comprise two 8-bit bytes via the serial-bus interface.

Configuration Register 00h (Read/Write)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	RST	—	—	—	AVG2	AVG1	AVG0	V_{BUS}CT2	V_{BUS}CT1	V_{BUS}CT0	V_{SH}CT2	V_{SH}CT1	V_{SH}CT0	MODE3	MODE2	MODE1
POR1 VALUE	0	1	0	0	0	0	0	1	0	0	1	0	0	1	1	1

The Configuration Register bit settings control the operating modes for the TPS2482 and TPS2483. This register controls the conversion time settings for both the shunt and bus voltage measurements as well as the averaging mode used. The operating mode that controls which signals are selected to be measured is also programmed in the Configuration Register.

The Configuration Register can be read from at any time without impacting or affecting the device settings or a conversion in progress. However, writing to the Configuration Register will halt any conversion in progress until the write sequence is completed, resulting in a new conversion starting based on the new contents of the Configuration Register. This prevents any uncertainty in the conditions used for the next completed conversion.

Configuration Register Bit Descriptions

RST:	**Reset Bit**
Bit 15	Setting this bit to '1' generates a system reset that is the same as power-on reset (POR1). Resets all registers to default values; this bit self-clears.
(RESERVED):	**Undefined and Reserved**
Bits 12-14	These bits are preset to '100', perform no defined function, and are not programmable by the user. Reserved for future use.
AVG:	**Averaging Mode**
Bits 9–11	Sets the number of samples that will be collected and averaged together. Table 4 summarizes the AVG bit options and related number of samples averaged for each bit combination. Applies to both shunt and bus voltage measurements.

Table 4. AVG Bit Settings [11:9](1)

AVG2 D11	AVG1 D10	AVG0 D9	NUMBER OF SAMPLES AVERAGED
0	0	0	1
0	0	1	4
0	1	0	16
0	1	1	64
1	0	0	128
1	0	1	256
1	1	0	512
1	1	1	1024

(1) Shaded values are POR1 default.

V_{BUS} CT: **Bus Voltage Conversion Time**

Bits 6–8

Sets the conversion time for each bus voltage measurement. Table 5 shows the V_{BUS} CT bit options and related conversion times for each bit combination. Applies to V_{BUS} measurement only.

Table 5. Bus Voltage CT Bit Settings [8:6] (1)

V_{BUS} CT2 D8	V_{BUS} CT1 D7	V_{BUS} CT0 D6	CONVERSION TIME
0	0	0	140µs
0	0	1	204µs
0	1	0	332µs
0	1	1	588µs
1	0	0	1.1ms
1	0	1	2.116ms
1	1	0	4.156ms
1	1	1	8.244ms

(1) Shaded values are POR1 default.

V_{SHUNT} CT: **Shunt Voltage Conversion Time**

Bits 3–5

Sets the conversion time for each shunt voltage measurement. Table 6 shows the V_{SHUNT} CT bit options and related conversion times for each bit combination. Applies to V_{SHUNT} measurement only.

Table 6. Shunt Voltage CT Bit Settings [5:3](1)

V_{SHUNT} CT2 D5	V_{SHUNT} CT1 D4	V_{SHUNT} CT0 D3	CONVERSION TIME
0	0	0	140µs
0	0	1	204µs
0	1	0	332µs
0	1	1	588µs
1	0	0	1.1ms
1	0	1	2.116ms
1	1	0	4.156ms
1	1	1	8.244ms

(1) Shaded values are POR1 default.

MODE: **Operating Mode**

Bits 0–2

Selects continuous, triggered, or power-down mode of operation. These bits default to continuous shunt and bus measurement mode. The mode-setting options are shown in Table 7.

Table 7. Operating Mode Settings [2:0](1)

MODE3 D2	MODE2 D1	MODE1 D0	OPERATING MODE
0	0	0	Power-Down
0	0	1	Shunt Voltage, Triggered
0	1	0	Bus Voltage, Triggered
0	1	1	Shunt and Bus, Triggered
1	0	0	Power-Down
1	0	1	Shunt Voltage, Continuous
1	1	0	Bus Voltage, Continuous
1	1	1	Shunt and Bus, Continuous

(1) Shaded values are POR1 default.

DATA OUTPUT REGISTERS

Shunt Voltage Register 01h (Read-Only)

The Shunt Voltage Register stores the most recent, fully-averaged shunt voltage measurement, V_{SHUNT}, represented by the LSB-weighted magnitude of that value.

Negative numbers are represented in twos complement format. Generate the twos complement of a negative number by complementing the absolute value binary number and adding '1'. Extend the sign, denoting a negative number by setting the MSB = '1'.

Example: For a value of V_{SHUNT} = –80 mV:

1. Take the absolute value: 80 mV
2. Translate this number to a whole decimal number (80 mV ÷ 2.5 µV) = 32000
3. Convert this number to binary = 111 1101 0000 0000
4. Complement the binary result = 000 0010 1111 1111
5. Add '1' to the complement to create the twos complement result = 000 0011 0000 0000
6. Extend the sign and create the 16-bit word: 1000 0011 0000 0000 = 8300h

Full-scale range = 81.9175 mV (hexadecimal = 7FFF); LSB-weight = 2.5 µV/bit.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SIGN	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
POR1 VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bus Voltage Register 02h (Read-Only)(1)

The Bus Voltage Register stores the most recent, fully-averaged input bus voltage measurement, V_{BUS}, represented by the LSB-weighted magnitude of that value.

Full-scale range = 40.96 V (hexadecimal = 7FFF); LSB-weight = 1.25 mV/bit. **However, do not apply more than 36 V to the input**.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	—	BD14	BD13	BD12	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0
POR1 VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) D15 is always zero because bus voltage can only be positive.

Power Register 03h (Read-Only)

The Power Register stores the product of the most recent current and bus voltage values, represented by the LSB-weighted magnitude of that calculation. The Power_LSB is internally programmed to equal 25 times the programmed value of the Current_LSB. The Power Register records power by multiplying the decimal values of the Current Register and the Bus Voltage Register and dividing by a scale-factor, according to Equation 23.

LSB-weight = Power_LSB. If measurement averaging is enabled, this register displays the final averaged value.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
POR1 VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Current Register 04h (Read-Only)

The Current Register stores the most recent input current calculation, represented by the LSB-weighted magnitude of that calculation. The Current Register records current by multiplying the decimal values of the Shunt Voltage Register and the Calibration Register and dividing by a scale-factor, according to Equation 22.

LSB-weight = Current_LSB. If measurement averaging is enabled, this register displays the final averaged value.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	CSIGN	CD14	CD13	CD12	CD11	CD10	CD9	CD8	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
POR1 VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Calibration Register 05h (Read/Write)

This register provides the TPS2482 and TPS2483 with the value of the shunt resistor which generates the measured differential voltage combined with the resolution of the Current Register and internal scaling. The Current_LSB and Power_LSB are set by the programming of this register. This register is also suitable for use in overall system calibration. See the Configure/Measure/Calculate Example for additional information on programming the Calibration Register.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	—	FS14	FS13	FS12	FS11	FS10	FS9	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0
POR1 VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mask/Enable Register 06h (Read/Write)

The Mask/Enable Register selects the function that is enabled to control the ALERT pin, as well as how that pin functions. If multiple functions are enabled, the highest significant bit position Alert Function (D15-D11) takes priority and responds to the Alert Limit Register.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SOL	SUL	BOL	BUL	POL	CNVR	—	—	—	—	—	AFF	CVRF	OVF	APOL	LEN
POR1 VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SOL: **Shunt Voltage Over-Voltage**

Bit 15 Setting this bit high configures the ALERT pin to be asserted when the Shunt Voltage Register exceeds the value in the Alert Limit Register.

SUL: **Shunt Voltage Under-Voltage**

Bit 14 Setting this bit high configures the ALERT pin to be asserted when the Shunt Voltage Register drops below the value in the Alert Limit Register.

BOL: **Bus Voltage Over-Voltage**

Bit 13 Setting this bit high configures the ALERT pin to be asserted when the Bus Voltage Register exceeds the value in the Alert Limit Register.

BUL: **Bus Voltage Under-Voltage**

Bit 12 Setting this bit high configures the ALERT pin to be asserted when the Bus Voltage Register drops below the value in the Alert Limit Register.

POL: **Power Over-Limit**

Bit 11 Setting this bit high configures the ALERT pin to be asserted when the Power Register exceeds the value in the Alert Limit Register.

CNVR:	**Conversion Ready**
Bit 10	Setting this bit high configures the ALERT pin to be asserted (independently of any Alert Function) when the Conversion Ready Flag, Bit 3, is asserted indicating that the device is ready for the next conversion.
AFF:	**Alert Function Flag**
Bit 4	While only one Alert Function can be monitored at the ALERT pin at a time, the Conversion Ready can also be simultaneously enabled to assert the ALERT pin. Reading the Alert Function Flag following an Alert allows the user to determine if the Alert Function was the source of the Alert. When the Alert Latch Enable bit is set to Latch mode, the Alert Function Flag clears only when the Mask/Enable Register is read. When the Alert Latch Enable bit is set to Transparent mode, the Alert Function Flag is cleared following the next conversion that does not result in an Alert condition.
CVRF:	**Conversion Ready Flag**
Bit 3	Although the TPS2482 and TPS2483 can be read at any time, and the data from the last conversion is available, the Conversion Ready bit is provided to help coordinate one-shot or triggered conversions. The Conversion bit is set after all conversions, averaging, and multiplications are complete. Conversion Ready clears under the following conditions: 1.) Writing to the Configuration Register (except for Power-Down or Disable selections) 2.) Reading the Mask/Enable Register
OVF:	**Math Overflow Flag**
Bit 2	This bit is set to '1' if an arithmetic operation resulted in an overflow error. It indicates that current and power data may be invalid. This bit is cleared by the next operation which does not result in an overflow error.
APOL:	**Alert Polarity bit; sets the ALERT pin logic polarity.**
Bit 1	1 = Inverted (active-high open-drain) 0 = Normal (active-low open-drain) (POR1 default)
LEN:	**Alert Latch Enable bit; configures the latching feature of the ALERT pin and Alert Function Flag bit.**
Bit 0	1 = Latch enabled 0 = Transparent (POR1 default) When the Alert Latch Enable bit is cleared to Transparent mode, the ALERT pin and Alert Function Flag bit will automatically reset to their idle states when the fault has been cleared. When the Alert Latch Enable bit is set to Latch mode, the ALERT pin and Alert Function Flag bit will remain active following a fault until the Mask/Enable Register has been read.

Alert Limit Register 07h (Read/Write)

The Alert Limit Register contains the value used to compare to the register selected in the Mask/Enable Register to determine if a limit has been exceeded.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	AUL15	AUL14	AUL13	AUL12	AUL11	AUL10	AUL9	AUL8	AUL7	AUL6	AUL5	AUL4	AUL3	AUL2	AUL1	AUL0
POR1 VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SERIAL-BUS OVERVIEW

The TPS2482 and TPS2483 serial-bus offers compatibility with both I^2C and SMBus interfaces. The I^2C and SMBus protocols are essentially compatible with one another.

The I^2C interface is used throughout this data sheet as the primary example, with SMBus protocol specified only when a difference between the two systems is discussed. Two bidirectional lines, SCL and SDA, connect the TPS2482 and TPS2483 to the bus. Both SCL and SDA are open-drain connections.

The device that initiates a data transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates START and STOP conditions.

To address a specific device, the master initiates a start condition by pulling the data signal line (SDA) from a high to a low logic level while SCL is high. All slaves on the bus shift in the slave address byte on the rising edge of SCL, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA low.

Data transfer is then initiated and eight bits of data are sent, followed by an *Acknowledge* bit (slave generated). During data transfer, SDA must remain stable while SCL is high. Any change in SDA while SCL is high is interpreted as a start or stop condition.

Once all data have been transferred, the master generates a stop condition, indicated by pulling SDA from low to high while SCL is high. The TPS2482 and TPS2483 includes a 28-ms timeout on its interface to prevent locking up the bus.

Serial-Bus Address

To communicate with the TPS2482 and TPS2483, the master must first address slave devices via a slave address byte. The slave address byte consists of seven address bits and a direction bit that indicates whether the action is to be a read or write operation.

The TPS2482 and TPS2483 has two address pins, A0 and A1. Table 8 describes the pin logic levels for each of the 16 possible addresses. The state of pins A0 and A1 is sampled on every bus communication and should be set before any activity on the interface occurs.

Table 8. TPS2482 and TPS2483 Address Pin Connections and Corresponding Slave Addresses

A1	A0	SLAVE ADDRESS
GND	GND	1000000
GND	V_S	1000001
GND	SDA	1000010
GND	SCL	1000011
V_S	GND	1000100
V_S	V_S	1000101
V_S	SDA	1000110
V_S	SCL	1000111
SDA	GND	1001000
SDA	V_S	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	V_S	1001101
SCL	SDA	1001110
SCL	SCL	1001111

Serial-Bus Interface

The TPS2482 and TPS2483 operates only as a slave device on both the I^2C bus and the SMBus. Connections to the bus are made via the open-drain I/O lines SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. While there is spike suppression integrated into the digital I/O lines, proper layout should be used to minimize the amount of coupling into the communication lines. This noise introduction could occur from capacitively coupling signal edges between the two communication lines themselves or from other switching noise sources present in the system. Routing traces in parallel with ground in between layers on a printed circuit board (PCB) typically reduces the effects of coupling between the communication lines. Shielding communication lines in general is recommended to reduce to possibility of unintended noise coupling into the digital I/O lines that could be incorrectly interpreted as start or stop commands.

The TPS2482 and TPS2483 supports the transmission protocol for Fast (1 kHz to 400 kHz) and High-speed (1 kHz to 3.4 MHz) modes. All data bytes are transmitted most significant byte first.

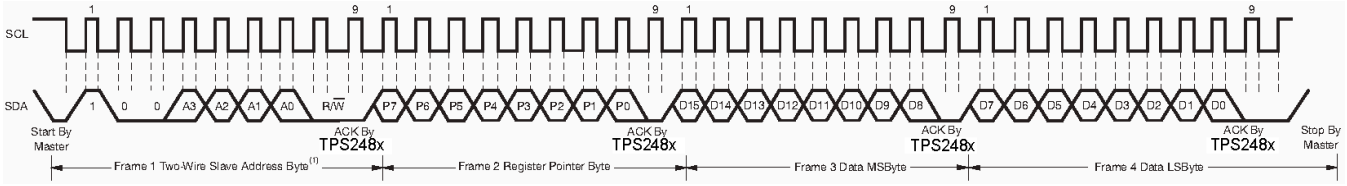
WRITING TO/READING FROM THE TPS2482 and TPS2483

Accessing a specific register on the TPS2482 and TPS2483 is accomplished by writing the appropriate value to the register pointer. Refer to Table 3 for a complete list of registers and corresponding addresses. The value for the register pointer (as shown in Figure 46) is the first byte transferred after the slave address byte with the R/$\overline{W}$ bit low. Every write operation to the TPS2482 and TPS2483 requires a value for the register pointer.

Writing to a register begins with the first byte transmitted by the master. This byte is the slave address, with the R/$\overline{W}$ bit low. The TPS2482 and TPS2483 then acknowledges receipt of a valid address. The next byte transmitted by the master is the address of the register which data will be written to. This register address value updates the register pointer to the desired register. The next two bytes are written to the register addressed by the register pointer. The TPS2482 and TPS2483 acknowledges receipt of each data byte. The master may terminate data transfer by generating a start or stop condition.

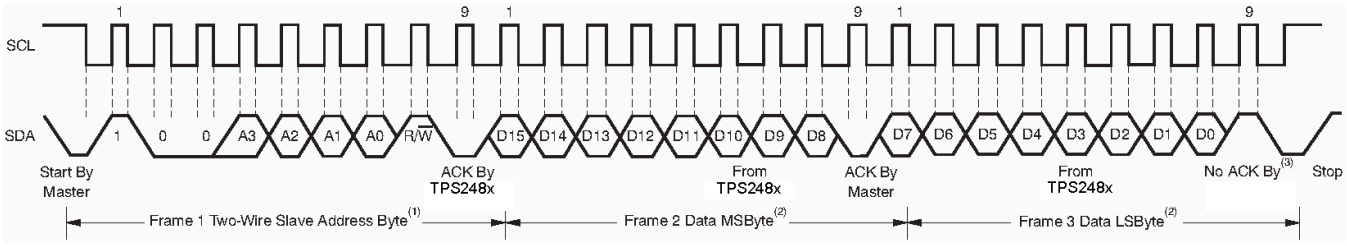
When reading from the TPS2482 and TPS2483, the last value stored in the register pointer by a write operation determines which register is read during a read operation. To change the register pointer for a read operation, a new value must be written to the register pointer. This write is accomplished by issuing a slave address byte with the R/$\overline{W}$ bit low, followed by the register pointer byte. No additional data are required. The master then generates a start condition and sends the slave address byte with the R/$\overline{W}$ bit high to initiate the read command. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the register pointer. This byte is followed by an *Acknowledge* from the master; then the slave transmits the least significant byte. The master acknowledges receipt of the data byte. The master may terminate data transfer by generating a *Not-Acknowledge* after receiving any data byte, or generating a start or stop condition. If repeated reads from the same register are desired, it is not necessary to continually send the register pointer bytes; the TPS2482 and TPS2483 retain the register pointer value until it is changed by the next write operation.

Figure 43 and Figure 44 show the write and read operation timing diagrams, respectively. Note that register bytes are sent most-significant byte first, followed by the least significant byte.



(1) The value of the Slave Address byte is determined by the settings of the A0 and A1 pins. Refer to Table 8.

Figure 43. Timing Diagram for Write Word Format



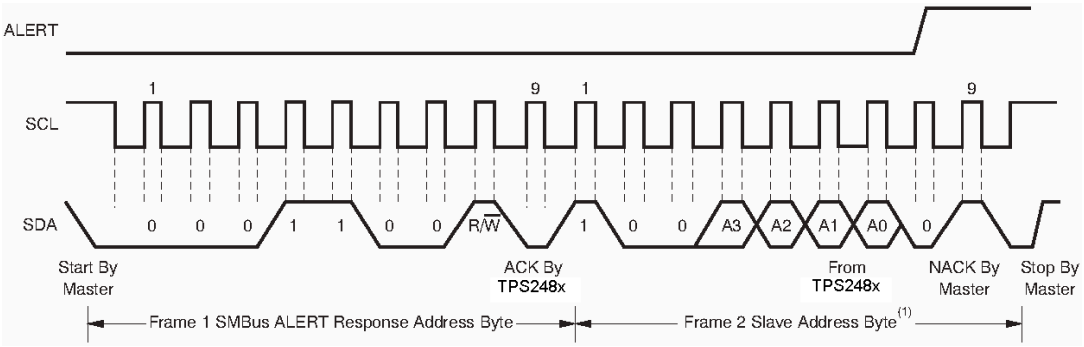
(1) The value of the Slave Address byte is determined by the settings of the A0 and A1 pins. Refer to Table 8.

(2) Read data is from the last register pointer location. If a new register is desired, the register pointer must be updated. See Figure 23.

(3) ACK by Master can also be sent.

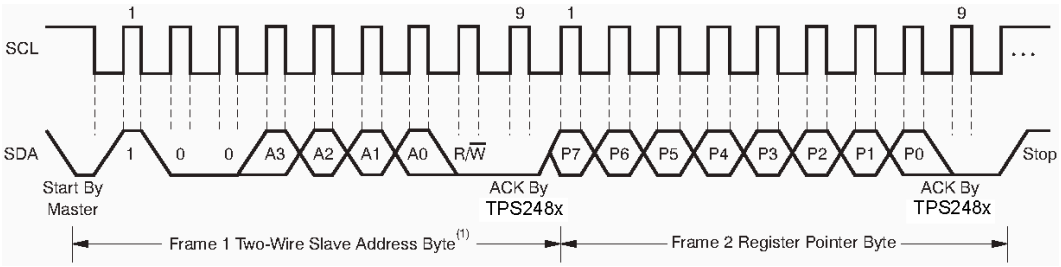
Figure 44. Timing Diagram for Read Word Format

Figure 45 shows the timing diagram for the SMBus Alert Response operation. Figure 46 illustrates a typical register pointer configuration.



(1) The value of the Slave Address Byte is determined by the settings of the A0 and A1 pins. Refer to Table 8.

Figure 45. Timing Diagram for SMBus ALERT



(1) The value of the Slave Address Byte is determined by the settings of the A0 and A1 pins. Refer to Table 8.

Figure 46. Typical Register Pointer Set

High-Speed I²C Mode

When the bus is idle, both the SDA and SCL lines are pulled high by the pull-up devices. The master generates a start condition followed by a valid serial byte containing High-Speed (HS) master code *00001XXX*. This transmission is made in fast (400 kHz) or standard (100 kHz) (F/S) mode at no more than 400 kHz. The TPS2482 and TPS2483 do not acknowledge the HS master code, but does recognize it and switches its internal filters to support 3.4 MHz operation.

The master then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 3.4 MHz are allowed. Instead of using a stop condition, repeated start conditions should be used to secure the bus in HS-mode. A stop condition ends the HS-mode and switches all the internal filters of the TPS2482 and TPS2483 to support the F/S mode.

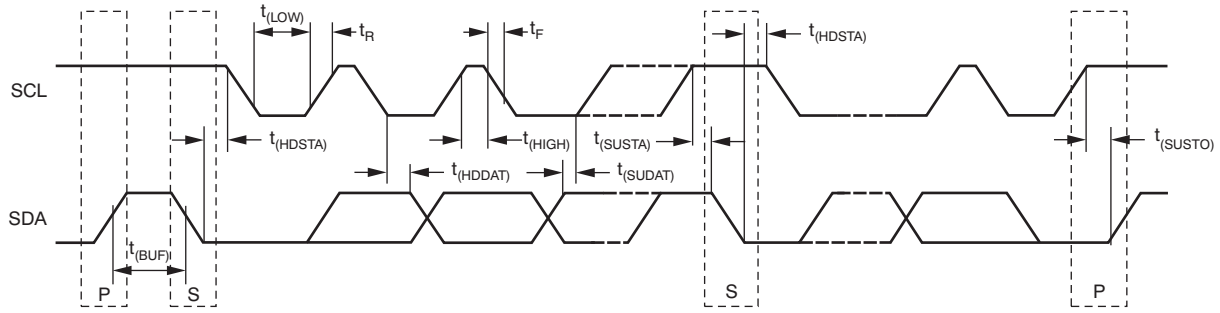


Figure 47. Bus Timing Diagram

Bus Timing Diagram Definitions

PARAMETER		FAST MODE		HIGH-SPEED MODE		UNITS
		MIN	MAX	MIN	MAX	
SCL operating frequency	$f_{(SCL)}$	0.001	0.4	0.001	3.4	MHz
Bus free time between STOP and START conditions	$t_{(BUF)}$	600		160		ns
Hold time after repeated START condition. After this period, the first clock is generated.	$t_{(HDSTA)}$	100		100		ns
Repeated start condition setup time	$t_{(SUSTA)}$	100		100		ns
STOP condition setup time	$t_{(SUSTO)}$	100		100		ns
Data hold time	$t_{(HDDAT)}$	0		0		ns
Data setup time	$t_{(SUDAT)}$	100		10		ns
SCL clock low period	$t_{(LOW)}$	1300		160		ns
SCL clock high period	$t_{(HIGH)}$	600		60		ns
Clock/data fall time	t_F		300		160	ns
Clock/data rise time	t_R		300		160	ns
Clock/data rise time for SCLK ≤ 100 kHz	t_R		1000			ns

SMBus Alert Response

The TPS2482 and TPS2483 are designed to respond to the SMBus Alert Response address. The SMBus Alert Response provides a quick fault identification for simple slave devices. When an Alert occurs, the master can broadcast the Alert Response slave address (0001 100) with the Read/Write bit set high, as seen in Figure 45. Following this Alert Response, any slave devices that generated an Alert will identify themselves by acknowledging the Alert Response and sending their respective address on the bus.

The Alert Response can activate several different slave devices simultaneously, similar to the I²C General Call. If more than one slave attempts to respond, bus arbitration rules apply. The losing device does not generate an Acknowledge and continues to hold the ALERT line low until the interrupt is cleared.

REVISION HISTORY

Changes from Original (December 2012) to Revision A **Page**

- Changed Shunt offset voltage, RTI vs Temperature TYP value From: 0.02 To: 0.1 and the MAX value From: 0.1 To: 0.4 5

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2482PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS2482	Samples
TPS2482PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS2482	Samples
TPS2483PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS2483	Samples
TPS2483PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS2483	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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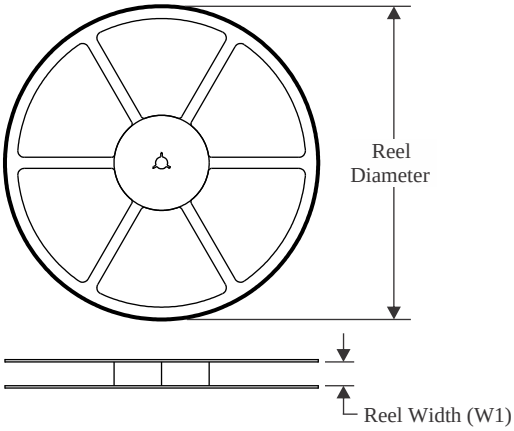
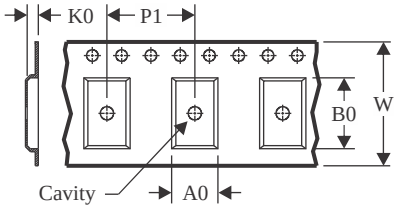
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

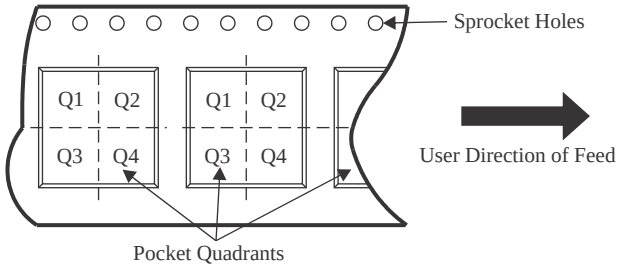


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

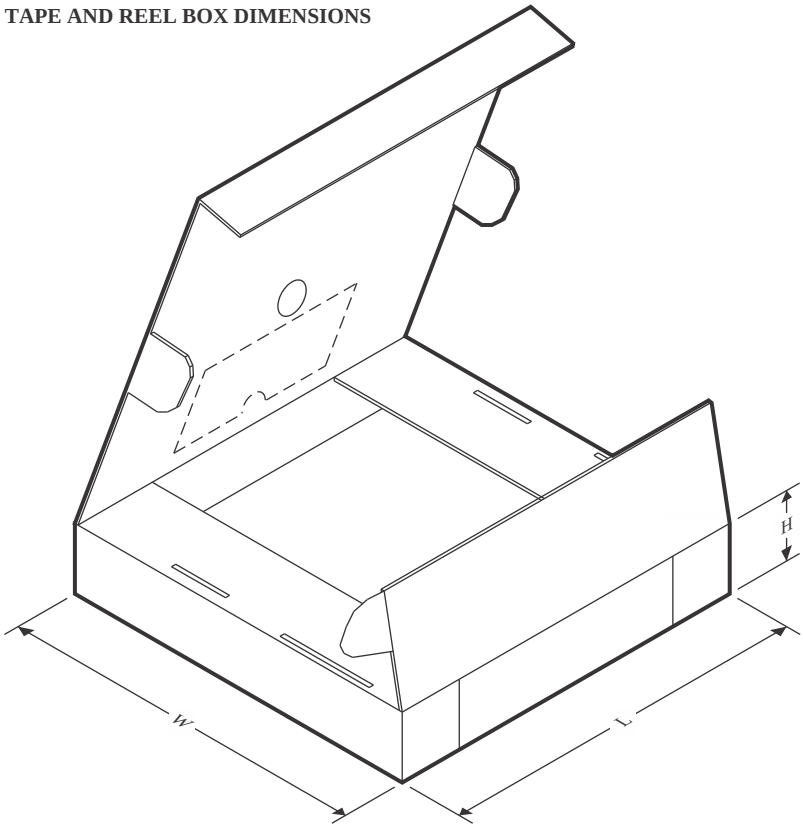
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2482PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS2483PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

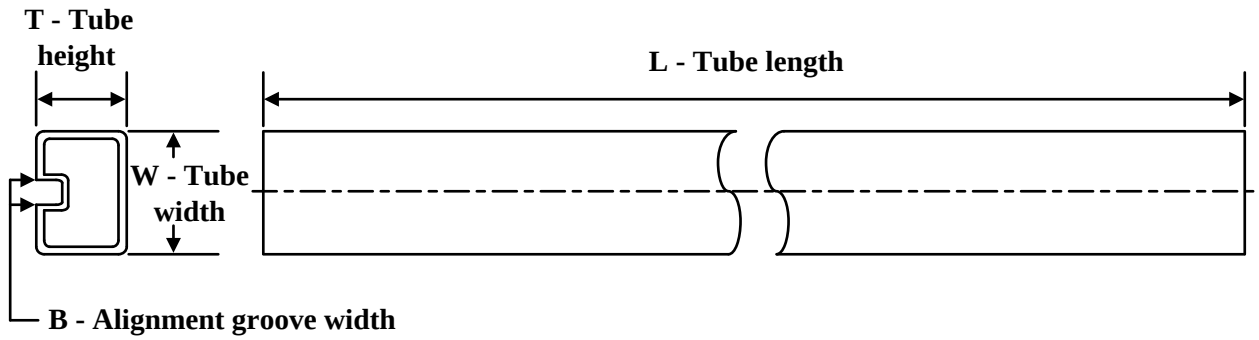
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2482PWR	TSSOP	PW	20	2000	356.0	356.0	35.0
TPS2483PWR	TSSOP	PW	20	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

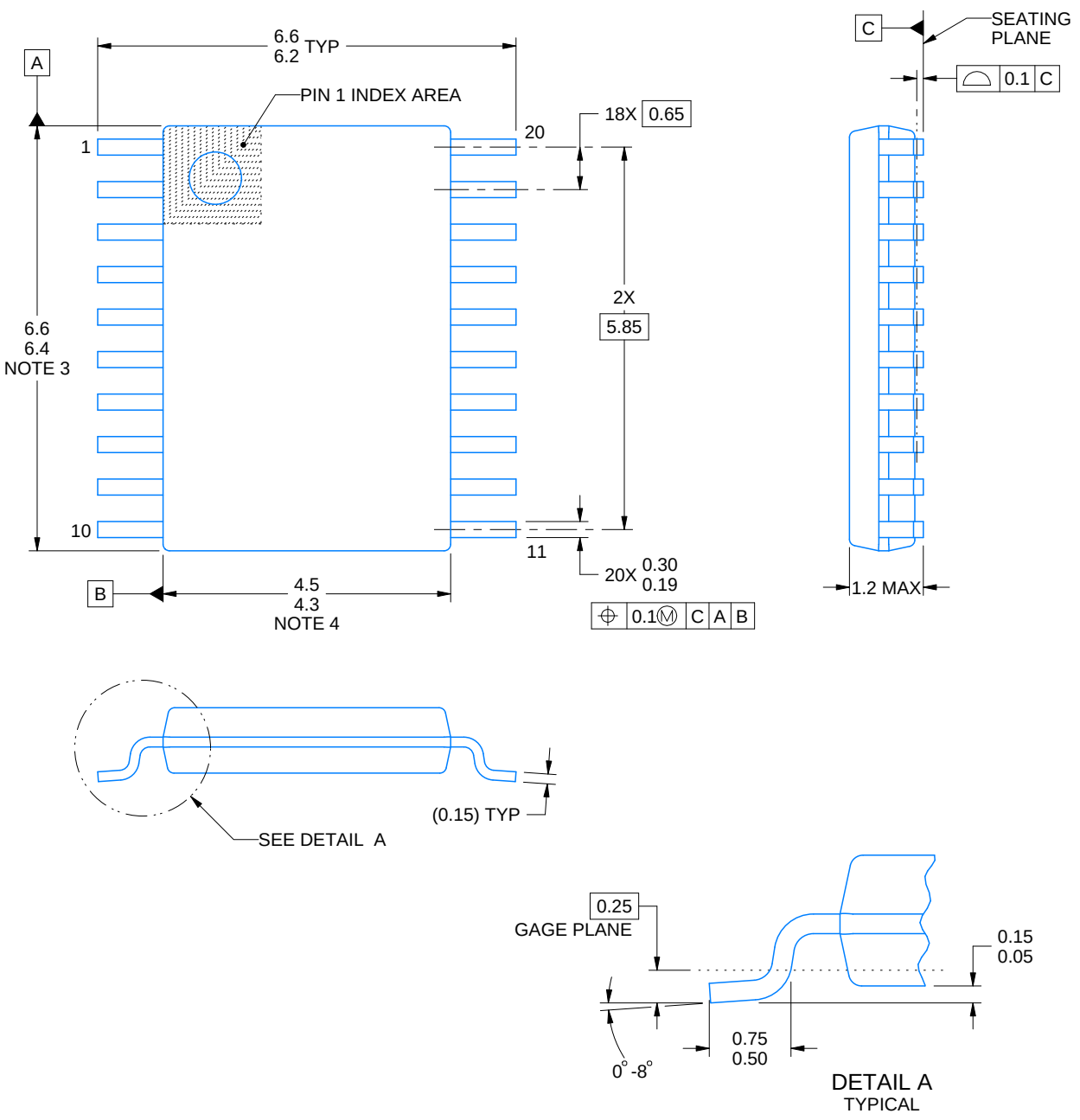
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS2482PW	PW	TSSOP	20	70	530	10.2	3600	3.5
TPS2483PW	PW	TSSOP	20	70	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0020A

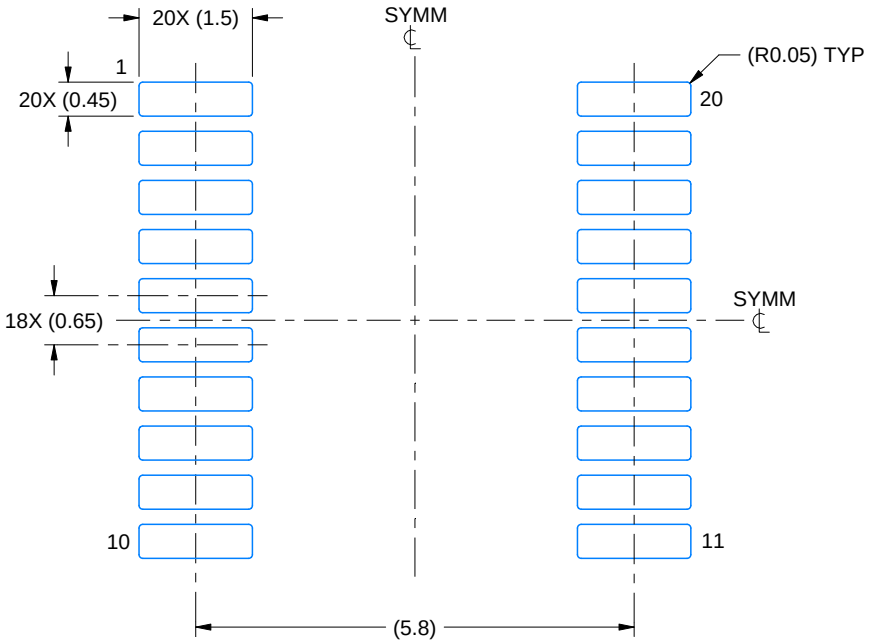
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



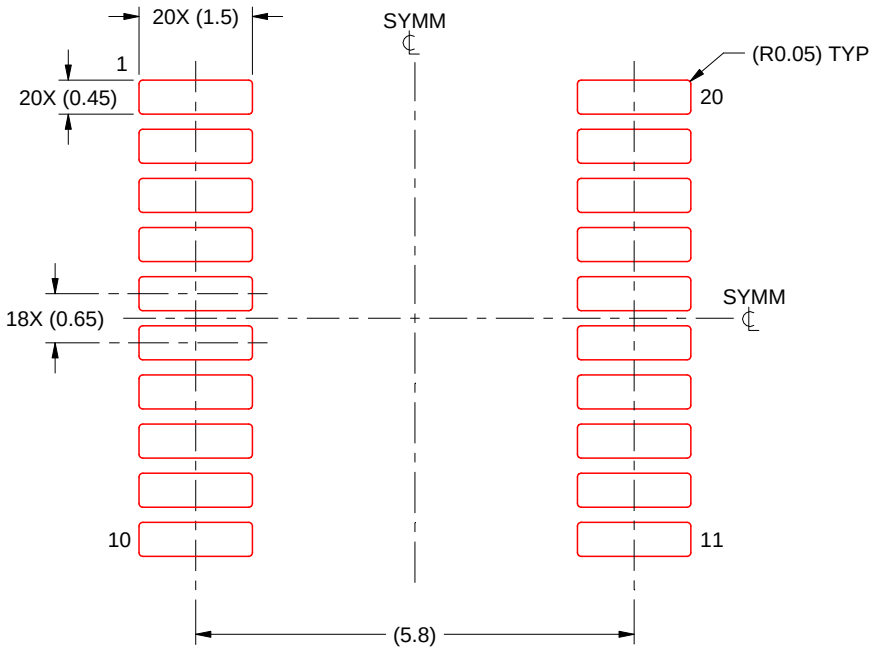
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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